Micropower, Dual Precision Instrumentation Switched Capacitor Building Block

FEATURES

- Low Power, I_S = 60μA(Max)
- Robust, Latch Up Proof
- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 5V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Two Independent Sections with One Clock
- Tiny SSOP-16 Package

APPLICATIONS

- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V–F and F–V Converters
- Sample-and-Hold
- Current Sources
- Precision Instrumentation Amplifiers

DESCRIPTION

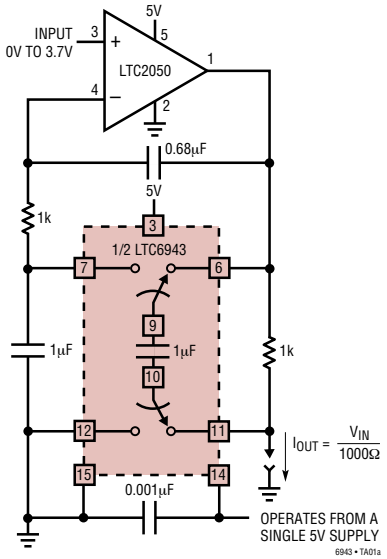
The LTC®6943 is a monolithic, charge-balanced, dual switched capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC6943 can also be driven with an external CMOS clock.

The LTC6943, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc.

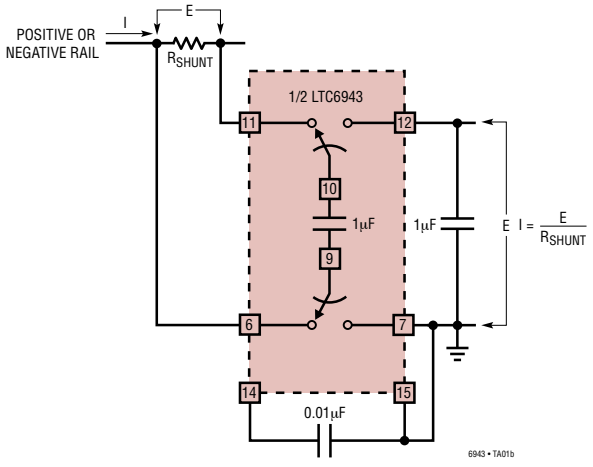
The LTC6943 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process, and it is functionally compatible with the LTC1043.

TYPICAL APPLICATION

Precision Voltage Controlled Current Source with Ground Referred Input and Output



Precision Current Sensing in Supply Rails

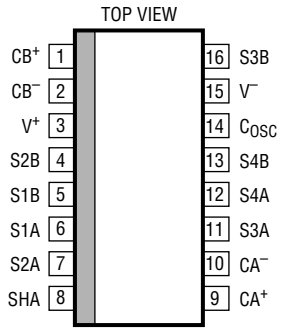


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 18V
Input Voltage at Any Pin ..... $-0.3V \le V_{IN} \le V^+ + 0.3V$
Operating Temperature Range
(Note 2) ..... –40°C to 125°C
Specified Temperature Range
(Note 2) .....–40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC6943CGN LTC6943IGN LTC6943HGN
GN PART MARKING
6943C 6943I 6943H

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 10V, V^- = 0V

SYMBOL	PARAMETER	CONDITIONS		LTC6943C LTC6943I MIN	LTC6943C LTC6943I TYP	LTC6943C LTC6943I MAX	LTC6943H MIN	LTC6943H TYP	LTC6943H MAX	UNITS
I_S	Power Supply Current	Pin 14 Connected High or Low	 ●		40	60 90		40	60 90	µA µA
		C_{OSC} (Pin 14 to V^-) = 100pF	 ●		80	150 170		80	150 170	µA µA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 3)	 ●		6	100 40		6	100 200	pA nA
R_{ON}	ON Resistance	Test Circuit 2, V_{IN} = 7V, 1 = ±0.5mA V^+ = 10V, V^- = 0V	 ●		240	400 700		240	400 700	Ω Ω
R_{ON}	ON Resistance	Test Circuit 2, V_{IN} = 3.1V, 1 = ±0.5mA V^+ = 5V, V^- = 0V	 ●		400	700 1		400	700 1	Ω kΩ
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 14 to V^-) = 0pF C_{OSC} (Pin 14 to V^-) = 100pF Test Circuit 3	 ●	 20 12	185 30	 50 75	 20 10	185 30	 50 75	kHz kHz kHz
I_{OSC}	Pin Source or Sink Current	Pin 14 at V^+ or V^-	 ●		40	70 100		40	70 100	µA µA
	Break-Before-Make Time				25			25		ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven			75			75		ns
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels			5			5		MHz
CMRR	Common Mode Rejection Ratio	V^+ = 5V, V^- = –5V, –5V < V_{CM} < 5V DC to 400Hz			120			120		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

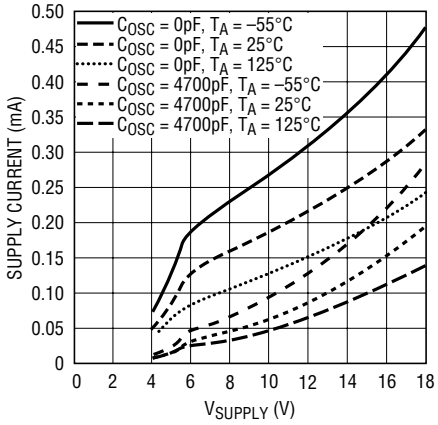
Note 2: All versions of the LTC6943 are guaranteed functional over the operating temperature range of –40°C to 125°C. The LTC6943CGN is guaranteed to meet 0°C to 70°C specifications and is designed, characterized and expected to meet the specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures.

The LTC6943IGN is guaranteed to meet specified performance from –40°C to 85°C. The LTC6943HGN is guaranteed to meet specified performance from –40°C to 125°C.

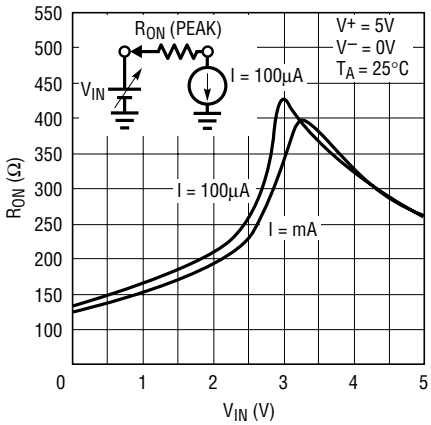
Note 3: OFF leakage current at 25°C is guaranteed by design and it is not 100% tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

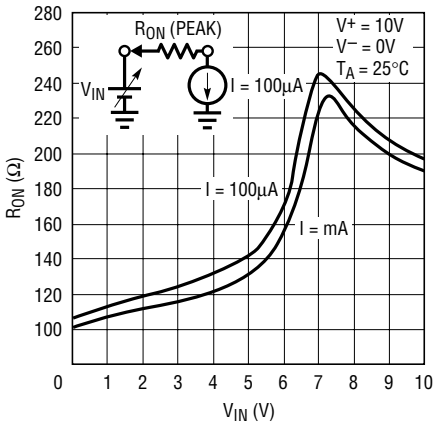
Power Supply Current vs Power Supply Voltage



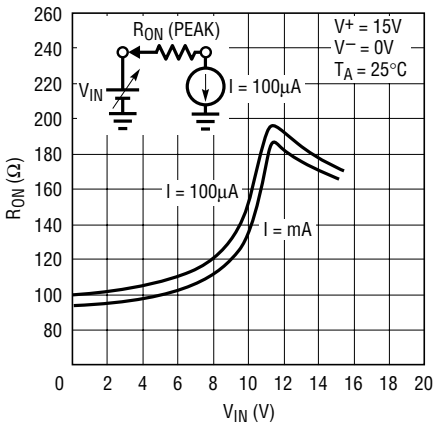
RON vs VIN



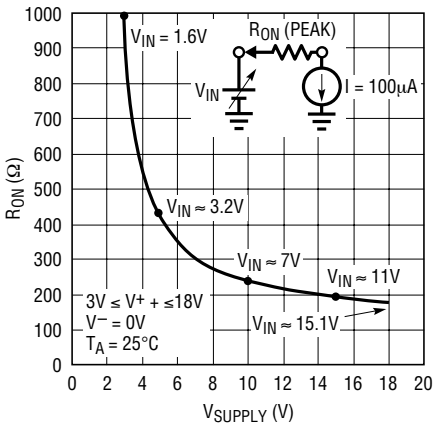
RON vs VIN



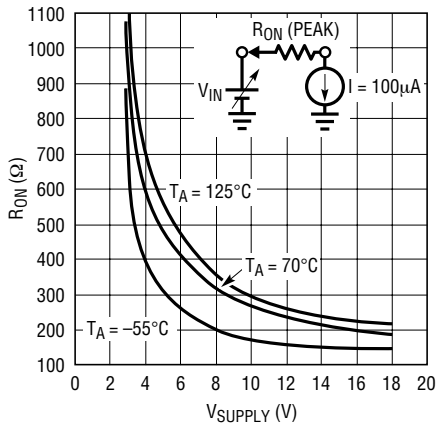
RON vs VIN



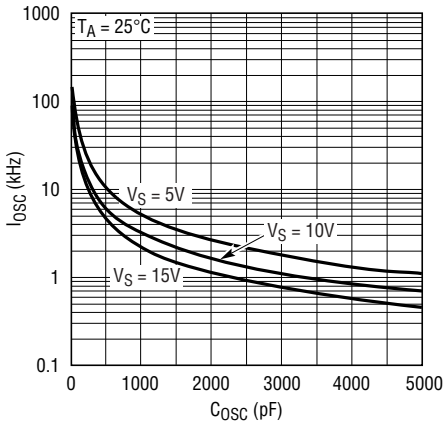
RON (Peak) vs Power Supply Voltage



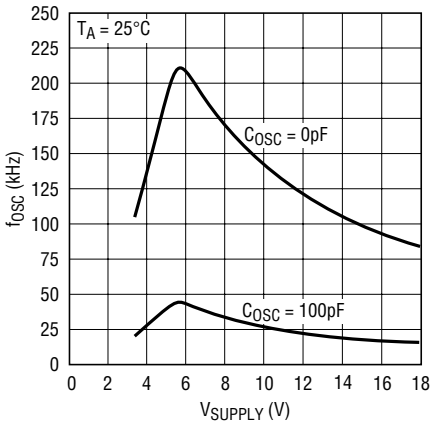
RON (Peak) vs Power Supply Voltage and Temperature



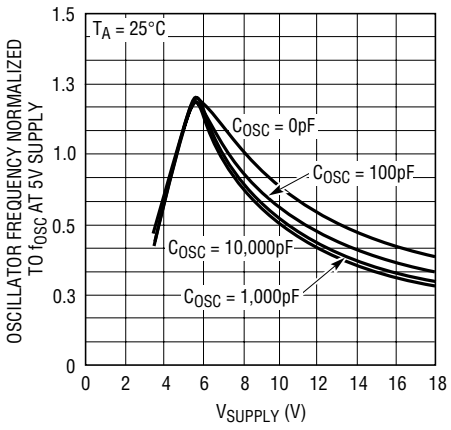
Oscillator Frequency, fOSC vs COSC



Oscillator Frequency, fOSC vs Supply Voltage

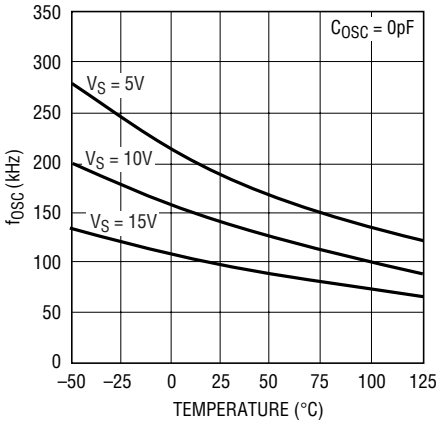


Normalized Oscillator Frequency, fOSC vs Supply Voltage



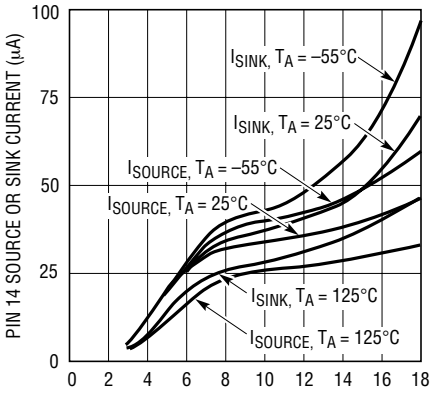
TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

Oscillator Frequency, f_{OSC} vs Ambient Temperature



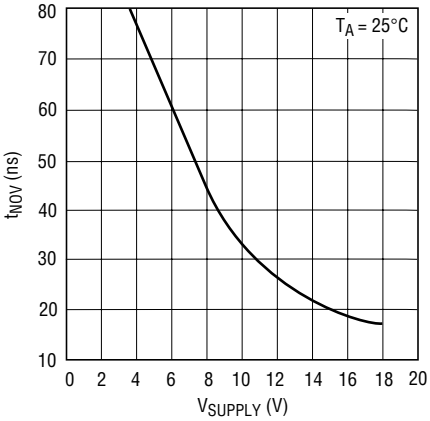
6943 TPC10

C_{OSC} Pin I_{SINK}, I_{SOURCE} vs Supply Voltage



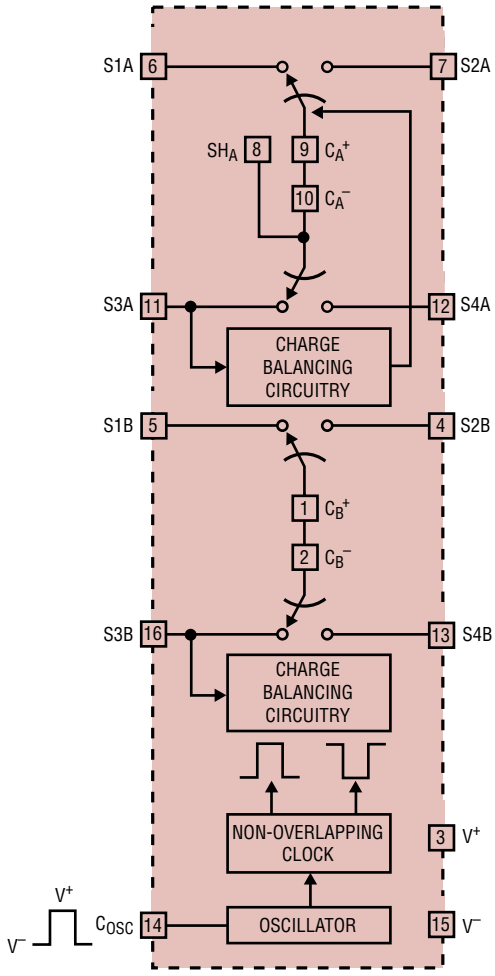
LTC1043 • TPC11

Break-Before-Make Time, t_{NOV}, vs Supply Voltage



LTC1043 • TPC12

BLOCK DIAGRAM



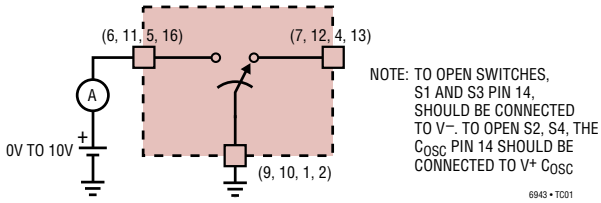
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 14 HIGH

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 14 HIGH) AND INJECTS A SMALL CHARGE AT THE C^+ PIN (PIN 14 LOW). THIS BOOSTS THE CMRR WHEN THE LTC6943 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END. FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED

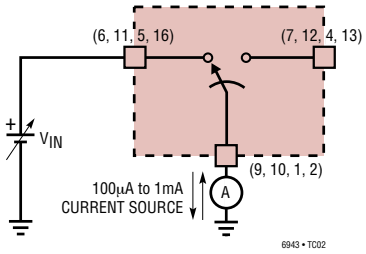
6943 • BD01

TEST CIRCUITS

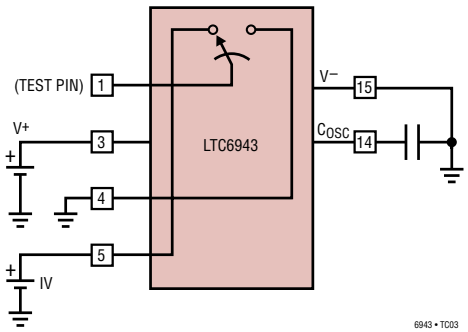
Test Circuit 1. Leakage Current Test



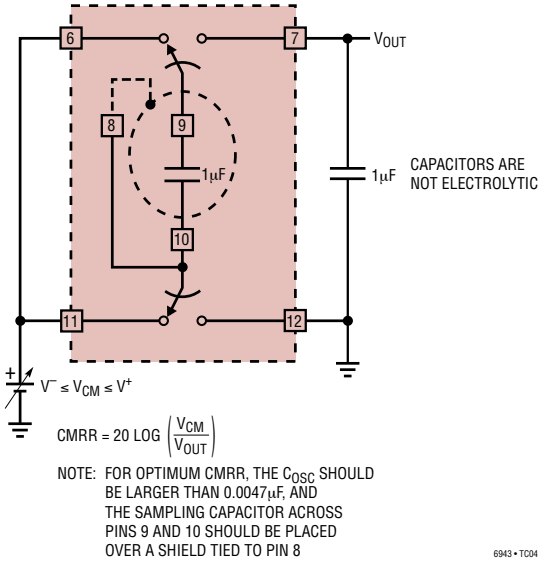
Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{OSC}



Test Circuit 4. CMRR Test



APPLICATIONS INFORMATION

Common Mode Rejection Ratio (CMRR)

The LTC6943, when used as a differential to single-ended converter rejects common mode signals and preserves differential voltages (Figure 1). Unlike other techniques, the LTC6943's CMRR does not degrade with increasing common mode voltage frequency. During the sampling mode, the impedance of Pins 1, 2 (and 9, 10) should be balanced, otherwise, common mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common mode voltages are not sampled, the common mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1 is measured by shorting Pins 6 and 11 and by observing, with a

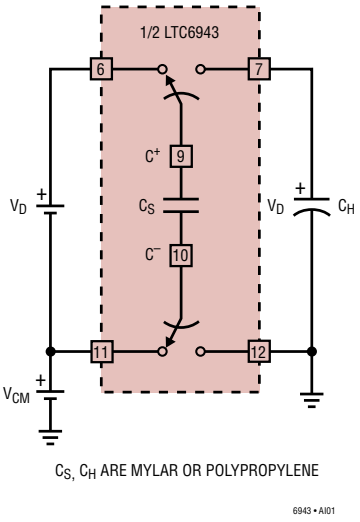


Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease (Figure 2).

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC6943, configured as a basic sample-and-hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC6943. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC6943, when powered with symmetrical dual supplies, will sample-and-hold small signals around ground without any significant error.

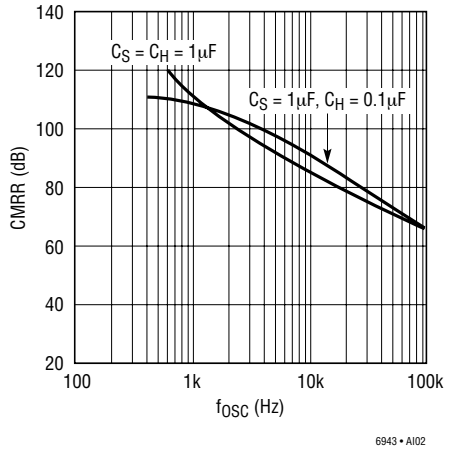


Figure 2. CMRR vs Sampling Frequency

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC6943 (Figure 1). The common mode error due to the internal junction capacitances of the C^+ Pin(s) 1 and 9 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. A shield placed underneath the sampling capacitor and connected to C^- helps to boost the CMRR to 120dB (Figure 5).

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC6943 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

C_{OSC} Pin (14)

The C_{OSC} pin can be used with an external capacitor, C_{OSC}, connected from Pin 14 to Pin 15, to modify the internal oscillator frequency. If Pin 16 is floating, the internal 24pF capacitor, plus any external interpin capacitance, set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 14 can also be driven with an external CMOS level clock to override the internal oscillator.

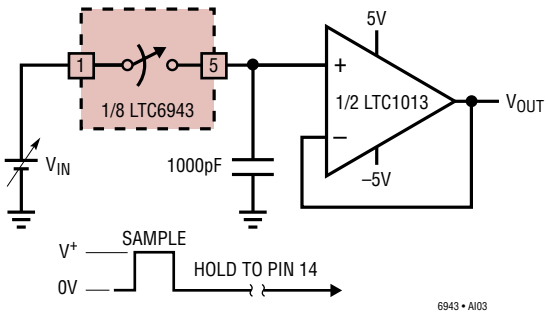


Figure 3

APPLICATIONS INFORMATION

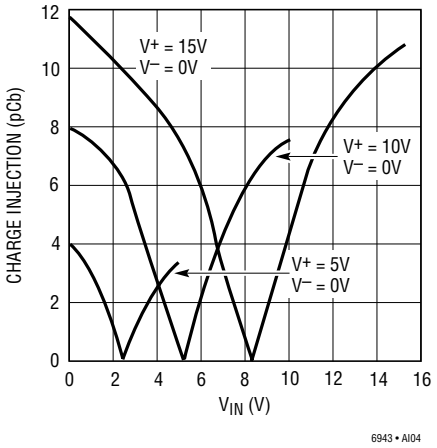


Figure 4. Individual Switch Charge Injection vs Input Voltage

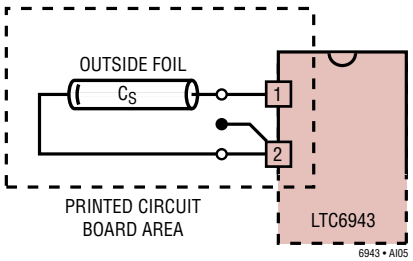
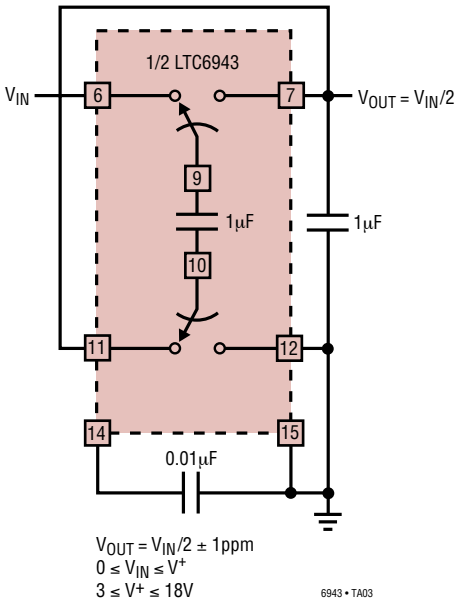


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

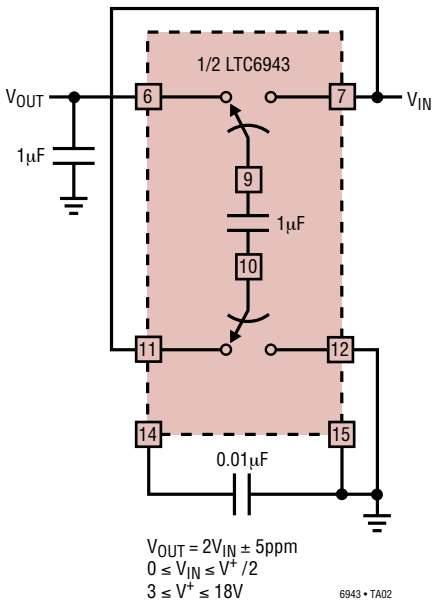
TYPICAL APPLICATIONS

Divide by 2



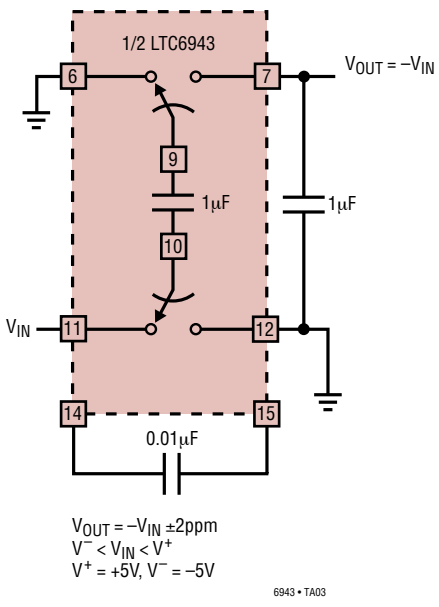
$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \le V_{IN} \le V^+$
$3 \le V^+ \le 18V$

Multiply by 2



$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \le V_{IN} \le V^+/2$
$3 \le V^+ \le 18V$

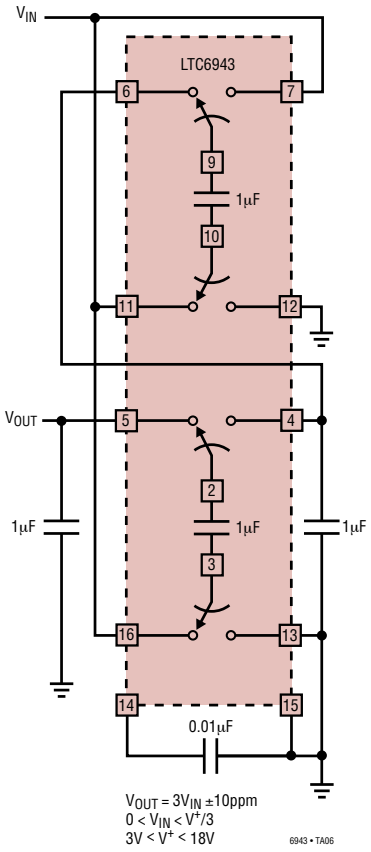
Ultra Precision Voltage Inverter



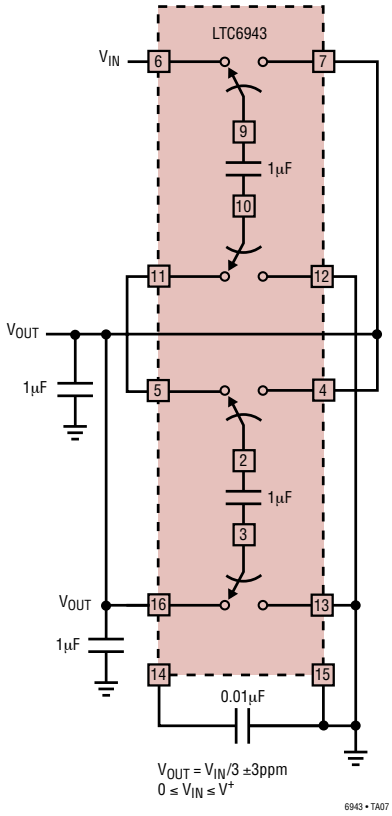
$V_{OUT} = -V_{IN} \pm 2ppm$
$V^- < V_{IN} < V^+$
$V^+ = +5V, V^- = -5V$

TYPICAL APPLICATIONS

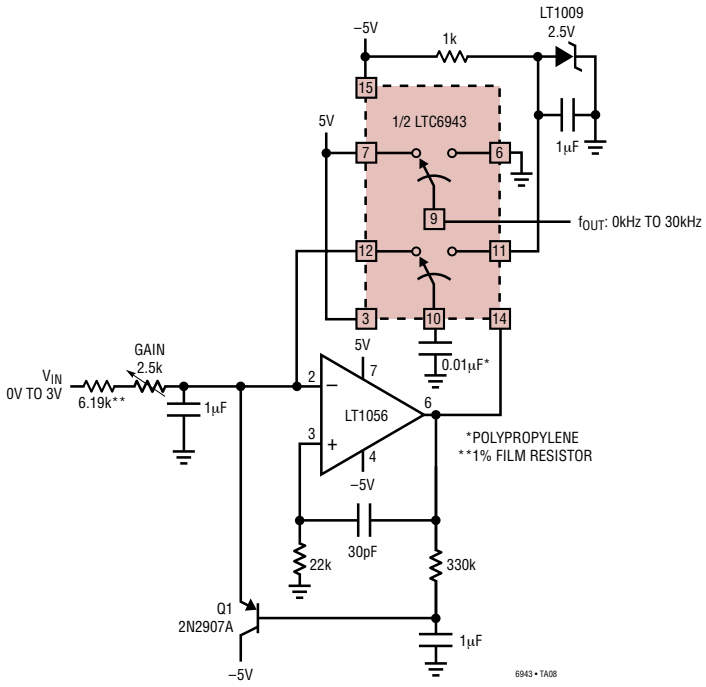
Precision Multiply by 3



Divide by 3

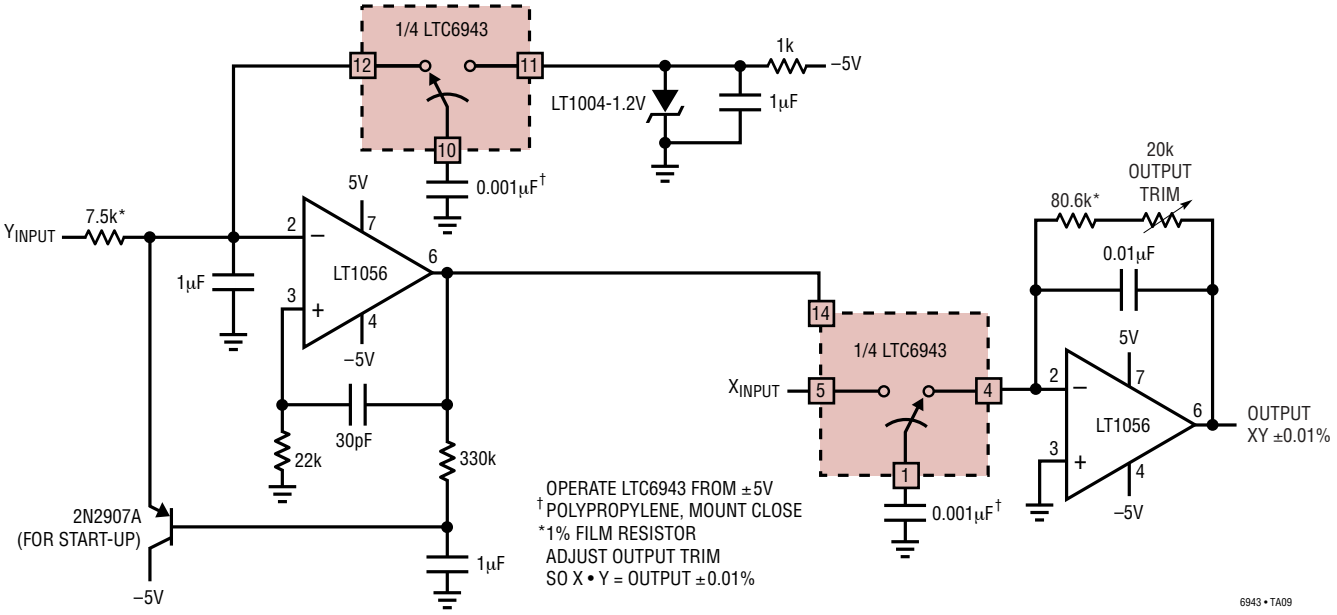


0.01% V/F Converter

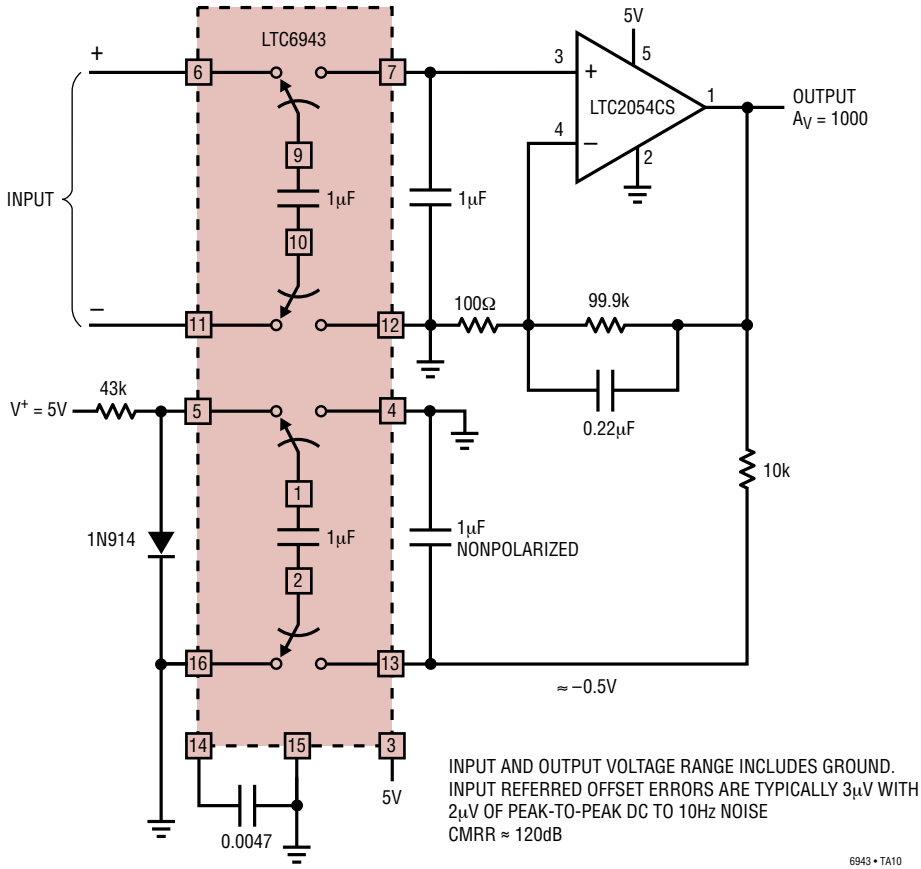


TYPICAL APPLICATIONS

0.01% Analog Multiplier

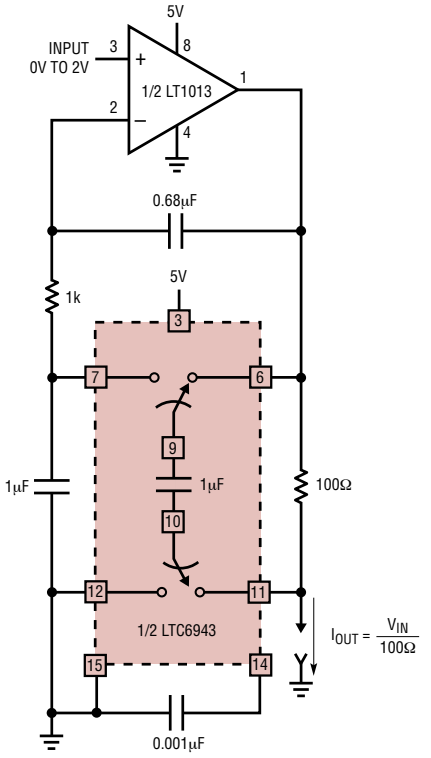


Single 5V Supply, Ultra Precision Low Power with True Rail-to-Rail In/Out Instrumentation Amplifier

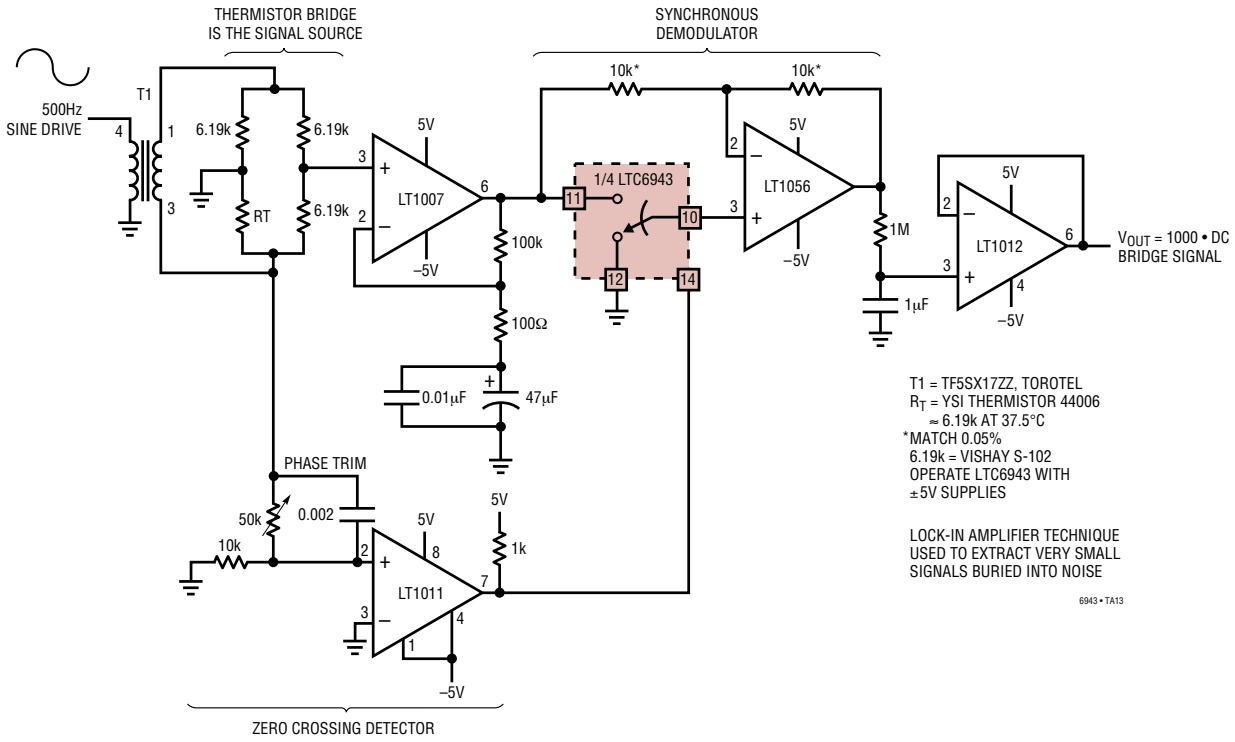


TYPICAL APPLICATIONS

Voltage Controlled Current Source with Ground Referred Input and Output

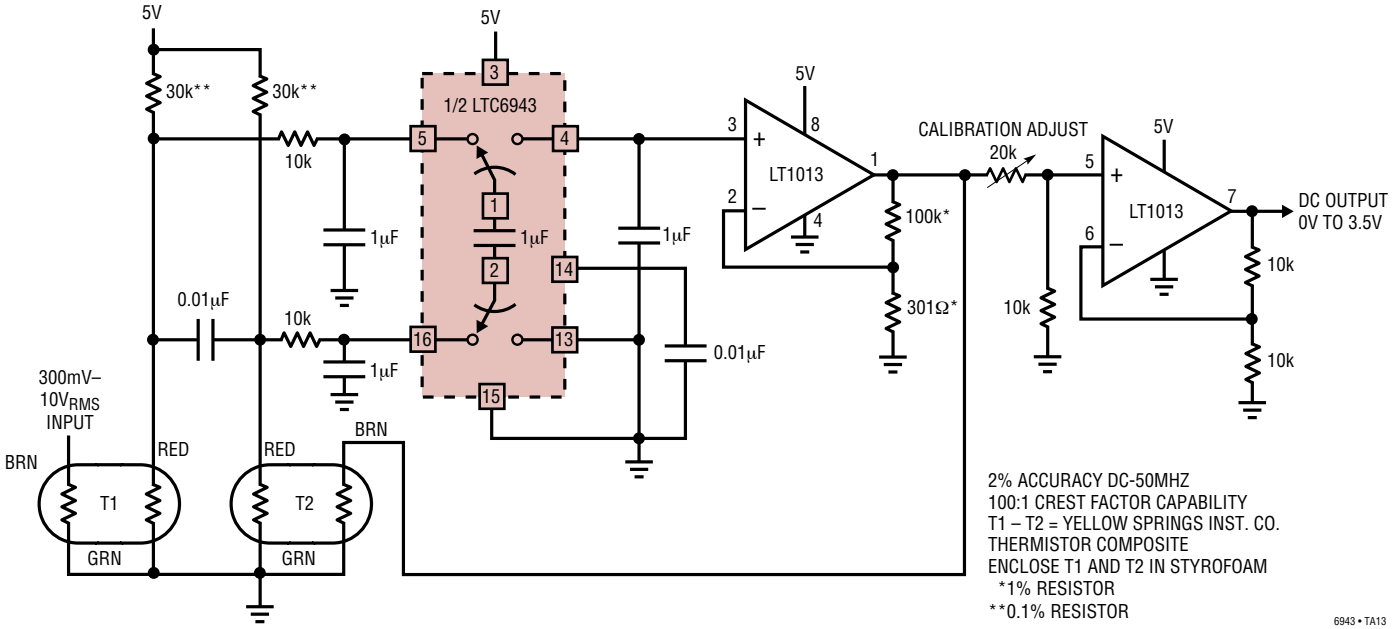


Lock-In Amplifier (= Extremely Narrow-Band Amplifier)



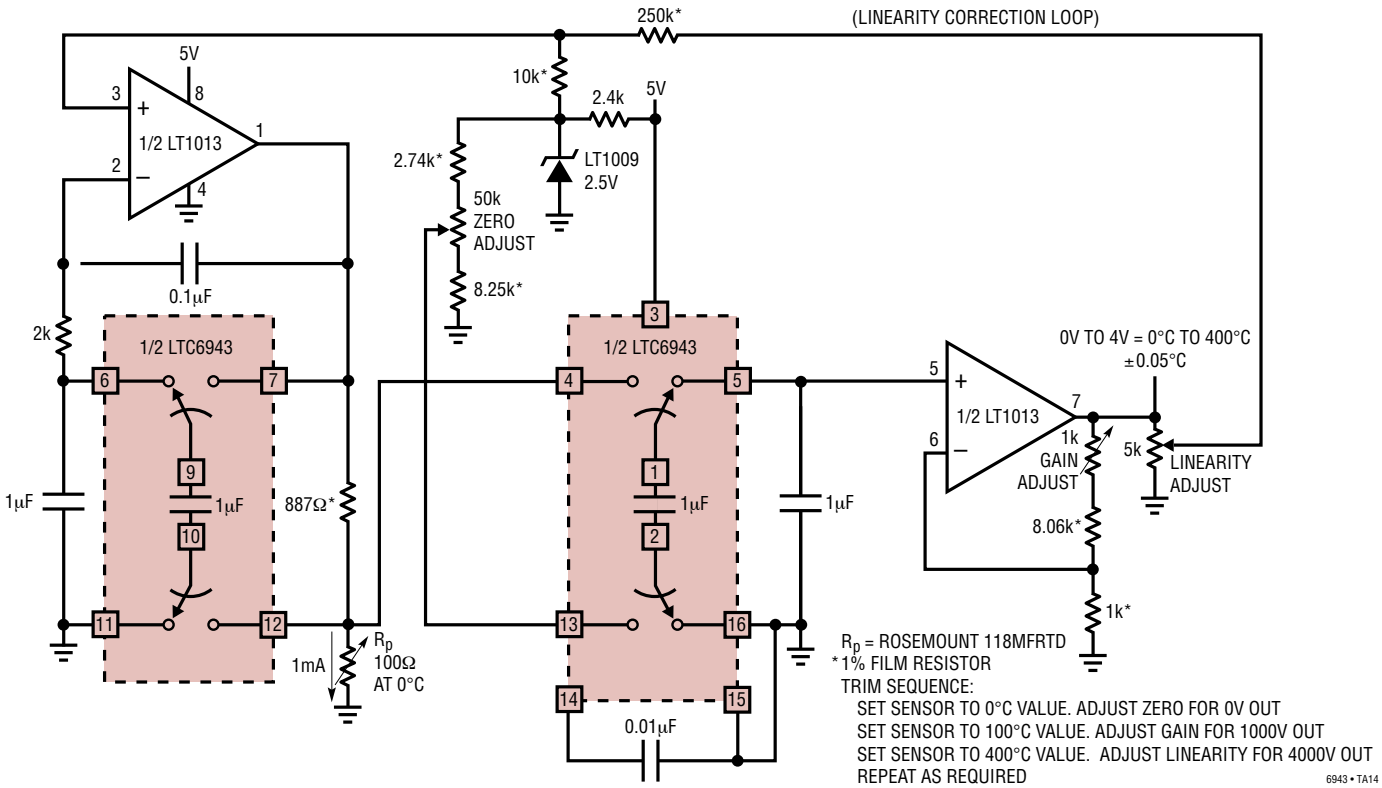
TYPICAL APPLICATIONS

50MHz Thermal RMS/DC Converter



6943 • TA13

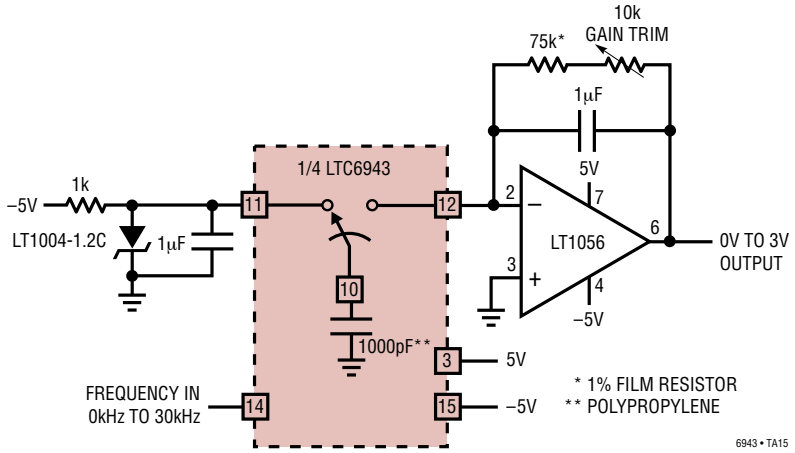
Single Supply Precision Linearized Platinum RTD Signal Conditioner



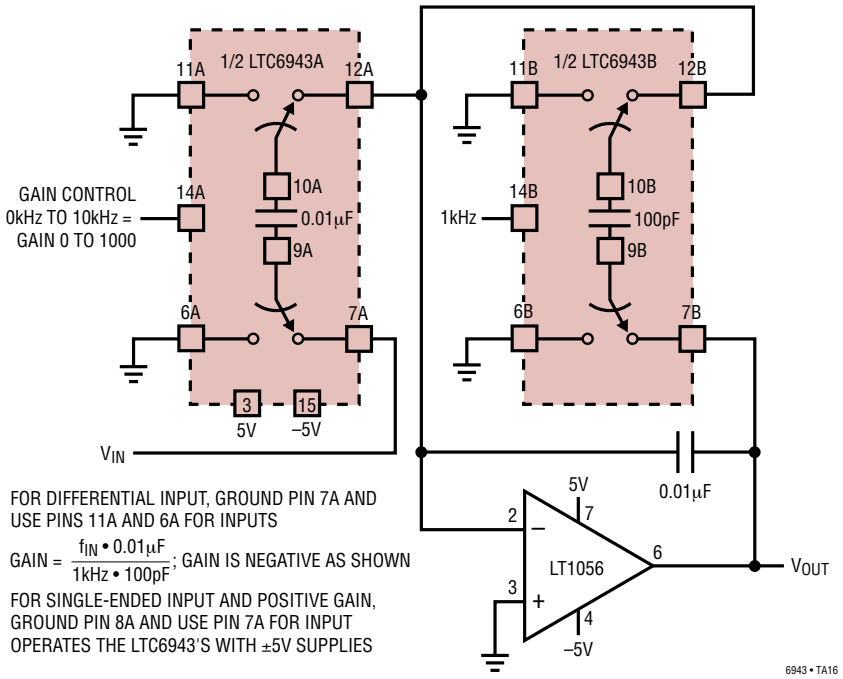
6943 • TA14

TYPICAL APPLICATIONS

0.01% F/V Converter

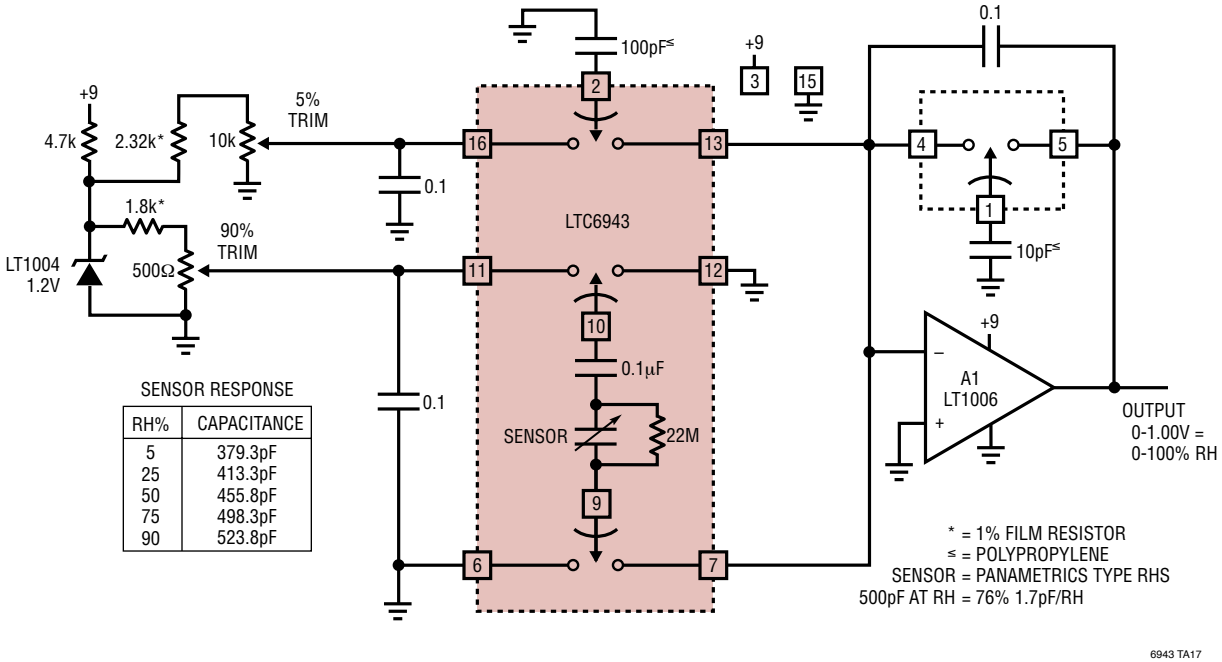


Frequency-Controlled Gain Amplifier

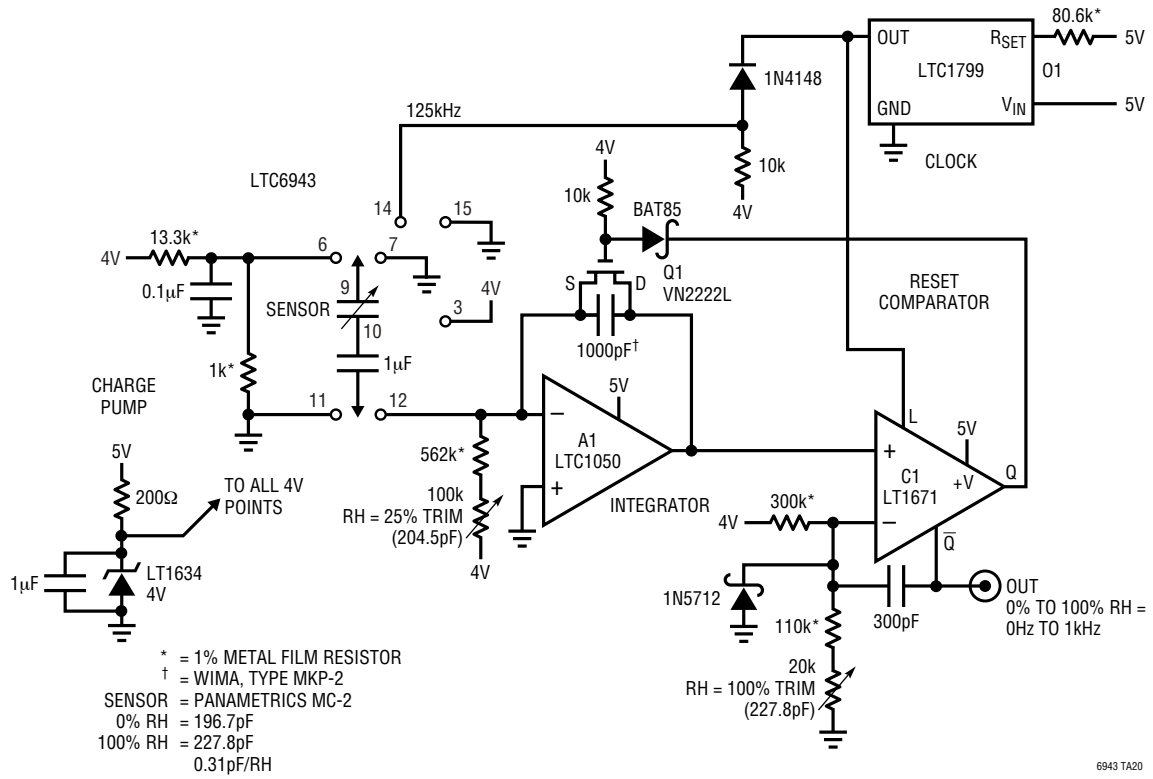


TYPICAL APPLICATIONS

Battery Powered Relative Humidity Sensor Signal Conditioner

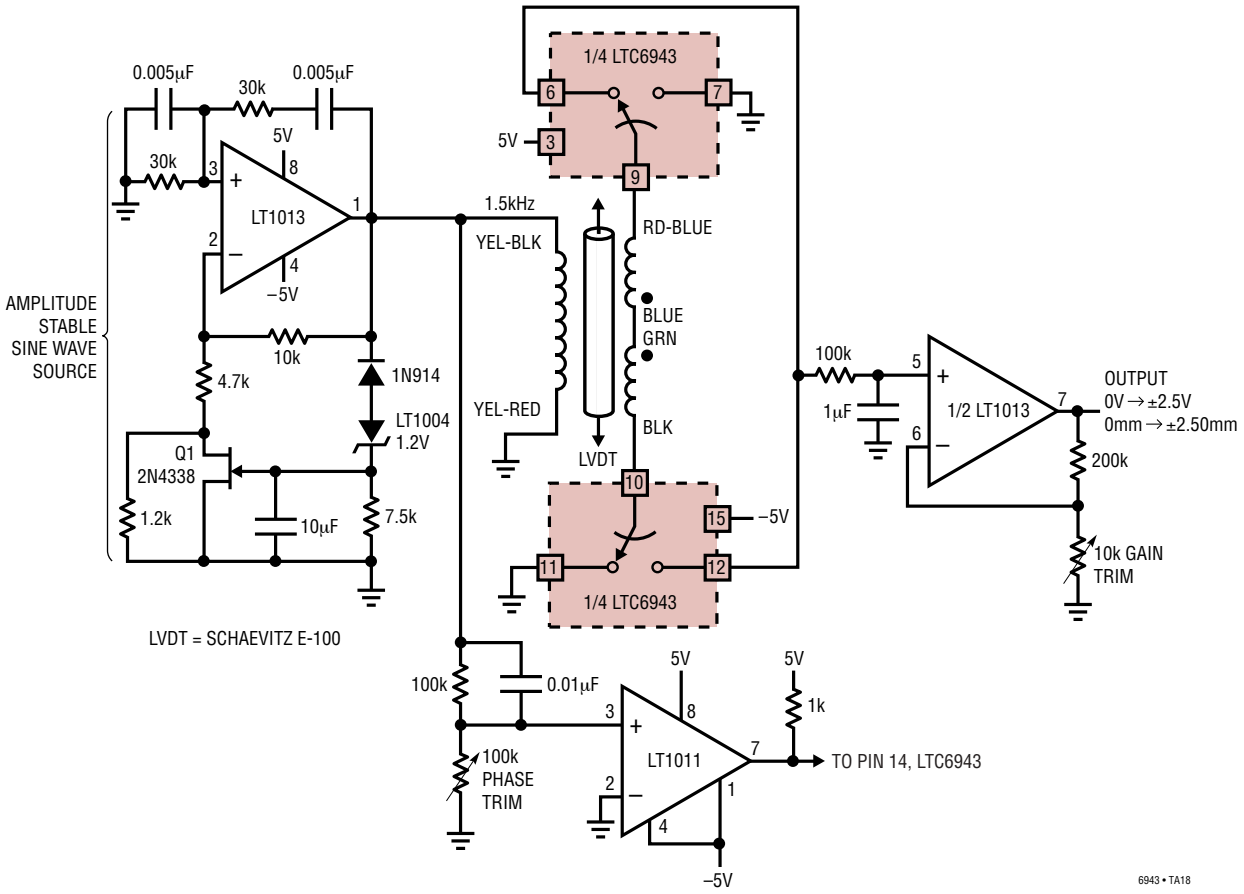


5V Powered, Frequency Output, Relative Humidity Sensor Signal Conditioner

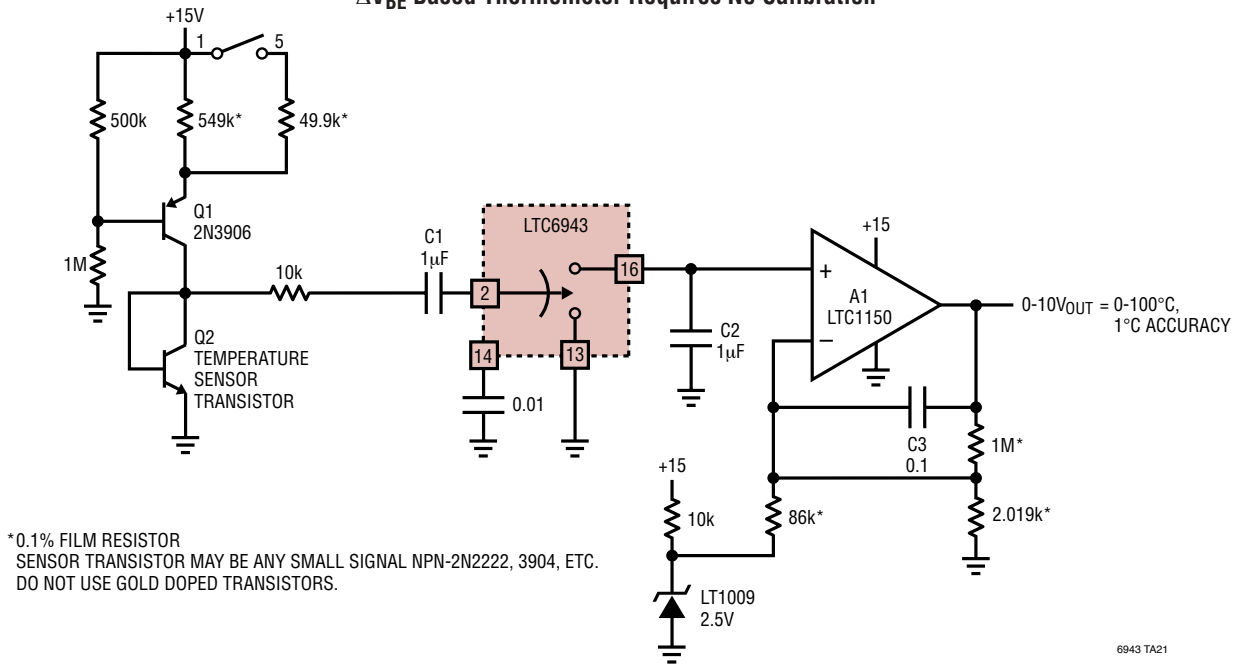


TYPICAL APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

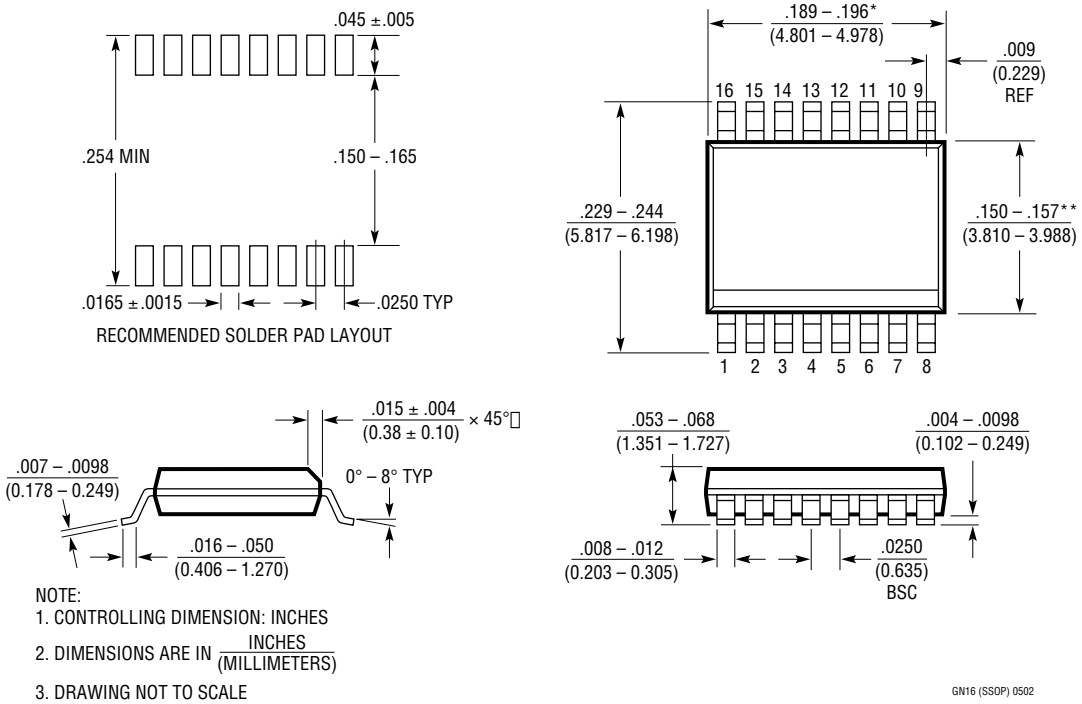


ΔV_{BE} Based Thermometer Requires No Calibration



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502