

TimerBlox: Delay Block/  
Debouncer

**FEATURES**

- **Delay Range: 1µs to 33.6 Seconds**
- Configured with 1 to 3 Resistors
- Delay Max Error:
  - <2.3% for Delay > 512µs
  - <3.4% for Delay of 8µs to 512µs
  - <5.1% for Delay of 1µs to 8µs
- Delay One or Both Rising/Falling Edges
- 2.25V to 5.5V Single Supply Operation
- 70µA Supply Current at 10µs Delay
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN
- AEC-Q100 Qualified for Automotive Applications

**APPLICATIONS**

- Noise Discriminators/Pulse Qualifiers
- Delay Matching
- Switch Debouncing
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

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



**DESCRIPTION**

The LTC6994 is a programmable delay block with a range of 1µs to 33.6 seconds. The LTC6994 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, R<sub>SET</sub>, programs an internal master oscillator frequency, setting the LTC6994's time base. The input-to-output delay is determined by this master oscillator and an internal clock divider, N<sub>DIV</sub>, programmable to eight settings from 1 to 2<sup>21</sup>:

$$t_{\text{DELAY}} = \frac{N_{\text{DIV}} \cdot R_{\text{SET}}}{50\text{k}\Omega} \cdot 1\mu\text{s}, N_{\text{DIV}} = 1, 8, 64, \dots, 2^{21}$$

The output (OUT) follows the input (IN) after delaying the rising and/or falling transitions. The LTC6994-1 will delay the rising or falling edge. The LTC6994-2 will delay both transitions, and adds the option to invert the output.

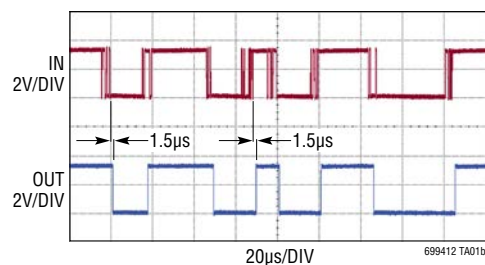
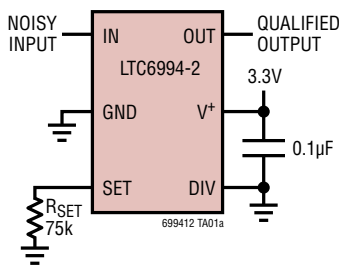
DEVICE	DELAY FUNCTION
LTC6994-1	 or 
LTC6994-2	 or 

The LTC6994 also offers the ability to dynamically adjust the delay time via a separate control voltage.

For easy configuration of the LTC6994, use the [TimerBlox LTC6994: Delay Web-Based Design Tool](#).

**TYPICAL APPLICATION**

Noise Discriminator

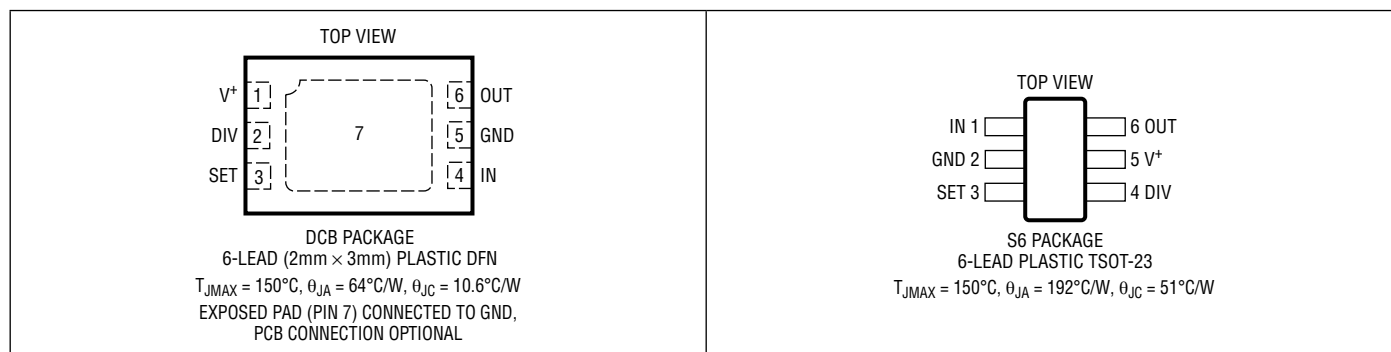


# LTC6994-1/LTC6994-2

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ( $V^+$ ) to GND .....	6V	Specified Temperature Range (Note 3)	
Maximum Voltage on Any Pin		LTC6994C .....	0°C to 70°C
..... ( $GND - 0.3V \leq V_{PIN} \leq (V^+ + 0.3V)$ )		LTC6994I .....	-40°C to 85°C
Operating Temperature Range (Note 2)		LTC6994H .....	-40°C to 125°C
LTC6994C .....	-40°C to 85°C	LTC6994MP .....	-55°C to 125°C
LTC6994I .....	-40°C to 85°C	Junction Temperature .....	150°C
LTC6994H .....	-40°C to 125°C	Storage Temperature Range .....	-65°C to 150°C
LTC6994MP .....	-55°C to 125°C	Lead Temperature (Soldering, 10 sec)	
		S6 Package .....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

### Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6994DCB-1#TRMPBF	LTC6994DCB-1#TRPBF	LFCT	6-Lead (2mm x 3mm) Plastic DFN	0°C to 70°C
LTC6994IDCB-1#TRMPBF	LTC6994IDCB-1#TRPBF	LFCT	6-Lead (2mm x 3mm) Plastic DFN	-40°C to 85°C
LTC6994HDCB-1#TRMPBF	LTC6994HDCB-1#TRPBF	LFCT	6-Lead (2mm x 3mm) Plastic DFN	-40°C to 125°C
LTC6994CS6-1#TRMPBF	LTC6994CS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6994IS6-1#TRMPBF	LTC6994IS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6994HS6-1#TRMPBF	LTC6994HS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6994DCB-2#TRMPBF	LTC6994DCB-2#TRPBF	LFCW	6-Lead (2mm x 3mm) Plastic DFN	0°C to 70°C
LTC6994IDCB-2#TRMPBF	LTC6994IDCB-2#TRPBF	LFCW	6-Lead (2mm x 3mm) Plastic DFN	-40°C to 85°C
LTC6994HDCB-2#TRMPBF	LTC6994HDCB-2#TRPBF	LFCW	6-Lead (2mm x 3mm) Plastic DFN	-40°C to 125°C
LTC6994CS6-2#TRMPBF	LTC6994CS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6994IS6-2#TRMPBF	LTC6994IS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6994HS6-2#TRMPBF	LTC6994HS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6994MPS6-1#TRMPBF	LTC6994MPS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	-55°C to 125°C
LTC6994MPS6-2#TRMPBF	LTC6994MPS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	-55°C to 125°C

## ORDER INFORMATION

### Lead Free Finish

#### AUTOMOTIVE PRODUCTS\*\*

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6994IS6-1#WTRMPBF	LTC6994IS6-1#WTRPBF	LTFCV	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6994HS6-1#WTRMPBF	LTC6994HS6-1#WTRPBF	LTFCV	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6994IS6-2#WTRMPBF	LTC6994IS6-2#WTRPBF	LTFCX	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6994HS6-2#WTRMPBF	LTC6994HS6-2#WTRPBF	LTFCX	6-Lead Plastic TSOT-23	-40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

**Tape and reel specifications.** Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

\*\*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V to }5.5\text{V}$ ,  $I_N = 0\text{V}$ ,  $\text{DIVCODE} = 0 \text{ to } 15$  ( $N_{\text{DIV}} = 1 \text{ to } 2^{21}$ ),  $R_{\text{SET}} = 50\text{k to }800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$t_{\text{DELAY}}$	Delay Time		1 $\mu$		33.55	sec	
$\Delta t_{\text{DELAY}}$	Delay Accuracy (Note 4)	$N_{\text{DIV}} \geq 512$		±1.7	±2.3 ±3.0	% %	
		$8 \leq N_{\text{DIV}} \leq 64$		±2.4	±3.4 ±4.4	% %	
		$N_{\text{DIV}} = 1$		±3.8	±5.1 ±6.2	% %	
$\Delta t_{\text{DELAY}}/\Delta T$	Delay Drift Over Temperature	$N_{\text{DIV}} \geq 512$		±0.006		%/°C	
		$N_{\text{DIV}} \leq 64$		±0.008		%/°C	
	Delay Change With Supply	$N_{\text{DIV}} \geq 512$	$V^+ = 4.5\text{V to }5.5\text{V}$	●	-0.6	-0.2	%
			$V^+ = 2.25\text{V to }4.5\text{V}$	●	-0.4	-0.1	%
		$8 \leq N_{\text{DIV}} \leq 64$	$V^+ = 4.5\text{V to }5.5\text{V}$	●	-0.9	-0.2	%
			$V^+ = 2.7\text{V to }4.5\text{V}$ $V^+ = 2.25\text{V to }2.7\text{V}$	● ●	-0.7 -1.1	-0.2 -0.1	0.4 0.9
	Delay Jitter (Note 10)	$N_{\text{DIV}} = 1$	$V^+ = 5.5\text{V}$		1.0	%p-p	
			$V^+ = 2.25\text{V}$		0.5	%p-p	
		$N_{\text{DIV}} = 8$		0.20	%p-p		
		$N_{\text{DIV}} = 64$		0.05	%p-p		
		$N_{\text{DIV}} = 512$		0.20	%p-p		
	$N_{\text{DIV}} = 4096$		0.03	%p-p			
$t_S$	Delay Change Settling Time (Note 9)	$t_{\text{MASTER}} = t_{\text{DELAY}}/N_{\text{DIV}}$		6 • $t_{\text{MASTER}}$		$\mu\text{s}$	

# LTC6994-1/LTC6994-2

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $I_N = 0\text{V}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $2^{21}$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power Supply</b>							
$V^+$	Operating Supply Voltage Range		● 2.25		5.5	V	
	Power-On Reset Voltage		●		1.95	V	
$I_{\text{S(IDLE)}}$	Supply Current (Idle)	$R_L = \infty$ , $R_{\text{SET}} = 50\text{k}$ , $N_{\text{DIV}} \leq 64$	● $V^+ = 5.5\text{V}$	165	200	$\mu\text{A}$	
			● $V^+ = 2.25\text{V}$	125	160	$\mu\text{A}$	
		$R_L = \infty$ , $R_{\text{SET}} = 50\text{k}$ , $N_{\text{DIV}} \geq 512$	● $V^+ = 5.5\text{V}$	135	175	$\mu\text{A}$	
			● $V^+ = 2.25\text{V}$	105	140	$\mu\text{A}$	
		$R_L = \infty$ , $R_{\text{SET}} = 800\text{k}$ , $N_{\text{DIV}} \leq 64$	● $V^+ = 5.5\text{V}$	70	110	$\mu\text{A}$	
			● $V^+ = 2.25\text{V}$	60	95	$\mu\text{A}$	
		$R_L = \infty$ , $R_{\text{SET}} = 800\text{k}$ , $N_{\text{DIV}} \geq 512$	● $V^+ = 5.5\text{V}$	65	100	$\mu\text{A}$	
			● $V^+ = 2.25\text{V}$	55	90	$\mu\text{A}$	
<b>Analog Inputs</b>							
$V_{\text{SET}}$	Voltage at SET Pin		● 0.97	1.00	1.03	V	
$\Delta V_{\text{SET}}/\Delta T$	$V_{\text{SET}}$ Drift Over Temperature		●	$\pm 75$		$\mu\text{V}/^\circ\text{C}$	
$R_{\text{SET}}$	Frequency-Setting Resistor		● 50		800	$\text{k}\Omega$	
$V_{\text{DIV}}$	DIV Pin Voltage		● 0		$V^+$	V	
$\Delta V_{\text{DIV}}/\Delta V^+$	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal $V_{\text{DIV}}/V^+ = (\text{DIVCODE} + 0.5)/16$	●		$\pm 1.5$	%	
	DIV Pin Input Current		●		$\pm 10$	nA	
<b>Digital I/O</b>							
	IN Pin Input Capacitance			2.5		pF	
	IN Pin Input Current	$I_N = 0\text{V}$ to $V^+$			$\pm 10$	nA	
$V_{\text{IH}}$	High Level IN Pin Input Voltage	(Note 6)	● $0.7 \cdot V^+$			V	
$V_{\text{IL}}$	Low Level IN Pin Input Voltage	(Note 6)	●		$0.3 \cdot V^+$	V	
$I_{\text{OUT(MAX)}}$	Output Current	$V^+ = 2.7\text{V}$ to $5.5\text{V}$		$\pm 20$		mA	
$V_{\text{OH}}$	High Level Output Voltage (Note 7)	$V^+ = 5.5\text{V}$	● $I_{\text{OUT}} = -1\text{mA}$	5.45	5.48	V	
			● $I_{\text{OUT}} = -16\text{mA}$	4.84	5.15	V	
		$V^+ = 3.3\text{V}$	● $I_{\text{OUT}} = -1\text{mA}$	3.24	3.27	V	
			● $I_{\text{OUT}} = -10\text{mA}$	2.75	2.99	V	
		$V^+ = 2.25\text{V}$	● $I_{\text{OUT}} = -1\text{mA}$	2.17	2.21	V	
			● $I_{\text{OUT}} = -8\text{mA}$	1.58	1.88	V	
$V_{\text{OL}}$	Low Level Output Voltage (Note 7)	$V^+ = 5.5\text{V}$	● $I_{\text{OUT}} = 1\text{mA}$		0.02	0.04	V
			● $I_{\text{OUT}} = 16\text{mA}$		0.26	0.54	V
		$V^+ = 3.3\text{V}$	● $I_{\text{OUT}} = 1\text{mA}$		0.03	0.05	V
			● $I_{\text{OUT}} = 10\text{mA}$		0.22	0.46	V
		$V^+ = 2.25\text{V}$	● $I_{\text{OUT}} = 1\text{mA}$		0.03	0.07	V
			● $I_{\text{OUT}} = 8\text{mA}$		0.26	0.54	V
$t_{\text{PD}}$	Propagation Delay	$V^+ = 5.5\text{V}$		10		ns	
		$V^+ = 3.3\text{V}$		14		ns	
		$V^+ = 2.25\text{V}$		24		ns	
$t_{\text{WIDTH}}$	Minimum Recognized Input Pulse Width	$V^+ = 3.3\text{V}$		5		ns	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $I_N = 0\text{V}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $2^{21}$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_r$	Output Rise Time (Note 8)	$V^+ = 5.5\text{V}$		1.1		ns
		$V^+ = 3.3\text{V}$		1.7		ns
		$V^+ = 2.25\text{V}$		2.7		ns
$t_f$	Output Fall Time (Note 8)	$V^+ = 5.5\text{V}$		1.0		ns
		$V^+ = 3.3\text{V}$		1.6		ns
		$V^+ = 2.25\text{V}$		2.4		ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6994C is guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**Note 3:** The LTC6994C is guaranteed to meet specified performance from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The LTC6994C is designed, characterized and expected to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  but it is not tested or QA sampled at these temperatures. The LTC6994I is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6994H is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . The LTC6994MP is guaranteed to meet specified performance from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 4:** Delay accuracy is defined as the deviation from the  $t_{\text{DELAY}}$  equation, assuming  $R_{\text{SET}}$  is used to program the delay.

**Note 5:** See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

**Note 6:** The IN pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to  $V^+$ . Typical values can be estimated at any supply voltage using:

$$V_{\text{IN(RISING)}} \approx 0.55 \cdot V^+ + 185\text{mV} \text{ and } V_{\text{IN(FALLING)}} \approx 0.48 \cdot V^+ - 155\text{mV}$$

**Note 7:** To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with  $5\text{pF}$  output load. These specifications are based on characterization.

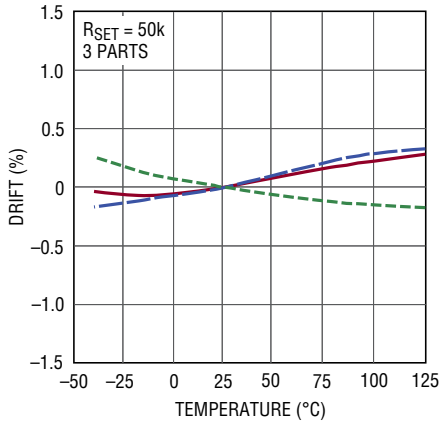
**Note 9:** Settling time is the amount of time required for the output to settle within  $\pm 1\%$  of the final delay after a  $0.5\times$  or  $2\times$  change in  $I_{\text{SET}}$ .

**Note 10:** Jitter is the ratio of the deviation of the programmed delay to the mean of the delay. This specification is based on characterization and is not 100% tested.

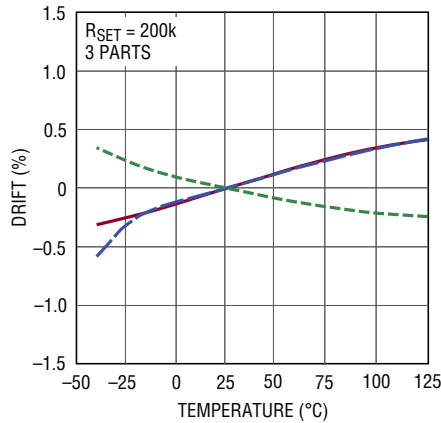
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

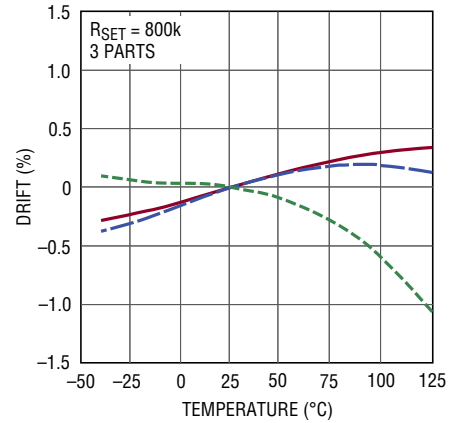
**Delay Drift vs Temperature**  
( $N_{DIV} \leq 64$ )



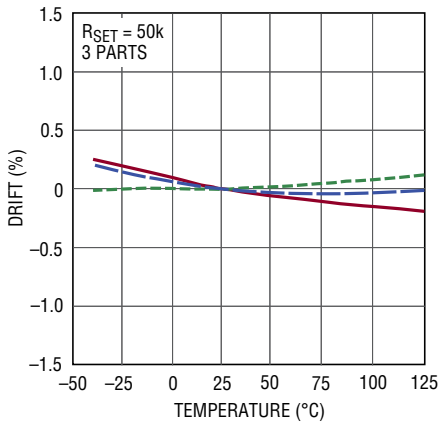
**Delay Drift vs Temperature**  
( $N_{DIV} \leq 64$ )



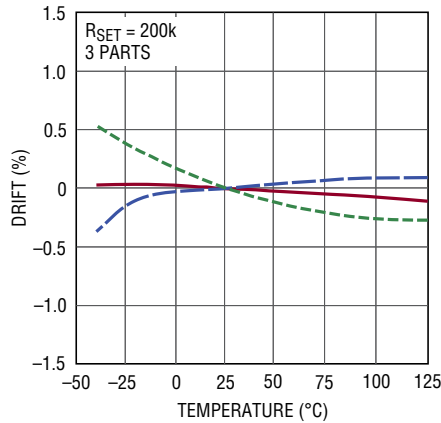
**Delay Drift vs Temperature**  
( $N_{DIV} \leq 64$ )



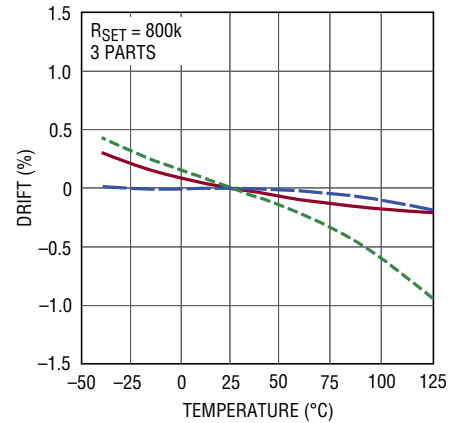
**Delay Drift vs Temperature**  
( $N_{DIV} \geq 512$ )



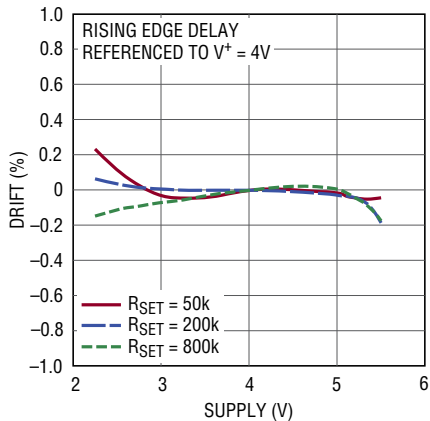
**Delay Drift vs Temperature**  
( $N_{DIV} \geq 512$ )



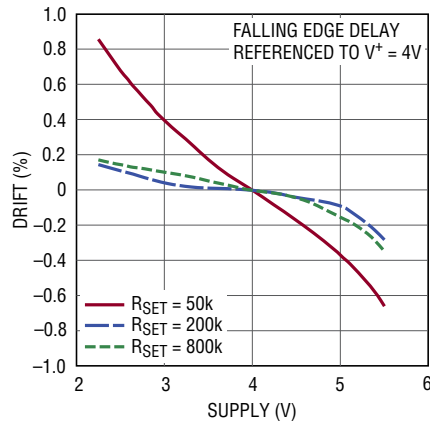
**Delay Drift vs Temperature**  
( $N_{DIV} \geq 512$ )



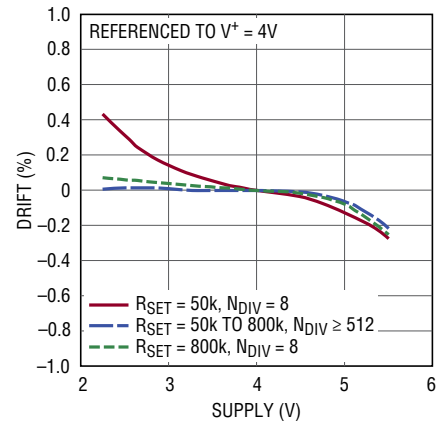
**Delay Drift vs Supply Voltage**  
( $N_{DIV} = 1$ )



**Delay Drift vs Supply Voltage**  
( $N_{DIV} = 1$ )



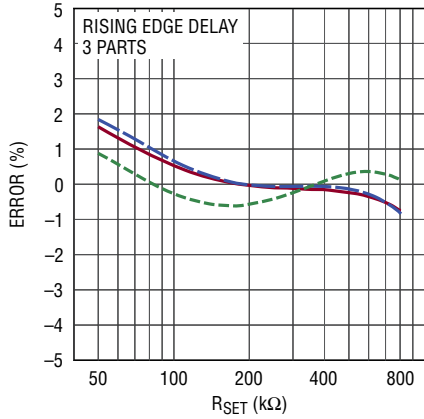
**Delay Drift vs Supply Voltage**  
( $N_{DIV} > 1$ )



# TYPICAL PERFORMANCE CHARACTERISTICS

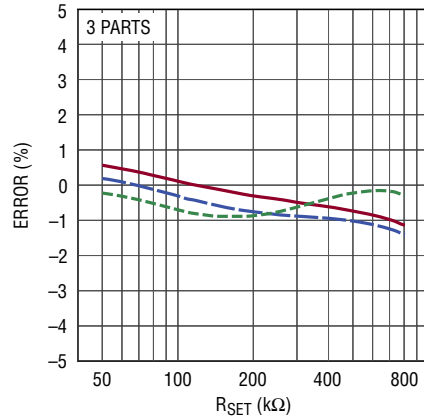
$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

**Delay Error vs  $R_{SET}$  ( $N_{DIV} = 1$ )**



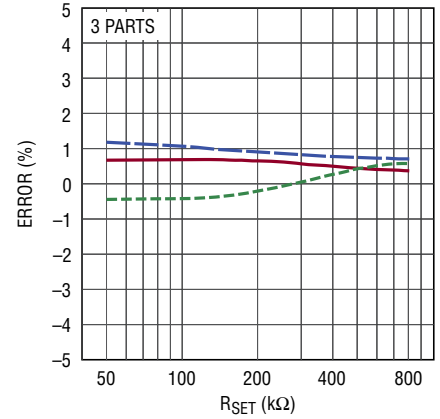
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**Delay Error vs  $R_{SET}$  ( $8 \leq N_{DIV} \leq 64$ )**



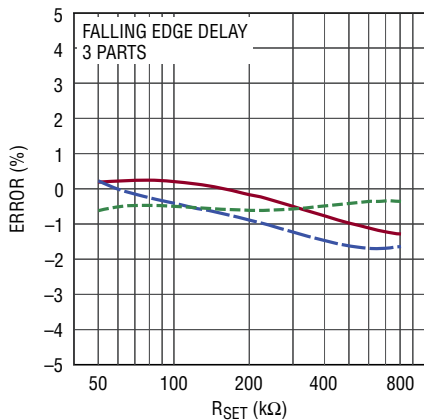
699412 G11

**Delay Error vs  $R_{SET}$  ( $N_{DIV} \geq 512$ )**



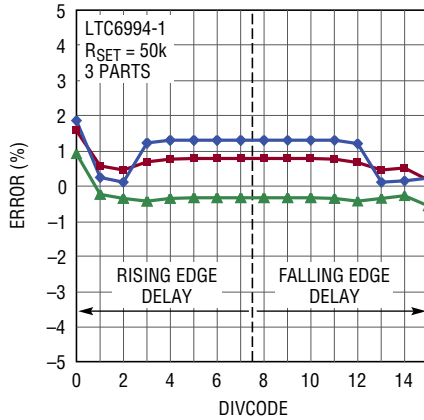
699412 G12

**Delay Error vs  $R_{SET}$  ( $N_{DIV} = 1$ )**



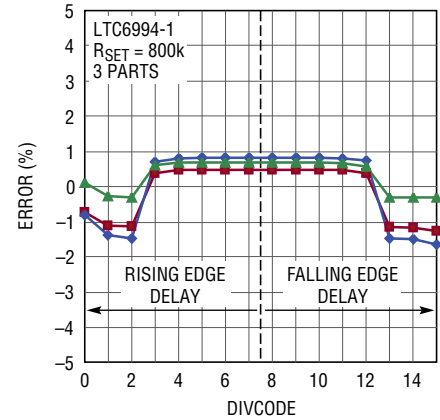
699412 G13

**Delay Error vs DIVCODE**



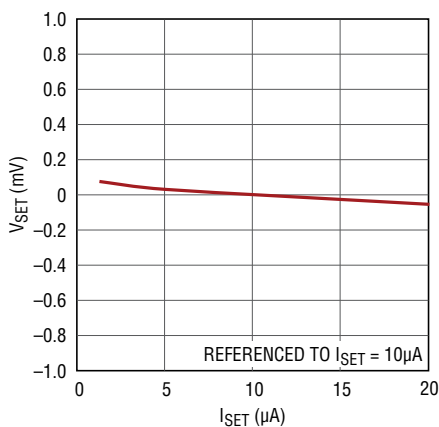
699412 G14

**Delay Error vs DIVCODE**



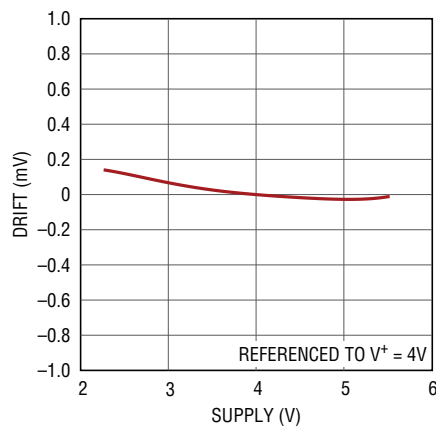
699412 G15

**$V_{SET}$  Drift vs  $I_{SET}$**



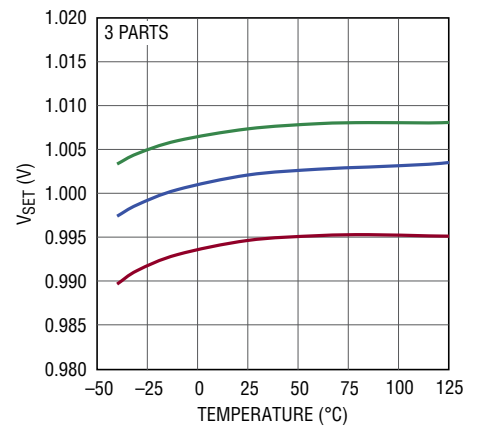
699412 G16

**$V_{SET}$  Drift vs Supply Voltage**



699412 G17

**$V_{SET}$  vs Temperature**



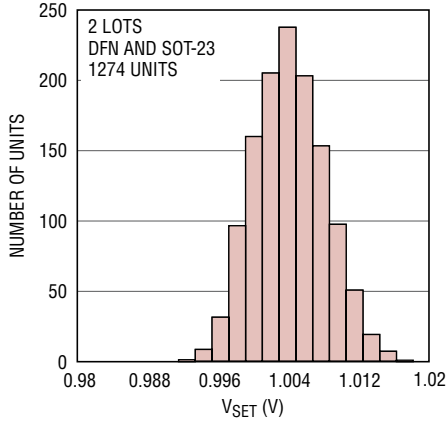
699412 G18

# LTC6994-1/LTC6994-2

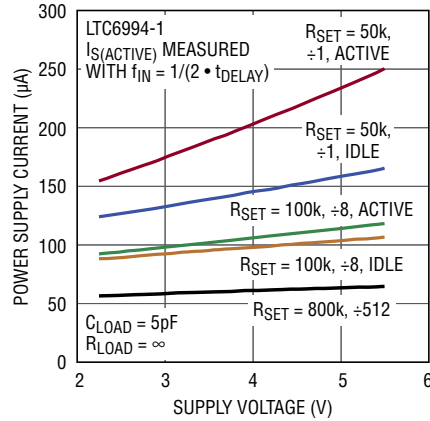
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

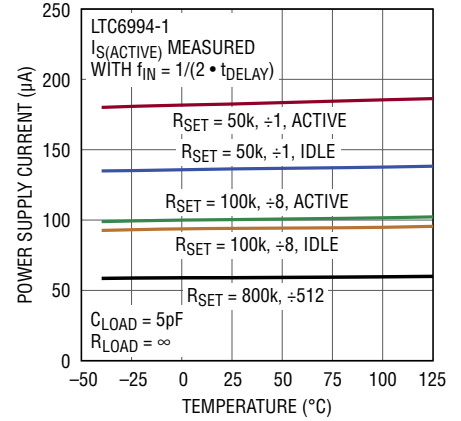
Typical  $V_{SET}$  Distribution



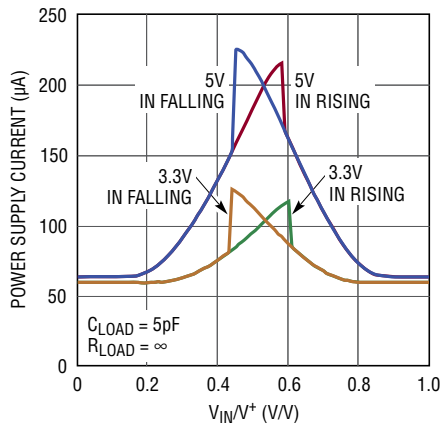
Supply Current vs Supply Voltage



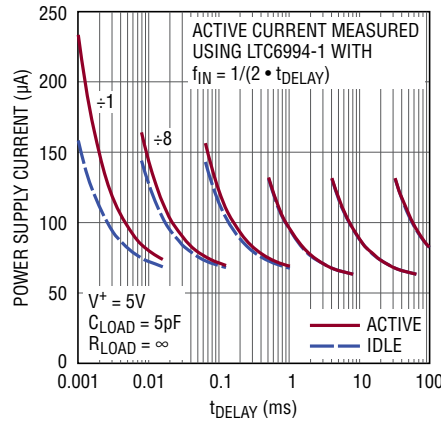
Supply Current vs Temperature



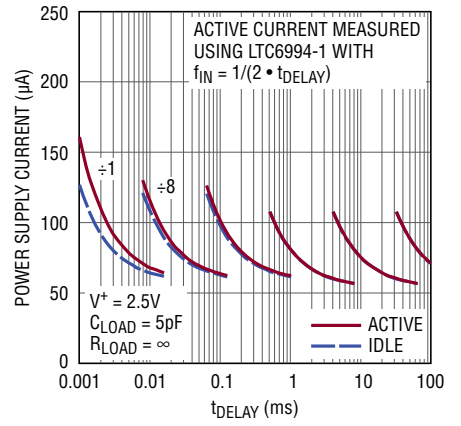
Supply Current vs IN Pin Voltage



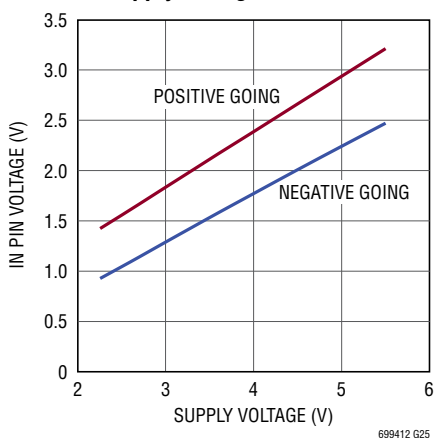
Supply Current vs  $t_{DELAY}$  (5V)



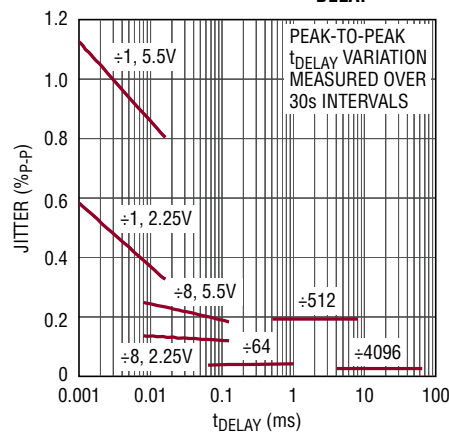
Supply Current vs  $t_{DELAY}$  (2.5V)



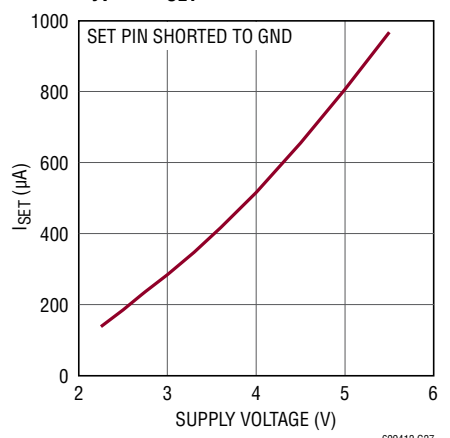
IN Threshold Voltage vs Supply Voltage



Peak-to-Peak Jitter vs  $t_{DELAY}$



Typical  $I_{SET}$  Current Limit vs  $V^+$

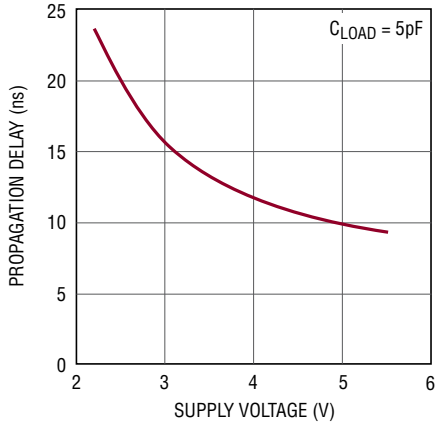




# TYPICAL PERFORMANCE CHARACTERISTICS

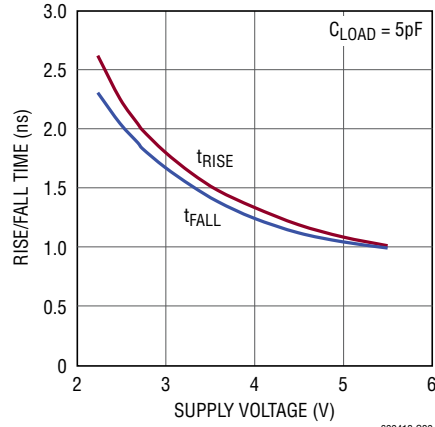
$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

**Input Propagation Delay ( $t_{PD}$ ) vs Supply Voltage**



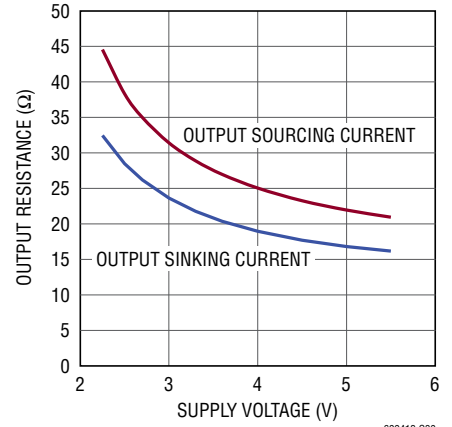
699412 G28

**Rise and Fall Time vs Supply Voltage**



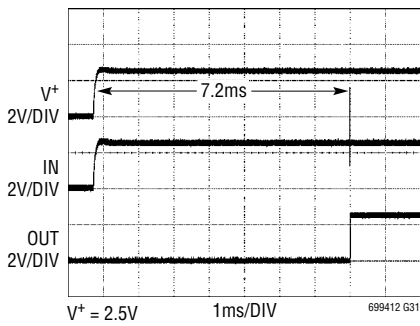
699412 G29

**Output Resistance vs Supply Voltage**



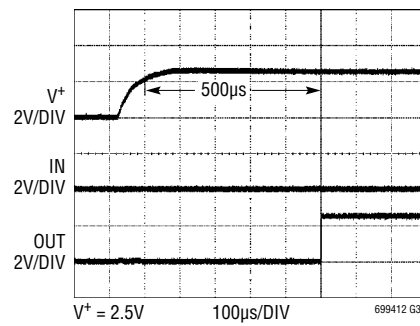
699412 G30

**Start-Up,  $R_{SET} = 800k$  (LTC6994-1)**



699412 G31

**Start-Up,  $R_{SET} = 50k$  (LTC6994-2, POL = 1)**



699412 G32

## PIN FUNCTIONS (DCB/S6)

**V<sup>+</sup> (Pin 1/Pin 5):** Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1μF capacitor.

**DIV (Pin 2/Pin 4):** Programmable Divider and Polarity Input. The DIV pin voltage ( $V_{DIV}$ ) is internally converted into a 4-bit result (DIVCODE).  $V_{DIV}$  may be generated by a resistor divider between V<sup>+</sup> and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that  $V_{DIV}$  settles quickly. The MSB of DIVCODE (POL) selects the delay functionality. For the LTC6994-1, POL = 0 will delay the rising transition and POL = 1 will delay the falling transition. For the LTC6994-2, both transitions are delayed so POL = 1 can be used to invert the output.

**SET (Pin 3/Pin 3):** Delay Setting Input. The voltage on the SET pin ( $V_{SET}$ ) is regulated to 1V above GND. The amount of current sourced from the SET pin ( $I_{SET}$ ) programs the master oscillator frequency. The  $I_{SET}$  current range is 1.25μA to 20μA. The delayed output transition will be not occur if  $I_{SET}$  drops below approximately 500nA. Once  $I_{SET}$  increases above 500nA the delayed edge will transition.

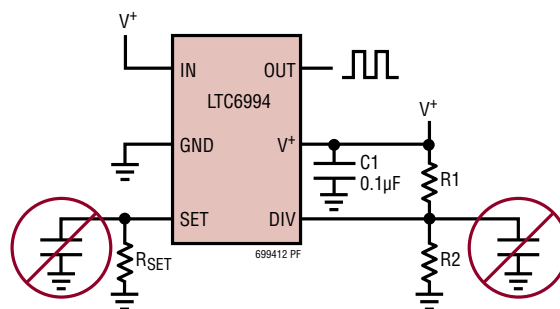
A resistor connected between SET and GND is the most accurate way to set the delay. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the  $V_{SET}$  voltage.

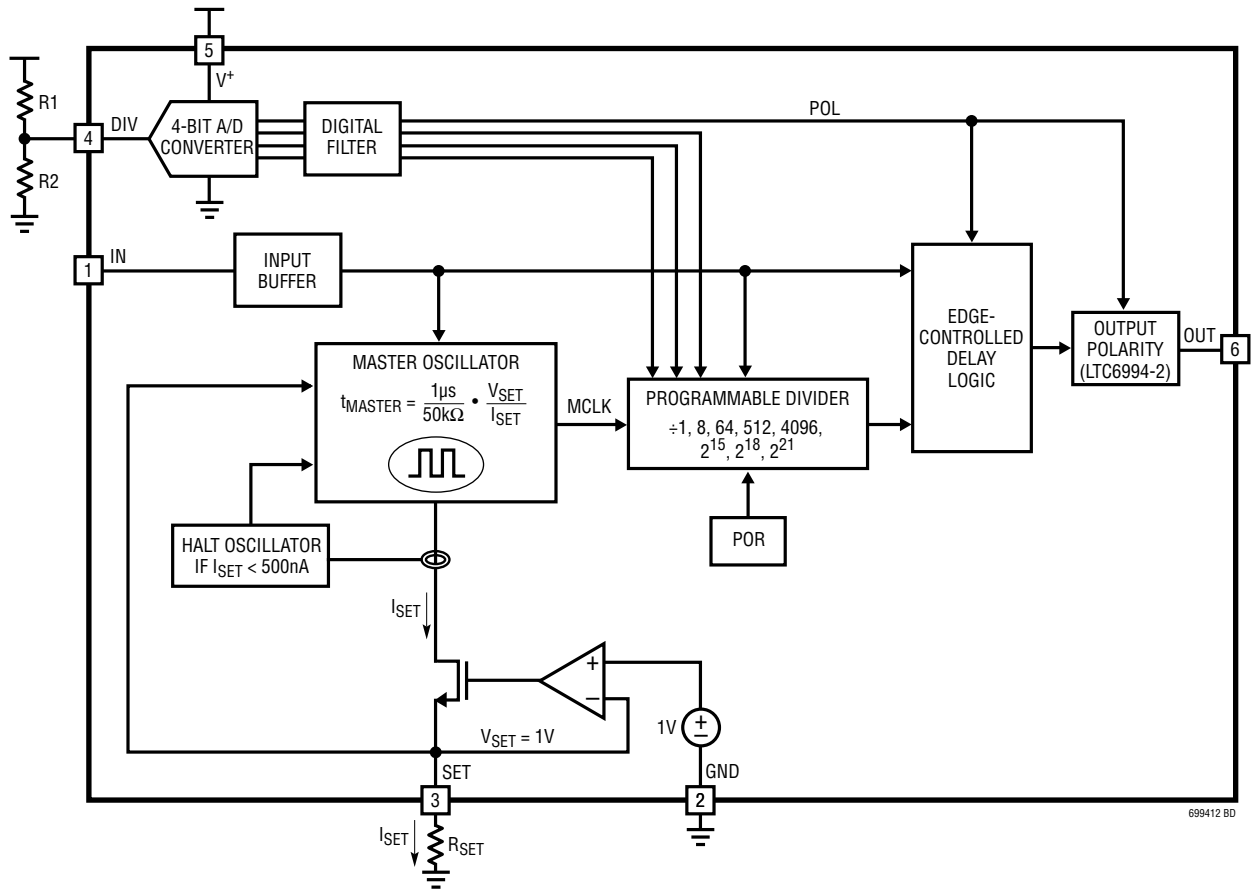
**IN (Pin 4/Pin 1):** Logic Input. Depending on the version and POL bit setting, rising or falling edges on IN will propagate to OUT after a programmable delay. The LTC6994-1 will delay only the rising or falling edge. The LTC6994-2 will delay both edges.

**GND (Pin 5/Pin 2):** Ground. Tie to a low inductance ground plane for best performance.

**OUT (Pin 6/Pin 6):** Output. The OUT pin swings from GND to V<sup>+</sup> with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.



**BLOCK DIAGRAM** (S6 package pin numbers shown)



699412 BD

## OPERATION

The LTC6994 is built around a master oscillator with a 1μs minimum period. The oscillator is controlled by the SET pin current ( $I_{SET}$ ) and voltage ( $V_{SET}$ ), with a 1μs/50kΩ conversion factor that is accurate to ±1.7% under typical conditions.

$$t_{MASTER} = \frac{1\mu s}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}}$$

A feedback loop maintains  $V_{SET}$  at 1V ±30mV, leaving  $I_{SET}$  as the primary means of controlling the input-to-output delay. The simplest way to generate  $I_{SET}$  is to connect a resistor ( $R_{SET}$ ) between SET and GND, such that  $I_{SET} = V_{SET}/R_{SET}$ . The master oscillator equation reduces to:

$$t_{MASTER} = 1\mu s \cdot \frac{R_{SET}}{50k\Omega}$$

From this equation, it is clear that  $V_{SET}$  drift will not affect the input-to-output delay when using a single program resistor ( $R_{SET}$ ). Error sources are limited to  $R_{SET}$  tolerance and the inherent accuracy  $\Delta t_{DELAY}$  of the LTC6994.

$R_{SET}$  may range from 50k to 800k (equivalent to  $I_{SET}$  between 1.25μA and 20μA).

When the input makes a transition that will be delayed (as determined by the part version and POL bit setting), the master oscillator is enabled to time the delay. When the desired duration is reached, the output is allowed to transition.

The LTC6994 also includes a programmable frequency divider which can further divide the frequency by 1, 8, 64, 512, 4096,  $2^{15}$ ,  $2^{18}$  or  $2^{21}$ . This extends the delay duration by those same factors. The divider ratio  $N_{DIV}$  is set by a resistor divider attached to the DIV pin.

$$t_{DELAY} = \frac{N_{DIV}}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}} \cdot 1\mu s$$

With  $R_{SET}$  in place of  $V_{SET}/I_{SET}$  the equation reduces to:

$$t_{DELAY} = \frac{N_{DIV} \cdot R_{SET}}{50k\Omega} \cdot 1\mu s$$

## DIVCODE

The DIV pin connects to an internal,  $V^+$  referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6994:

1. DIVCODE determines the frequency divider setting,  $N_{DIV}$ .
2. The DIVCODE MSB is the POL bit, and configures a different polarity setting on the two versions.
  - a. LTC6994-1: POL selects rising or falling-edge delays. POL = 0 will delay rising-edge transitions. POL = 1 will delay falling-edge transitions.
  - b. LTC6994-2: POL selects the output inversion. POL = 1 inverts the output signal.

$V_{DIV}$  may be generated by a resistor divider between  $V^+$  and GND as shown in Figure 1.

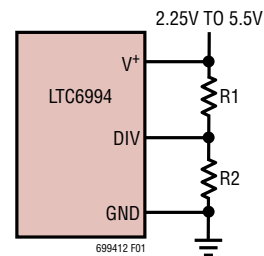


Figure 1. Simple Technique for Setting DIVCODE

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding  $N_{DIV}$  and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The  $V_{DIV}/V^+$  ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)
2. The driving impedance ( $R1 || R2$ ) does not exceed 500kΩ.

## OPERATION

If the voltage is generated by other means (i.e., the output of a DAC) it must track the V<sup>+</sup> supply voltage. The last column in Table 1 shows the ideal ratio of V<sub>DIV</sub> to the supply voltage, which can also be calculated as:

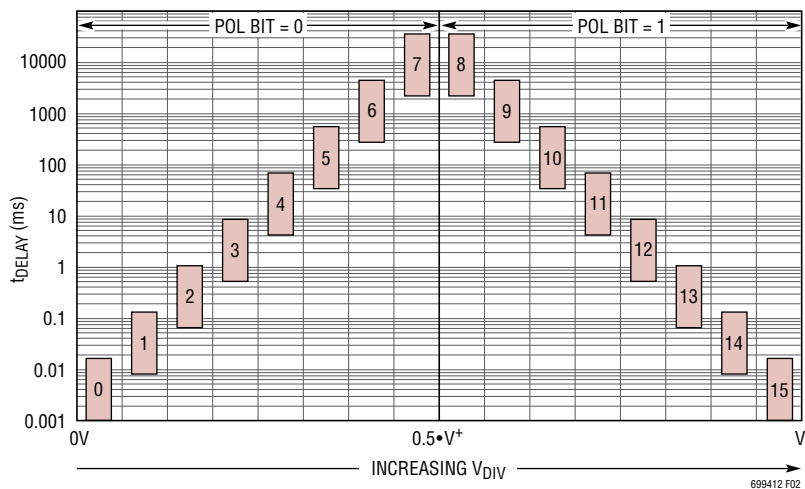
$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V<sub>DIV</sub> = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N<sub>DIV</sub> is symmetric around the DIVCODE midpoint.

**Table 1. DIVCODE Programming**

DIVCODE	POL	N <sub>DIV</sub>	Recommended t <sub>DELAY</sub>	R1 (k)	R2 (k)	V <sub>DIV</sub> /V <sup>+</sup>
0	0	1	1μs to 16μs	Open	Short	≤ 0.03125 ±0.015
1	0	8	8μs to 128μs	976	102	0.09375 ±0.015
2	0	64	64μs to 1.024ms	976	182	0.15625 ±0.015
3	0	512	512μs to 8.192ms	1000	280	0.21875 ±0.015
4	0	4,096	4.096ms to 65.54ms	1000	392	0.28125 ±0.015
5	0	32,768	32.77ms to 524.3ms	1000	523	0.34375 ±0.015
6	0	262,144	262.1ms to 4.194sec	1000	681	0.40625 ±0.015
7	0	2,097,152	2.097sec to 33.55sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2.097sec to 33.55sec	887	1000	0.53125 ±0.015
9	1	262,144	262.1ms to 4.194sec	681	1000	0.59375 ±0.015
10	1	32,768	32.77ms to 524.3ms	523	1000	0.65625 ±0.015
11	1	4,096	4.096ms to 65.54ms	392	1000	0.71875 ±0.015
12	1	512	512μs to 8.192ms	280	1000	0.78125 ±0.015
13	1	64	64μs to 1.024ms	182	976	0.84375 ±0.015
14	1	8	8μs to 128μs	102	976	0.90625 ±0.015
15	1	1	1μs to 16μs	Short	Open	≥ 0.96875 ±0.015



**Figure 2. Delay Range and POL Bit vs DIVCODE**

## OPERATION

### Edge-Controlled Delay

The LTC6994 is a programmable delay or pulse qualifier. It can perform noise filtering, which distinguishes it from a delay line (which simply delays all input transitions).

When the voltage on the LTC6994 input pin (IN) transitions low or high, the LTC6994 can delay the corresponding output transition by any time from 1 $\mu$ s to 33.6 seconds.

### LTC6994-1 Functionality

Figure 3 details the basic operation of the LTC6994-1 when configured to delay rising edge transitions (POL = 0). A rising edge on the IN pin initiates the timing. OUT remains

low for the duration of  $t_{DELAY}$ . If IN stays high then OUT will transition high after this time. If the input doesn't remain high long enough for OUT to transition high then the timing will restart on each successive rising edge. In this way, the LTC6994-1 can serve as a pulse qualifier, filtering out noisy or short signals.

On a falling edge at the input, the output will follow immediately (after a short propagation delay  $t_{PD}$ ). Note that the output pulse width may be extremely short if IN falls immediately after OUT rises.

Figure 4 details the operation of the LTC6994-1 when configured to delay falling edges (POL = 1).

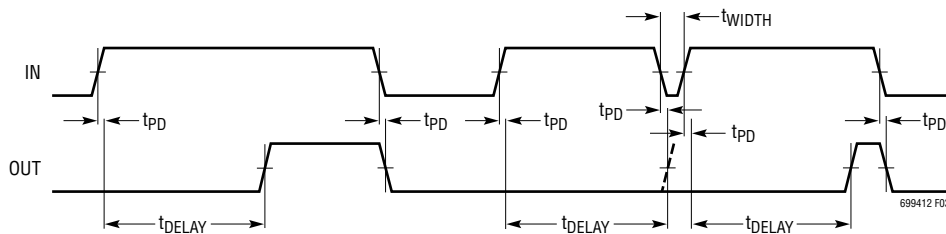


Figure 3. Rising-Edge Delayed Timing Diagram (LTC6994-1, POL = 0)

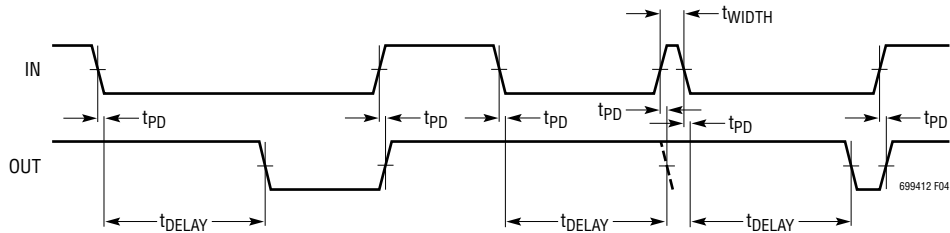


Figure 4. Falling-Edge Delayed Timing Diagram (LTC6994-1, POL = 1)

## OPERATION

### LTC6994-2 Functionality

Figure 5 details the basic operation of the LTC6994-2 when configured for noninverting operation ( $POL = 0$ ). As before, a rising edge on the IN pin initiates the timing and, if IN remains high, OUT will transition high after  $t_{DELAY}$ .

Unlike the LTC6994-1, falling edges are delayed in the same way. When IN transitions low, OUT will follow after  $t_{DELAY}$ .

If the input doesn't remain high or low long enough for OUT to follow, the timing will restart on the next transition.

Also unlike the LTC6994-1, the output pulse width can never be less than  $t_{DELAY}$ . Therefore, the LTC6994-2 can generate pulses with a defined minimum width.

Figure 6 details the operation of the LTC6994-2 when the output is inverted ( $POL = 1$ ).

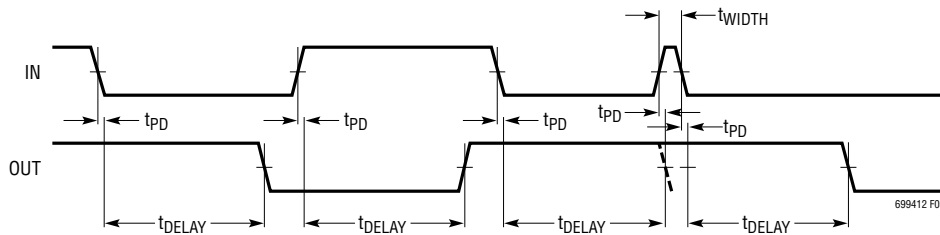


Figure 5. Both Edges Delayed Timing Diagram (LTC6994-2,  $POL = 0$ )

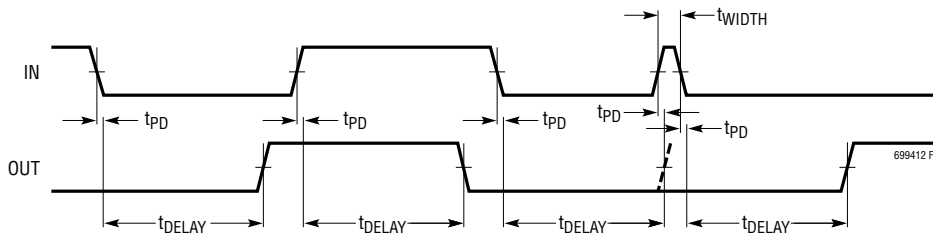


Figure 6. Both Edges Delayed (Inverting) Timing Diagram (LTC6994-2,  $POL = 1$ )

## OPERATION

### Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring  $V_{DIV}$  for changes. Changes to DIVCODE will be recognized slowly, as the LTC6994 places a priority on eliminating any “wandering” in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \cdot (\Delta DIVCODE + 6) \cdot t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. However, if the delay timing is active during the transition, the actual delay can take on a value between the two settings.

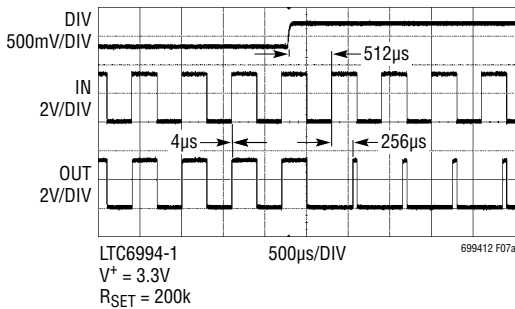


Figure 7a. DIVCODE Change from 0 to 2

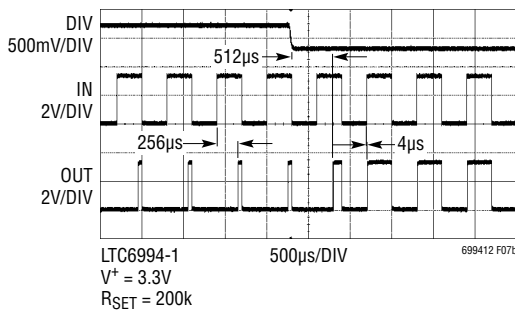


Figure 7b. DIVCODE Change from 2 to 0

### Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time,  $t_{START}$ . The OUT pin is held low during this time and the IN pin has no control over the output. The typical value for  $t_{START}$  ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of  $N_{DIV}$ ):

$$t_{START(TYP)} = 500 \cdot t_{MASTER}$$

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the LTC6994 can respond to an input. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track  $V^+$ . Less than 100pF will not extend the start-up time.

At the end of  $t_{START}$  the DIVCODE and IN pin settings are recognized, and the state of the IN pin is transferred to the output (without additional delay). If IN is high at the end of  $t_{START}$ , OUT will go high. Otherwise OUT will remain low. The LTC6994-2 with POL = 1 is the exception because it inverts the signal. At this point, the LTC6994 is ready to respond to rising/falling edges on the input.

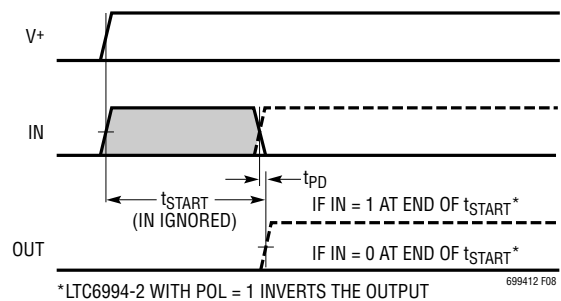


Figure 8. Start-Up Timing Diagram



## APPLICATIONS INFORMATION

### Basic Operation

The simplest and most accurate method to program the LTC6994 is to use a single resistor,  $R_{SET}$ , between the SET and GND pins. The design procedure is a 3-step process. Alternatively, Linear Technology offers the easy-to-use TimerBlox Designer tool to quickly design any LTC6994 based circuit. Use the free [TimerBlox LTC6994: Delay Web-Based Design Tool](#).

#### Step 1: Select the LTC6994 Version and POL Bit Setting.

Choose LTC6994-1 to delay one (rising or falling) input transition. The POL bit then defines which edge is to be delayed. POL = 0 delays rising edges. POL = 1 delays falling edges.

Choose LTC6994-2 to delay rising and falling edges. Set POL = 0 for normal operation, or POL = 1 to invert the output.

#### Step 2: Select the $N_{DIV}$ Frequency Divider Value.

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the  $N_{DIV}$  value. For a given delay time ( $t_{DELAY}$ ),  $N_{DIV}$  should be selected to be within the following range:

$$\frac{t_{DELAY}}{16\mu s} \leq N_{DIV} \leq \frac{t_{DELAY}}{1\mu s} \quad (1)$$

To minimize supply current, choose the lowest  $N_{DIV}$  value. However, in some cases a higher value for  $N_{DIV}$  will provide better accuracy (see Electrical Characteristics).

Table 1 can also be used to select the appropriate  $N_{DIV}$  values for the desired  $t_{DELAY}$ .

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or  $V_{DIV}/V^+$  ratio to apply to the DIV pin.

#### Step 3: Calculate and Select $R_{SET}$ .

The final step is to calculate the correct value for  $R_{SET}$  using the following equation:

$$R_{SET} = \frac{50k}{1\mu s} \cdot \frac{t_{DELAY}}{N_{DIV}} \quad (2)$$

Select the standard resistor value closest to the calculated value.

*Example:* Design a circuit to delay falling edges by  $t_{DELAY} = 100\mu s$  with minimum power consumption.

#### Step 1: Select the LTC6994 Version and POL Bit Setting.

To delay negative transitions, choose the LTC6994-1 with POL = 1.

#### Step 2: Select the $N_{DIV}$ Frequency Divider Value.

Choose an  $N_{DIV}$  value that meets the requirements of Equation (1), using  $t_{DELAY} = 100\mu s$ :

$$6.25 \leq N_{DIV} \leq 100$$

Potential settings for  $N_{DIV}$  include 8 and 64.  $N_{DIV} = 8$  is the best choice, as it minimizes supply current by using a large  $R_{SET}$  resistor. POL = 1 and  $N_{DIV} = 8$  requires DIVCODE = 14. Using Table 1, choose  $R1 = 102k$  and  $R2 = 976k$  values to program DIVCODE = 14.

#### Step 3: Select $R_{SET}$ .

Calculate the correct value for  $R_{SET}$  using Equation (2).

$$R_{SET} = \frac{50k}{1\mu s} \cdot \frac{100\mu s}{8} = 625k$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a  $-0.97\%$  shift in  $t_{DELAY}$  is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 9.

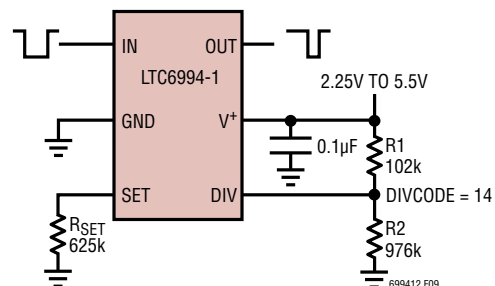


Figure 9. 100µs Negative-Edge Delay

## APPLICATIONS INFORMATION

### Voltage-Controlled Delay

With one additional resistor, the LTC6994 output delay can be manipulated by an external voltage. As shown in Figure 10, voltage  $V_{CTRL}$  sources/sinks a current through  $R_{MOD}$  to vary the  $I_{SET}$  current, which in turn modulates the delay as described in Equation (3):

$$t_{DELAY} = \frac{N_{DIV} \cdot R_{MOD}}{50k\Omega} \cdot \frac{1\mu s}{1 + \frac{R_{MOD}}{R_{SET}} - \frac{V_{CTRL}}{V_{SET}}} \quad (3)$$

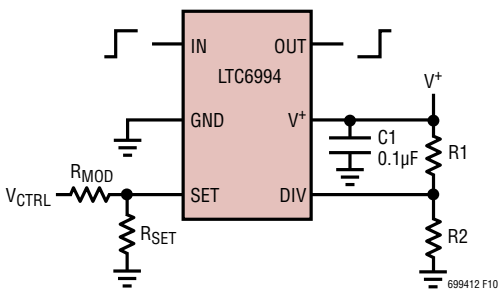


Figure 10. Voltage-Controlled Delay

### Digital Delay Control

The control voltage can be generated by a DAC (digital-to-analog converter), resulting in a digitally-controlled delay. Many DACs allow for the use of an external reference. If such a DAC is used to provide the  $V_{CTRL}$  voltage, the  $V_{SET}$  dependency can be eliminated by buffering  $V_{SET}$  and using it as the DAC's reference voltage, as shown in Figure 11. The DAC's output voltage now tracks any  $V_{SET}$  variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC's REF input would affect the delay.

### $I_{SET}$ Extremes (Master Oscillator Frequency Extremes)

When operating with  $I_{SET}$  outside of the recommended 1.25µA to 20µA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for  $I_{SET} < 1.25\mu A$ . At approximately 500nA, the oscillator will stop. Under this condition, the delay timing can still be initiated, but will not terminate until  $I_{SET}$  increases and the master oscillator starts again.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

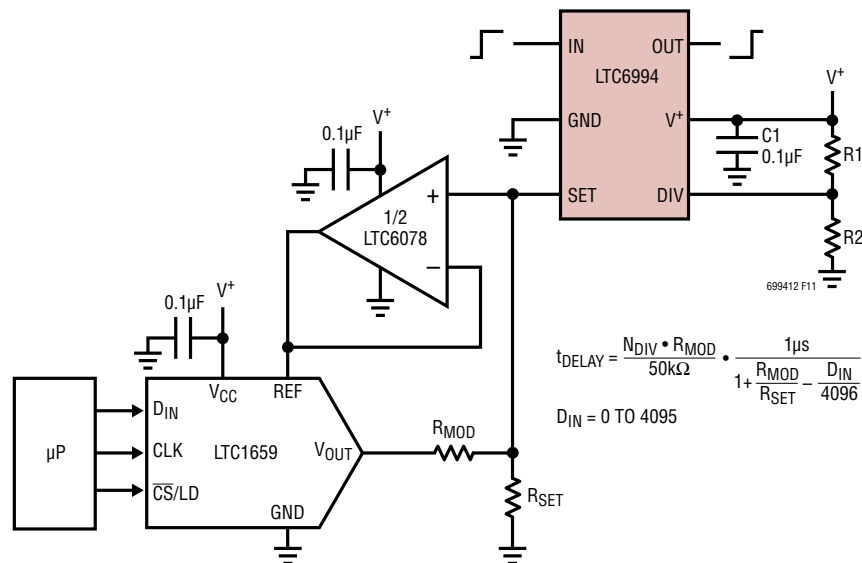


Figure 11. Digitally Controlled Delay

## APPLICATIONS INFORMATION

### Settling Time

Following a  $2\times$  or  $0.5\times$  step change in  $I_{SET}$ , the output delay takes approximately six master clock cycles ( $6 \cdot t_{MASTER}$ ) to settle to within 1% of the final value. An example is shown in Figure 12, using the circuit in Figure 10.

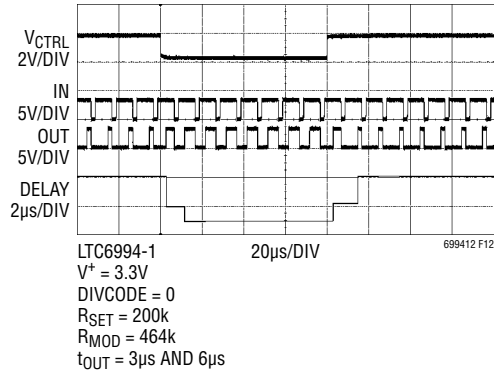


Figure 12. Typical Settling Time

### Coupling Error

The current sourced by the SET pin is used to bias the internal master oscillator. The LTC6994 responds to changes in  $I_{SET}$  almost immediately, which provides excellent settling time. However, this fast response also makes the SET pin sensitive to coupling from digital signals, such as the IN input.

Even an excellent layout will allow *some* coupling between IN and SET. Additional error is included in the specified accuracy for  $N_{DIV} = 1$  to account for this. Figure 13 shows that  $\pm 1$  supply variation is dependent on coupling from rising or falling inputs.

A very poor layout can actually degrade performance further. The PCB layout should avoid routing SET next to IN (or any other fast-edge, wide-swing signal).

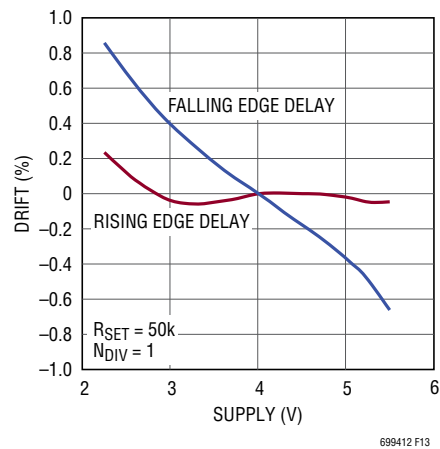


Figure 13. Delay Drift vs Supply Voltage

## APPLICATIONS INFORMATION

### Power Supply Current

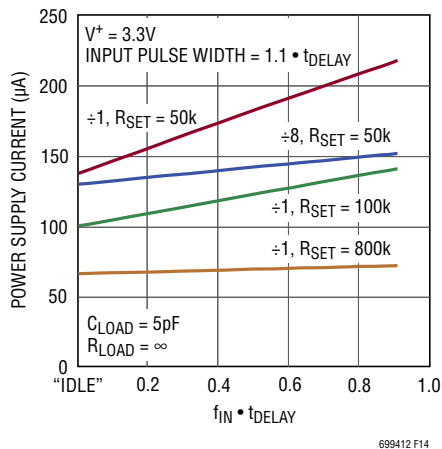
The Electrical Characteristics table specifies the supply current while the part is idle (waiting for an input transition).  $I_{S(IDLE)}$  varies with the programmed  $t_{DELAY}$  and the supply voltage, as described by the equations in Table 2, valid for both the LTC6994-1 and LTC6994-2.

**Table 2. Approximate Idle Supply Current Equations**

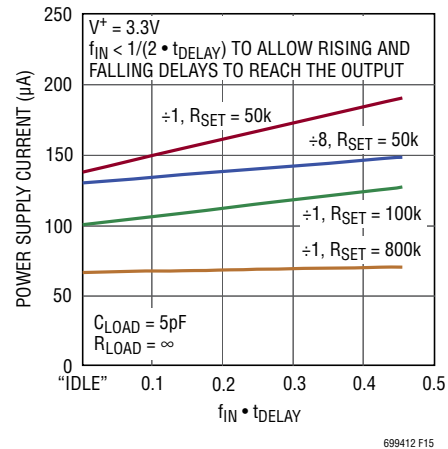
CONDITION	TYPICAL $I_{S(IDLE)}$
$N_{DIV} \leq 64$	$\frac{V^+ \cdot (N_{DIV} \cdot 7pF + 4pF)}{t_{DELAY}} + \frac{V^+}{500k\Omega} + 2.2 \cdot I_{SET} + 50\mu A$
$N_{DIV} \geq 512$	$\frac{V^+ \cdot N_{DIV} \cdot 7pF}{t_{DELAY}} + \frac{V^+}{500k\Omega} + 1.8 \cdot I_{SET} + 50\mu A$

When an input transition starts the delay timing circuitry, the instantaneous supply current increases to  $I_{S(ACTIVE)}$ .

$$I_{S(ACTIVE)} = I_{S(IDLE)} + \Delta I_{S(ACTIVE)}$$



**Figure 14.  $I_{S(ACTIVE)}$  vs Input Frequency, LTC6994-1**



**Figure 15.  $I_{S(ACTIVE)}$  vs Input Frequency, LTC6994-2**

$\Delta I_{S(ACTIVE)}$  can be estimated using the equations in Table 3, assuming a periodic input with frequency  $f_{IN}$ . The equations assume the input pulse width is greater than  $t_{DELAY}$ ; otherwise, the output will not transition (and the increase in supply current will be less).

**Table 3. Active Increase in Supply Current**

CONDITION	DEVICE	TYPICAL $\Delta I_{S(ACTIVE)}$ *
$N_{DIV} \leq 64$	LTC6994-1	$f_{IN} \cdot V^+ \cdot (N_{DIV} \cdot 5pF + 18pF + C_{LOAD})$
	LTC6994-2	$f_{IN} \cdot V^+ \cdot (N_{DIV} \cdot 10pF + 22pF + C_{LOAD})$
$N_{DIV} \geq 512$	Either Version	$f_{IN} \cdot V^+ \cdot C_{LOAD}$

\* Ignoring resistive loads (assumes  $R_{LOAD} = \infty$ )

Figures 14 and 15 show how the supply current increases from  $I_{S(IDLE)}$  as the input frequency increases. At higher  $N_{DIV}$  settings, the increase in active current is smaller.

## APPLICATIONS INFORMATION

### Supply Bypassing and PCB Layout Guidelines

The LTC6994 is an accurate monostable multivibrator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 16 shows example PCB layouts for both the SOT-23 and DCB packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6994. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V<sup>+</sup> and GND pins using a low inductance path. The connection from C1 to the V<sup>+</sup> pin is easily done directly on the top layer. For the DCB package, C1's connection to GND is also simply done on the top layer. For the SOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1μF ceramic capacitor.

2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R<sub>SET</sub> as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the output delay. Having a short connection minimizes the exposure to signal pickup.
4. Connect R<sub>SET</sub> directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

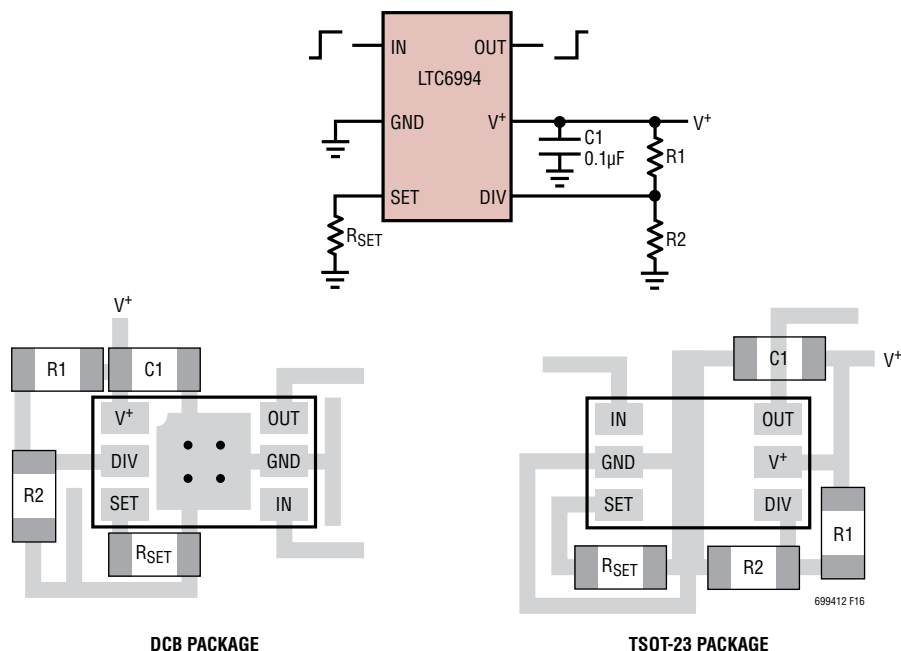
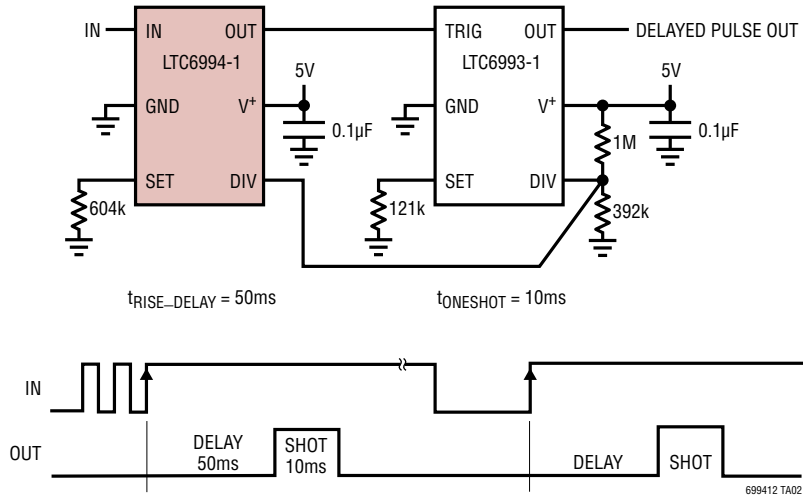


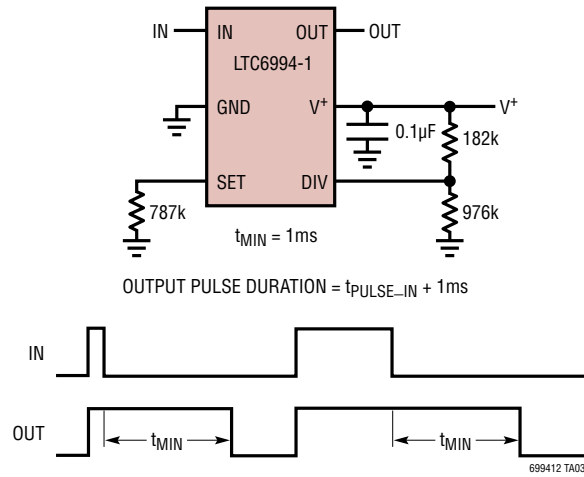
Figure 16. Supply Bypassing and PCB Layout

## TYPICAL APPLICATIONS

### Delayed One-Shot

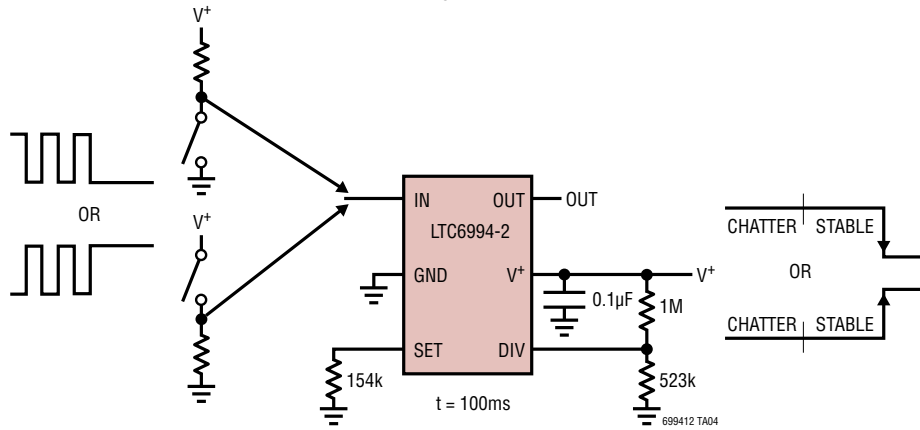


### Pulse Stretcher



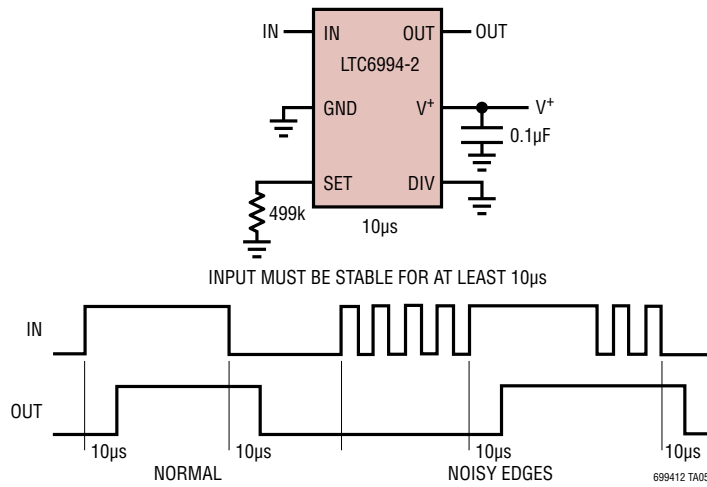
# TYPICAL APPLICATIONS

## Switch/Relay Debouncer



OUTPUT GOES TO SAME FINAL LEVEL OF INPUT AFTER STABLE FOR 100ms

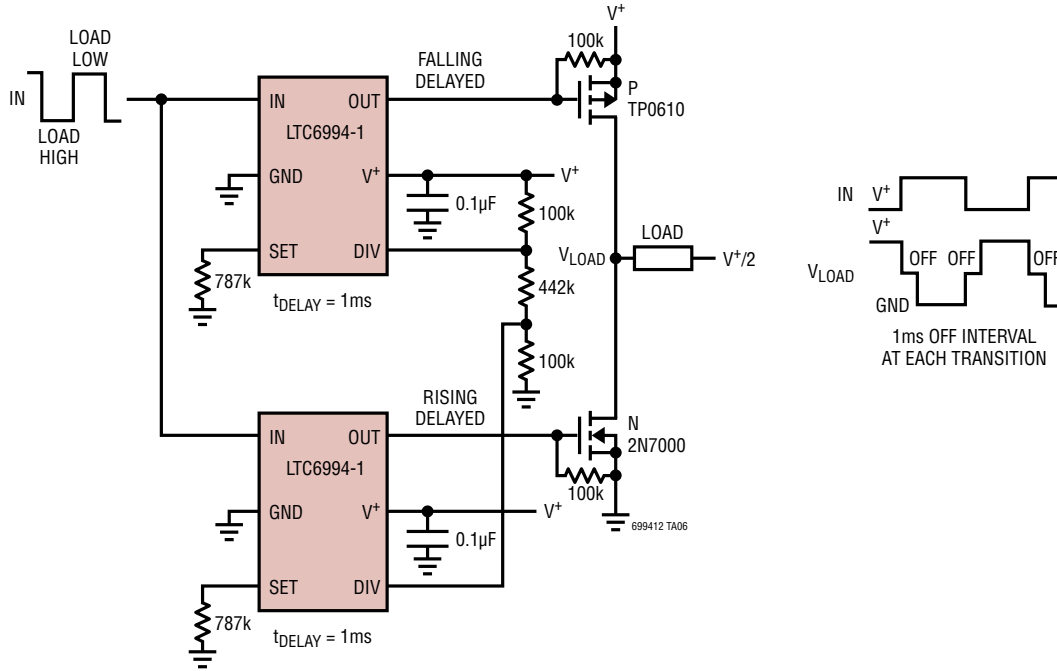
## Edge Chatter Filter



INPUT MUST BE STABLE FOR AT LEAST 10µs

## TYPICAL APPLICATIONS

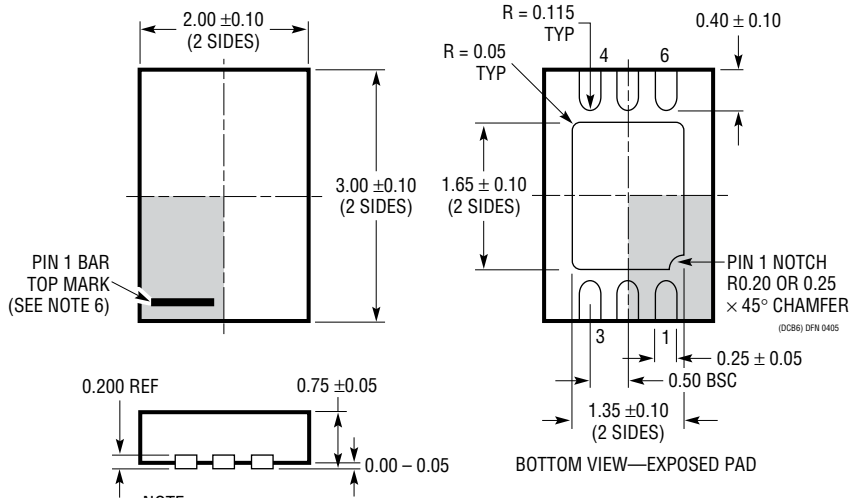
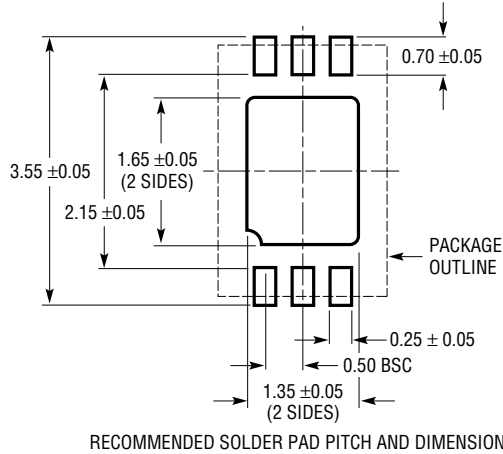
Crossover Gate—Break-Before-Make Interval Timer





# PACKAGE DESCRIPTION

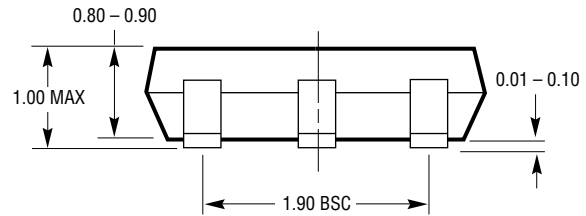
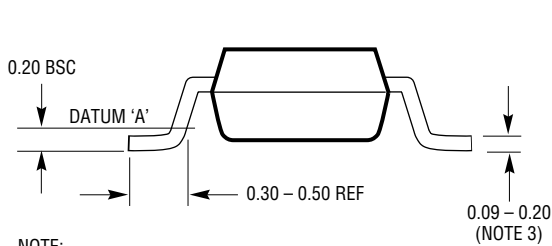
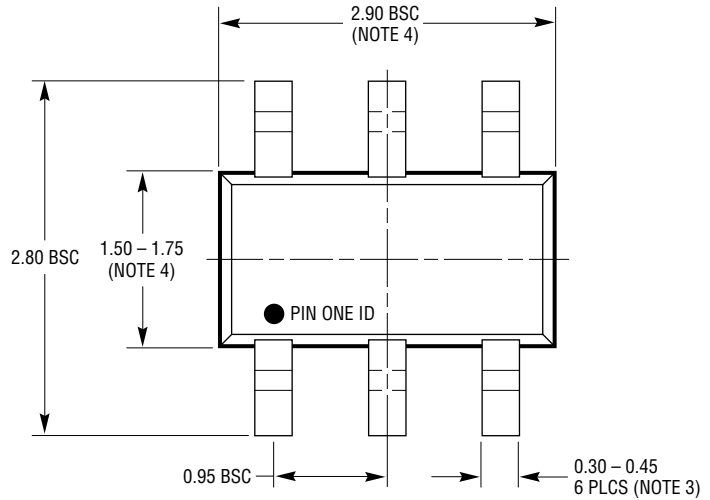
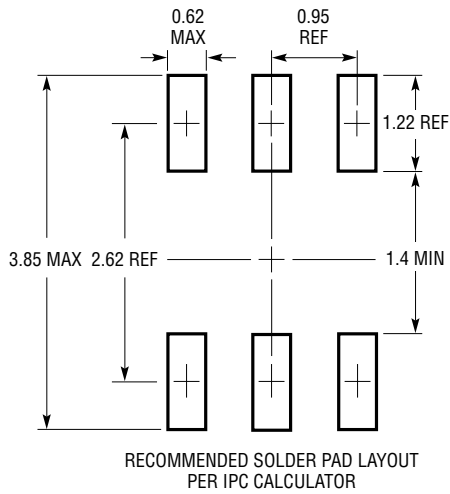
**DCB Package**  
**6-Lead Plastic DFN (2mm × 3mm)**  
 (Reference LTC DWG # 05-08-1715 Rev A)



1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

**S6 Package**  
**6-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1636)



S6 TSOT-23 0302 REV B

- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

**REVISION HISTORY**

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/11	Revised the Description section.	1
		Added text to Basic Operation paragraph in the Applications Information section.	16
B	1/12	Added MP-Grade.	1, 2, 4
		Corrected sizing of the Typical Performance Characteristics curves G31 and G32.	8
C	11/19	Added AEC-Q100 Qualified Note to Front Page	1
		Added W Grade Order Information	3