Fast 60V High Side NMOS Static Switch Driver

FEATURES

- **Wide Operating V_{IN}: Up to 60V**
- **1Ω Pull-Down, 2.2Ω Pull-Up for Fast Turn-On and Turn-Off Times with 35ns Propagation Delays**
- **Internal Charge Pump for 100% Duty Cycle**
- Adjustable Turn-On Slew Rate
- Gate Driver Supply from 3.5V to 15V
- Adjustable V_{IN} Overvoltage Lockout
- Adjustable Driver Supply V_{CC} Undervoltage Lockout
- CMOS Compatible Input
- Thermally Enhanced, High Voltage Capable 10-Lead MSOP Package
- AEC-Q100 Qualified for Automotive Applications

DESCRIPTION

The LTC®7004 is a fast high side N-channel MOSFET gate driver that operates from input voltages up to 60V. It contains an internal charge pump that fully enhances an external N-channel MOSFET switch, allowing it to remain on indefinitely.

Its powerful driver can easily drive large gate capacitances with very short transition times, making it well suited for both high frequency switching applications or static switch applications that require a fast turn-on and/or turn-off time.

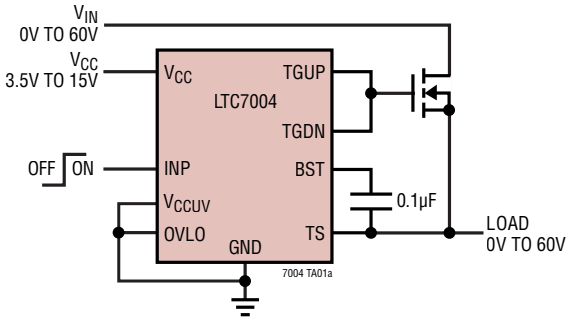
The LTC7004 is available in the thermally-enhanced 10-lead MSOP package.

APPLICATIONS

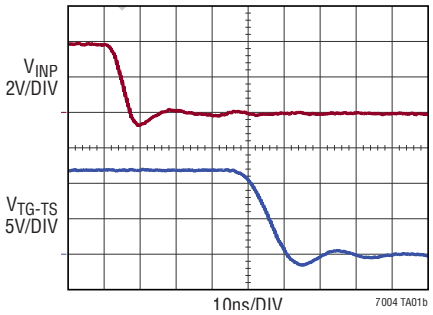
- Static Switch Driver
- Load and Supply Switch Driver
- Electronic Valve Driver
- High Frequency High Side Gate Driver

TYPICAL APPLICATION

High Voltage, High Side Switch with 100% Duty Cycle



LTC7004 Driving a 1nF Capacitive Load



ABSOLUTE MAXIMUM RATINGS

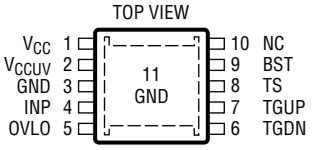
(Note 1)

Supply Voltages
- BST-TS ..... –0.3V to 15V
- V_{CC} ..... –0.3V to 15V

TS Voltage ..... –6V to 65V
BST Voltage ..... –0.3V to 80V
INP Voltage ..... –6V to 15V
Driver Outputs TGUP, TGDN ..... (Note 6)
V_{CCUV} Voltage ..... –0.3 to 6V
OVLO Voltage ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 4)
- LTC7004E, LTC7004I, ... –40°C to 125°C
- LTC7004H, ... –40°C to 150°C
- LTC7004MP ..... –55°C to 150°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
- MSOP Package ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7004EMSE#PBF	LTC7004EMSE#TRPBF	LTHBV	10-Lead Plastic MSOP	–40°C to 125°C
LTC7004IMSE#PBF	LTC7004IMSE#TRPBF	LTHBV	10-Lead Plastic MSOP	–40°C to 125°C
LTC7004HMSE#PBF	LTC7004HMSE#TRPBF	LTHBV	10-Lead Plastic MSOP	–40°C to 150°C
LTC7004MPMSE#PBF	LTC7004MPMSE#TRPBF	LTHBV	10-Lead Plastic MSOP	–55°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC7004IMSE#WPBF	LTC7004IMSE#WTRPBF	LTHBV	10-Lead Plastic MSOP	–40°C to 125°C
LTC7004JMSE#WPBF	LTC7004JMSE#WTRPBF	LTHBV	10-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BST} = 10V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supplies							
	TS Operating Voltage Range			0		60	V
	Total Supply Current (Note 7) ON or Sleep, Charge Pump Regulating	V_{BST} = OPEN, V_{TS} = 12V			225		µA
	V_{CC} Supply Current, Charge Pump Overdriven (Note 5) ON Mode Sleep Mode	V_{BST-TS} = 13V V_{INP} = 4V V_{INP} = 0.4V			27 27	50 50	µA µA
V_{CC} UVLO	V_{CC} Undervoltage Lockout	V_{CCUV} = OPEN V_{CC} Rising V_{CC} Falling Hysteresis V_{CCUV} = 0V V_{CC} Rising V_{CC} Falling Hysteresis V_{CCUV} = 1.5V V_{CC} Rising V_{CC} Falling Hysteresis	 ● ● ● ● 	 6.5 5.8 3.1 2.8 9.7 9.1 	 7.0 6.4 600 3.5 3.2 300 10.5 9.9 600	 7.5 6.9 3.7 3.4 10.9 10.3 	 V V mV V V mV V V mV
Bootstrapped Supply (BST-TS)							
V_{BST-TS}	V_{TG} Above V_{TS} with INP = 3V (DC)	V_{CC} = V_{TS} = 7V, I_{BST} = 0µA V_{CC} = V_{TS} = 10V, I_{BST} = 0µA V_{TS} = 60V, I_{BST} = 0µA	 ● ●	9 10 10	11 12 12	14 14 14	V V V
	Charge Pump Output Current	V_{TS} = 20V, V_{BST-TS} = 10V	●	–15	–30		µA
	BST-TS Floating UVLO	V_{BST-TS} Rising V_{BST-TS} Falling			3.1 2.8		V V
Output Gate Driver (TG)							
	TG Pull-Up Resistance	V_{CC} = V_{BST} = 12V	●		2.2	7	Ω
	TG Pull-Down Resistance	V_{CC} = V_{BST} = 12V	●		1	4	Ω
t_r	Output Rise Time	10% to 90%, CL = 1nF 10% to 90%, CL = 10nF			13 90		ns ns
t_f	Output Fall Time	10% to 90%, CL = 1nF 10% to 90%, CL = 10nF			13 40		ns ns
t_{PLH} t_{PHL}	Input to Output Propagation Delay	V_{INP} Rising, CL = 1nF V_{INP} Falling, CL = 1nF	● ●		35 35	70 70	ns ns
Operation							
V_{IH} V_{IL}	Input Threshold Voltages	V_{INP} Rising V_{INP} Falling Hysteresis	● ●	1.7 1.3	2 1.6 400	2.2 1.8	V V mV
	Input Pull-Down Resistance	V_{INP} = 1V			1		MΩ
	OVLO Pin Threshold Voltage	Rising Falling Hysteresis		1.16 1.05	1.21 1.10 110	1.26 1.15	V V mV
	OVLO Pin Leakage Current	V_{OVLO} = 1.3V		–100	0	100	nA
	V_{VCCUV} Pull-Up Current	V_{VCCUV} = 1V		–11.3	–10	8.7	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7004 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7004E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7004I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC7004H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC7004MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range.

High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} is 45°C/W.

Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

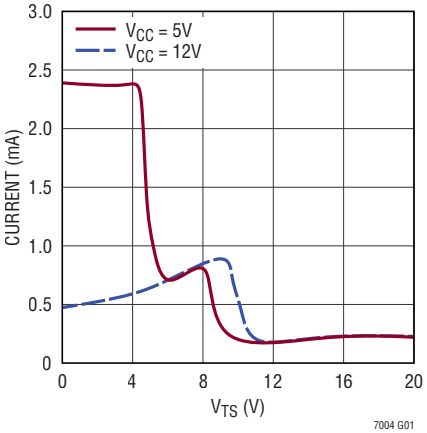
Note 6: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only; otherwise permanent damage may occur.

Note 7: Total supply current is the sum of the current into the VCC and TS pins.

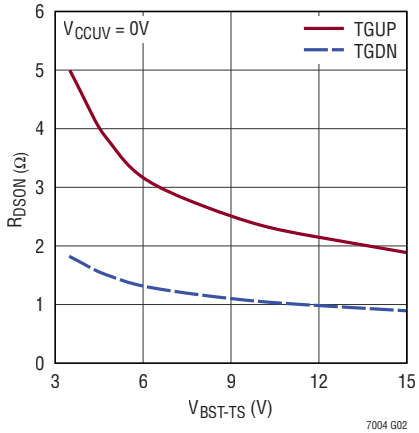
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

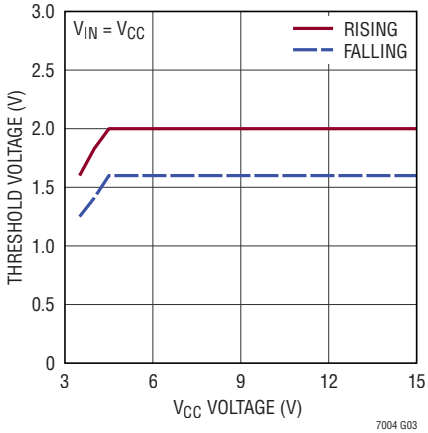
Total Supply Current with External FET ON vs TS Voltage



Driver On Resistance vs V_{BST-TS} Voltage



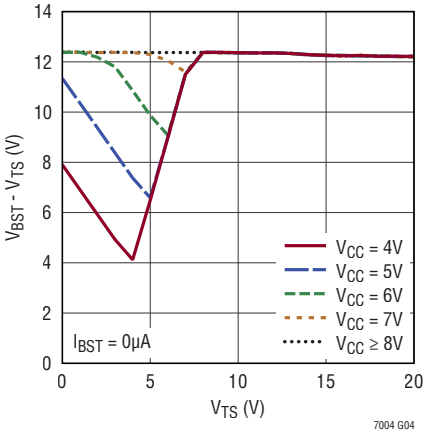
Input Threshold Voltage vs V_{CC} Supply Voltage



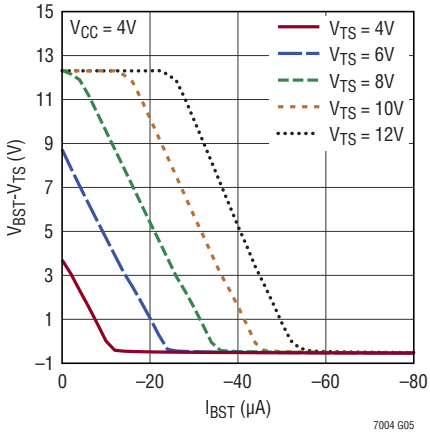
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

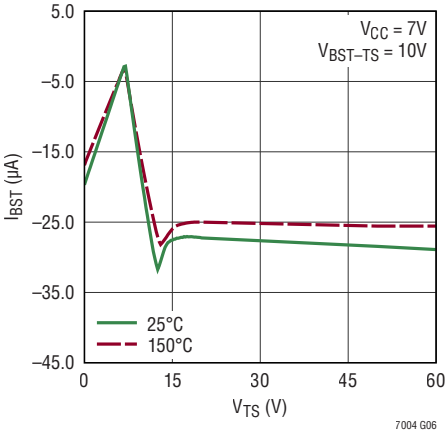
Charge Pump No-Load Output Voltage vs V_{TS}



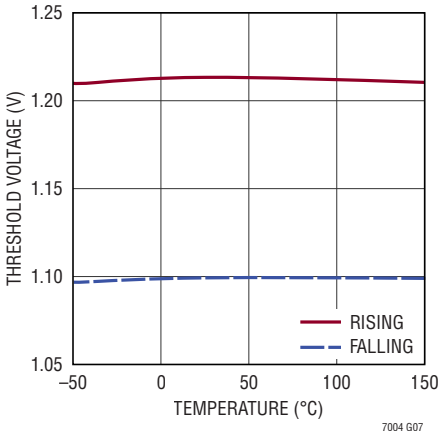
Charge Pump Load Regulation



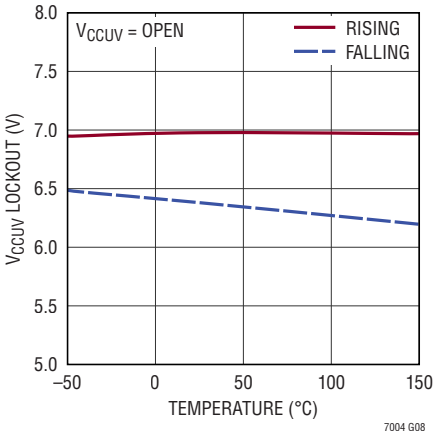
Charge Pump Output Current vs V_{TS}



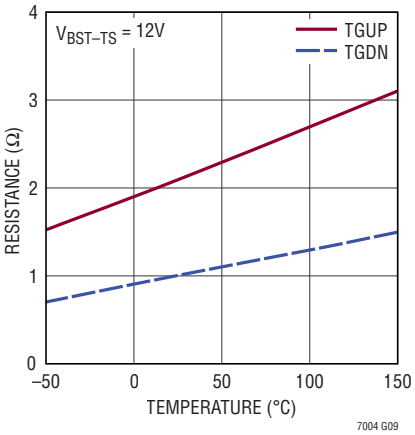
OVLO Threshold Voltage vs Temperature



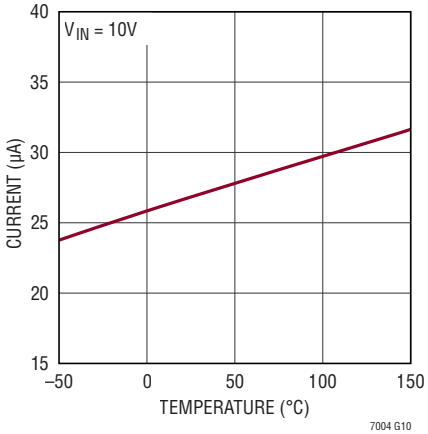
V_{CCUV} Lockout vs Temperature



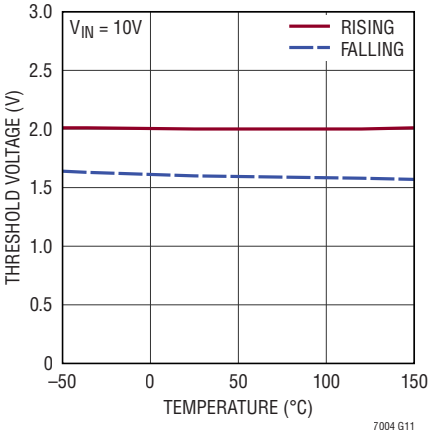
Driver On Resistance vs Temperature



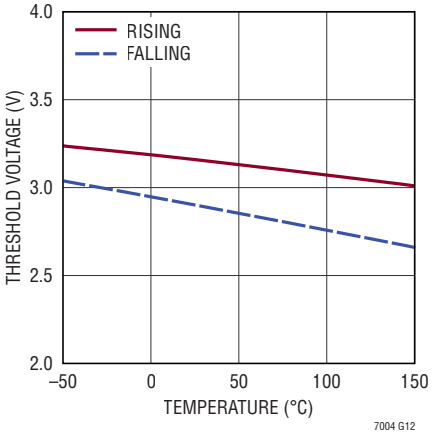
V_{CC} Supply Current vs Temperature



Input Threshold Voltage vs Temperature



V_{BST-TS} Floating UVLO Voltage vs Temperature



PIN FUNCTIONS

V_{CC} (Pin 1): Main Supply Pin. A bypass capacitor with a minimum value of 0.1µF should be tied between this pin and GND.

V_{CCUV} (Pin 2): V_{CC} Supply Undervoltage Lockout. A resistor on this pin sets the reference for the Gate Drive undervoltage lockout. The voltage on this pin in the range of 0.5V to 1.5V is multiplied by seven to be the undervoltage lockout for the Gate Drive (V_{CC} pin). Short to ground to set the minimum gate drive UVLO of 3.5V. Leave open to set gate drive UVLO to 7.0V

GND (Pin 3, Exposed Pad Pin 11): Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

INP (Pin 4): Input Signal. CMOS compatible input reference to GND that sets the state of TGDN and TGUP pins (see Applications Information). INP has an internal 1MΩ pull-down to GND to keep TGDN pulled to TS during startup transients.

OVLO (Pin 5): Overvoltage Lockout Input. Connect to the input supply through a resistor divider to set the lockout level. A voltage on this pin above 1.21V causes TGDN to be pulled to TS. Normal operation resumes when the voltage on this pin decreases below 1.11V. OVLO should be tied to GND when not used.

TGDN (Pin 6): High Current Gate Driver Pull-Down. This pin pulls down to TS. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.

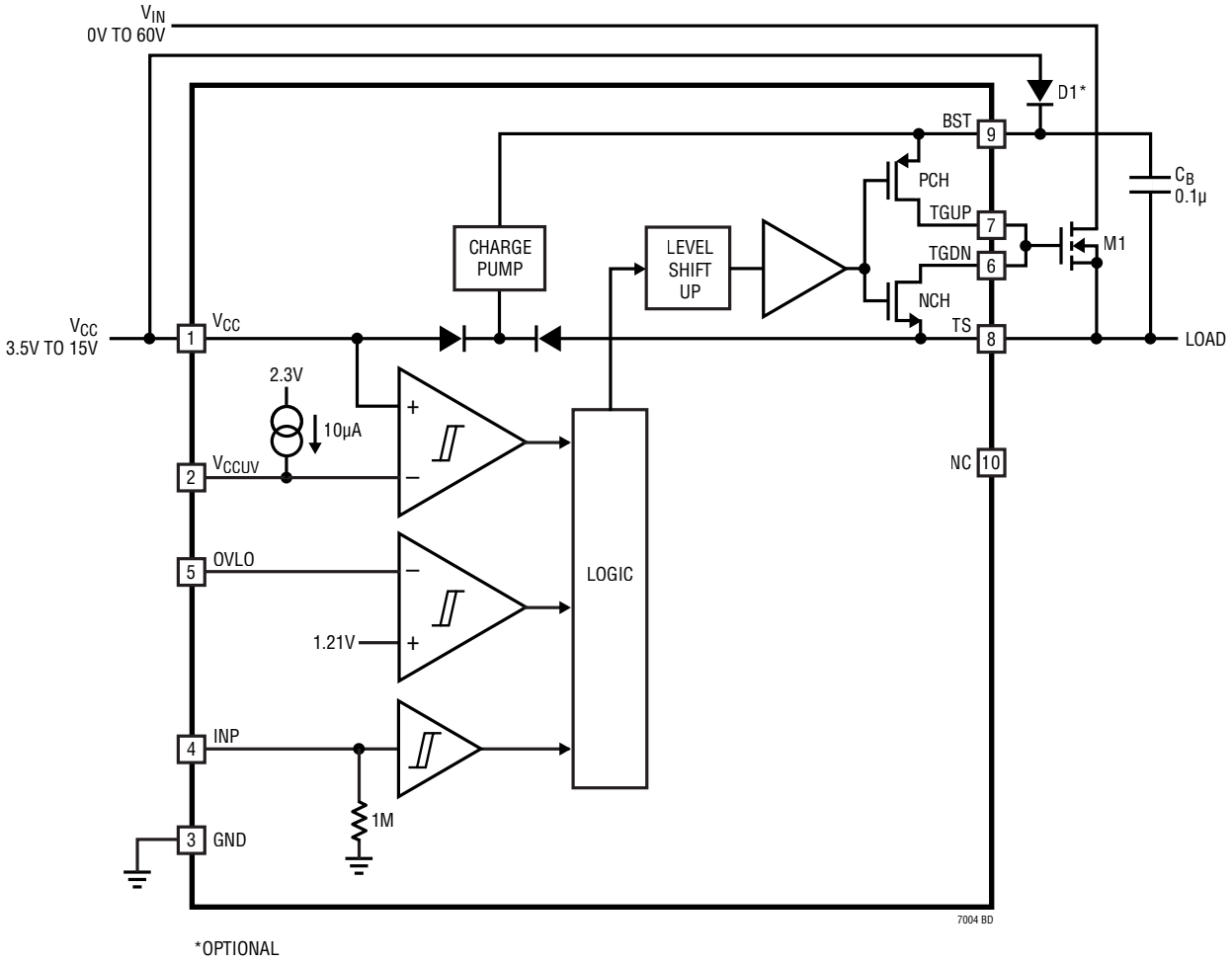
TGUP (Pin 7): High Current Gate Driver Pull-Up. This pin pulls up to BST. Tie this pin to TGDN for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the inrush current during turn-on. See Applications Information.

TS (Pin 8): Top (High Side) source connection or GND if used in ground referenced applications.

BST (Pin 9): High Side Bootstrapped Supply. An external capacitor with a minimum value of 0.1µF should be tied between this pin and TS. Voltage swing on this pin is 12V to (V_{TS} + 12V).

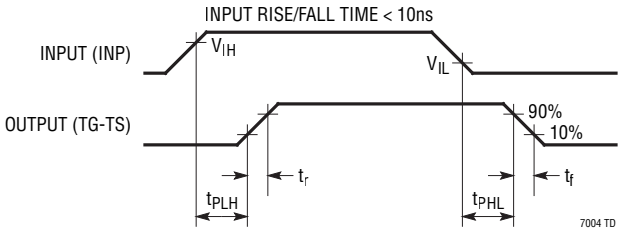
NC (Pin 10): No Connect. This pin should be floated.

BLOCK DIAGRAM



*OPTIONAL

TIMING DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC7004 is designed to receive a ground-referenced, low voltage digital input signal, INP and quickly drive a high side N-channel power MOSFET whose drain can be up to 60V above ground. The LTC7004 is capable of driving a 1nF load using a 12V bootstrapped supply voltage (V_{BST}–V_{TS}) with 35ns of propagation delay and fast rise/fall times. The high gate drive voltage reduces external power losses associated with external MOSFET on-resistance. The strong drivers not only provide fast turn on and off times but hold the TGUP and TGDN to TS voltages in the desired state in the presence of high slew rate transients which can occur driving inductive loads at high voltages.

Internal Charge Pump

The LTC7004 contains an internal charge pump that enables the MOSFET gate drive to have 100% duty cycle. The charge pump regulates the BST-TS voltage to 12V reducing external power losses associated with external MOSFET on-resistance. The charge pump uses the higher voltage of TS or V_{CC} as the source for the charge.

Protection Circuitry

When using the LTC7004, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, the LTC7004 incorporates an overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7004 will enter thermal shutdown mode and TGDN will be pulled to TS. After the part has cooled below 160°C, TGDN will be allowed to go back high. The overtemperature level is not production tested. The LTC7004 is guaranteed to start at temperatures below 150°C.

The LTC7004 additionally implements protection features which prohibit TGDN from going high when V_{CC} or (V_{BST}–V_{TS}) are not within proper operating ranges. By using a resistive divider from V_{IN} to ground the OVLO pin can serve as a precise input supply voltage overvoltage lockout. TGDN is pulled to TS when OVLO rises above 1.21V, so OVLO can be configured to limit switching to a specific range on input supply voltages.

V_{CC} contains an undervoltage lockout feature that will pull TGDN to TS and is configured by the V_{CCUV} pin. If V_{CCUV} is open, TGDN is pulled to TS until V_{CC} is greater than 7.0V. By using a resistor from V_{CCUV} to ground, the rising undervoltage lockout on V_{CC} can be adjusted from 3.5V to 10.5V.

An additional internal undervoltage lockout is included that will pull TGDN to TS when the floating voltage from BST to TS is less than 3.1V (typical).

APPLICATIONS INFORMATION

Input Stage

The LTC7004 employs CMOS compatible input thresholds that allow a low voltage digital signal connected to INP to drive standard power MOSFETs. The LTC7004 contains an internal voltage regulator which biases the input buffer connected to INP allowing the input thresholds (V_{IH} = 2.0V, V_{IL} = 1.6V) to be independent of variations in V_{CC}. The 400mV hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise events. However, care should be taken to keep INP from any noise pickup, especially in high frequency, high voltage applications.

INP also contains an internal 1MΩ pull-down resistor to ground, keeping TGDN pulled to TS during startup and other unknown transient events.

INP has an Absolute Maximum of –6V to +15V which allows the signal driving INP to have voltage excursions outside the normal power supply and ground range. It is not uncommon for signals routed with long PCB traces and driven with fast rise/fall times to inductively ring to voltages higher than power supply or lower than ground.

Output Stage

A simplified version of the LTC7004 output stage is shown in Figure 1. The pull-down device is an N-channel MOSFET with a typical 1Ω $R_{DS(ON)}$ and the pull-up device is a P-channel MOSFET with a typical 2.2Ω $R_{DS(ON)}$. The pull-up and pull-down pins have been separated to allow the turn-on transient to be controlled while maintaining a fast turn-off.

The LTC7004 powerful output stage (1Ω pull-down and 2.2Ω pull-up) minimizes transition losses when driving external MOSFETs and keeps the MOSFET in the state commanded by INP even if high voltage and high frequency transients couple from the power MOSFET back to the driving circuitry.

The large gate drive voltage on TGUP and TGDN reduces conduction losses in the external MOSFET because $R_{DS(ON)}$ is inversely proportional to its gate overdrive ($V_{GS} – V_{TH}$).

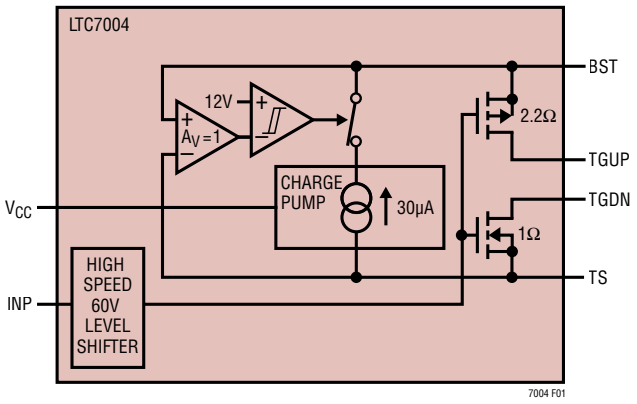


Figure 1. Simplified Output Stage

External Overvoltage Lockout

The OVLO pin can be configured as a precise overvoltage (OVLO) lockout on the V_{IN} supply with a resistive divider from V_{IN} to ground. A simple resistive divider can be used as shown in Figure 2 to meet specific V_{IN} voltage requirements. When OVLO is greater than 1.21V, TGDN will be pulled to TS and the external MOSFET will be turned off.

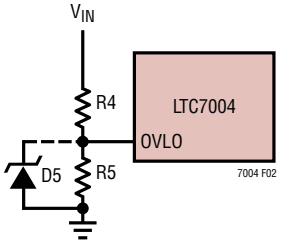


Figure 2. Adjustable OV Lockout

The current that flows through the R4 – R5 divider will directly add to the current drawn from V_{IN} and care should be taken to minimize the impact of this current on the overall current used by the application circuit. Resistor values in the megaohm range may be required to keep the impact of the quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R4 + R5 (R_{TOTAL}) should

APPLICATIONS INFORMATION

be chosen first based on the allowable DC current that can be drawn from V_{IN}. The individual values of R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ OVLO Threshold}}$$

$$R4 = R_{TOTAL} - R5$$

For applications that do not need a precise external OVLO the OVLO pin is required to be tied directly to ground.

Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relationship should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R4 + R5} \right) < 6V$$

If the $V_{IN(MAX)}$ relationship for the OVLO pin cannot be satisfied, an external 5V Zener diode should also be placed from OVLO to ground in addition to any lockout setting resistors.

Bootstrapped Supply (BST-TS)

An external bootstrapped capacitor, C_B, connected between BST and TS supplies the gate drive voltage for the MOSFET driver. The LTC7004 keeps the BST-TS supply charged with an internal charge pump, allowing for duty cycles up to 100 %. When the high side external MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the high side MOSFET and turns it on. The source of the MOSFET, TS, rises to V_{IN} and the BST pin follows. With the high side MOSFET on, the BST voltage is above the input supply; $V_{BST} = V_{TS} + 12V$. The boost capacitor, C_B, supplies the charge to turn on the external MOSFET and needs to have at least 10 times the charge to turn on the external MOSFET fully. The charge to turn on the external MOSFET is referred to gate charge, Q_G, and is typically specified in the external MOSFET data sheet. Gate charge can range from 5nC to hundreds nCs and is influenced by the gate drive level and the type of external MOSFET used. For most applications, a capacitor value of 0.1µF for C_B will be sufficient. However, the following relationship for C_B should be maintained:

$$C_B > \frac{\text{External MOSFET } Q_G}{1V}$$

The internal charge pump that charges the BST-TS supply outputs approximately 30µA to the BST pin. If the time to charge the external bootstrapped capacitor, C_B from initial power-up with the internal charge pump is not sufficient for the application, a low reverse leakage external silicon diode, D1 with a reverse voltage rating greater than V_{IN} connected between V_{CC} and BST should be used as shown in Figure 3. An external silicon diode between V_{CC} and BST should be used if the following relationship cannot be met:

$$\text{BST Diode Required if Power-Up to INP Going High} < \frac{C_B \bullet 12V}{30\mu A} \cong 40ms$$

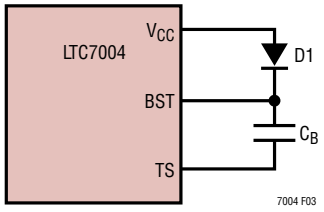


Figure 3. External BST Diode

Another reason to use an external silicon diode between V_{CC} and BST is if the external MOSFET is switched at frequency so high that the BST-TS supply collapses. An external silicon diode between V_{CC} and BST should be used if the following relationship cannot be met:

$$\text{BST Diode Required if Switching Frequency} > \frac{30\mu A}{2 \bullet \text{MOSFET } Q_G} \cong 500Hz$$

APPLICATIONS INFORMATION

A Schottky diode should not be used between V_{CC} and BST, because the reverse leakage of the Schottky diode at hot will be more current than the charge pump can overcome.

Some example silicon diodes with low leakage include:

- BAS116 Series, Multiple Vendors
- BAS416, Nexperia
- BAQ34, Vishay Semiconductors
- CMOD6001, Central Semiconductor

V_{CC} Undervoltage Comparator

The LTC7004 contains an adjustable undervoltage lockout (UVLO) on the V_{CC} voltage that pulls TGDN to TS and can be easily programmed using a resistor (R_{VCCUV}) between the V_{CCUV} pin and ground. The voltage generated on V_{CCUV} by R_{VCCUV} and the internal 10µA current source set the V_{CC} UVLO. The rising V_{CC} UVLO is internally limited within the range of 3.5V and 10.5V. If V_{CCUV} is open the rising V_{CC} UVLO is set internally to 7.0V. The typical value of resistor for a particular rising V_{CC} UVLO can be selected using Figure 4 or the following equation:

$$R_{VCCUV} = \frac{\text{Rising } V_{CC} \text{ UVLO}}{70\mu A}$$

Where 3.5V < Rising VCC UVLO < 10.5V.

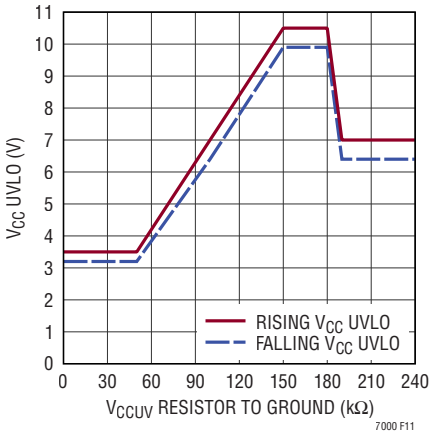


Figure 4. V_{CCUV} Resistor Selection

MOSFET Selection

The most important parameters in high voltage applications for MOSFET selection are the breakdown voltage BV_{DSS}, on-resistance $R_{DS(ON)}$ and the safe operating area, SOA.

The MOSFET, when off, will see the full input range of the input power supply plus any additional ringing than can occur when driving an inductive load.

External conduction losses are minimized when using low $R_{DS(ON)}$ MOSFETs. Since many high voltage MOSFETs have higher threshold voltages (typical $V_{TH} \geq 5V$) and $R_{DS(ON)}$ is directly related to the (V_{GS}–V_{TH}) of the MOSFET, the LTC7004 maximum gate drive of greater than 10V makes it an ideal solution to minimize external conduction losses associated with external high voltage MOSFETs.

SOA is specified in Typical Characteristic curves in power N-channel MOSFET data sheets. The SOA curves show the relationship between the voltages and current allowed in a timed operation of a power MOSFET without causing damage to the MOSFET.

Limiting Inrush Current During Turn-On

Large capacitive loads such as complex electrical systems with large bypass capacitors should be driven using the circuit shown in Figure 5. The pull-up gate drive to the power MOSFET from TGUP is passed through an RC delay network, R_G and C_G, which greatly reduces the turn-on ramp rate of the MOSFET. Since the MOSFET source voltage follows the gate voltage, the load is powered smoothly from ground. This dramatically reduces the inrush current from the source supply and reduces the transient ramp rate of the load, allowing for slower activation of sensitive electrical loads. The turn-off of the MOSFET is not affected by the R_C delay network as the pull-down for the MOSFET gate is directly from the TGDN pin. Note that the voltage rating on capacitor C_G needs to be the same or higher than the external MOSFET and C_{LOAD}.

APPLICATIONS INFORMATION

Adding C_G to the gate of the external MOSFET can cause high frequency oscillation. A low power, low ohmic value resistor (10Ω) should be placed in series with C_G to dampen the oscillations as shown in Figure 5 whenever C_G is used in an aplication. Alternatively, the low ohmic value resistor can be placed in series with the gate of the external MOSFET.

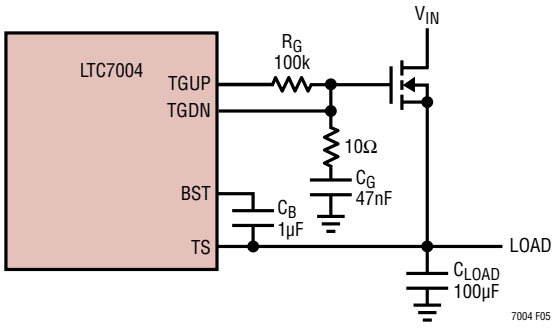


Figure 5. Powering Large Capacitive Loads

The values for R_G and C_G to limit the inrush current can be calculated from the below equation:

$$I_{IN\_RUSH} \cong \frac{0.7 \bullet 12V \bullet C_{LOAD}}{R_G \bullet C_G}$$

For the values shown in Figure 5 the inrush current will be:

$$I_{IN\_RUSH} \cong \frac{0.7 \bullet 12V \bullet 100\mu F}{100k\Omega \bullet 0.047\mu F} \cong 180mA$$

Correspondingly, the ramp rate at the load for the circuit in Figure 5 is approximately:

$$\frac{\Delta V_{LOAD}}{\Delta T} \cong \frac{0.7 \bullet 12V}{R_G \bullet C_G} \cong 2V/ms$$

When C_G is added to the circuit in Figure 5, the value of the bootstrap capacitor, C_B, must be increased to be able to supply the charge to both to MOSFET gate and capacitor C_G. The relationship for C_B that needs to be maintained when C_G is used is given by:

$$C_B > \frac{MOSFET\ Q_G}{1V} + 10 \bullet C_G$$

Optional Schottky Diode Usage on TS

When turning off a power MOSFET that is connected to an inductive component (inductor, long wire or complex load), the TS pin can be pulled below ground until the current in the inductive component has completely discharged. The TS pin is tolerant of voltages down to –6V, however, an optional Schottky diode with a voltage rating at least as high as the load voltage should be connected between TS and ground to prevent discharging the inductive through the TS pin of the LTC7004. See Figure 6.

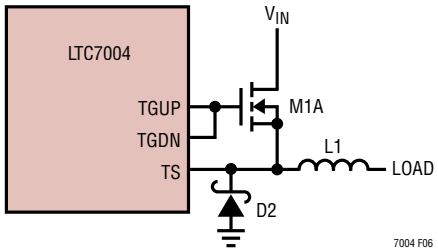


Figure 6. Optional Schottky Diode Usage

APPLICATIONS INFORMATION

Reverse Current Protection

To protect the load from discharging back into V_{IN} when the external MOSFET is off and the V_{IN} voltage drops below the load voltage, two external N-channel MOSFETs should be used and must be in a back-to-back arrangement as shown in Figure 7. Dual N-channel packages such as the following devices are good choices for space saving designs:

- FDS3890, Fairchild/ON Semiconductor
- IRF7380PbF, Infineon/IR
- SQJB80EP, Vishay/Siliconix

PC Board Layout Considerations

1. *Solder the exposed pad* on the backside of the LTC7004 package directly to the ground plane of the board.
2. Limit the resistance of the TS trace, by making it short and wide.
3. C_B needs to be close to chip.
4. Always include an option in the PC board layout to place a resistor in series with the gate of any external MOSFET. High frequency oscillations are design dependent, and having the option to add a series dampening resistor can save a design iteration of the PC board.

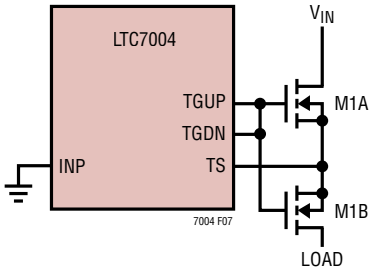
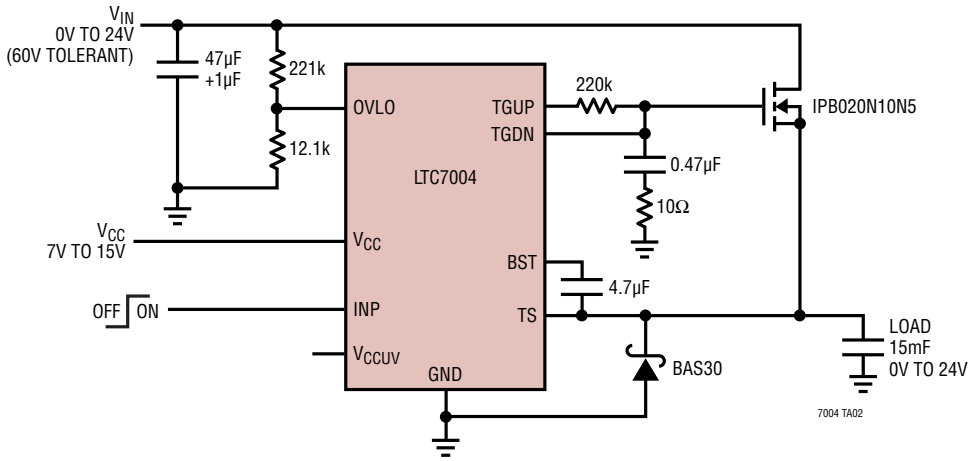


Figure 7. Protecting Load from Voltage Drops on V_{IN}

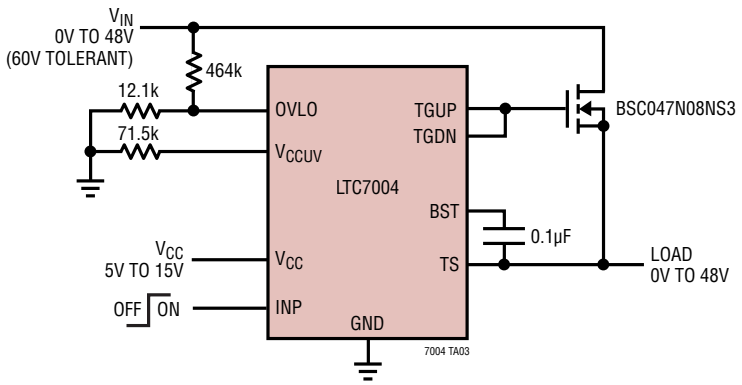
TYPICAL APPLICATIONS

High Side Switch with Inrush Control and OVLO



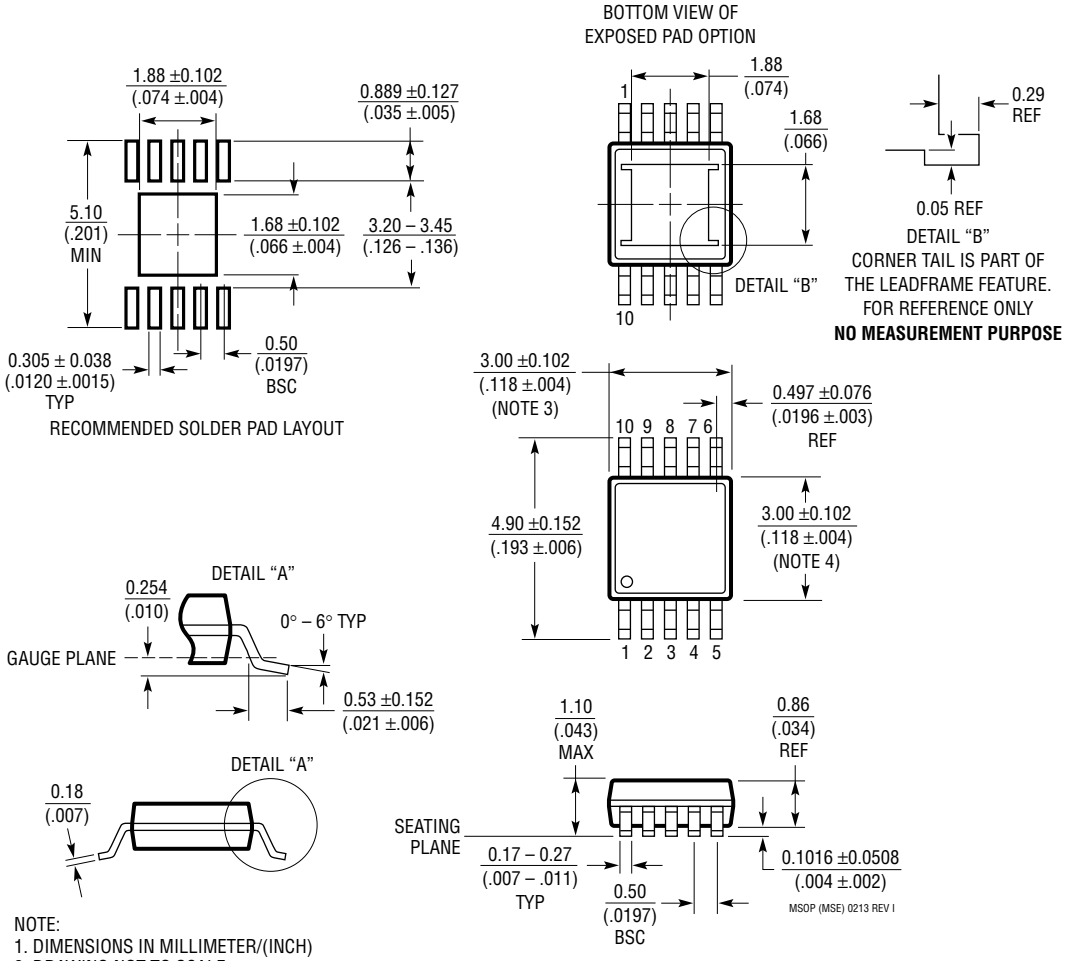
TYPICAL APPLICATIONS

High Side Switch with V_{CCUV} and OVLO



PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/17	Top Mark correction.	2
B	08/18	Added Note 7.	4
		Removed factor of 10 from C_B equation.	10
C	04/21	Added AEC-Q100 Qualified for Automotive Applications to the Features section.	1
		Added automotive part numbers to the Order Information section.	2