150V Half-Bridge Driver with Floating Grounds and Adjustable Dead-Time

FEATURES

- **Unique Symmetric Floating Gate Driver Architecture**
- **High Noise Immunity,Tolerates ±10V Ground Difference between Input and Output Grounds**
- **140V Maximum Input Voltage Independent of IC Supply Voltage V_{CC}**
- **6V to 14V V_{CC} Operating Voltage**
- **4V to 14V Gate Driver Voltage**
- **0.8Ω Pull-Down, 1.5Ω Pull-Up for Fast Turn-On/Off**
- **Adaptive Shoot-Through Protection**
- Programmable Dead-Time
- Three-State PWM Input with Enable Pin
- V_{CC} UVLO/OVLO and Floating Supplies UVLO
- Drives Dual N-Channel MOSFETs
- Open-Drain Fault Indicator
- Available in Thermally Enhanced 12-Lead MSOP
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Industrial Power Systems
- Telecommunication Power Systems
- Half-Bridge and Full-Bridge Converters

DESCRIPTION

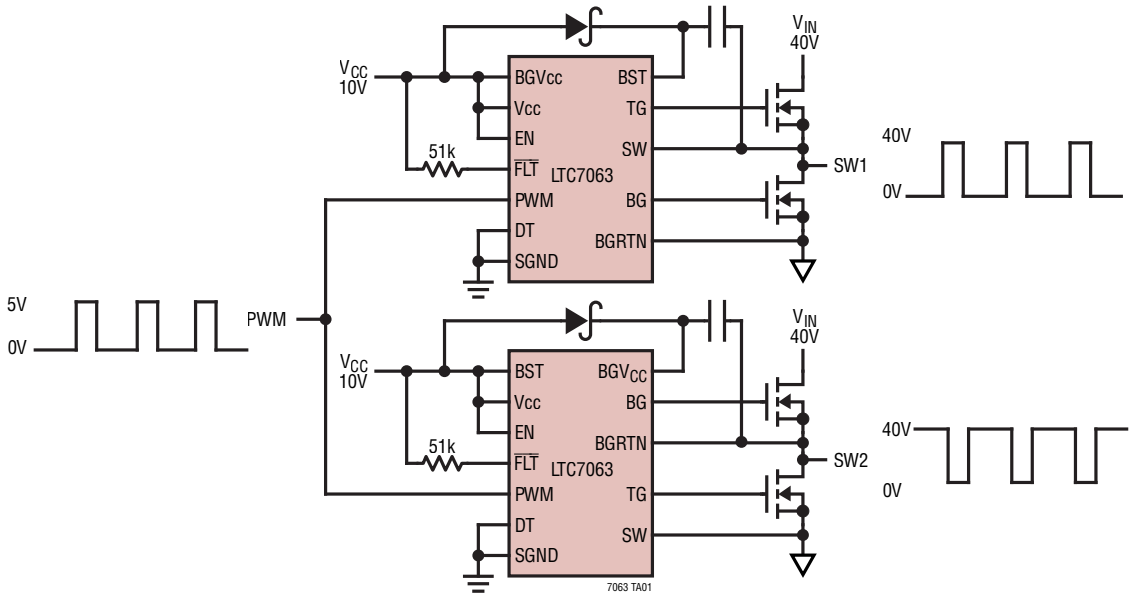
The LTC®7063 drives two N-Channel MOSFETs in a half-bridge configuration with supply voltages up to 140V. Both high-side and low-side drivers can drive the MOSFETs with a different ground reference, providing excellent noise and transient immunity.

Its powerful 0.8Ω pull-down and 1.5Ω pull-up MOSFET drivers allows the use of large gate capacitance high voltage MOSFETs. Additional features include UVLO, Three-State PWM input, adjustable turn-on/-off delays and shoot-through protection.

See chart below for a similar driver in this product family.

PARAMETER	LTC7060	LTC7061	LTC7062	LTC7063
Input Signal	Three-State PWM	CMOS/ TTL Logic	CMOS/ TTL Logic	Three-State PWM
Shoot-Through Protection	Yes	Yes	No	Yes
Absolute Max Voltage	115V	115V	115V	150V
V_{CC} Falling UVLO	5.3V	4.3V	4.3V	5.3V

TYPICAL APPLICATION



Rev. 0

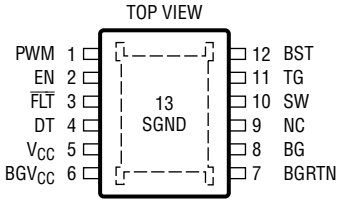
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage ..... –0.3V to 15V
Top Side Driver Voltage (BST) ..... –0.3V to 150V
Bottom Side Driver Voltage (BGV_{CC})..... –0.3V to 150V
SW, BGRTN.....–10V to 150V
(BST-SW)..... –0.3V to 15V
(BGV_{CC}-BGRTN) ..... –0.3V to 15V
EN, $\overline{FLT}$ ..... –0.3V to 15V
DT, PWM..... –0.3V to 6V
Driver Output TG (with Respect to SW)..... –0.3V to 15V
Driver Output BG
(with Respect to BGRTN)..... –0.3V to 15V
Operating Junction Temperature Range
(Note 2, 3)..... .....–40°C to 150°C
Storage Temperature Range .....–65°C to 150°C

Note: All voltages are referred to SGND unless otherwise noted.

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7063RMSE#PBF	LTC7063RMSE#TRPBF	LTC7063	12-Lead Plastic MSSOP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC7063RMSE#WPBF	LTC7063RMSE#WTRPBF	LTC7063	12-Lead Plastic MSSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BGVCC} = V_{BST} =10V, V_{BGRTN} = V_{SW} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply and V_{CC} Supply							
V_{IN}	Input Supply Operating Range					140	V
V_{CC}	IC Supply Operating Range			6		14	V
I_{VCC}	V_{CC} Supply Current	V_{EN} = V_{PWM} = 0V, R_{DT} = 100kΩ			0.4		mA
V_{UVLO_VCC}	V_{CC} Undervoltage Lockout Threshold	V_{CC} Falling		5	5.3	5.6	V
		Hysteresis			0.3		V
V_{OVLO_VCC}	V_{CC} OVLO Threshold	V_{CC} Rising			14.6		V
		Hysteresis			0.8		V
BG Gate Driver Supply (BGV_{CC}-BGRTN)							
$V_{BGVCC-BGRTN}$	BG Driver Supply Voltage Range (With Respect to BGRTN)			4		14	V
I_{BGVCC}	Total BGV_{CC} Current (Note 4)	BG = Low			8		µA
		BG = High			100		µA
V_{UVLO_BGVCC}	Undervoltage Lockout Threshold	BGV_{CC} Falling, With Respect to BGRTN			3.4		V
		Hysteresis			0.3		V
TG Gate Driver Supply (BST-SW)							
V_{BST-SW}	TG Driver Supply Voltage Range (With Respect to SW)			4		14	V
I_{BST}	Total BST Current (Note 4)	TG = Low			8		µA
		TG = High			100		µA
V_{UVLO_BST}	Undervoltage Lockout Threshold	BST Falling, With Respect to SW			3.4		V
		Hysteresis			0.3		V
Input Signal (PWM, EN)							
$V_{IH(TG)}$	TG Turn-On Input Threshold	PWM Rising	●	2.6	3.1	3.6	V
$V_{IL(TG)}$	TG Turn-Off Input Threshold	PWM Falling	●	2.45	2.95	3.45	V
$V_{IH(BG)}$	BG Turn-On Input Threshold	PWM Falling	●	0.5	1	1.5	V
$V_{IL(BG)}$	BG Turn-Off Input Threshold	PWM Rising	●	0.75	1.25	1.75	V
V_{PWM_TRI}	PWM Input Three-State Float Voltage			1.9	2.1	2.3	V
R_{UP_PWM}	PWM Internal Pull-Up Resistor	To Internal 4.5V Supply			48		kΩ
R_{DOWN_PWM}	PWM Internal Pull-Down Resistor				42		kΩ
V_{ENR}	EN Pin Rising Threshold	EN Rising	●	1.1	1.2	1.3	V
V_{ENF}	EN Pin Falling Threshold	EN Falling			1.1		V
R_{EN}	EN Pin Internal Pull-Down Resistor				2		MΩ
Dead-Time and FAULT (DT, $\overline{FLT}$)							
$t_{PLH(BG)}$ / $t_{PLH(TG)}$	BG/TG Low to TG/BG High Propagation Delay (Dead-Time)	R_{DT} = 0Ω			32		ns
		R_{DT} = 24.9kΩ			43		ns
		R_{DT} = 64.9kΩ			62		ns
		R_{DT} = 100kΩ			76		ns
		R_{DT} = Open			250		ns
R_{FLTb}	Open Drain Pull-Down Resistance				60		Ω
t_{FLTb}	$\overline{FLT}$ Pin Release Delay	Low to High			100		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BGVCC} = V_{BST} =10V, V_{BGRTN} = V_{SW} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side Gate Driver Output (BG)							
$V_{OH(BG)}$	BG High Output Voltage	I_{BG} = –100mA, $V_{OH(BG)}$ = V_{BGVCC} – V_{BG}			150		mV
$V_{OL(BG)}$	BG Low Output Voltage	I_{BG} = 100mA, $V_{OL(BG)}$=V_{BG} – V_{BGRTN}			80		mV
$R_{UP(BG)}$	BG Pull-Up Resistance	$V_{BGVCC-BGRTN}$ =10V			1.5		Ω
$R_{DOWN(BG)}$	BG Pull-Down Resistance	$V_{BGVCC-BGRTN}$ =10V			0.8		Ω
High-Side Gate Driver Output (TG)							
$V_{OH(TG)}$	TG High Output Voltage	I_{TG} = –100mA, $V_{OH(TG)}$ = V_{BST} – V_{TG}			150		mV
$V_{OL(TG)}$	TG Low Output Voltage	I_{TG} = 100mA, $V_{OL(TG)}$ = V_{TG} – V_{SW}			80		mV
$R_{UP(TG)}$	TG Pull-Up Resistance	V_{BST-SW} = 10V			1.5		Ω
$R_{DOWN(TG)}$	TG Pull-Down Resistance	V_{BST-SW} = 10V			0.8		Ω
Switching Time							
$t_{PHL(BG)}$	PWM High to BG Low Propagation Delay				17		ns
$t_{PHL(TG)}$	PWM Low to TG Low Propagation Delay				17		ns
$t_{r(BG)}$	BG Output Rise Time	C_{LOAD} = 3.3nF (Note 5)			18		ns
$t_{f(BG)}$	BG Output Fall Time	C_{LOAD} = 3.3nF (Note 5)			13		ns
$t_{r(TG)}$	TG Output Rise Time	C_{LOAD} = 3.3nF (Note 5)			18		ns
$t_{f(TG)}$	TG Output Fall Time	C_{LOAD} = 3.3nF (Note 5)			13		ns
$t_{PH(EN)}$	EN High to TG/BG High Propagation Delay				30		ns
$t_{PL(EN)}$	EN Low to TG/BG Low Propagation Delay				36		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC7063R is specified over –40°C to 150°C operating junction temperature range. High junction temperature degrades operation lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environment factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula

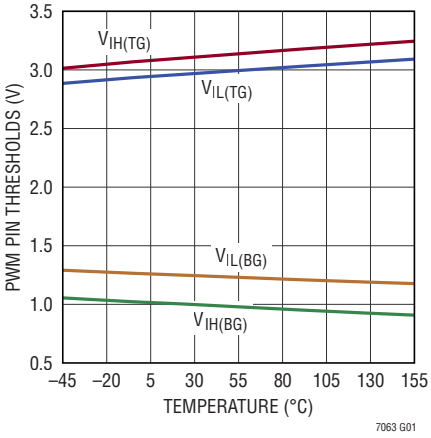
$$T_J = T_A + (P_D \bullet 40°C/W) \text{ for MSOP package.}$$

Note 4: The total current includes both the current from BGV_{CC}/BST to BGRTN/SW and the current to SGND. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

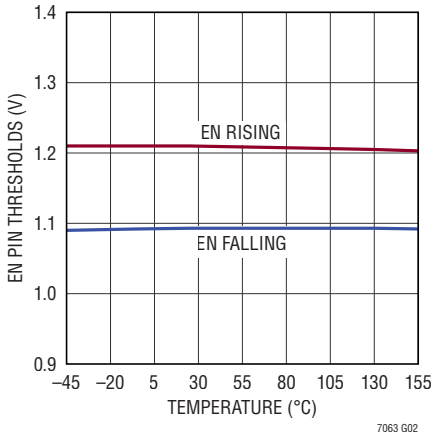
Note 5: Rise and fall times are measured using 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

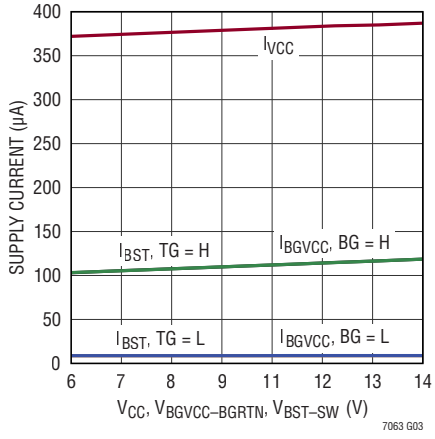
PWM Pin Thresholds vs Temperature



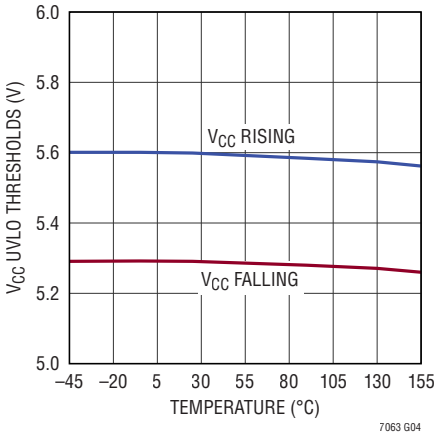
EN Pin Thresholds vs Temperature



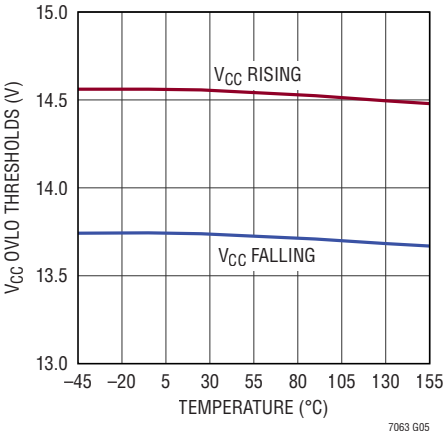
Quiescent Supply Current vs Supply Voltage



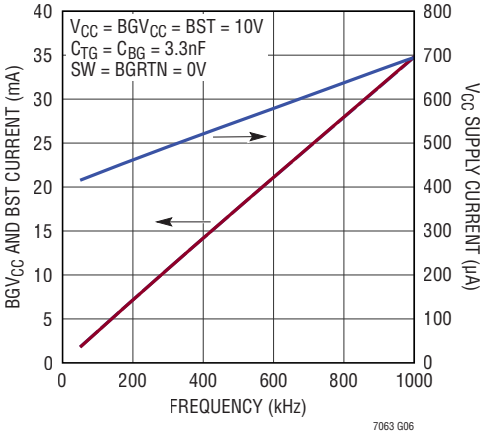
V_{CC} Undervoltage Lockout Thresholds vs Temperature



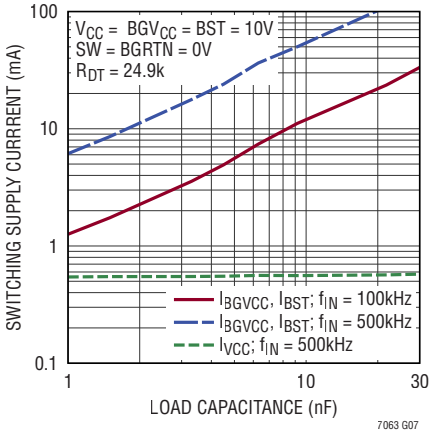
V_{CC} Overvoltage Lockout Thresholds vs Temperature



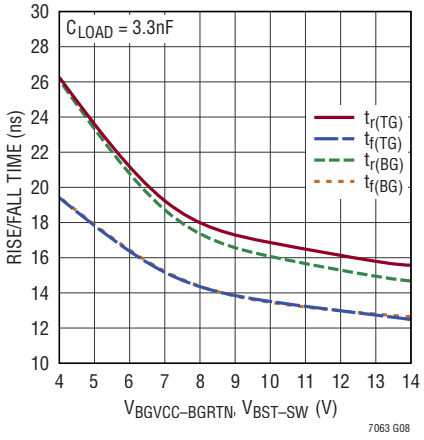
Supply Current vs Input Frequency



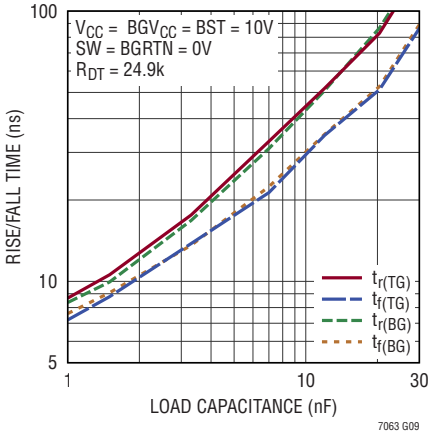
Switching Supply Current vs Load Capacitance



Rise and Fall Time vs Floating Supply Voltage

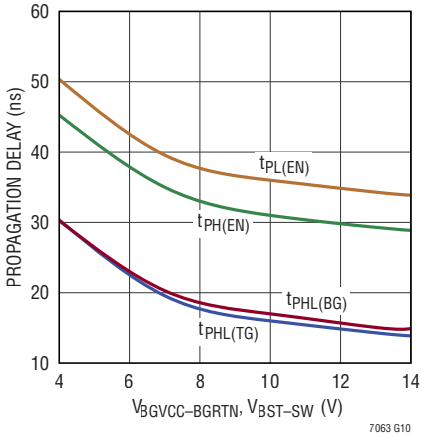


Rise and Fall Time vs Load Capacitance

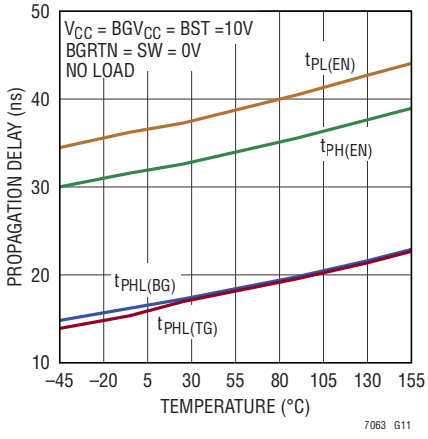


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

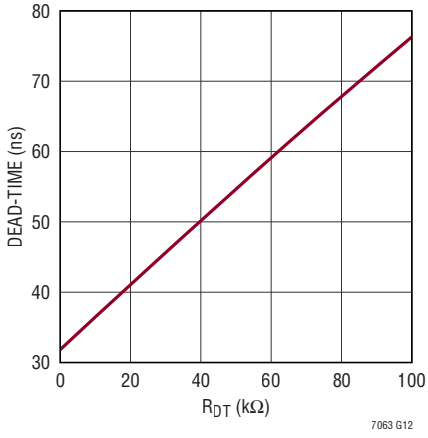
Propagation Delay vs Floating Supply Voltage



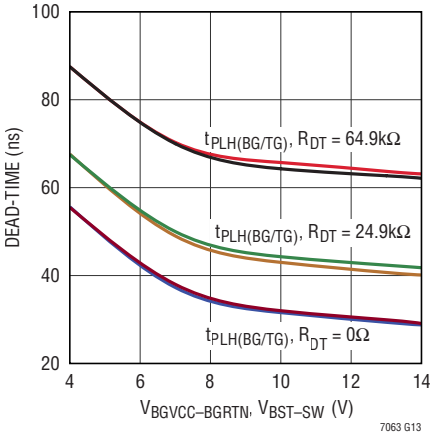
Propagation Delay vs Temperature



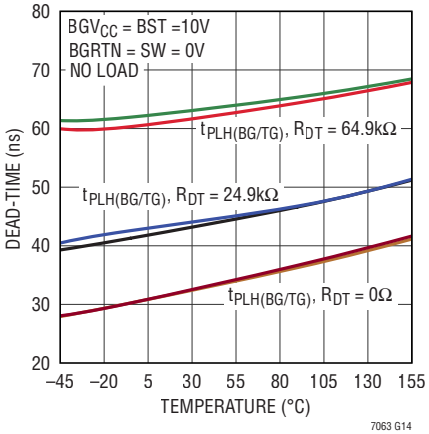
Dead-Time vs R_{DT}



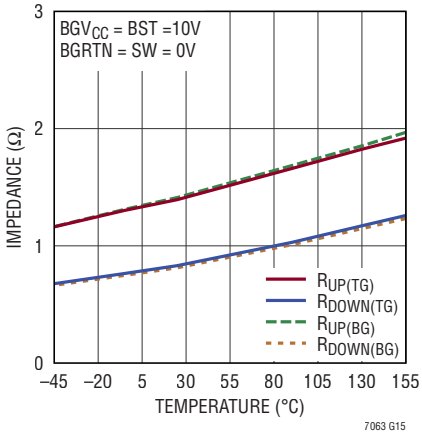
Dead-Time vs Floating Supply Voltage



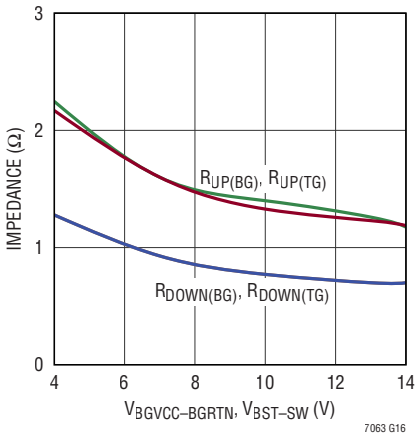
Dead-Time vs Temperature



TG/BG Pull-Up and Pull-Down Resistance vs Temperature



TG/BG Pull-Up and Pull-Down Resistance vs Floating Supply Voltage



PIN FUNCTIONS

V_{CC}: V_{CC} Supply. IC bias supply referred to the SGND pin. An internal 4.5V supply is generated from the V_{CC} supply to bias most of the internal circuitry. A bypass capacitor with a minimum value of 0.1uF should be tied between this pin and the SGND pin.

BGV_{CC}: Bottom MOSFET Driver Supply. The bottom MOSFET gate driver is biased between this pin and the BGRTN pin. An external capacitor should be tied between this pin and BGRTN and placed close to the IC.

BGRTN: Bottom MOSFET Driver Return. The bottom gate driver is biased between BGV_{CC} and BGRTN. Kelvin connect BGRTN to the bottom MOSFET source pin for high noise immunity. The voltage difference between the BGRTN pin and the SGND can be –10V to 150V.

BG: Bottom MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between BGRTN and BGV_{CC}.

BST: Top MOSFET Driver Supply. The top MOSFET gate driver is biased between this pin and the SW pin. An external capacitor should be tied between this pin and the SW pin and placed close to the IC.

SW: Top MOSFET Driver Return. The top gate driver is biased between BST and SW. Kelvin connect SW to the top MOSFET source pin for high noise immunity. The voltage difference between the SW pin and SGND can be –10V to 150V.

TG: Top MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between SW and BST.

DT: Dead-Time Program Pin Referred to the SGND Pin. A single resistor from this pin to SGND sets the BG/TG low to TG/BG high propagation delay. See the operation section for details.

PWM: Three-State Gate Driver Input Signal Referred to the SGND Pin. The TG/BG state is determined by the voltage at this pin. If this pin is floating, an internal resistor divider triggers the High-Z mode in which both BG and TG are turned off. Trace capacitance on this pin should be minimized.

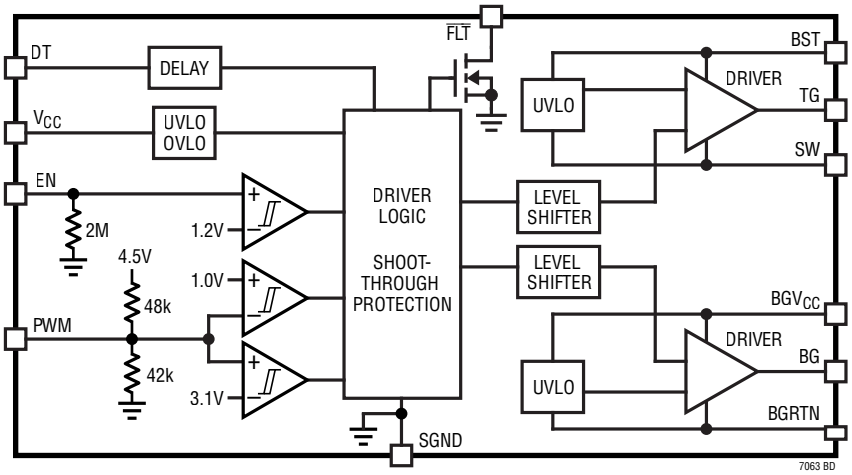
EN: Enable Control Input Pin Referred to the SGND Pin. A voltage on this pin above 1.2V enables the gate drivers. The TG and BG pins are both in the low state if this pin is logic low.

$\overline{FLT}$: Open Drain Fault Output Pin Referred to the SGND Pin. Open-drain output that pulls to SGND during V_{CC} UVLO/OVLO and floating supplies UVLO condition. The typical pull-down resistance is 60Ω.

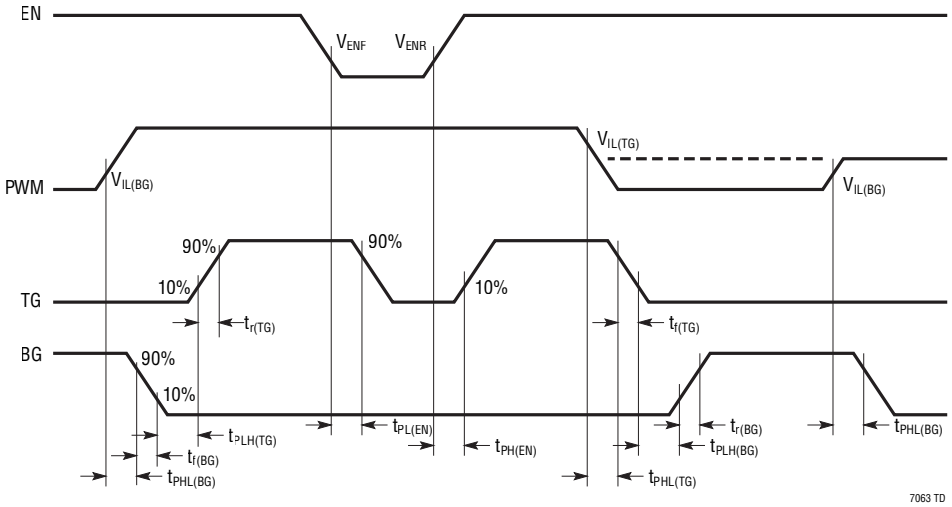
NC: No Internal Connection. Always keep this pin floating. It is intentionally skipped to isolate adjacent high voltage pins.

SGND: Chip Ground. The exposed pad must be soldered to the PCB ground for electrical contact and for rated thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

OVERVIEW

The LTC7063 receives a ground-referenced, low voltage digital PWM signal to drive two N-channel power MOSFETs in a half-bridge configuration. The gate of the low-side MOSFET is driven high or low, swinging between BGV_{CC} and BGRTN, depending on the state of the PWM pin. Similarly, the gate of the high-side MOSFET is driven complimentary to the low-side MOSFET, swinging between BST and SW.

Both the low-side and high-side drivers are floating gate drivers. The unique double floating architecture makes the gate driver outputs robust and less sensitive to ground noise. The symmetric design allows the half-bridge output to be inverting or non-inverting of the input logic.

V_{CC} SUPPLY

V_{CC} is the power supply for the LTC7063's internal circuitry. An internal 4.5V supply is generated from the V_{CC} supply to bias most of the internal circuits referred to SGND. The V_{CC} pin may be tied to the BGV_{CC} pin if SGND and BGRTN are at the same potential. V_{CC} is independent of V_{IN}.

INPUT STAGE (PWM, EN)

The LTC7063 employs a three-state PWM input with fixed transition thresholds. The relationship between the transition thresholds and three input states of the LTC7063 is illustrated in Figure 1. When the voltage on PWM is greater than the threshold $V_{IH(TG)}$, TG is pulled up to BST, turning the high-side MOSFET on. This MOSFET will stay on until PWM falls below $V_{IL(TG)}$. Similarly, when PWM is less than $V_{IH(BG)}$, BG is pulled up to BGV_{CC}, turning the low-side MOSFET on. BG will stay high until PWM increases above the threshold $V_{IL(BG)}$.

The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to the noise during switch transitions. However, care should be taken to keep noise from coupling into the PWM pin, particularly in high frequency, high voltage applications.

The thresholds are positioned to allow for a region in which both BG and TG are low. An internal resistor divider

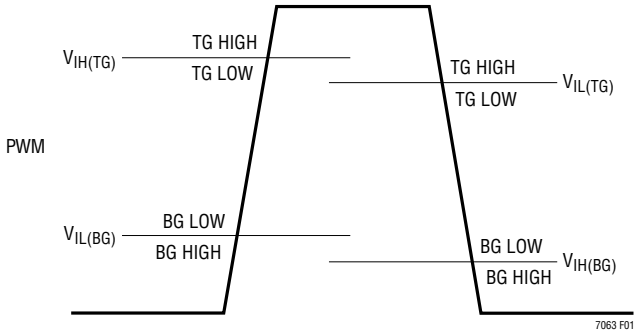


Figure 1. Three-State PWM Operation

OPERATION

sets the PWM pin voltage into this region if the signal driving the PWM pin goes into a high impedance state.

The EN pin can also be used to keep both BG and TG low if the high impedance state is not available from the PWM driving signal. Driving the EN pin low keeps both TG and BG off, and driving the EN pin high enables TG and BG switching based on the PWM input. There is an internal 2MΩ pull-down resistor from the EN pin to SGND, keeping the EN default state low if its input is not driven.

Both three-state PWM and EN pin can be used by the controller IC to perform the Discontinuous Conduction Mode (DCM) in switching regulator applications.

OUTPUT STAGE

A simplified version of the LTC7063's output stage is shown in Figure 2. The BG and TG design are symmetric and they both have floating gate driver outputs. The pull-up device is a PMOS with a typical 1.5Ω $R_{DS(ON)}$ and the pull-down device is a NMOS with a typical 0.8Ω $R_{DS(ON)}$. The wide driver supply voltage ranging from 4V to 14V enables the driving of different power MOSFETs, such as logic level or higher threshold MOSFETs. However, the LTC7063 is optimized for higher threshold MOSFETs (e.g. BST-SW = 10V and BGV_{CC}-BGRTN = 10V). The driver

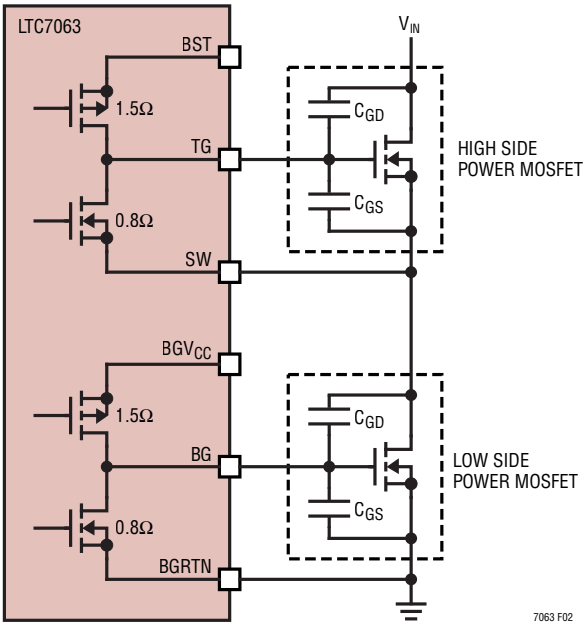


Figure 2. Simplified Output Stage in Half-Bridge Configuration

output pull-up and pull-down resistance may increase with lower driver supply voltage.

Since the power MOSFETs generally account for the majority of the power loss in a converter, it is important to turn them on and off quickly, thereby minimizing the transition time and power loss. The LTC7063's typical 1.5Ω pull-up resistance and 0.8Ω pull-down resistance are equivalent to 3A peak pull-up current and 6A peak pull down current at a 10V driver supply. Both BG and TG can produce a rapid turn-on transition for the MOSFETs with capability of driving a 3.3nF load with 18ns rise time.

Furthermore, a strong pull-down on the driver outputs prevents cross-conduction current. For example, in the half-bridge configuration shown in Figure 2, when BG turns the low-side power MOSFET off and TG turns the high-side power MOSFET on, the voltage on the SW pin could rise to V_{IN} very rapidly. This high frequency positive voltage transient will couple through the C_{GD} capacitance of the low-side power MOSFET to the BG pin. If the BG pin is not held down sufficiently, the voltage on the BG pin could rise above the threshold voltage of the low-side power MOSFET, momentarily turning it back on. As a result, both the high-side and low-side MOSFETs would be conducting, which would cause significant cross-conduction current to flow through the MOSFETs from V_{IN} to ground, thereby incurring substantial power loss and potentially damaging the MOSFETs. For this reason, short PCB traces for the BG and TG pins, which minimize the parasitic inductances, are recommended.

PROTECTION CIRCUITRY

When using the LTC7063, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, the LTC7063 incorporates overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7063 will enter thermal shutdown mode and BG will be pulled to BGRTN; TG will be pulled to SW. Normal operation will resume when the junction temperature cools down below 165°C. The overtemperature level is not production tested. The LTC7063 is guaranteed to operate below 150°C.

OPERATION

The LTC7063 contains both undervoltage and overvoltage lockout detectors that monitor the V_{CC} supply. When V_{CC} falls below 5.3V or rises above 14.6V, BG and TG pins are pulled to BGRTN and SW, respectively, turning off both the external MOSFETs. When V_{CC} has adequate supply voltage but less than the overvoltage threshold, normal operation will resume.

Additional undervoltage lockout circuitry is included in each floating driver supply. The BG will be pulled down to BGRTN when the floating voltage from BGV_{CC} to BGRTN falls below 3.3V. Similarly, the TG will be pulled down to SW when the floating voltage from BST to SW is less than 3.3V.

The normal operation and undervoltage/overvoltage logic table is shown in Table 1.

Table 1. Normal Operation and Undervoltage/Overvoltage Logic

PWM	EN	V_{CC} UVLO or OVLO	(BST-SW) UVLO	(BGV_{CC}-BGRTN) UVLO	TG	BG
X	L	X	X	X	L	L
X	X	Y	X	X	L	L
L	H	N	X	N	L	H
L	H	N	X	Y	L	L
H	H	N	N	X	H	L
H	H	N	Y	X	L	L
HIGH-Z	H	X	X	X	L	L

Note: “X” means "Don't Care"

ADAPTIVE SHOOT-THROUGH PROTECTION

Internal adaptive shoot-through protection circuitry monitors the external MOSFETs to ensure that they do not conduct simultaneously. The LTC7063 does not allow the bottom MOSFET to turn on until the gate-source voltage on the top MOSFET is sufficiently low, and vice-versa. This feature improves efficiency and reliability by eliminating potential shoot-through current through the MOSFETs during switching transitions.

PROGRAMMABLE DEAD-TIME

To ensure robust shoot-through protection in high voltage half-bridge configuration and switched capacitor converter applications, the LTC7063 provides a DT pin which can be used to program the propagation delay during BG/TG low to TG/BG high transition (Dead-Time). An external resistor (R_{DT}) from the DT pin to the SGND equally sets both the BG low to TG high propagation delay and the TG low to BG high propagation delay. Their relationship can be seen in Figure 3. The Dead-Time can be estimated by the following equation when the R_{DT} is less than 100kΩ:

$$\text{Dead-Time} = R_{DT} \bullet 0.44\text{ns/k}\Omega + 32\text{ns}$$

If the DT pin is shorted to SGND, the Dead-Time is 32ns. If the DT Pin is floating, the Dead-Time is around 250ns.

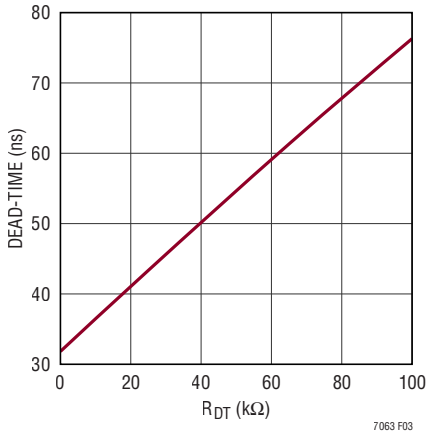


Figure 3. Dead-Time vs R_{DT}

FAULT FLAG

The $\overline{FLT}$ pin is connected to the open-drain of an internal N-channel MOSFET. It needs a pull-up resistor (e.g. 51k) tied to a supply such as V_{CC} or any other bias voltage up to 15V. The $\overline{FLT}$ pin is pulled low to SGND immediately if any of these conditions are met:

a. The V_{CC} is below its UVLO threshold or above its OVLO threshold.

b. (BGV_{CC}-BGRTN) is below its UVLO threshold.

c. (BST-SW) is below its UVLO threshold.

d. The junction temperature reaches approximately 180°C.

When all the faults are cleared, the $\overline{FLT}$ pin is pulled up by the external resistor after a built-in 100µs delay.

APPLICATIONS INFORMATION

BOOTSTRAPPED SUPPLY (BGV_{CC}-BGRTN, BST-SW)

Either or both of the BGV_{CC}-BGRTN and BST-SW supplies can be bootstrapped supplies. An external boost capacitor, C_B, connected between BGV_{CC} and BGRTN, or between BST and SW, supplies the gate driver voltage for its respective MOSFET driver. When the external MOSFET is turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns it on.

The charge to turn on the external MOSFET is referred to gate charge, Q_G, and is typically specified in the external MOSFET data sheet. The boost capacitor, C_B, needs to have at least 10 times the gate capacitance to turn on the external MOSFET fully. Gate charge can range from 5nC to hundreds of nC and is influenced by the gate drive level and type of external MOSFET used. For most applications, a capacitor value of 0.1uF for C_B will be sufficient. However, if multiple MOSFETs are paralleled and driven by the LTC7063, C_B capacitance needs to be increased correspondingly.

An external supply, typically V_{CC} connected through a Schottky diode, is required to keep the C_B charged. The LTC7063 does not charge the C_B and always discharges the C_B. When the BG/TG is high, the total current from BGV_{CC}/BST to BGRTN/SW and SGND is typically 100µA; when the BG/TG is low, the total current from BGV_{CC}/BST is typically 8µA.

POWER DISSIPATION

To ensure proper operation and long-term reliability, the LTC7063 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA})$$

where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

P_{DC} = quiescent power loss

P_{AC} = internal switching loss at input frequency f_{IN}

P_{QG} = loss due to turning on and off external MOSEFT with gate charge Q_G at frequency f_{IN}

The LTC7063 consumes very little quiescent current. The DC power loss at V_{CC} = 10V is only (10V)(0.4mA) = 4mW.

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on BG and TG at switching frequency f_{IN}, the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BST-SW})^2 + (V_{BGVCC-BGRTN})^2]$$

In a typical synchronous buck configuration, the V_{CC} is connected to the power for the bottom MOSFET driver, BGV_{CC}. V_{BST-SW} is equal to V_{CC} -V_D, where V_D is the forward voltage drop of the external Schottky diode between V_{CC} and BST. If this drop is small relative to V_{CC}, the load losses can be approximated as:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G. The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves. For identical MOSFETs on BG and TG:

$$P_{QG} \approx 2(Q_G)(f_{IN})(V_{CC})$$

APPLICATIONS INFORMATION

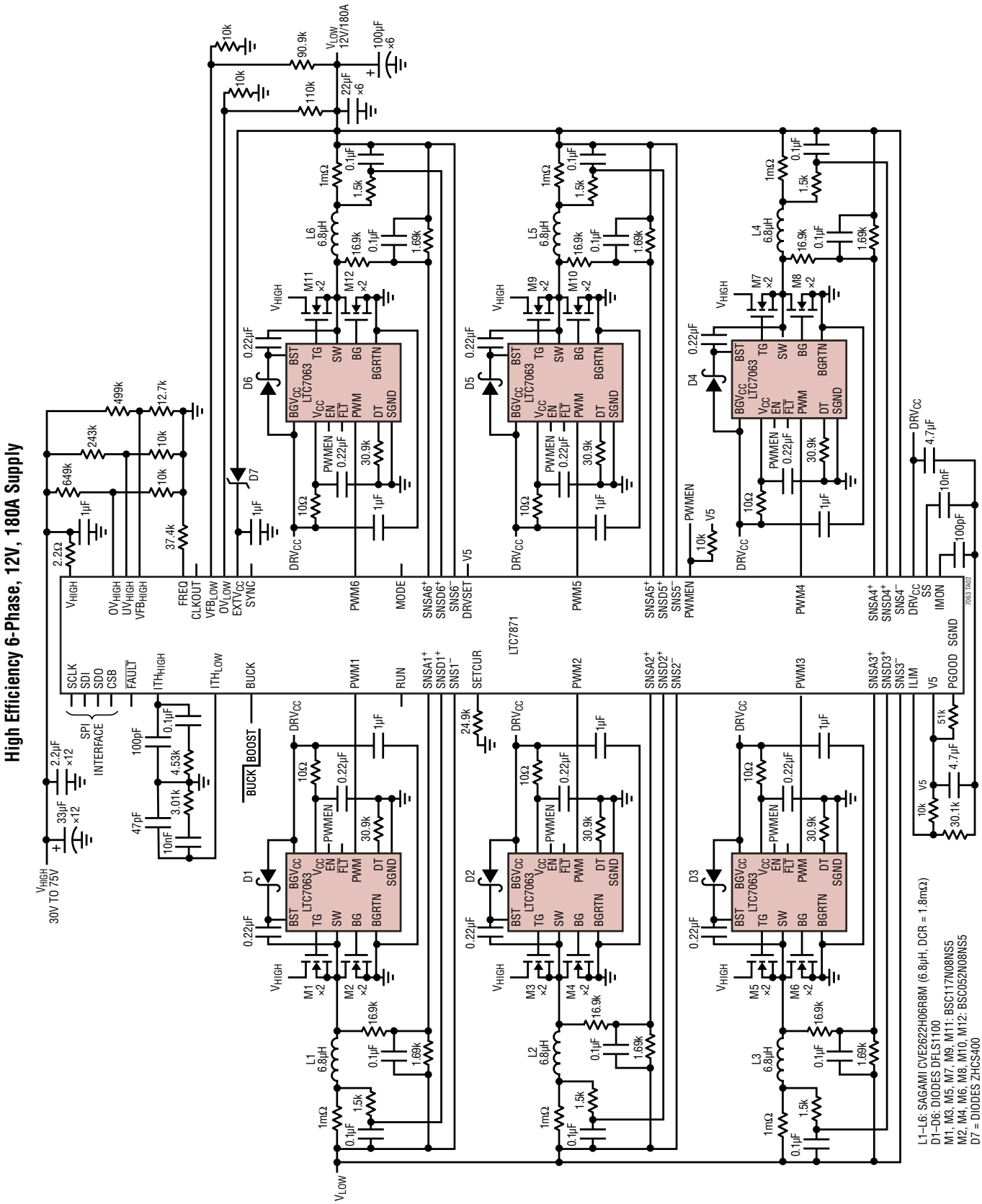
BYPASSING AND GROUNDING

The LTC7063 requires proper bypassing on the V_{CC}, V_{BST-SW}, and $V_{BGVCC-BGRTN}$ supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance form the LTC7063:

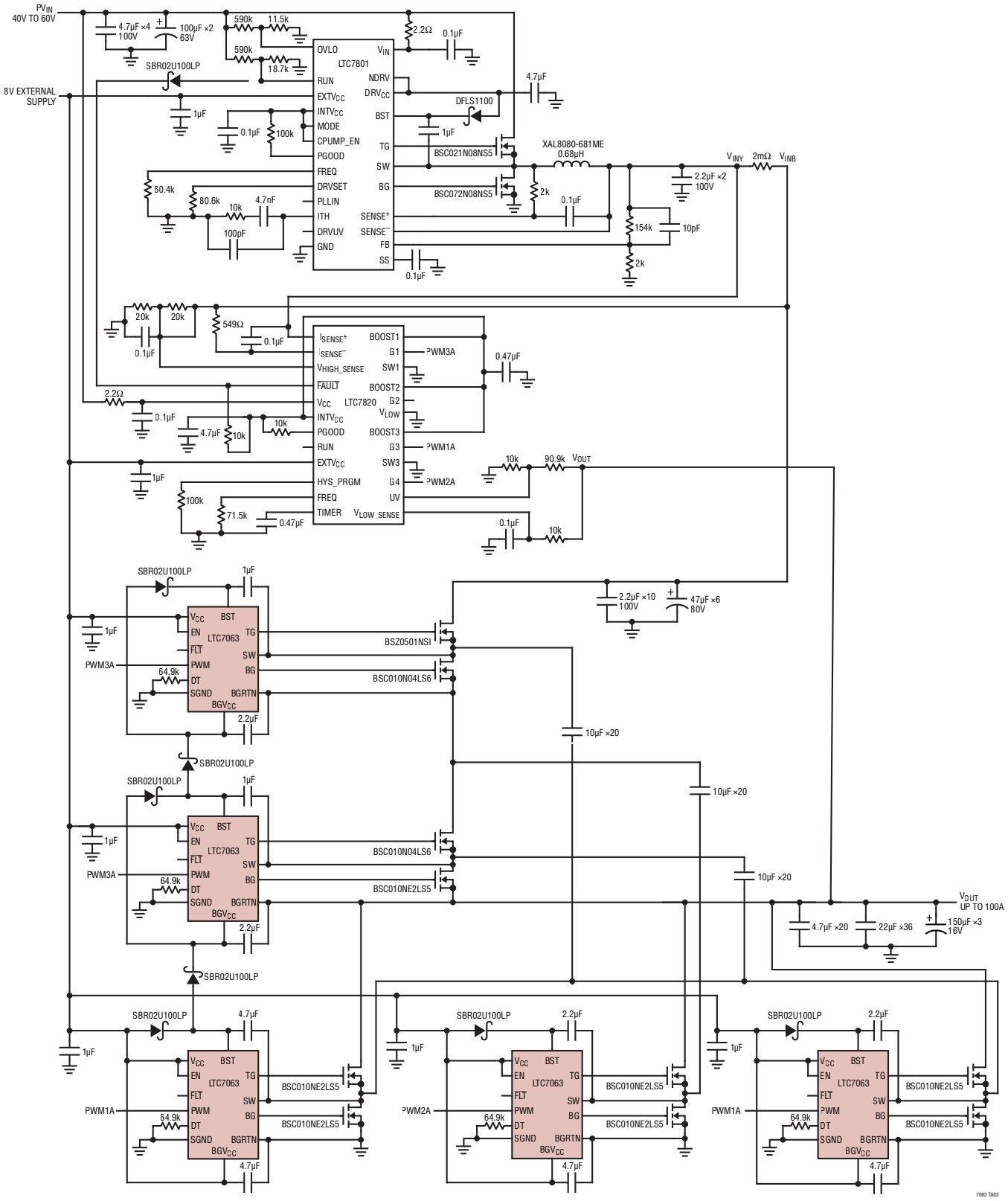
- Mount the bypass capacitors as close as possible between the V_{CC} and SGND pins, the BGV_{CC} and BGRTN pins, and the BST and SW pins. The leads should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC7063 switches greater than 5A peak currents and any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Kelvin connect the TG pin to the top MOSFET gate and SW pin to the top MOSFET source. Kelvin connect the BG pin to the bottom MOSFET gate and BGRTN to the bottom MOSFET source. Keep the copper trace between the driver output pin and load short and wide.
- Be sure to solder the Exposed Pad on the back side of the LTC7063 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than specified for the packages.

TYPICAL APPLICATIONS



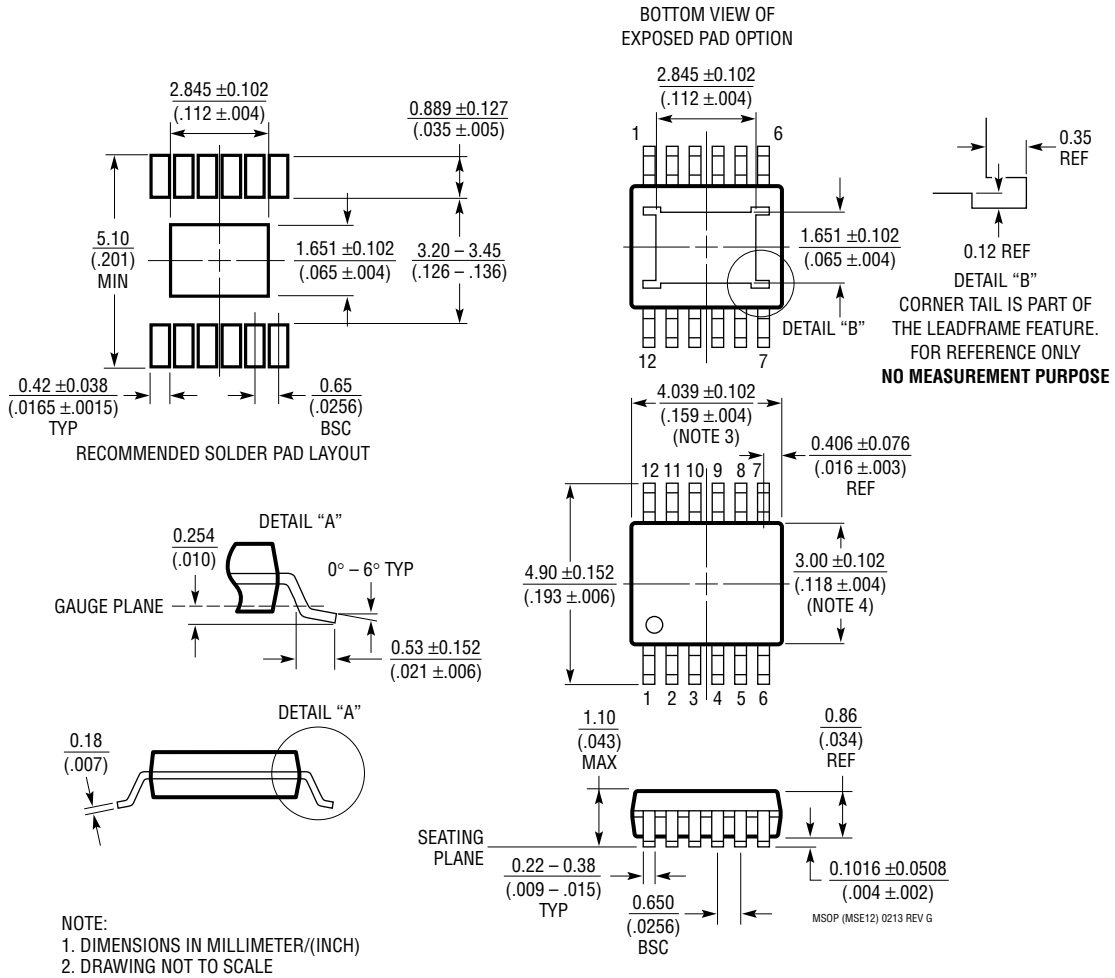
TYPICAL APPLICATIONS

Up to 100A High Efficiency 4 to 1 Switched Capacitor Converter



PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.