2-Phase Dual Output Nonsynchronous Boost Controller with Hiccup Mode

FEATURES

- **Wide V_{IN} Range: 5.5V to 60V**
- **Configurable for Dual Phase Single/Dual Output Operation**
- **Peak Current Mode Control with Smooth Quadratic Slope Compensation and Dynamic Slope Recovery**
- **Adjustable Max Duty Cycle**
- **Adjustable Min On-Time**
- **Hiccup Mode for Overcurrent Protection**
- **Adjustable Current Sense Limit**
- Output Overvoltage Protection
- Programmable and Phase-Lockable Operating Frequency (from 50kHz to 425kHz)
- Adjustable Soft-Start Current Ramping
- ±1% Internal Voltage Reference
- Internal 10V LDO Regulator for Gate Driver
- Two RUN Pins and Dual Power Good Monitors
- Flexible Topology for Boost, SEPIC and Flyback

APPLICATIONS

- Automotive System, Telecom System and Industrial Power Supplies

DESCRIPTION

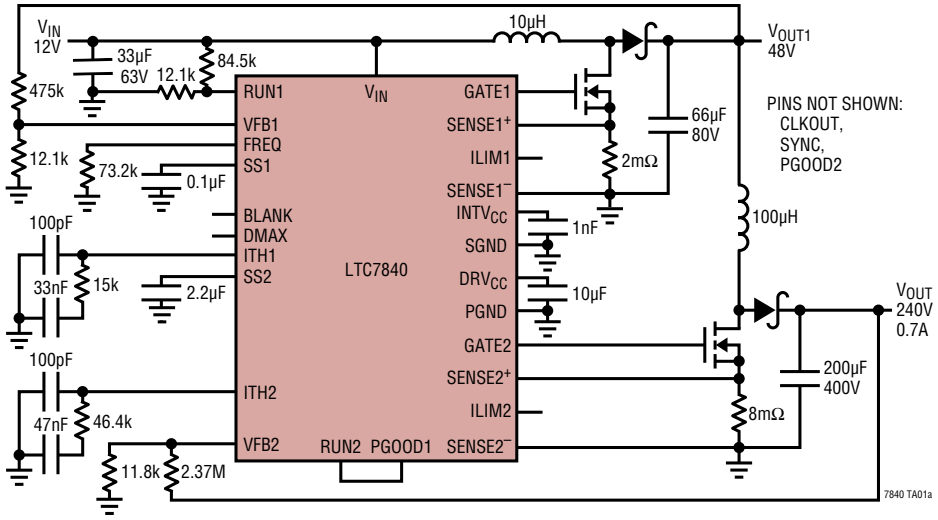
The LTC®7840 is a dual phase dual output, constant frequency current mode, nonsynchronous boost controller that drives N-channel power MOSFETs. The nonsynchronous topology makes the output voltage dependent on the choice of external components.

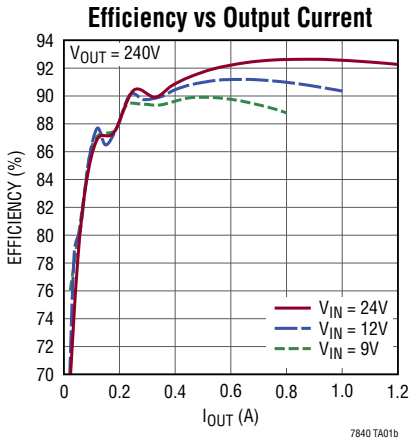
A wide 5.5V to 60V input supply range can accommodate high input voltage surges. The LTC7840 can be configured as a dual phase single output or dual output controller. It can be also configured for the SEPIC and flyback topologies. The switching frequency is programmed by the voltage on the FREQ pin or synchronized to an external clock. The LTC7840 features a precise 1.2V internal reference. It has two RUN pins and two power good output indicators.

The LTC7840 has an internal 10V LDO with undervoltage lockout protection for its on-chip gate driver. The maximum duty cycle and blanking time can be programmed by the voltage on D_{MAX} and BLANK pins, respectively. The hiccup mode protects the system in the event of faults.

The LTC7840 is available in a 28-lead thermally enhanced TSSOP package (FE28) or a 28-lead QFN package (UFD28).

TYPICAL APPLICATION





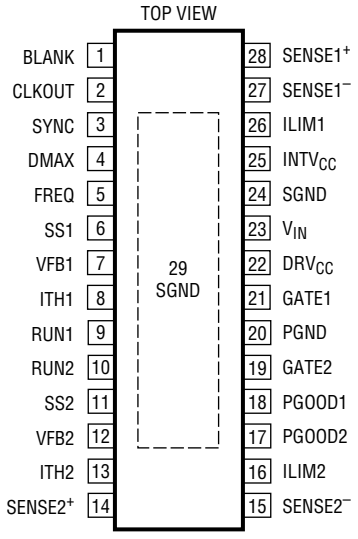
Rev 0

ABSOLUTE MAXIMUM RATINGS

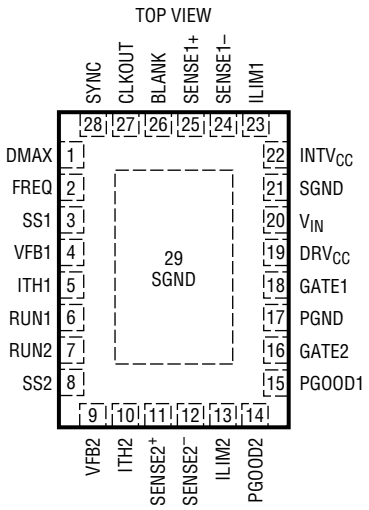
(Notes 1, 2)

Input Supply Voltage (V_{IN}) ..... –0.3V to 65V
RUN1, RUN2 Voltage ..... –0.3V to 6V
SENSE1+, SENSE2+ Voltage ..... –0.3V to $INTV_{CC}$
D_{MAX}, BLANK Voltage ..... –0.3V to $INTV_{CC}$
PGOOD1, PGOOD2 Voltage ..... –0.3V to 6V
VFB1, VFB2 Voltage ..... –0.3V to $INTV_{CC}$
SS1, SS2 Voltage ..... –0.3V to $INTV_{CC}$
ITH1, ITH2 Voltage ..... –0.3V to $INTV_{CC}$
ILIM1, ILIM2 Voltage ..... –0.3V to $INTV_{CC}$
FREQ, SYNC Voltage ..... –0.3V to $INTV_{CC}$
DRV_{CC} Peak Output Current 100mA
Operating Junction Temperature Range (Note 3)
LTC7840E ..... –40°C to 125°C
LTC7840I ..... –40°C to 125°C
LTC7840H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Reflow Peak Body Temperature ..... 260°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 47°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7840EFE#PBF	LTC7840EFE#TRPBF	LTC7840 FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC7840IFE#PBF	LTC7840IFE#TRPBF	LTC7840 FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC7840HFE#PBF	LTC7840HFE#TRPBF	LTC7840 FE	28-Lead Plastic TSSOP	–40°C to 150°C
LTC7840EUFD#PBF	LTC7840EUFD#TRPBF	7840	28-Lead Plastic (4mm × 5mm) QFN	–40°C to 125°C
LTC7840IUFD#PBF	LTC7840IUFD#TRPBF	7840	28-Lead Plastic (4mm × 5mm) QFN	–40°C to 125°C
LTC7840HUFD#PBF	LTC7840HUFD#TRPBF	7840	28-Lead Plastic (4mm × 5mm) QFN	–40°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{RUN} = 2V and SS1,2 = open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Range			5.5		60	V
I_Q	Input DC Supply Current Normal Operation Shutdown	(Note 5) V_{IN} = 12V, V_{RUN} = 2V, No Switching V_{RUN} = 0V			 3 40	 5 80	 mA µA
$UVLO_{\_DRVCC}$	DRV_{CC} Undervoltage Lockout Threshold	DRV_{CC} Rising DRV_{CC} Falling			4.4 3.9		V V
$UVLO_{\_INTVCC}$	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising $INTV_{CC}$ Falling			3.3 3		V V
V_{FB1}, V_{FB2}	Regulated Feedback Voltage	$I_{TH1,2}$ Voltage = 1V (Note 6)	●	1.188	1.2	1.212	V
I_{FB1}, I_{FB2}	Feedback Current	(Note 6)			±5	±50	nA
D_{MAX}	Maximum Duty Cycle	V_{DMAX} = 0V (Note 8) V_{DMAX} = Float V_{DMAX} = $INTV_{CC}$			96 84 75		% % %
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB1}, V_{FB2}		8.5	10.5	12.5	%
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 5.5V to 60V (Note 6)			0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 6) In Servo Loop; ΔI_{TH} Voltage = 1V to 0.7V In Servo Loop; ΔI_{TH} Voltage = 1V to 1.3V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
g_{m1}, g_{m2}	EA Transconductance	$I_{TH1,2}$ Voltage = 1V; Sink/Source 5µA (Note 6)			0.8		mmho
I_{LIM1}, I_{LIM2}	Current Limit Setting Current	$I_{ILIM1,2}$ Voltage = 0.3V		9.5	10	10.5	µA
V_{ITH1}, $V_{ITH2(PSKIP)}$	Pulse Skip Mode I_{TH} Voltage	I_{TH} Voltage Rising (Note 6) Hysteresis			0.5 40		V mV
$I_{SS1,2}$	Soft Start Charge Current	$V_{TK/SS1,2}$ = 0V			10		µA
V_{RUN1}, V_{RUN2}	RUN Pin On Threshold	$V_{RUN1,2}$ Rising	●	1.1	1.22	1.35	V
$V_{RUN1,2}$ HYS	RUN Pin ON Hysteresis				80		mV
$I_{RUN1,2}$ HYS	RUN Pin Current Hysteresis				4.5		µA
Current Sensing							
I_{SENSE}+	Current Sense Pin Bias Current				–10		µA
I_{SENSE}–	Current Sense Pin Bias Current	V_{ITH} = 1.4V			–20		µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$I_{LIM1,2}$ = Float	●	70	75	80	mV
$I_{MISMATCH}$	Channel-to-Channel Current Mismatch	ILIM = Float				5	%
Gate Drivers							
$R_{UP1,2}$	Driver Pull-Up $R_{DS(ON)}$	GATE High			2		Ω
$R_{DOWN1,2}$	Driver Pull-Down $R_{DS(ON)}$	GATE Low			1.0		Ω
$t_{ON(MIN)1}$	Minimum On-Time	V_{BLANK} = 0V (Note 7)			120		ns
$t_{ON(MIN)2}$	Minimum On-Time	V_{BLANK} = Float (Note 7)			160		ns
$t_{ON(MIN)3}$	Minimum On-Time	V_{BLANK} = $INTV_{CC}$ (Note 7)			200		ns
DRV_{CC} Linear Regulator							
DRV_{CC}	Internal LDO Output Voltage for Gate Driver	12V < V_{IN} < 60V		9.6	10	10.4	V
ΔDRV_{CC}(Load)	DRV_{CC} Load Regulation	I_{CC} = 0 to 20mA			0.5	2	%

ELECTRICAL CHARACTERISTICS

(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{RUN} = 2V and SS1,2 = open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
$INTV_{CC}$	Internal LDO Output Voltage for Control Circuit			3.65	3.8	3.95	V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.03V (Note 3)	 ●	185 160	200 200	215 240	kHz kHz
f_{RANGE}	Frequency Range			50		425	kHz
f_{SYNC}	SYNC Frequency Range			50		450	kHz
V_{SYNC}	SYNC Input Threshold	V_{SYNC} Rising V_{SYNC} Falling		1.6		 0.3	V V
Φ2 – Φ1	Channel 2 to Channel 1 Phase Delay				180		Deg
Power Good Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 3V				1	µA
V_{PG}	PGOOD Trip Level	$V_{FB1,FB2P}$ with Respect to Set Output Voltage $V_{FB1,FB2P}$ Ramping Up $V_{FB1,FB2P}$ Ramping Down			 10 –10		 % %
T_{DELAY}	V_{PGOOD} High to Low Delay Time	(Note 9)			135		µs

Note 1: Stresses beyond those listed in under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The LTC7840E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7840I is guaranteed over the full –40°C to 125°C operating junction temperature range and the LTC7840H is guaranteed over the full –40°C to 150°C operating temperature range. High junction temperature degrades operating lifetimes. Operating lifetime is degraded at junction temperature greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: The LTC7840 includes over-temperature protection that is intended to protect the devices during momentary overload conditions. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: Supply current in normal operation is dominated by the current needed to charge the external MOSFET gates. This current will vary with the supply voltage and the external MOSFETs used. See Applications Information.

Note 6: The LTC7840 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,FB2}$.

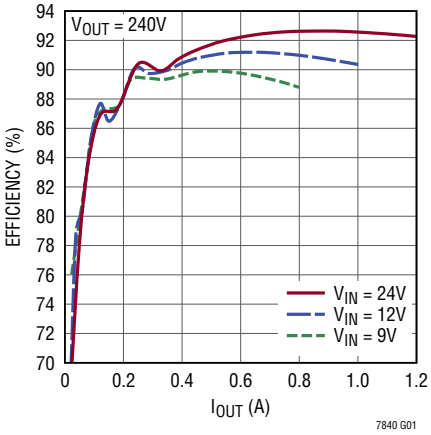
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥30% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: The maximum duty cycle limit is derived from an internal clock that runs at 12x the programmed switching frequency. See the Applications Information section for additional information.

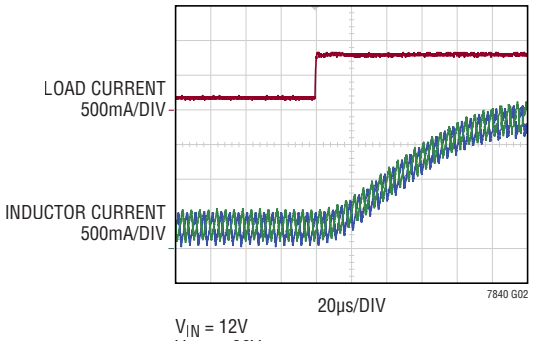
Note 9: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

Output Efficiency

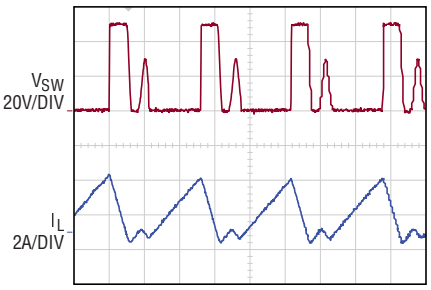


Dual Phase Single Output Load Transient (0.2A to 0.8A) (Circuit on Last Page)



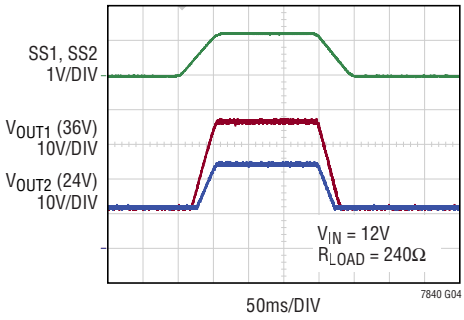
VIN = 12V
VOUT = 36V

Switch Node Voltage and Inductor Current at Light Load (300mA)

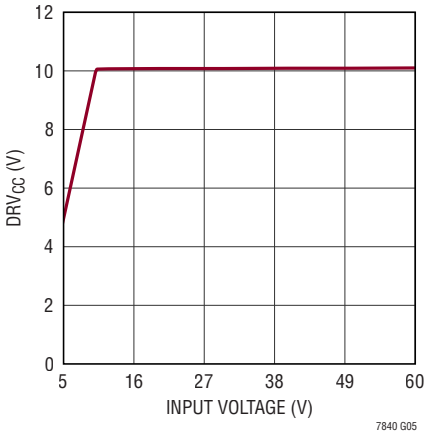


VIN = 12V
VOUT=48V

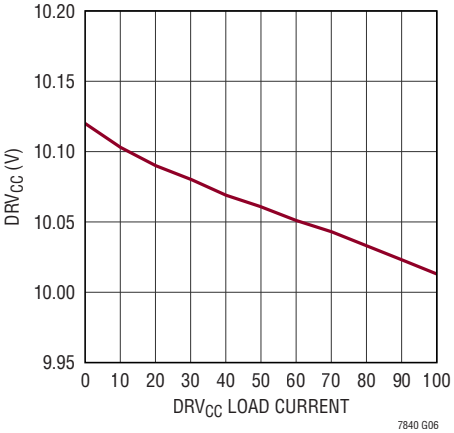
Output Voltage Tracking Up and Down with External Ramp



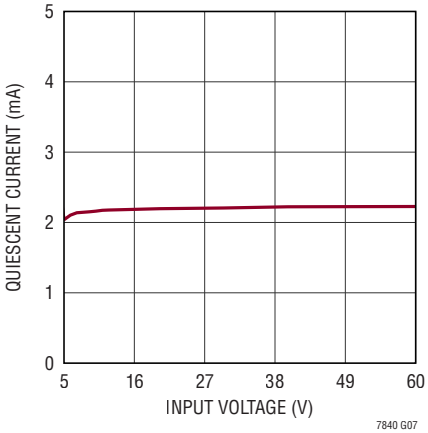
DRVCC Line Regulation



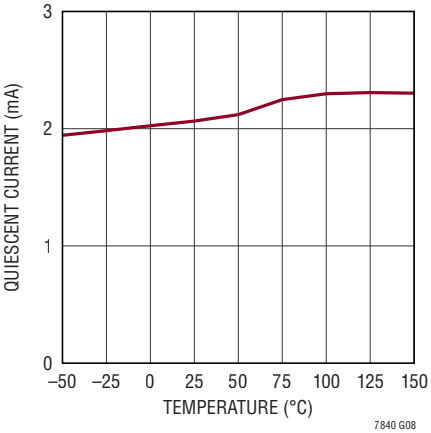
DRVCC Load Regulation



Quiescent Current vs Input Voltage

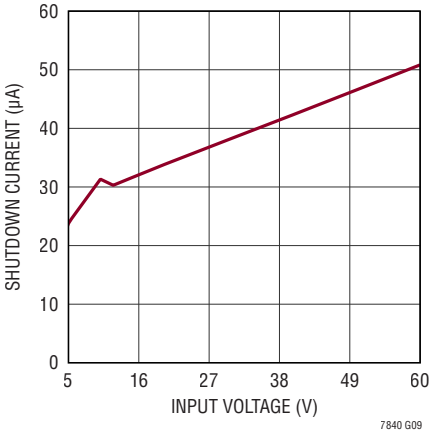


Quiescent Current vs Temperature

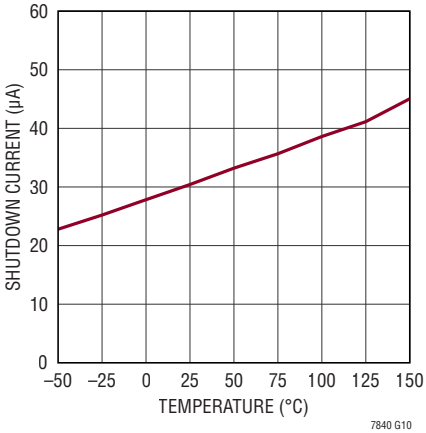


TYPICAL PERFORMANCE CHARACTERISTICS

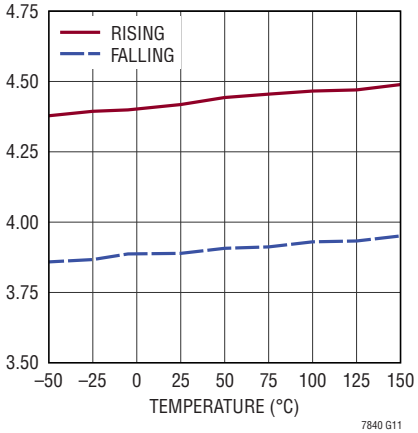
Shutdown Current vs Input Voltage



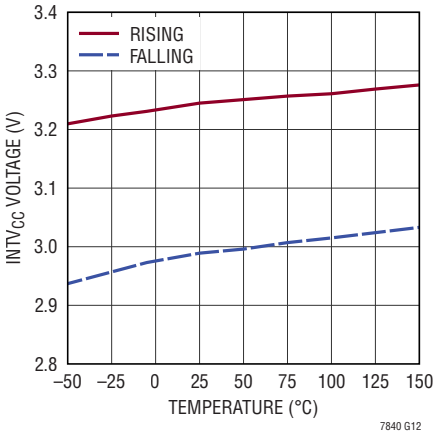
Shutdown Current vs Temperature



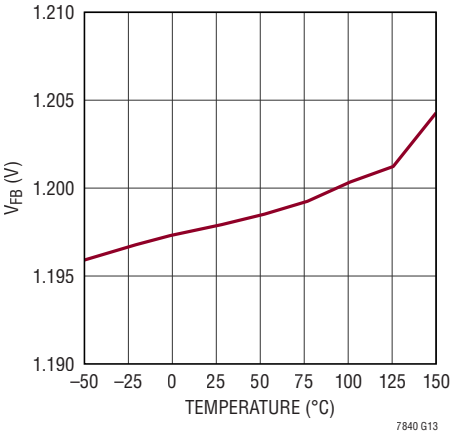
DRV_{CC} UVLO Threshold vs Temperature



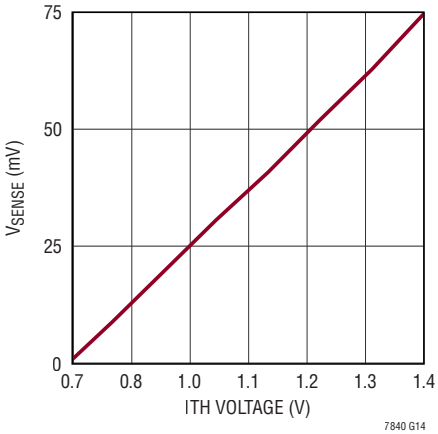
$INTV_{CC}$ UVLO Threshold vs Temperature



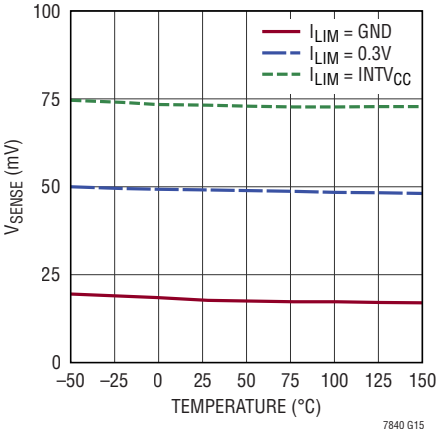
Feedback Voltage vs Temperature



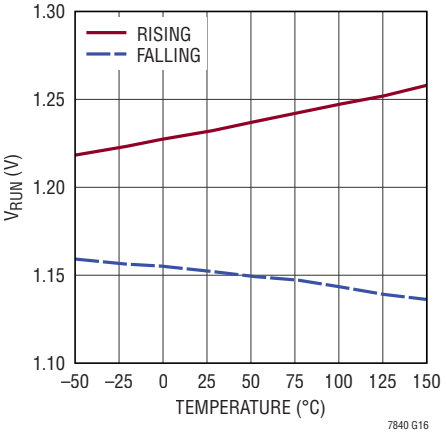
Current Sense Threshold vs ITH Voltage (ILIM Pin Float)



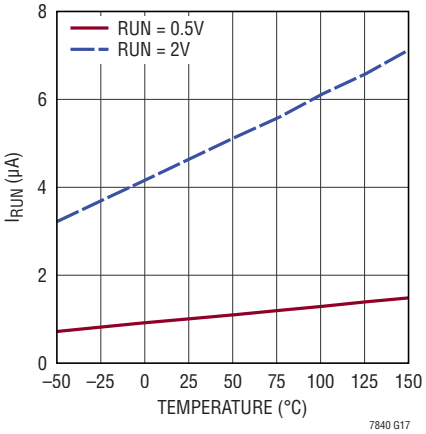
Current Sense Threshold vs Temperature



RUN Threshold vs Temperature

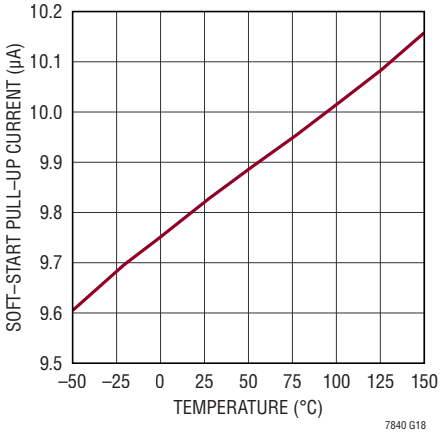


RUN Source Current vs Temperature

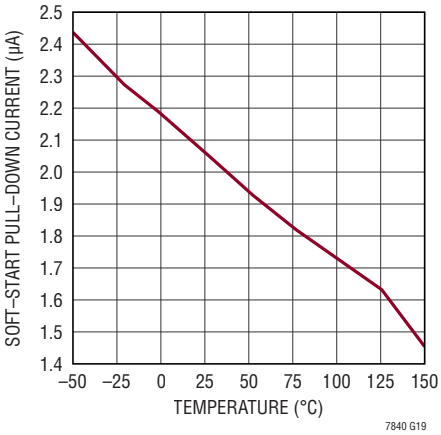


TYPICAL PERFORMANCE CHARACTERISTICS

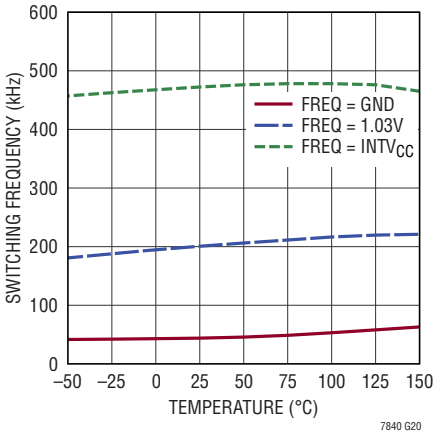
SS Pin Pull-Up Current vs Temperature



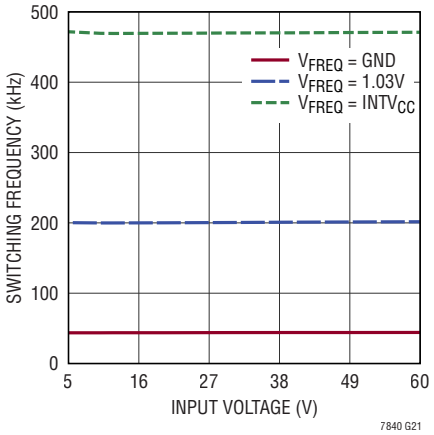
SS Pin Pull-Down Current vs Temperature



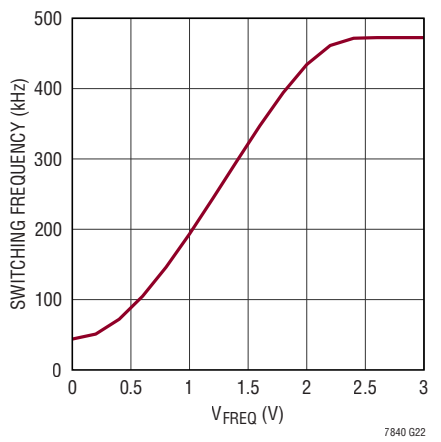
Switching Frequency vs Temperature



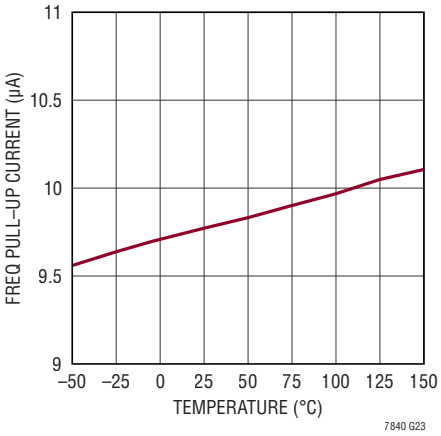
Switching Frequency vs Input Voltage



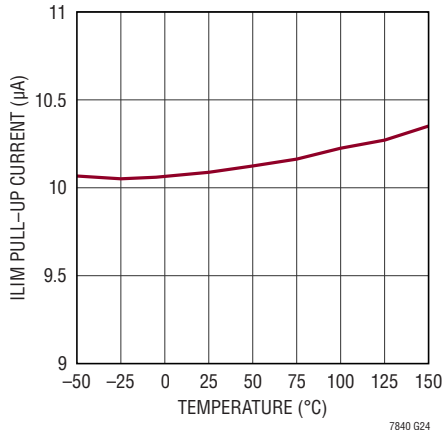
Switching Frequency vs FREQ Pin Voltage



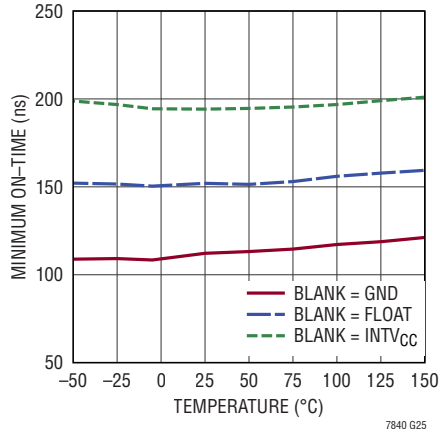
FREQ Pin Pull-Up Current vs Temperature



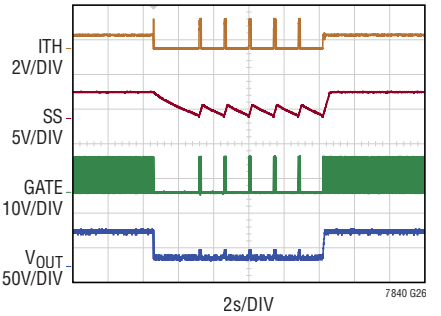
ILIM Pin Pull-Up Current vs Temperature



Minimum On-Time vs Temperature



Hiccup Mode Overcurrent Protection and Recovery (1µF SS Capacitor)



PIN FUNCTIONS (TSSOP/QFN)

RUN1 (Pin 9/Pin 6): Channel 1 Run Control Input. A voltage above 1.22V on this pin turns on the Channel 1. However, forcing this pin below 1.14V causes the Channel 1 to shut down. There is a 1.0µA pull-up current for this pin. Once the Run pin rises above 1.22V, an additional 4.5µA pull-up current is added to the pin.

RUN2 (Pin 10/Pin 7): Channel 2 Run Control Input. A voltage above 1.22V on this pin turns on the Channel 2. However, forcing this pin below 1.14V causes the Channel 2 to shut down. There is a 1.0µA pull-up current for this pin. Once the Run pin rises above 1.22V, an additional 4.5µA pull-up current is added to the pin.

$INTV_{CC}$ (Pin 25/Pin 22): Internal 3.8V LDO Output. The low voltage analog and digital circuits are powered from this voltage. Bypass this pin to SGND with 1nF low ESR ceramic capacitor.

ILIM1 (Pin 26/Pin 23): Channel 1 Current Comparator's Sense Voltage Range Input Pin. There is a precise 10µA current flowing out of this pin. A resistor to SGND can set the voltage on this pin to program the maximum current sense threshold to any voltage lower than 75mV. Alternatively, a DC voltage which is lower than 0.5V can be added to this pin to adjust the maximum current sense threshold. Floating this pin makes the current comparator's maximum sense voltage be 75mV.

ILIM2 (Pin 16/Pin 13): Channel 2 Current Comparator's Sense Voltage Range Input Pin. There is a precise 10µA current flowing out of this pin. A resistor to SGND can set the voltage on this pin to program the maximum current sense threshold to any voltage lower than 75mV. Alternatively, a DC voltage which is lower than 0.5V can be added to this pin to adjust the maximum current sense threshold. Floating this pin makes the current comparator's maximum sense voltage be 75mV.

D_{MAX} (Pin 4/Pin 1): Maximum Duty Cycle. This pin programs the maximum duty cycle. Floating this pin provides 84% duty cycle. Connecting this pin to $INTV_{CC}$ provides 75% duty cycle, while connecting this pin to SGND provides 96% duty cycle.

VFB1 (Pin 7/Pin 4): Channel 1 Error Amplifier Feedback Input. This pin connects to the center tap of an external resistor divider across the Channel 1 output.

VFB2 (Pin 12/Pin 9): Channel 2 Error Amplifier Feedback Input. This pin connects to the center tap of an external resistor divider across the Channel 2 output.

FREQ (Pin 5/Pin 2): Oscillator Frequency Control Input. There is a precise 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

GATE1 (Pin 21/Pin 18): Channel 1 Gate Drive Output. The LTC7840 provides a 10V gate drive referred to PGND to drive a high voltage MOSFET.

GATE2 (Pin 19/Pin 16): Channel 2 Gate Drive Output. The LTC7840 provides a 10V gate drive referred to PGND to drive a high voltage MOSFET.

DRV_{CC} (Pin 22/Pin 19): Internal 10V LDO Output. The gate drivers are powered from this voltage. Bypass this pin to PGND with a minimum of 4.7µF low ESR ceramic capacitor.

ITH1 (Pin 8/Pin 5): Channel 1 Current Control Threshold and Error Amplifier Compensation Point. Channel 1's current comparator's tripping threshold increases with this control voltage.

ITH2 (Pin 13/Pin 10): Channel 2 Current Control Threshold and Error Amplifier Compensation Point. Channel 2's current comparator's tripping threshold increases with this control voltage.

SGND (Pin 24/Pin 21 and Exposed Pad): Signal Ground Pin. All small-signal components and compensation components should connect to this ground.

PGND (Pin 20/Pin 17): Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs and the negative terminals of the V_{IN} and DRV_{CC} bypassing capacitors.

PIN FUNCTIONS (TSSOP/QFN)

BLANK (Pin 1/Pin 26): Blanking Time Pin. Floating this pin provides a nominal minimum on-time of 160ns. Connecting this pin to $INTV_{CC}$ provides a minimum on-time of 200ns, while connecting this pin to SGND provides a minimum on-time of 120ns.

SENSE1+ (Pin 28/Pin 25): Positive Terminal of Channel 1 Current Comparator. This pin is normally connected to a sense resistor in series with the source of the power MOSFET.

SENSE2+ (Pin 14/Pin 11): Positive Terminal of Channel 2 Current Comparator. This pin is normally connected to a sense resistor in series with the source of the power MOSFET.

SENSE1- (Pin 27/Pin 24): Negative Terminal of Channel 1 Current Comparator. This pin is normally connected to the bottom of the sense resistor.

SENSE2- (Pin 15/Pin 12): Negative Terminal of Channel 2 Current Comparator. This pin is normally connected to the bottom of the sense resistor.

SS1 (Pin 6/Pin 3): Soft Start Inputs. A capacitor to SGND at this pin sets the ramp rate for Channel 1's output voltage. An internal soft start current of 10µA charges this pin. The Hiccup Mode timing is also set by this pin. At least 0.1µF capacitor is needed between this pin and SGND.

SS2 (Pin 11/Pin 8): Soft Start Inputs. A capacitor to SGND at this pin sets the ramp rate for Channel 2's output voltage. An internal soft start current of 10µA charges this pin. The Hiccup Mode timing is also set by this pin. At least 0.1µF capacitor is needed between this pin and SGND.

SYNC (Pin 3/Pin 28): PLL Synchronization Input. Applying an external clock between 50 kHz and 450 kHz will force the operating frequency to synchronize to the clock. The PLL compensation network is integrated into the IC. This pin has an internal 100kΩ pull down resistor. An external clock signal with amplitude greater than 1.6V is considered active high, while with amplitude less than 0.3V is considered active low.

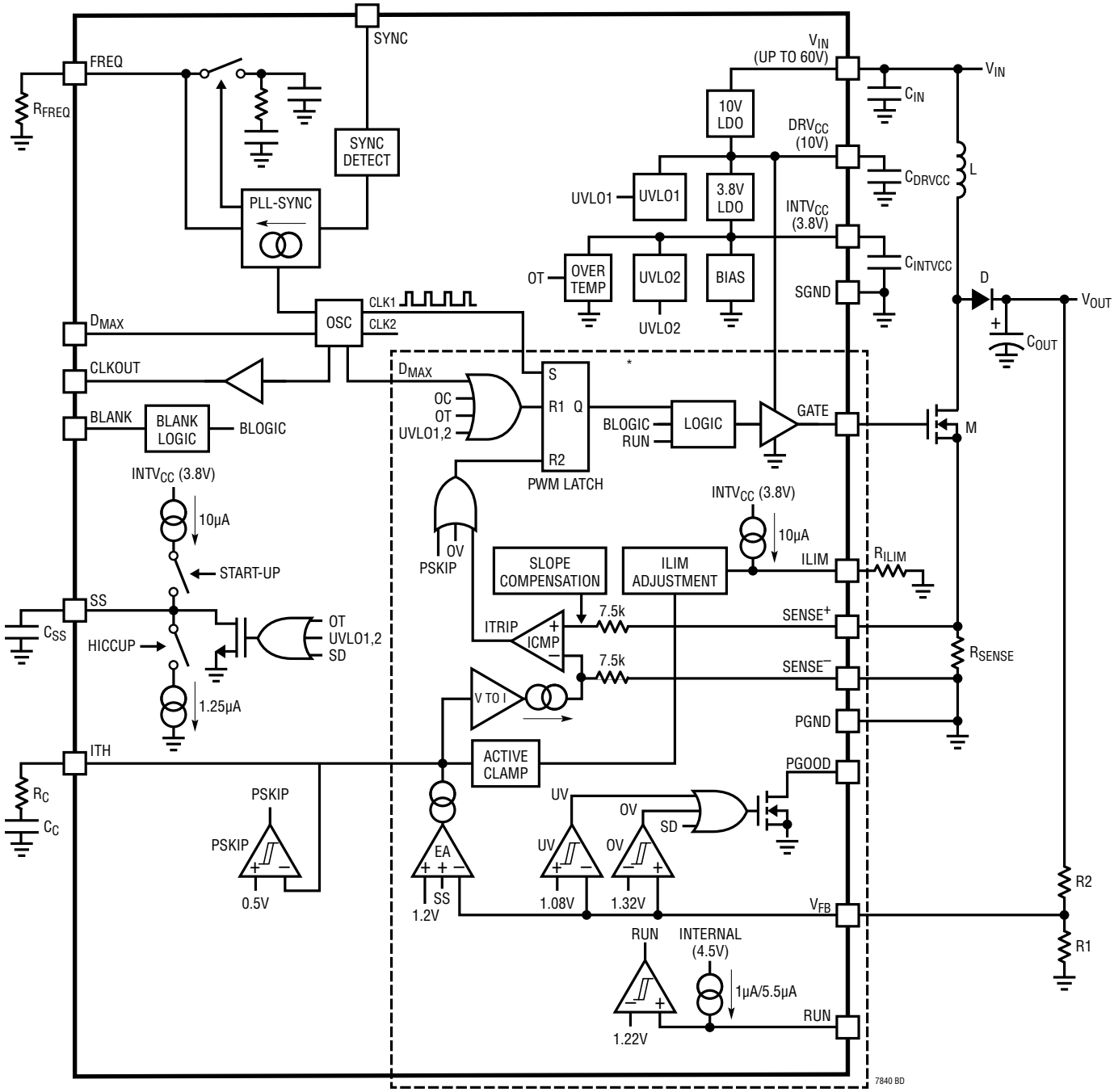
PGOOD1 (Pin 18/Pin 15): Power Good Indicator Output for Channel 1. Open drain logic that is pulled to ground when Channel 1's output exceeds its ±10% regulation window after the internal 135µs power bad mask timer expires.

PGOOD2 (Pin 17/Pin 14): Power Good Indicator Output for Channel 2. Open drain logic that is pulled to ground when Channel 2's output exceeds its ±10% regulation window after the internal 135µs power bad mask timer expires.

V_{IN} (Pin 23/Pin 20): Main Input Supply. Bypass this pin to PGND with a capacitor (0.1µF to 1 µF).

CLKOUT (Pin 2/Pin 27): Clock Output Pin. Clock output used for daisy-chaining multiple LTC7840 ICs in multiphase systems. The phase shift from Channel 1 to Clock Output is 90°.

BLOCK DIAGRAM



* DUPLICATE FOR SECOND CHANNEL

OPERATION

The Control Loop

The LTC7840 is a constant frequency, current mode, boost controller with two channels operating 180° out-of-phase. During normal operation, each external MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The error amplifier compares the output feedback signal at the VFB pin to the internal 1.2V reference and generates an error signal at the I_{TH} pin. When the load current increases, it causes a slight decrease in the feedback relative to the 1.2V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the MOSFET is turned off, the inductor current flows through the boost diode into the output capacitor and load, until the beginning of the next clock cycle.

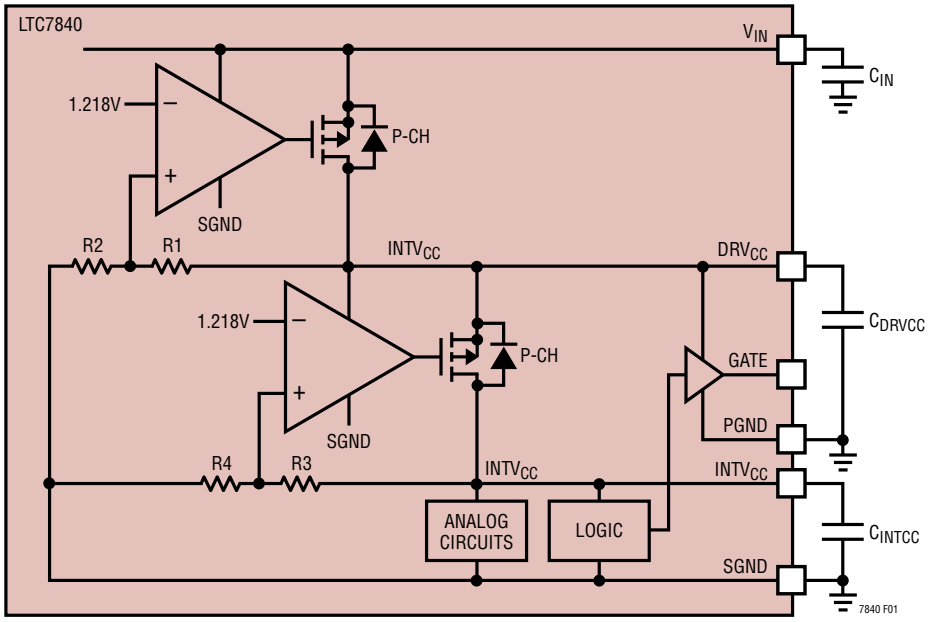
Cascaded LDOs Supply Power to the Gate Driver and Control Circuitry

The LTC7840 contains two cascaded PMOS output stage low dropout regulators (LDOs), one for the gate driver supply (DRV_{CC}) and one for the low voltage analog and digital control circuitry ($INTV_{CC}$). A block diagram of this power supply architecture is shown in Figure 1.

The output of either LDO cannot be biased from external power supply. Otherwise, two possible failure modes will be caused. As shown in Figure 1, there are body diodes in parallel with the PMOS output transistors in the two LDO regulators. If the DRV_{CC} or $INTV_{CC}$ supply comes up before the V_{IN} supply, high current will flow from the external DRV_{CC} or $INTV_{CC}$ supply through the body diode to the input capacitor and V_{IN} pin. This high current flow could cause catastrophic failure of the IC.

If the V_{IN} supply comes up before the DRV_{CC} or $INTV_{CC}$ supply, or if the DRV_{CC} or $INTV_{CC}$ pins are biased to any voltage lower than the regulated voltage by low-impedance voltage sources, the LDO will attempt to pull up its output voltage and this current will result in excessive power dissipation and possible thermal overload of the LTC7840.

Also, in multi-chip parallel applications, the output pins of LDOs should not be connected together. When two or more LDO outputs are tied together, the highest voltage regulator supplies all of the gate driver and control



NOTE: PLACE C_{DRVCC} AND C_{INTVCC} CAPACITORS AS CLOSE AS POSSIBLE TO DEVICE PINS

Figure 1. Cascaded LDOs Provide Gate Driver and Control Circuitry Power

OPERATION

circuit current, but the other regulators are off. This would place a thermal burden on the highest output voltage LDO and could cause the maximum die temperature to be exceeded. In multi-chip parallel applications, each LDO output should be independently bypassed to its respective GND pin as close as possible to each IC.

The Gate Driver Supply LDO (DRV_{CC})

The 10V output (DRV_{CC}) of the first LDO is powered from V_{IN} and supplies power to the power MOSFET gate drivers. The DRV_{CC} pin should be bypassed to PGND with a minimum of 4.7µF ceramic capacitor (X5R or better) placed as close as possible to the IC pin. If two power MOSFETs are connected in parallel for each channel in order to increase the output power level, or if a single MOSFET with a Q_g greater than 50nC is used, then it is recommended that the bypass capacitor be increased to a minimum of 10µF.

An under voltage lockout (UVLO) circuit senses the DRV_{CC} regulator output in order to protect the power MOSFETs from operating with the inadequate gate drive. For the LTC7840, the rising UVLO threshold is 4.4V and the hysteresis is typically 500mV. In low V_{IN} applications, the low threshold MOSFET (<3.5V) may be used. In high V_{IN} applications, higher UVLO may be programmed as shown in Figure 5. The LTC7840 is optimized for high voltage power MOSFETs with $R_{DS(ON)}$ ratings at a V_{GS} of 6V.

The Low Voltage Analog and Digital Supply LDO ($INTV_{CC}$)

The second LDO within the LTC7840 is powered from DRV_{CC} and serves as the supply to the low voltage analog and digital control circuitry. The output ($INTV_{CC}$) voltage of this LDO is 3.8V. The $INTV_{CC}$ pin should be bypassed to SGND with a 1nF ceramic capacitor (X5R or better) placed as close as possible to the IC pin. This LDO is not intended to be used as a supply for external circuitry.

Thermal Considerations and Package Options

The LTC7840 is offered in two package options. The 28-lead thermally enhanced TSSOP package (FE28) has a thermal resistance $R_{TH(JA)}$ of 30°C/W, and the 4mm x 5mm 28-lead QFN package (UFD28) has a thermal resistance of 47°C/W. The TSSOP package has a lead pitch of 0.65mm, whereas the QFN package has a lead pitch of 0.5mm.

The DRV_{CC} LDO can supply up to 100mA current. As a result, care must be taken to ensure that the maximum junction temperature of the IC should not be exceeded. The junction temperature can be estimated by the following equations:

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

$$P_{DISS} = V_{IN} \bullet (I_Q + Q_{G(TOT)} \bullet f$$

$$T_J = T_A + P_{DISS} \bullet R_{TH(JA)}$$

The total quiescent current ($I_{Q(TOT)}$) consists of the static supply current (I_Q) and the current required to charge the gate capacitance of the power MOSFETs. The value of $Q_{G(TOT)}$ should come from the plot of V_{GS} vs Q_G in the Typical Performance Characteristics section of the MOSFET data sheet. The value listed in the electrical specifications may be measured at a higher V_{GS}, such as 15V, whereas the value of interest is at the 10V DRV_{CC} gate drive voltage.

As an example of the required thermal analysis, consider a 2-phase boost converter with a 5.5V to 24V input voltage range and an output voltage of 72V at 1.5A. The switching frequency is 150kHz and the maximum ambient temperature is 70°C. The power MOSFET used for this application is the Renesas HAT2267H, which has a typical $R_{DS(ON)}$ of 13mΩ at V_{GS} = 10V. From the plot of V_{GS} vs Q_G, the total gate charge at V_{GS} = 10V is 30nC (the temperature coefficient of the gate charge is low). One power MOSFET is used for each phase. For the QFN package option:

$$I_{Q(TOT)} = 3mA + 2 \bullet 30nC \bullet 150kHz = 12mA$$

$$P_{DISS} = 24V \bullet 12mA = 288mW$$

$$T_J = 70°C + 288mW \bullet 30°C/W = 78.64°C$$

In this example, the junction temperature rise is only 8.64°C. These equations demonstrate how the gate charge current typically dominates the quiescent current of the IC, and how the choice of package option and board heat sinking can have a significant effect on the thermal performance of the solution.

OPERATION

To prevent the maximum junction temperature from being exceeded, the input supply current to the IC should be checked when operating in continuous mode (heavy load) at maximum V_{IN}. A trade-off between the operating frequency and the size of the power MOSFETs may need to be made in order to maintain a reliable junction temperature. As an option, an external regulator shown in Figure 3 can be used to reduce the total power dissipation on the IC. Finally, it is important to verify the calculations by performing a thermal analysis of the final PCB using an infrared camera or thermal probe.

Thermal Shutdown Protection

In the event of an overtemperature condition (external or internal), an internal thermal monitor will shut down the gate drivers and reset the soft-start capacitor if the die temperature exceeds 170°C. This thermal sensor has a hysteresis of 10°C to prevent erratic behavior at hot temperatures. The LTC7840's internal thermal sensor is intended to protect the device during momentary overtemperature conditions. Continuous operation above the specified maximum operating junction temperature, however, may result in device degradation.

Operation at Low Supply Voltage

The LTC7840 has a minimum input voltage of 5.5V, making it a good choice for applications that require high voltage power MOSFETs with 6V $R_{DS(ON)}$ ratings. The gate driver for the LTC7840 consists of PMOS pull-up and NMOS pull-down devices, allowing the full DRV_{CC} voltage to be applied to the gates during power MOSFET switching. Nonetheless, care should be taken to determine the minimum gate drive supply voltage (DRV_{CC}) in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage ($V_{IN(MIN)}$), the LDO dropout voltage, the Q_G of the power MOSFETs, and the operating frequency.

If the input voltage V_{IN} is low enough for the DRV_{CC} LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{DRVCC} = V_{IN(MIN)} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 3mA). A curve of dropout voltage vs output current for the LDO is shown in Figure 2.

The total Q-current ($I_{Q(TOT)}$) flowing in the LDO is the sum of the controller quiescent current (3mA) and the total gate charge drive current.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

After the calculations have been completed, it is important to measure the gate drive waveforms and the gate driver supply voltage (DRV_{CC} to PGND) over all operating conditions (low V_{IN}, nominal V_{IN} and high V_{IN}, as well as from light load to full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured V_{GS}, and verify your thermal calculations by measuring the component temperatures using an infrared camera or thermal probe.

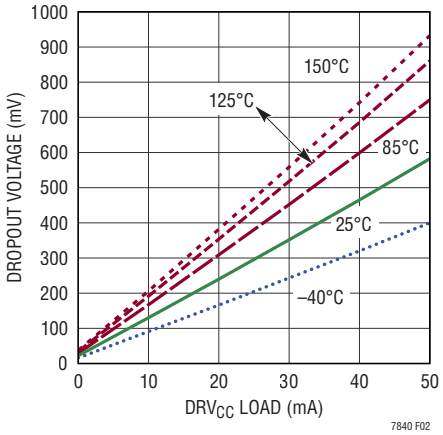


Figure 2. DRV_{CC} LDO Dropout Voltage vs Current

OPERATION

Operation at High Supply Voltage

At high input voltages, the LTC7840's internal LDO can dissipate a significant amount of power, which could cause the maximum junction temperature to be exceeded. Conditions such as a high operating frequency, or the use of more than one power MOSFET per channel, could push the junction temperature rise to high levels. If the thermal equations above indicate too high a rise in the junction temperature, an external bias supply can always be used to reduce the power dissipation on the IC, as shown in Figure 3.

For example, a 12V system rail that is available would be more suitable than the 24V main input power rail to power the LTC7840. Also, the bias power can be generated with a separate switching or LDO regulator. An example of an LDO regulator is shown in Figure 3. The output voltage of the LDO regulator can be set by selecting an appropriate zener diode to be higher than 10V but low enough to divide the power dissipation between LTC7840 and Q1 in Figure 3.

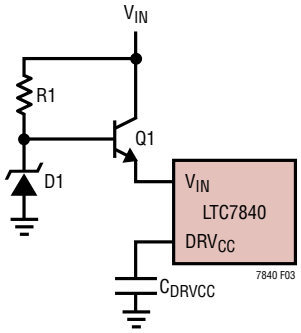


Figure 3. Using the LTC7840 with an External Bias Supply

Programming the Output Voltage

The output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 1.2V\left(1+\frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in Figure 4. Resistor R1 is normally chosen so that the output voltage error caused by the current flowing out of the V_{FB} pin during normal operation is negligible compared to the current in the divider. For an output voltage error due to the error amp input bias current of less than 0.5%, this translates to a maximum value of R1 of about 30k.

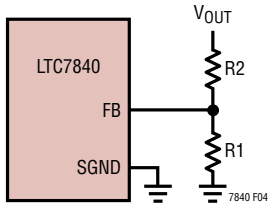


Figure 4. Programming the Output Voltage with a Resistor Divider

Shutdown and Start-Up (RUN1, RUN2 and SS1, SS2 Pins)

The two channels of the LTC7840 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.14V shuts down the main control loop for that channel. Pulling both pins low disables both channels and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ regulator. Releasing either RUN pin allows an internal 1µA current to pull up the pin and enable the controller. Alternatively, the RUN pins may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on these pins.

Thirdly, the RUN1 and RUN2 pins can also be used to detect V_{IN} undervoltage condition. The circuit shown in Figure 5 provides an example. When the voltage on either RUN pin exceeds 1.22V, the pull up current is switched from 1µA to 5.5µA to provide some hysteresis. The user can program both the rising threshold and the amount of hysteresis by adjusting the values of the resistors in the external divider, as shown in the following equations:

$$V_{IN(ON)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 1\mu A \bullet R_A$$

$$V_{IN(OFF)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 5.5\mu A \bullet R_A$$

OPERATION

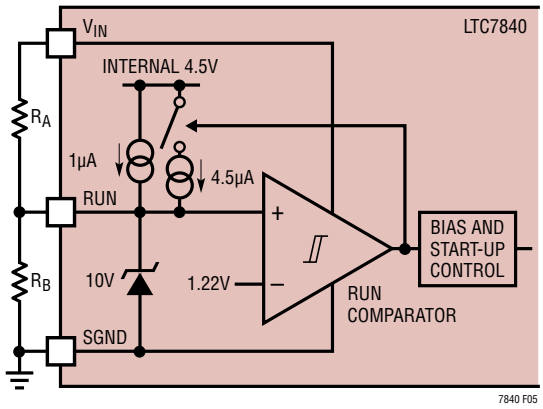


Figure 5. Programming the Input Voltage Turn-On and Turn-Off Thresholds Using the RUN Pin

The start-up of each channel's output voltage, V_{OUT}, is controlled by the voltage on its SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC7840 regulates the V_{FB} voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program the soft-start period by connecting an external capacitor from the SS pin to SGND. An internal 10µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. The soft-start-up time can be estimated by:

$$t_{START\text{-}UP} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

$$= 0.12 \bullet C_{SS}$$

The SS pin has an internal open-drain NMOS pull-down transistor that turns on when the RUN pin is pulled low, when the voltage on the $INTV_{CC}$ pin or DRV_{CC} pin is below its undervoltage lockout threshold, or during an overtemperature condition.

Frequency Selection and Phase-Locked Loop (FREQ and SYNC Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC7840's controller can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 50kHz to 425kHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. The curve in Figure 6 shows the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is integrated on the LTC7840 to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin. The PLL loop filter network is also integrated inside the LTC7840. The phase-locked loop is capable of locking to any frequency within the range of 50kHz to 450kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency to the same value as the synchronized frequency before locking to the external clock. The lock-in time can be minimized by this way. It also ensures that the operating frequency remains essentially constant in the event the sync signal is lost. The SYNC pin has an internal 100k resistor to ground.

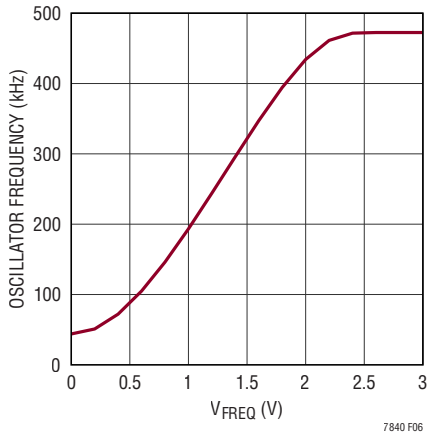


Figure 6. Switching Frequency vs FREQ Pin Voltage

Power Good (PGOOD1, PGOOD2 Pins)

When either feedback voltage is not within ±10% of the 1.2V reference voltage, its respective PGOOD pin is pulled low. A PGOOD pin will also pull low when its channel is in the soft-start or UVLO. Both PGOOD pins pull low when

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the RUN pin is below 1.14V. The PGOOD pins will flag power good immediately when their feedback voltages are within ±10% of the reference window. However, there is an internal 135µs power bad mask when feedback voltages go out of the ±10% window. The PGOOD pins are allowed to be pulled up by external resistors to sources of up to 6V.

Multichip Operations (CLKOUT Pin)

The LTC7840 uses CLKOUT pin to allow multiple ICs to be daisy-chained together for higher current multi-phase applications. For a 4-phase design, the CLKOUT signal of the master controller is connected to the SYNC input of the slave controller in order to synchronize additional power stages for a single high current output. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used, and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

In LTC7840, Channel 1 and Channel 2 have 180° phase shift, whereas, CLKOUT signal has 90° phase shift relative to Channel 1. The duty cycle of CLKOUT signal is 50%.

Using the LTC7840 Transconductance (g_m) Error Amplifier in Multi-Phase Applications

The LTC7840 error amplifier is a transconductance, or g_m amplifier, meaning that it has high DC gain but high output impedance (the output of the error amplifier is a current proportional to the differential input voltage). This style of error amplifier greatly eases the task of implementing a multi-phase solution, because the amplifiers from two or more chips can be connected in parallel. In this case the FB pins of multiple LTC7840s can be connected together, as well as the I_{TH} pins, as shown in Figure 7. The g_m of the composite error amplifier is simply n times the transconductance of one amplifier, or $g_{m(TOT)} = n \bullet 800\mu S$, where n is the number of amplifiers connected in parallel. The transfer function from the I_{TH} pin to the current comparator inputs was carefully designed to be accurate, both from channel-to-channel and chip-to-chip. This way the peak inductor current matching is kept accurate.

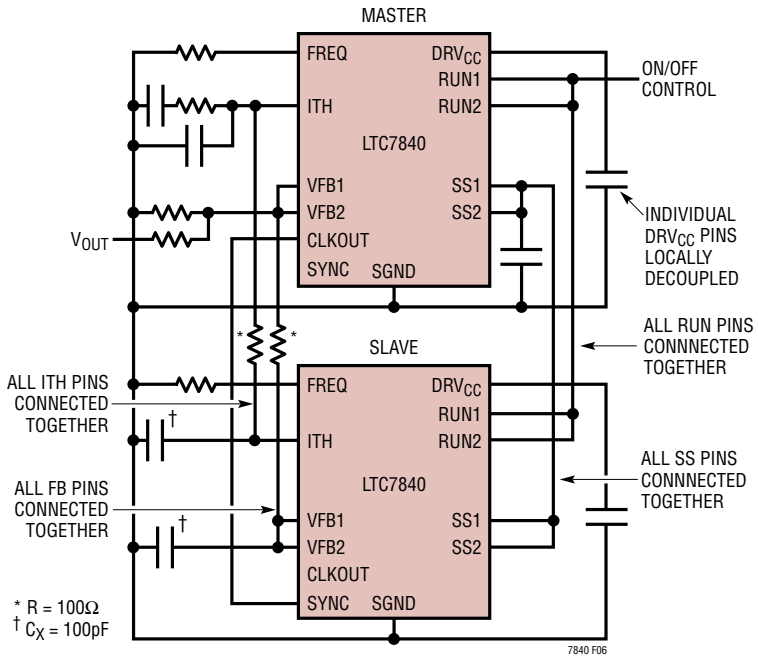

Figure 7. LTC7840 Error Amplifier Configuration for Multi-Phase Operation

OPERATION

A buffered version of the output of the error amplifier determines the threshold at the input of the current comparator. The I_{TH} voltage that represents zero peak current is 0.7V and the voltage that represents current limit is from 1.4V (at zero duty cycle) to 2.1V (at 100% duty cycle). There is a circuit in the LTC7840 to recover the slope compensation signal, so that the maximum peak inductor current keeps constant over the duty cycle.

In multi-phase applications that use more than one LTC7840 controller, it is possible for ground currents on the PCB to disturb the control lines between the ICs, resulting in erratic behavior. In these applications the FB pins should be connected to each other through 100Ω resistors and each slave FB pin should be decoupled locally with a 100pF capacitor to ground, as shown in Figure 7.

Pulse-Skipping Operation at Light Load

As the load current decreases, the loop will make the I_{TH} voltage drop and the peak inductor current will reduce accordingly. If the load current keeps decreasing, the controller will enter discontinuous mode (DCM) automatically. The peak inductor current can reduce until the minimum on-time of the controller is reached. Any further decrease in the load current will cause I_{TH} voltage to continue going down until it reaches 0.5V, then the controller will enter pulse-skipping mode in order to maintain output regulation. The internal pulse-skip-mode comparator has a 50mV hysteresis.

Programmable Blanking and the Minimum On-Time

The BLANK pin on the LTC7840 allows the user to program the amount of leading edge blanking at the SENSE pins. Connecting the BLANK pin to SGND results in a minimum on-time of 120ns, floating the pin increases this time to 160ns, and connecting the BLANK pin to the $INTV_{CC}$ supply results in a minimum on-time of 200ns. The majority of the minimum on-time consists of this leading edge blanking, due to the inherently low propagation delay of the current comparator and logic circuitry.

The purpose of leading edge blanking is to filter out noise on the SENSE pins at the leading edge of the power MOSFET turn-on. During the turn-on of the power MOSFET the gate drive current, the discharge of any parasitic capacitance on the SW node, the recovery of the boost diode charge, and parasitic series inductance in the high di/dt path all contribute to overshoot and high frequency noise that could cause false-tripping of the current comparator. Due to the wide range of LTC7840 applications, fixing one value of the internal leading edge blanking time would have required the longest delay time to have been used. Providing a means to program the blank time allows users to optimize the SENSE pin filtering for each application. Figure 8 illustrates the effect of the programmable leading edge blank time on the minimum on-time of a boost converter.

Programmable Maximum Duty Cycle

In order to maintain constant frequency and a low output ripple voltage, a single-ended boost (or flyback or SEPIC) converter is required to turn off the switch every cycle for some minimum amount of time. This off-time allows the transfer of energy from the inductor to the output capacitor and load, and prevents excessive ripple current and voltage. For inductor-based topologies like boost and SEPIC converters, having a maximum duty cycle as close as possible to 100% may be desirable, especially in low V_{IN} to high V_{OUT} applications. However, for transformer-based solutions, having a maximum duty cycle near 100% is undesirable, due to the need for V • sec reset during the primary switch off-time.

In order to satisfy these different applications requirements, the LTC7840 has a simple way to program the maximum duty cycle. Connecting the D_{MAX} pin to SGND limits the maximum duty cycle to 96%. Floating this pin limits the duty cycle to 84% and connecting the D_{MAX} pin to $INTV_{CC}$ limits the duty cycle to 75%. Figure 9 illustrates the effect of limiting the maximum duty cycle on the SW node waveform of a boost converter.

The LTC7840 contains an oscillator that runs at 12× the programmed switching frequency. A digital counter is used to divide down the fundamental oscillator frequency. Since the maximum duty cycle limit is obtained from this digital counter, the percentage maximum duty cycle does not vary with process tolerances or temperature.

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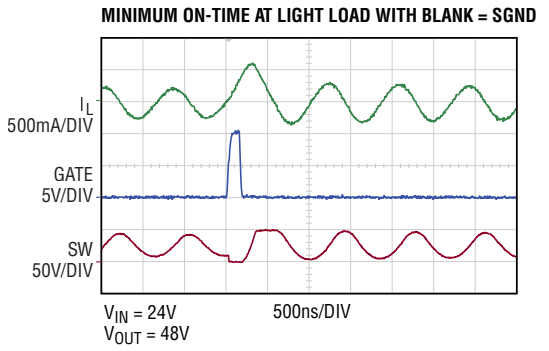

Figure 8. Leading Edge Blanking Effects on the Minimum On-Time

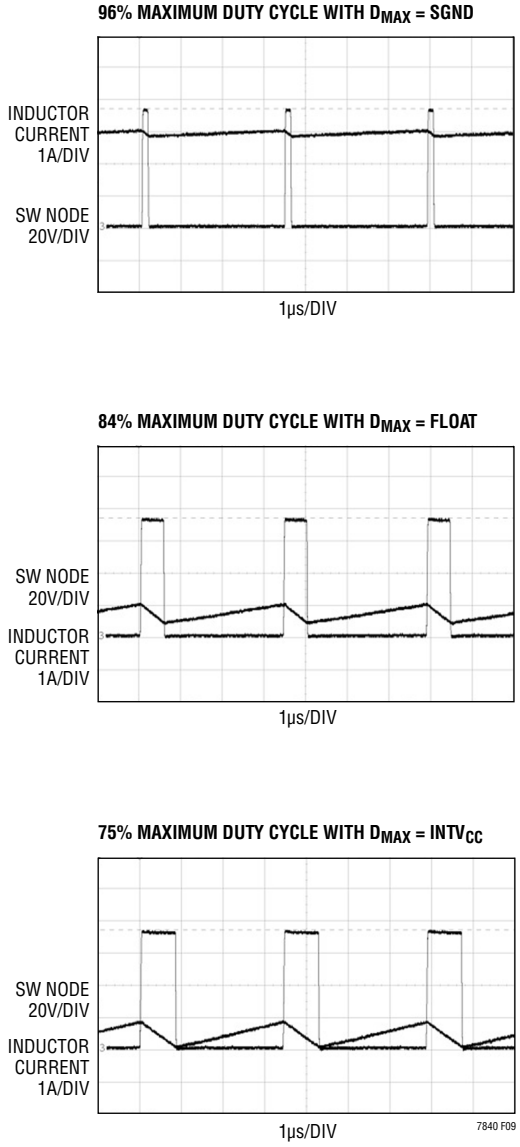

Figure 9. SW Node Waveforms with Different Duty Cycle Limits

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The SENSE+ and SENSE– Pins

Since the LTC7840 contains leading edge blanking, an external RC filter is not required for proper operation. However, if an external filter is used, the filter components should be placed close to the SENSE+ and SENSE– pins on the IC, as shown in Figure 10. The positive and negative sense node traces should then run parallel to each other to a Kelvin connection underneath the sense resistor, as shown in Figure 11. Sensing current elsewhere on the board can add parasitic inductance and capacitance to the current sense element, degrading the information at the sense pins and making the programmed current limit unpredictable. Avoid the temptation to connect the SENSE– line to the ground plane using a PCB via; this could result in unpredictable behavior.

The sense resistor should be connected to the source of the power MOSFET and the ground node using short, wide PCB traces, as shown in Figure 11. Ideally, the bottom terminal of the sense resistors will be immediately adjacent to the negative terminal of the output capacitor, since this path is a part of the high di/dt loop formed by the switch, boost diode, output capacitor and sense resistor. Placement of the inductors is less critical, since the current in the inductors is a triangle waveform.

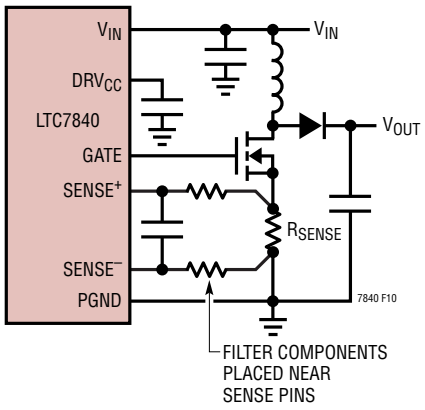

Figure 10. Proper Current Sense Filter Component Placement

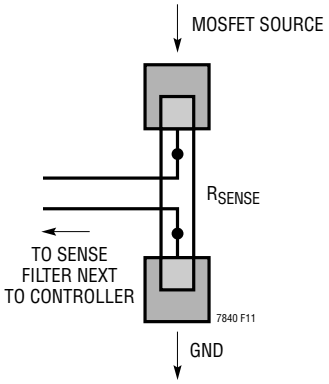

Figure 11. Connecting the SENSE+ and SENSE– Traces to the Sense Resistor Using a Kelvin Connection

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the external power MOSFET is turned off until the overvoltage condition is cleared.

Overcurrent Protection (ILIM1, ILIM2 Pins and Hiccup Mode)

The LTC7840 has ILIM1 and ILIM2 pins to set the maximum inductor current limit of each channel respectively, as described in the ILIM1 and ILIM2 pins function. The voltage on each ILIM pin is used to generate the internal I_{TH} clamp voltage. Along with the increase of load current, I_{TH} voltage will rise to allow higher inductor current flowing to the load. If the load current keeps increasing, the I_{TH} voltage will finally reach the clamp voltage and the inductor current cannot go up any more. This situation is thought as an overcurrent event by the controller. If this event lasts for 16 continuous switching periods, the controller will enter hiccup mode. The I_{TH} voltage is pulled down to GND and the external power MOSFET is turned off. The inductor current will gradually reduce to zero. At this moment, the soft-start capacitor connected

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between the SS pin and SGND is discharged by a 1.25µA current. When the voltage on SS pin reaches 0V, the I_{TH} pin is released and the controller retries to soft-start, as described in the Shutdown and Start-Up section. The hiccup mode is disabled during the soft-start period. To realize the function of the hiccup mode, a minimum 0.1µF soft-start capacitor has to be connected between the SS pin and SGND. The sleep time can be estimated by:

$$t_{SLEEP} = C_{SS} \bullet \frac{1.5V}{1.25\mu A} = 1.2 \bullet C_{SS}$$

Compared with the start-up time estimated in the Shutdown and Start-Up section, the sleep time is roughly 10 times the start-up time.

If the overcurrent situation is removed continuously for two or more switching periods before the 16 switching period timer expires, the 16 switching period timer will reset to zero and the output will soft recover by using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance, this may have resulted in output overshoot.

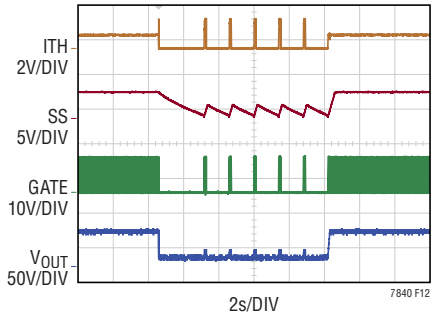

Figure 12. Hiccup Mode Overcurrent Protection and Recovery

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The LTC7840 is a dual-phase constant frequency current mode nonsynchronous step-up controller. This topology makes the output voltage not limited by the IC voltage. The LTC7840 can be configured in many ways as:

- a dual-phase dual-output boost converter with each phase operating independently;
- a dual-phase dual-output boost converter with one phase's output connected to the other phase's input. As a result of this two-step-up configuration, a much higher output voltage can be obtained;
- a dual-phase single-output boost converter;
- SEPIC topology;
- Other applications.

A wide 5.5V to 60V input voltage range can accommodate high input voltage surges. With the selectable leading edge blanking time, the noise on the SENSE pins at the leading edge of the power MOSFET turn-on is filtered out maximally. The programmable maximum duty cycle provides the flexibility to the user for configuring different topologies with LTC7840. The maximum current limit can be adjusted by the user based on the sense resistor value. For light load application, once I_{TH} drops below 0.5V, the controller is forced to skip cycles to maintain output regulation. Each channel of the LTC7840 has a power good indicator output to reflect if this channel's output voltage is within the regulation window. The LTC7840 can be configured for single-phase, dual-phase and 4-phase operation. The SYNC pin allows the IC to be synchronized to an external clock. Without the external clock, the switching frequency of the controller can be set by the voltage on the FREQ pin. The LTC7840 provides overcurrent protection by the hiccup mode. The controller also has output overvoltage protection.

In general, the external component selection is driven by the characteristics of the load and the input supply. Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left(\frac{V_O + V_F - V_{IN}}{V_O + V_F} \right) = t_{ON} \bullet f$$

where V_F is the forward voltage of the boost diode. The minimum on-time for a given application operating in CCM is:

$$t_{ON(MIN)} = \frac{1}{f}\left(\frac{V_O + V_F - V_{IN(MAX)}}{V_O + V_F} \right)$$

For a given input voltage range and output voltage, it is important to know how close the minimum on-time of the application comes to the minimum on-time of the control IC. The LTC7840 minimum on-time can be programmed from 120ns to 200ns using the BLANK pin.

Minimum On-Time Limitations

In a boost converter, two steady-state conditions can result in operation at the minimum on-time of the controller. The first condition is when the input voltage is close to the output voltage. When V_{IN} approaches V_{OUT} the voltage across the inductor approaches zero during the switch off-time. Under this operating condition the converter can become unstable and the output can experience high ripple voltage oscillation at audible frequencies. For applications where the input voltage can approach or exceed the output voltage, consider using a SEPIC or buck-boost topology instead of a boost converter.

The second condition that can result in operation at the minimum on-time of the controller is at light load, in deep discontinuous mode. As the load current is decreased, the on-time of the switch decreases, until the minimum on-time limit of the controller is reached. Any further decrease in the output current will result in pulse-skipping, a typically benign condition where cycles are skipped in order to maintain output regulation.

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Maximum Duty Cycle Limitations

Another operating extreme occurs at high duty cycle, when the input voltage is low and the output voltage is high. In this case:

$$D_{MAX} = \left(\frac{V_O + V_F - V_{IN(MIN)}}{V_O + V_F} \right)$$

A single-ended boost converter needs a minimum off-time every cycle in order to allow energy transfer from the input inductor to the output capacitor. This minimum off-time translates to a maximum duty cycle for the converter. The equation above can be rearranged to obtain the maximum output voltage for a given minimum input or maximum duty cycle.

$$V_{O(MAX)} = \frac{V_{IN}}{1 - D_{MAX}} - V_F$$

The equation for D_{MAX} above can be used as an initial guideline for determining the maximum duty cycle of the application circuit. However, losses in the inductor, input and output capacitors, the power MOSFETs, the sense resistors and the controller (gate drive losses) all contribute to an increasing of the duty cycle. The effect of these losses will be to *decrease* the maximum output voltage for a given minimum input voltage.

After the initial calculations have been completed for an application circuit, it is important to build a prototype of the circuit and measure it over the entire input voltage range, from light load to full load, and over temperature, in order to verify proper operation of the circuit.

Peak and Average Input Currents

The control circuit in the LTC7840 measures the input current (by means of resistors in the sources of the power MOSFETs), so the output current needs to be reflected back to the input in order to dimension the power MOSFETs properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The peak current in each inductor is:

$$I_{IN(PK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2} \right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

where n represents the number of phases and χ represents the percentage peak-to-peak ripple current in the inductor. For example, if the design goal is to have 30% ripple current in the inductor, then $\chi = 0.30$, and the peak current is 15% greater than the average.

Inductor Selection

Given an input voltage range, operating frequency and ripple current, the inductor value can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

where:

$$\Delta I_L = \frac{\chi}{n} \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

Choosing a larger value of ΔI_L allows the use of a lower value inductor but results in higher output voltage ripple, greater core losses, and higher ripple current ratings for the input and output capacitors. A reasonable starting point is 30% ripple current in the inductor ($\chi = 0.3$), or:

$$\Delta I_L = \frac{0.3}{n} \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The inductor saturation current rating needs to be higher than the worst-case peak inductor current during an overload condition. If $I_{O(MAX)}$ is the maximum rated load

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current, then the maximum current limit value ($I_{O(CL)}$) would normally be chosen to be some factor (e.g., 30%) greater than $I_{O(MAX)}$.

$$I_{O(CL)} = 1.3 \bullet I_{O(MAX)}$$

Reflecting this back to the input, where the current is being measured, and accounting for the ripple current, gives a minimum saturation current rating for the inductor of:

$$I_{L(SAT)} \geq \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1 - D_{MAX}}$$

The saturation current rating for the inductor should be determined at the minimum input voltage (which results in the highest duty cycle and maximum input current), maximum output current and the maximum expected core temperature. The saturation current ratings for most commercially available inductors drop at high temperature. To verify safe operation, it is a good idea to characterize the inductor's core/winding temperature under the following conditions: 1) worst-case operating conditions, 2) maximum allowable ambient temperature and 3) with the power supply mounted in the final enclosure. Thermal characterization can be done by placing a thermocouple in intimate contact with the winding/core structure, or by burying the thermocouple within the windings themselves.

Remember that a single-ended boost converter is **not** short-circuit protected, and that under a shorted output condition, the output current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, consider using a SEPIC or forward converter topology.

Power MOSFET Selection

The peak-to-peak gate drive level is set by the DRV_{CC} voltage is 10V for the LTC7840 under normal operating conditions. Selection criteria for the power MOSFETs include the $R_{DS(ON)}$, gate charge Q_G, drain-to-source breakdown voltage BV_{DSS}, maximum continuous drain current $I_{D(MAX)}$, and thermal resistances $R_{TH(JA)}$ and $R_{TH(JC)}$—both junction-to-ambient and junction-to-case.

The gate driver for the LTC7840 consists of PMOS pull-up and NMOS pull-down devices, allowing the full DRV_{CC} voltage to be applied to the gates during power MOSFET switching. Nonetheless, care must be taken to ensure that the minimum gate drive voltage is still sufficient to full enhance the power MOSFET. Check the MOSFET data sheet carefully to verify that the $R_{DS(ON)}$ of the MOSFET is specified for a voltage less than or equal to the nominal DRV_{CC} voltage of 10V.

Also pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Check the switching waveforms of the MOSFET directly on the drain terminal using a single probe and a high bandwidth oscilloscope. Ensure that the drain voltage ringing does not approach the BV_{DSS} of the MOSFET. Excessive ringing at high frequency is normally an indicator of too much series inductance in the high di/dt current path that includes the MOSFET, the boost diode, the output capacitor, the sense resistor and the PCB traces connecting these components.

The GATE of MOSFET Q1 could experience transient voltage spikes during turn-on and turn-off of the MOSFET, due to parasitic lead inductance and improper PCB layout. These voltage spikes could exceed the absolute maximum voltage ratings of LTC7840's GATE pin. The GATE pins are rated for an absolute maximum voltage of –0.3V minimum and 11V maximum. Hence it is recommended to add an external buffer close to the GATE of the MOSFET as shown in Figure 13.

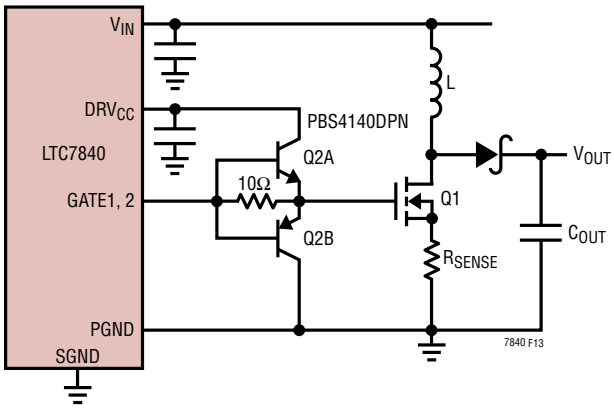

Figure 13. External Buffer Circuit

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Finally, check the MOSFET manufacturer's data sheet for an avalanche energy rating (EAS). Some MOSFETs are not rated for body diode avalanche and will fail catastrophically if the V_{DS} exceeds the device BV_{DSS}, even if only by a fraction of a volt. Avalanche-rated MOSFETs are better able to sustain high frequency drain-to-source ringing near the device BV_{DSS} during the turn-off transition.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$). As a result, some iterative calculation is normally required to determine a reasonably accurate value.

The power dissipated by the MOSFET in a multi-phase boost converter with n phases is:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{n \bullet (1 - D_{MAX})} \right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T + k \bullet V_{OUT}{}^2 \bullet \frac{I_{O(MAX)}}{n \bullet (1 - D_{MAX})} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 14 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

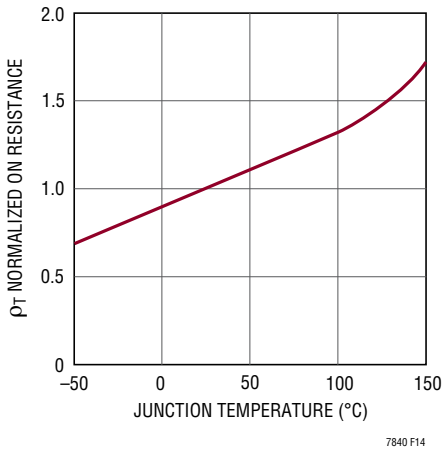

Figure 14. Normalized Power MOSFET $R_{DS(ON)}$ vs Temperature

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

It is tempting to choose a power MOSFET with a very low $R_{DS(ON)}$ in order to reduce conduction losses. In doing so, however, the gate charge Q_G is usually significantly higher, which increases switching and gate drive losses. Since the switching losses increase with the square of the output voltage, applications with a low output voltage generally have higher MOSFET conduction losses, and high output voltage applications generally have higher MOSFET switching losses. At high output voltages, the highest efficiency is usually obtained by using a MOSFET with a higher $R_{DS(ON)}$ and lower Q_G. The equation above can easily be split into two components (conduction and switching) and entered into a spreadsheet, in order to compare the performance of different MOSFETs.

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Programming the Current Limit

The LTC7840 has ILIM1 and ILIM2 pins to adjust the current comparator's maximum sense voltage for Channel 1 and Channel 2 respectively. There is a precise 10µA current flowing out of ILIM pin. A resistor to SGND can set the voltage on ILIM pin to program the peak current sense threshold to any voltage lower than 75mV. Alternatively, a DC voltage which is lower than 0.5V can be added to ILIM pin to adjust the maximum current sense threshold. Floating ILIM pin or adding any voltage higher than 0.5V make the current comparator's maximum sense voltage be 75mV.

For a boost converter where the current limit value is chosen to be 30% higher than the maximum load current, the peak current in the MOSFET and sense resistor is:

$$I_{SW(MAX)} = I_{R(SENSE)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1 - D_{MAX}}$$

The sense resistor value is then:

$$R_{SENSE} = \frac{V_{SENSE(MAX)} \bullet n \bullet \left(1 - D_{MAX}\right)}{1.3 \bullet \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)}}$$

Again, the factor n is the number of phases used, and χ represents the percentage ripple current in the inductor. The number 1.3 represents the factor by which the current limit exceeds the maximum load current, $I_{O(MAX)}$. For example, if the current limit needs to exceed the maximum load current by 50%, then the 1.3 factor should be replaced with 1.5.

The average power dissipated in the sense resistor can easily be calculated as:

$$P_{R(SENSE)} = \left(\frac{1.3 \bullet I_{O(MAX)}}{n \bullet \left(1 - D_{MAX}\right)}\right)^2 \bullet R_{SENSE} \bullet D_{MAX}$$

This equation assumes no temperature coefficient for the sense resistor. If the resistor chosen has a significant temperature coefficient, then substitute the worst-case high resistance value into the equation.

The resistor temperature can be calculated using the equation:

$$T_D = T_A + P_{R(SENSE)} \bullet R_{TH(JA)}$$

Selecting the Output Diodes

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is required. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current:

$$I_{IN} = \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}}$$

Although the average diode current is equal to the output current, in very high duty cycle applications (low V_{IN} to high V_{OUT}) the peak diode current can be several times higher than the average, as shown in Figure 15. In this case check the diode manufacturer's data sheet to ensure that its peak current rating exceeds the peak current in the equation above. In addition, when calculating the power dissipation in the diode, use the value of the forward voltage (V_F) measured at the peak current, not the average output current. Excess power will be dissipated in the series resistance of the diode, which would not be accounted for if the average output current and forward voltage were used in the equations. Finally, this additional power dissipation is important when deciding on a diode current rating, package type, and method of heat sinking.

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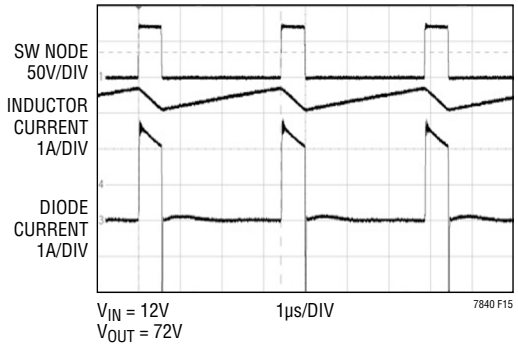

Figure 15. Diode Current Waveform for a High Duty Cycle Application

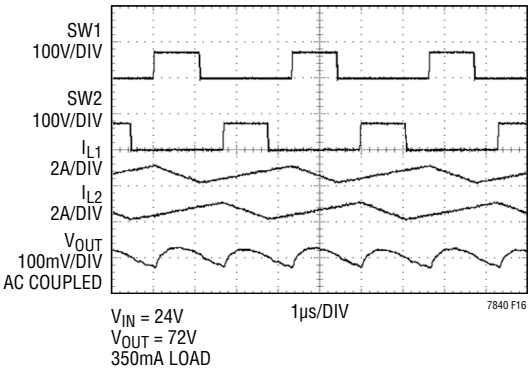

Figure 16. Switching Waveforms for a Boost Converter

To a close approximation, the power dissipated by the diode is:

$$P_D = I_{D(PEAK)} \bullet V_{F(PEAK)} \bullet (1 - D_{MAX})$$

The diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. Once the proper diode has been selected and the circuit performance has been verified, measure the temperature of the power components using a thermal probe or infrared camera over all operating conditions to ensure a good thermal design.

Finally, remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct combination of output capacitors for a boost converter application. The effects of these three parameters on the output voltage ripple waveform are illustrated in Figure 16 for a typical boost converter.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

One of the key benefits of multi-phase operation is a reduction in the peak current supplied to the output capacitor by the boost diodes. As a result, the ESR requirement of the capacitor is relaxed. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

where:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The factor n represents the number of phases and the factor χ represents the percentage inductor ripple current.

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For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet n \bullet V_{OUT} \bullet f}$$

For many designs it will be necessary to use one type of capacitor to obtain the required ESR, and another type to satisfy the bulk capacitance. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

The voltage rating of the output capacitor must be greater than the maximum output voltage, with sufficient derating to account for the maximum capacitor temperature.

Because the ripple current in the output capacitor is a square wave, the ripple current requirements for this capacitor depend on the duty cycle, the number of phases and the maximum output current. Figure 17 illustrates the normalized output capacitor ripple current as a function of duty cycle. In order to choose a ripple current rating for the output capacitor, first establish the duty cycle range, based on the output voltage and range of input voltage.

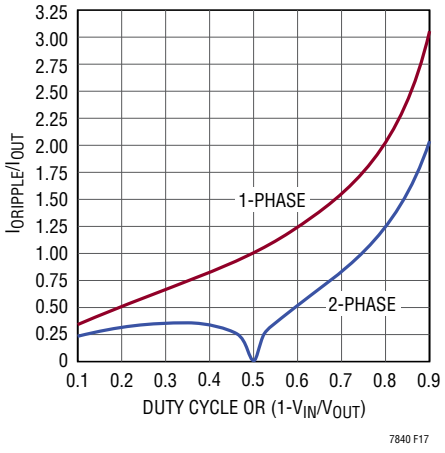

Figure 17. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

Referring to Figure 17, choose the worst-case high normalized ripple current, as a percentage of the maximum load current.

The output ripple current is divided between the various capacitors connected in parallel at the output voltage. Although ceramic capacitors are generally known for low ESR (especially X5R and X7R), these capacitors suffer from a relatively high voltage coefficient. Therefore, it is not safe to assume that the entire ripple current flows in the ceramic capacitor. Aluminum electrolytic capacitors are generally chosen because of their high bulk capacitance, but they have a relatively high ESR. As a result, some amount of ripple current will flow in this capacitor. If the ripple current flowing into a capacitor exceeds its RMS rating, the capacitor will heat up, reducing its effective capacitance and adversely affecting its reliability. After the output capacitor configuration has been determined using the equations provided, measure the individual capacitor case temperatures in order to verify good thermal performance.

Input Capacitor Selection

The input capacitor voltage rating in a boost converter should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of the input capacitor is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The input ripple current in a multi-phase boost converter is relatively low (compared with the output ripple current), because this current is continuous and is being divided

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between two or more inductors. Nonetheless, significant stress can be placed on the input capacitor, especially in high duty cycle applications. Figure 18 illustrates the normalized input ripple current, where:

$$I_{NORM} = \frac{V_{IN}}{L \bullet f}$$

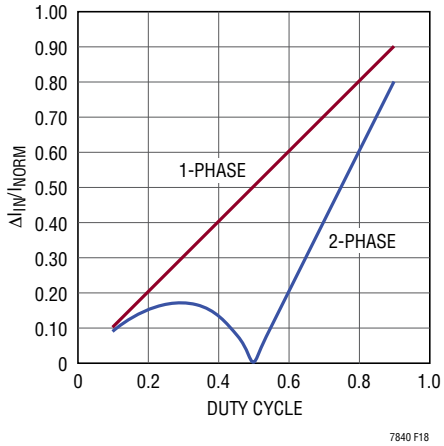

Figure 18. Normalized Input Peak-to-Peak Ripple Current

Soft Start (SS Pin) Capacitor Selection

The LTC7840 has hiccup mode to protect the system in the event of overcurrent. Because the hiccup mode timing is set by discharging the soft start capacitor, at least 0.1µF capacitor must be tied between SS pin and SGND. At start up, an 10µA current flowing out of SS pin to charge the soft start capacitor. The hiccup mode is disabled until the voltage on SS pin ramps up to 1.32V (10% higher than the 1.2V internal reference). For a properly configured system, the output's feedback voltage tracks the voltage on SS pin until it reaches 1.2V. At this moment, the converter's output voltage reaches the regulated value and the system enters the steady state. If the target output voltage is high or if heavy loaded, the soft start capacitor needs to be larger to slow down the ramp up speed, otherwise, the converter's output voltage cannot follow the voltage on SS pin in time. At the same time, the system keeps operating at the maximum current limit. This situation is thought as overcurrent event by the controller. Once the voltage on SS pin reaches 1.32V, the hiccup mode is enabled to make the converter enter the sleep mode even though the output voltage hasn't reached the target value. In this case, the system cannot start up normally.

Checking the Load Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The I_{TH} series R_C • C_C filter sets the dominant pole-zero loop compensation. The transfer function for boost and flyback converters contains a right half plane zero that normally requires the loop crossover frequency to be reduced significantly in order to maintain good phase margin. The R_C • C_C filter values can typically be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type(s) and value(s) have been determined. The output capacitor configuration needs to be selected in advance because the effective ESR and bulk capacitance have a significant effect on the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense

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of the overall loop stability without breaking the feedback loop. Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a fast load step condition. The initial output voltage step resulting from the step change in the output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. Figure 19 illustrates the load step response of a properly compensated boost converter.

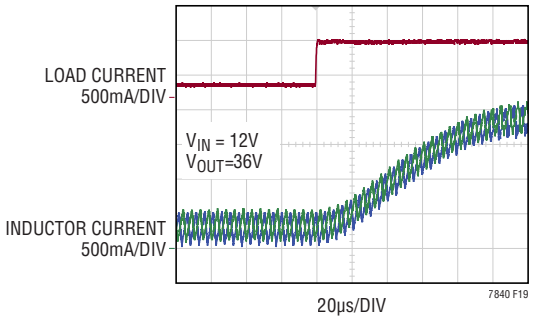

Figure 19. Load Step Response of a Properly Compensated Boost Converter

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the converter:

1. For lower power applications a 2-layer PC board is sufficient. However, for higher power levels, a multilayer PC board is recommended. Using a solid ground plane and proper component placement under the circuit is the easiest way to ensure that switching noise does not affect the operation.
2. In order to help dissipate the power from the MOSFETs and diodes, keep the ground plane on the layers closest to the power components. Use power planes for the MOSFETs and diodes in order to maximize the heat spreading from these components into the PCB.
3. Place all power components in a tight area. This will minimize the size of high current loops. The high di/dt loops formed by the sense resistor, power MOSFET, the boost diode and the output capacitor should be kept as small as possible to avoid EMI.
4. Orient the input and output capacitors and current sense resistors in a way that minimizes the distance between the pads connected to the ground plane. Keep the capacitors for $INTV_{CC}$, DRV_{CC} and V_{IN} as close as possible to LTC7840.
5. Place the DRV_{CC} decoupling capacitor as close as possible to the DRV_{CC} and PGND pins, on the same layer as the IC. A low ESR (X5R or better) 4.7µF to 10µF ceramic capacitor should be used.
6. Use a local via to ground plane for all pads that connect to the ground. Use multiple vias for power components.

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7. Place the small-signal components away from high frequency switching nodes on the board. The pinout of the LTC7840 was carefully designed in order to make component placement easy. All of the power components can be placed on one side of the IC, away from all of the small-signal components.
8. The exposed area on the bottom of the package is internally connected to SGND.
9. The MOSFETs should also be placed on the same layer of the board as the sense resistors. The MOSFET source should connect to the sense resistor using a short, wide PCB trace.
10. The output resistor divider should be located as close as possible to the IC, with the bottom resistor connected between VFB pin and SGND. The PCB trace connecting the top resistor to the upper terminal of the output capacitor should avoid any high frequency switching nodes.
11. Since the inductor acts like a current source in a peak current mode control topology, its placement on the board is less critical than the high di/dt components.
12. The $SENSE^+$ and $SENSE^-$ PCB traces should be routed parallel to one another with minimum spacing in between all the way to the sense resistor. These traces should avoid any high frequency switching nodes in the layout. These PCB traces should also be Kelvin-connected to the interior of the sense resistor pads, in order to avoid sensing errors due to parasitic PCB resistance IR drops.
13. If an external RC filter is used between the sense resistor and the $SENSE^+$ and $SENSE^-$ pins, these filter components should be placed as close as possible to the $SENSE^+$ and $SENSE^-$ pins of the IC. Ensure that the $SENSE^-$ line is connected to the ground only at the point where the current sense resistor is grounded.
14. Keep the MOSFET drain nodes (SW1, SW2) away from sensitive small-signal nodes, especially from the opposite channel's current-sensing signals. The SW nodes can have slew rates in excess of 1V/ns relative to ground and should therefore be kept on the "output side" of the LTC7840.
15. Check the stress on the power MOSFETs by independently measuring the drain-to-source voltages directly across the devices terminals. Beware of inductive ringing that could exceed the maximum voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, choose a higher voltage rated MOSFET or consider using a snubber.
16. When synchronizing the LTC7840 to an external clock, use a low impedance source such as a logic gate to drive the SYNC pin and keep the lead as short as possible.

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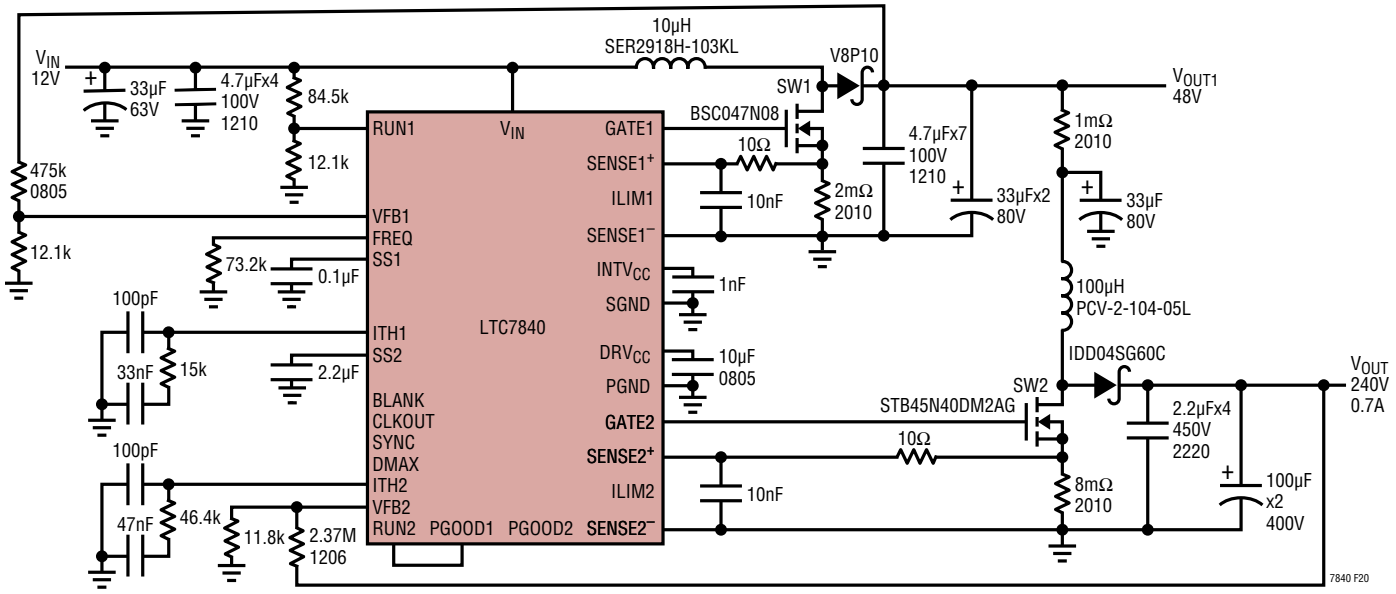

Figure 20. 12V Input, 240V/0.7A Output Two-Stage Boost Converter

Design Example

A two-stage step up converter is shown in Figure 20. The two channels of LTC7840 are connected in cascade, i.e., the output of Channel 1 is tied to the input of Channel 2. The output voltage of Channel 1 is 48V and the output voltage of Channel 2 is 240V. The input voltage range of Channel 1 is 9V to 36V. The maximum output current of Channel 2 is 0.7A when the input voltage of Channel 1 is 12V.

1. The duty cycle range is:

$$D_{MAX1} = \left(\frac{V_{O1} + V_F - V_{IN1}}{V_{O1} + V_F}\right) = \left(\frac{48V + 0.5V - 12V}{48V + 0.5V}\right) = 75.3\%$$

$$D_{MIN1} = \left(\frac{48V + 0.5V - 36V}{48V + 0.5V}\right) = 25.8\%$$

$$D_{MAX2} = \left(\frac{V_{O2} + V_F - V_{O1}}{V_{O2} + V_F}\right) = \left(\frac{240V + 0.5V - 48V}{240V + 0.5V}\right) = 80\%$$

2. The operating frequency is chosen to be 150kHz so the period is 6.67µs. From Figure 6, the resistor from the FREQ pin to SGND is 73.2k.

3. Channel 2 maximum DC input current is:

$$I_{IN2(MAX)} = \frac{I_{O2(MAX)}}{1 - D_{MAX2}} = \frac{0.7A}{1 - 0.8} = 3.5A$$

Channel 1 maximum DC input current is:

$$I_{IN1(MAX)} = \frac{I_{O1(MAX)}}{1 - D_{MAX1}} = \frac{I_{IN2(MAX)}}{1 - D_{MAX1}} = \frac{3.5A}{1 - 0.753} = 14.17A$$

4. A ripple current of 40% is chosen so the peak current in each inductor is:

$$I_{L1(PK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{IN1(MAX)} = \left(1 + \frac{0.4}{2}\right) \bullet 14.17A = 17A$$

$$I_{L2(PK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{IN2(MAX)} = \left(1 + \frac{0.4}{2}\right) \bullet 3.5A = 4.2A$$

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5. The inductor peak-to-peak ripple current is:

$$\Delta I_{L1} = 40\% \bullet I_{IN1(MAX)} = 0.4 \bullet 14.17A = 5.67A$$

$$\Delta I_{L2} = 40\% \bullet I_{IN2(MAX)} = 0.4 \bullet 3.5A = 1.4A$$

6. The inductor value is therefore:

$$L1 = \frac{V_{IN1}}{\Delta I_{L1} \bullet f} \bullet D_{MAX1} = \frac{12V}{5.67A \bullet 150kHz} \bullet 0.753$$
$$= 10.62\mu H$$

$$L2 = \frac{V_{IN2}}{\Delta I_{L2} \bullet f} \bullet D_{MAX2} = \frac{48V}{1.4A \bullet 150kHz} \bullet 0.8$$
$$= 183\mu H$$

7. For a current limit value 30% higher than the maximum load current, the saturation current rating of the inductors must therefore exceed:

$$I_{L1(SAT)} \geq 1.3 \bullet I_{L1(PK)} = 1.3 \bullet 17A = 22.1A$$

$$I_{L2(SAT)} \geq 1.3 \bullet I_{L2(PK)} = 1.3 \bullet 4.2A = 5.46A$$

   In order to obtain higher efficiency with acceptable ripple, the Channel 1 inductor value chosen is 10µH and the part number is SER2918H-103KL. This inductor has a saturation current rating of 28A. The Channel 2 inductor chosen is 100µH and the part number is PCV-2-104-05L.

8. The power MOSFET of Channel 1 chosen for this application is an Infineon BSC047N08. This MOSFET has a typical $R_{DS(ON)}$ of 3.9mΩ at V_{GS} = 10V. The BV_{DSS} is rated at a minimum of 80V and the maximum continuous drain current is 100A. The typical gate charge is 52nC for V_{GS} = 0V to 10V. The power MOSFET of Channel 2 chosen for this application is an STMicroelectronics STB45N40DM2AG. This MOSFET has a typical $R_{DS(ON)}$ of 63mΩ at V_{GS} = 10V. The BV_{DSS} is rated at a minimum of 400V and the maximum continuous drain current is 38A. The typical gate charge is 56nC for V_{GS} = 10V.

9. The total IC quiescent current, IC power dissipation and maximum junction temperature are approximately:

$$I_{Q(TOT)} = I_Q + Q_{G1(TOT)} \bullet f + Q_{G2(TOT)} \bullet f$$
$$= 3mA + 52nC \bullet 150kHz + 56nC \bullet 150kHz$$
$$= 19.2mA$$

$$P_{DISS} = 12V \bullet 19.2mA = 230.4mW$$

$$T_J = 70°C + 230.4mW \bullet 30°C/W = 76.9°C$$

10. For a current limit set at 30% above the maximum load current, the peak switch and sense resistor currents are:

$$I_{SW1(PK)} = I_{R1(PK)} = 1.3 \bullet I_{L1(PK)} = 1.3 \bullet 17A = 22.1A$$

$$I_{SW2(PK)} = I_{R2(PK)} = 1.3 \bullet I_{L2(PK)} = 1.3 \bullet 4.2A = 5.46A$$

11. The maximum current sense threshold for the LTC7840 is 75mV when ILIM1 and ILIM2 pins are floating. This threshold keeps constant over duty cycle. The sense resistor is calculated to be:

$$R_{SENSE1} = \frac{V_{SENSE(MAX)}}{I_{SW1(PK)}} = \frac{75mV}{22.1A} = 3.4m\Omega$$

$$R_{SENSE2} = \frac{V_{SENSE(MAX)}}{I_{SW2(PK)}} = \frac{75mV}{5.46A} = 13.7m\Omega$$

   For this application, a 2mΩ surface mount resistor is used for Channel 1 and an 8mΩ surface mount resistor is used for Channel 2.

12. The power dissipation in the sense resistors at current limit is:

$$P_{R1(SENSE)} = \left(1.3 \bullet I_{IN1(MAX)}\right)^2 \bullet R_{SENSE1} \bullet D_{MAX1}$$
$$= \left(1.3 \bullet 14.17A\right)^2 \bullet 2m\Omega \bullet 0.753$$
$$= 0.51W$$

$$P_{R2(SENSE)} = \left(1.3 \bullet I_{IN2(MAX)}\right)^2 \bullet R_{SENSE2} \bullet D_{MAX2}$$
$$= \left(1.3 \bullet 3.5A\right)^2 \bullet 8m\Omega \bullet 0.8$$
$$= 0.13W$$

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13. The average current in the boost diodes is half the output current:

$$I_{D1} = \frac{I_{O1(MAX)}}{2} = \frac{3.5A}{2} = 1.75A$$

$$I_{D2} = \frac{I_{O2(MAX)}}{2} = \frac{0.7A}{2} = 0.35A$$

14. The peak current in each boost diode is:

$$I_{D1(PK)} = I_{L1(PK)} = 17A$$

$$I_{D2(PK)} = I_{L2(PK)} = 4.2A$$

The diode chosen for Channel 1 is the V8P10, manufactured by Vishay General Semiconductor. This surface mount diode has a maximum average forward current of 8A at 25°C and a maximum reverse voltage of 100V. The maximum forward voltage at 25°C is 0.522V at 25°C and 0.466V at 125°C when forward current is 4A. The diode chosen for Channel 2 is the IDD04SG60C, manufactured by Infineon. This diode has a maximum average forward current of 4A when temperature is lower than 130°C and a maximum reverse voltage of 600V at 25°C. The maximum forward voltage at 25°C is 2.1V at 25°C and 2.8V at 125°C when forward current is 4A.

The power dissipated by the diode is approximately:

$$P_{D1} = I_{D1(PK)} \bullet V_{F1(PK)} \bullet (1 - D_{MAX1})$$
$$= 17A \bullet 0.466V \bullet (1 - 0.753) = 1.96W$$

$$P_{D2} = I_{D2(PK)} \bullet V_{F2(PK)} \bullet (1 - D_{MAX2})$$
$$= 4.2A \bullet 2.8V \bullet (1 - 0.8) = 2.35W$$

15. Two types of output capacitors are connected in parallel for this application; a low ESR ceramic capacitor and an aluminum electrolytic for bulk storage. For a 1% contribution to the total ripple voltage, the maximum ESR of the composite output capacitance is approximately:

$$ESR_{COUT1} \le \frac{0.01 \bullet V_{OUT1}}{I_{D1(PK)}} = \frac{0.01 \bullet 48V}{17A} = 0.028\Omega$$

$$ESR_{COUT2} \le \frac{0.01 \bullet V_{OUT2}}{I_{D2(PK)}} = \frac{0.01 \bullet 240V}{4.2A} = 0.57\Omega$$

For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT1} \ge \frac{I_{O1(MAX)}}{0.01 \bullet V_{OUT1} \bullet f} = \frac{3.5A}{0.01 \bullet 48V \bullet 150kHz}$$
$$= 48.6\mu F$$

$$C_{OUT2} \ge \frac{I_{O2(MAX)}}{0.01 \bullet V_{OUT2} \bullet f} = \frac{0.7A}{0.01 \bullet 240V \bullet 150kHz}$$
$$= 1.94\mu F$$

For this application, in order to obtain both low ESR and an adequate ripple current rating, Channel 1 has two 33µF, 80V aluminum electrolytic capacitors connected in parallel with seven 4.7µF, 100V ceramic capacitors. Channel 2 has two 100µF, 400V aluminum electrolytic capacitors connected in parallel with four 2.2µF, 450V ceramic capacitors.

TYPICAL APPLICATIONS

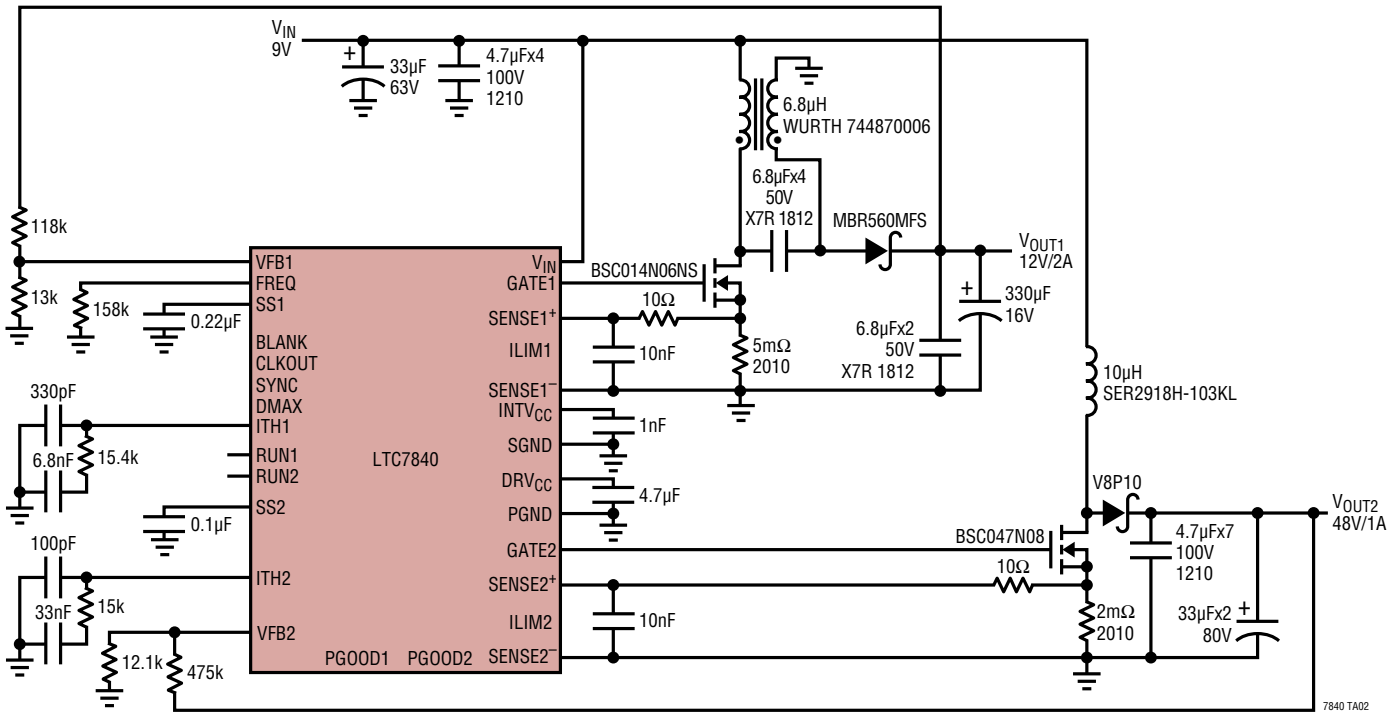
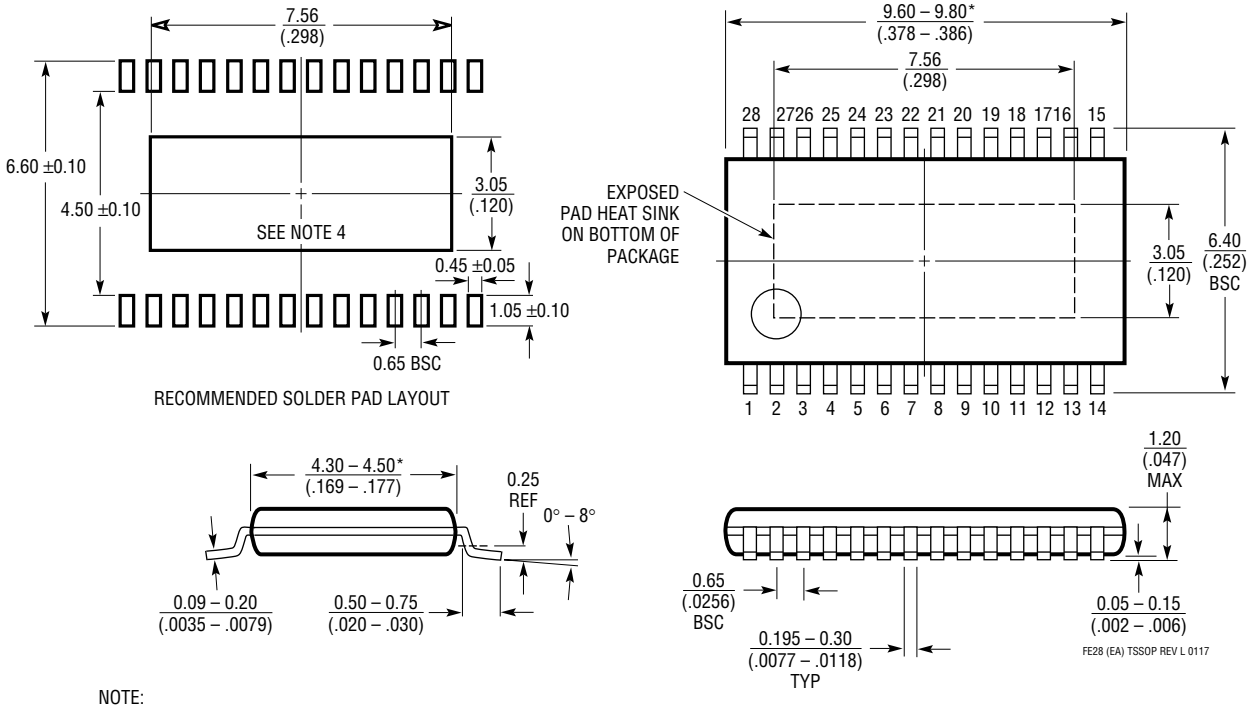


Figure 21. Dual Output 12V/2A, 48V/1A Converter with Channel 1 Configured as SEPIC and Channel 2 Configured as Boost Converter

PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EA

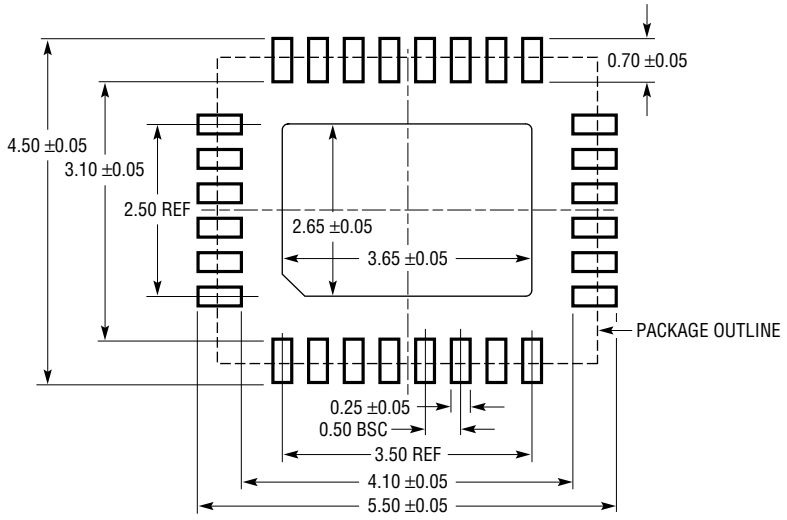


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

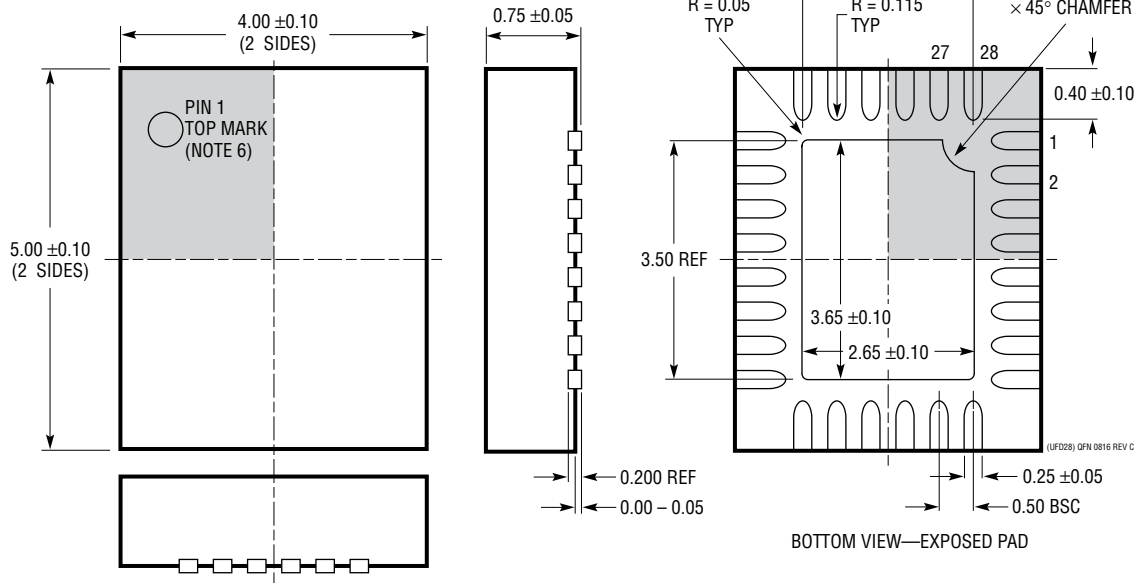
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE