48-Port IEEE 802.3bt PoE PSE Controller

FEATURES

- **Fully Compliant IEEE 802.3bt Type 3 and 4 PSE**
- **Fully Compliant IEEE 802.3at Type 2 PSE**
- **Software-Compatible with LTC4291-1/LTC4292**
- **Up to 48 PSE Ports with One Power Channel per Port**
- **Up to 24 PSE Ports with Two Power Channels per Port**
- **ECC-Protected eFlash and Data RAMs**
- **Low Power Path Dissipation per Channel**
  - **100mΩ Sense Resistance**
  - **30mΩ or Lower MOSFET $R_{DS(ON)}$**
- **Chipset Provides Electrical Isolation**
  - **Eliminates Optos and Isolated 3.3V Supply**
- **Very High Reliability Multipoint PD Detection**
  - **Connection Check Distinguishes Single-Signature and Dual-Signature PDs**
- Continuous Per-Port Power and Current Monitoring
- 1MHz I^2C Compatible Serial Control Interface
- Pin or I^2C Programmable PD Power
- Available in 24-Lead 4mm × 4mm (LTC9101-1) and a 64-Lead 7mm × 11mm (LTC9102/LTC9103) QFN Packages

APPLICATIONS

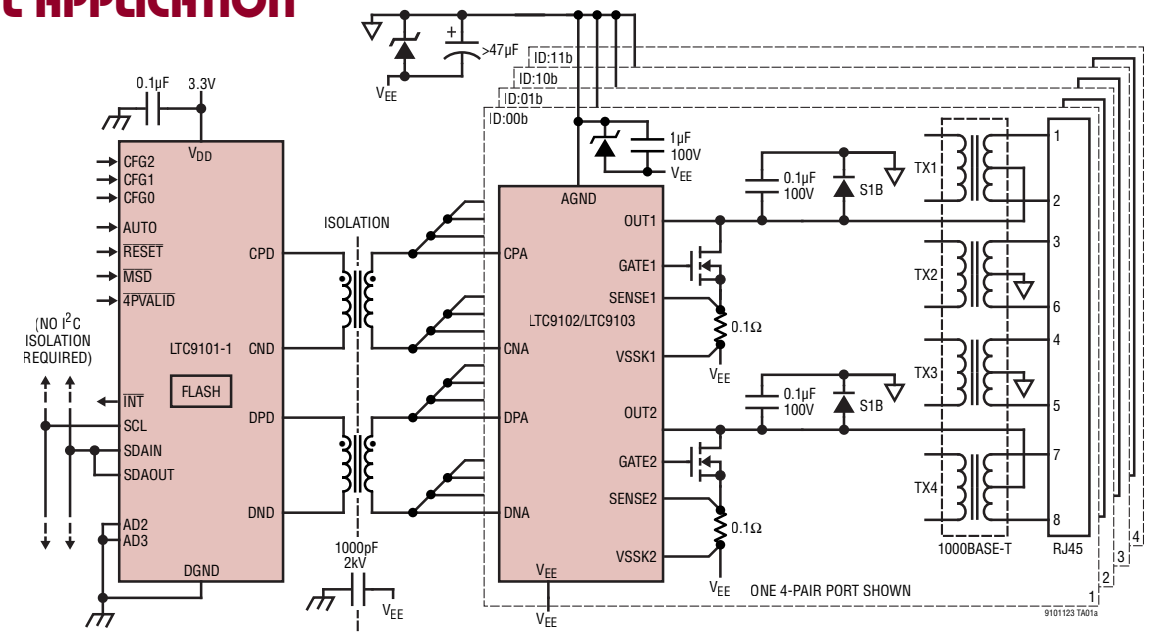
- PoE PSE Switches/Routers and Midspans

DESCRIPTION

The LTC®9101-1/LTC9102/LTC9103 chipset is a 48-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 2, 802.3bt Type 3 and 4 compliant Power over Ethernet (PoE) systems. The LTC9101-1/LTC9102/LTC9103 is designed to power compliant 802.3af, 802.3at, and 802.3bt PDs. The LTC9101-1/LTC9102/LTC9103 chipset delivers lowest-in-industry heat dissipation by utilizing low-$R_{DS(ON)}$ external MOSFETs and 0.1Ω sense resistance per power channel. A transformer-isolated communication protocol replaces expensive opto-couplers and complex isolated 3.3V supply, resulting in significant BOM cost savings.

Advanced power management features include per-port 14-bit current/power monitoring, programmable current/power limits, and versatile fast shut-down of preselected ports. An advanced power management host software layer is available. PD detection uses a proprietary multipoint detection mechanism ensuring excellent immunity from false PD identification. Autoclass and 5-event physical classification are supported. The LTC9101-1/LTC9102/LTC9103 includes an I^2C serial interface operable up to 1MHz. The LTC9101-1/LTC9102/LTC9103 is pin or I^2C programmable to negotiate PD delivered power up to 71.3W.

TYPICAL APPLICATION



Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

LTC9101-1

Supply Voltages (with respect to DGND)
- V_{DD} ..... –0.3V to 3.6V
- CAP1, CAP2 .....–0.3V to 1.32V

Digital Pins
- ADn, AUTO, CFGn, $\overline{MSD}$, SDAIN, SDAOUT, SCL, $\overline{RESET}$, $\overline{INT}$, $\overline{4PVALID}$ ..... –0.3V to V_{DD} + 0.3V

Analog Pins
- CPD, CND, DPD, DND ..... –0.3V to V_{DD} + 0.3V

Operating Ambient Temperature ..... –40°C to 85°C
Operating Junction Temperature (Note 2).. –40°C to 125°C
Storage Temperature ..... –65°C to 150°C

(Notes 1, 4)

LTC9102/LTC9103

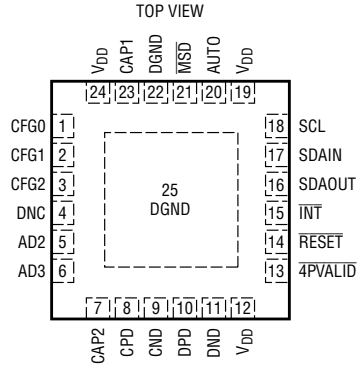
Supply Voltages (with respect to V_{EE})
- AGND ..... –0.3V to 80V
- PWRIN ..... –0.3V to 80V
- CAP3, CAP4 ..... –0.3V to 5V
- VSSKn ..... –0.3V to 0.3V

Analog Pins
- SENSEn, OUTn ..... –20V to 80V
- GATEn, IDn, PWRMD ..... –0.3V to 80V
- CPA, CNA, DPA, DNA .....–0.3V to CAP3 + 0.3V
- EXT3.....–0.3V to 30V

Operating Ambient Temperature .....–40°C to 85°C
Operating Junction Temperature (Note 2)...–40°C to 125°C
Storage Temperature .....–65°C to 150°C

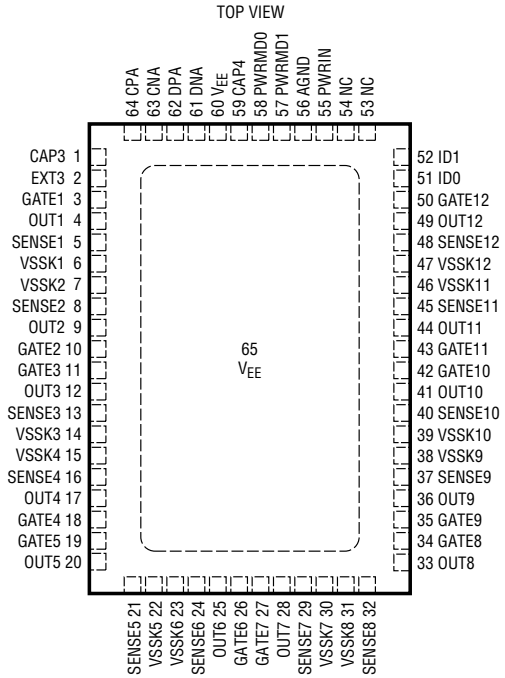
PIN CONFIGURATION

LTC9101-1



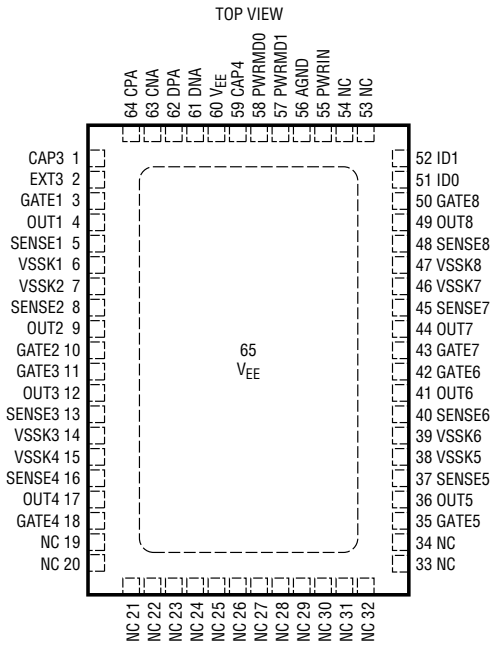
UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
θ_{JC} = 4°C/W, θ_{JA} = 47°C/W
EXPOSED PAD (PIN 25) IS DGND, MUST BE SOLDERED TO PCB

LTC9102



UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
θ_{JC} = 1°C/W, θ_{JA} = 22°C/W
EXPOSED PAD (PIN 65) IS V_{EE}, MUST BE SOLDERED TO PCB

LTC9103



UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
θ_{JC} = 1°C/W, θ_{JA} = 22°C/W
EXPOSED PAD (PIN 65) IS V_{EE}, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC9101AUF-1#PBF	LTC9101AUF-1#TRPBF	91011	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC9102AUKJ#PBF	LTC9102AUKJ#TRPBF	LTC9102	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 85°C
LTC9103AUKJ#PBF	LTC9103AUKJ#TRPBF	LTC9103	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Main PoE Supply Voltage	AGND – V_{EE}					
		Type 2 or 3 Compliant Output	●	51		57	V
		Type 4 Compliant Output	●	53		57	V
	LTC9102/LTC9103 Undervoltage Lock-Out	AGND – V_{EE}	●		8.2	9	V
V_{DD}	V_{DD} Supply Voltage	V_{DD} – DGND	●	3	3.3	3.6	V
	Undervoltage Lock-Out				2.8		V
	V_{DD} Slew Rate, Falling	2.4 ≤ V_{DD} – DGND ≤ 3.0 (Note 7)				20	mV/µs
V_{CAP1}, V_{CAP2}	Internal Regulator Supply Voltage	V_{CAP1} – DGND, V_{CAP2} – DGND (Note 13)			1.2		V
V_{CAP3}	Internal 3.3V Regulator Supply Voltage	CAP3 – V_{EE} (Note 13)	●	3	3.3	3.6	V
$t_{CAP3EXT}$	CAP3 External Supply Rise Time	0.5V < CAP3 < CAP3(Min), EXT3 Tied to CAP3 (Note 7)	●			1	ms
V_{CAP4}	Internal 4.3V Regulator Supply Voltage	CAP4 – V_{EE} (Note 13)	●		4.3		V
I_{EE}	V_{EE} Supply Current	PWRIN Pin Connected to AGND, EXT3 LOW, All Gates Fully Enhanced.		7.7	11	14	mA
	3.3V Rail Supply Current	From CAP3 = 3.3V (EXT3 HIGH)		4.2	5.4	6.6	mA
I_{DD}	V_{DD} Supply Current	(V_{DD} – DGND) = 3.3V	●		40	60	mA
Detection/Connection Check							
	Forced Current	Load Resistance 15.5k to 32k	●	220	240	260	µA
			●	143	160	180	µA
	Forced Voltage	Load Resistance 18.5k to 27.5k	●	7	8	9	V
			●	3	4	5	V
	Detection/Connection Check Current Compliance	AGND – OUTn = 0V	●		0.8	0.9	mA
V_{OC}	Detection/Connection Check Voltage Compliance	AGND – OUTn, Open Port	●		10.4	12	V
	Detection/Connection Check Voltage Slew Rate	AGND – OUTn, C_{PORT} = 150nF (Note 7)	●			0.01	V/µs
	Min. Valid Signature Resistance		●	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		●	27.5	29.7	32	kΩ
Classification							
V_{CLASS}	Classification Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	●	16		20.5	V
	Classification Current Compliance	SENSEn – VSSKn, OUTn = AGND (Note 15)	●	7	8	9	mV
	Classification Threshold	SENSEn – VSSKn (Note 15)					
		Class Signature 0 – 1	●	0.5	0.65	0.8	mV
		Class Signature 1 – 2	●	1.3	1.45	1.6	mV
		Class Signature 2 – 3	●	2.1	2.3	2.5	mV
		Class Signature 3 – 4	●	3.1	3.3	3.5	mV
		Class Signature 4 – Overcurrent	●	4.5	4.8	5.1	mV
V_{MARK}	Classification Mark State Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	●	7.5	9	10	V
	Mark State Current Compliance	OUTn = AGND	●	7	8	9	mV
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, GATEn = V_{EE} + 5V			1		mA
	GATE Pin Fast Pull-Down Current	GATEn = V_{EE} + 5V			65		mA
	GATE Pin On Voltage	GATEn – V_{EE}, I_{GATEn} = 1µA	●	11		14	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	OUTn – V_{EE}	●	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGND	Port On			2500		kΩ
		Port Off	●	300	500	700	kΩ
Current Sense							
V_{LIM-2P}	Active Current Limit, Single-Signature PD	OUTn – V_{EE} < 10V					
		Class 1 – Class 3	●	40	42.5	45	mV
		Class 4 – Class 6	●	80	85	90	mV
		Class 7	●	100	106	112	mV
		Class 8	●	110	117	124	mV
	Active Current Limit, Dual-Signature PD	OUTn – V_{EE} < 10V					
		Class 1 – Class 3	●	40	42.5	45	mV
		Class 4	●	80	85	90	mV
		Class 5	●	110	117	124	mV
$V_{INRUSH-2P}$	Active Current Limit, Inrush	OUTn – VEE < 30V (Note 16)	●				
		Single-Signature, Class 1–4, 4-Pair Power	●	20	21.3	22.5	mV
		All Others		40	42.5	45	mV
$V_{HOLD-2P}$	DC Disconnect Sense Voltage	SENSEn – VSSKn					
		Single-Signature Class 1–4, 4-Pair Power	●	200	350	500	µV
		Single-Signature Class 1–4, 2-Pair Power	●	500	700	900	µV
		Single-Signature Class 5–8, 4-Pair Power	●	200	350	700	µV
		Dual Signature, 2-Pair or 4-Pair Power	●	200	350	700	µV
V_{SC}	Short-Circuit Sense	SENSEn – VSSKn – V_{LIM-2P}			60		mV
Port Current Readback (See Typical Performance Characteristics, Note 17)							
	Full-Scale Range	(Notes 7, 15)			204.6		mV
	LSB Weight	|SENSEn – VSSKn|, VSSKn = V_{EE} (Note 15)			24.98		µV/LSB
	Conversion Period				1.967		ms
V_{EE} Readback (See Typical Performance Characteristics, Note 17)							
	Full-Scale Range	(Note 7)			82		V
	LSB Weight	|AGND – V_{EE}|			10.01		mV/LSB
	Conversion Period				1.967		ms
Digital Interface							
V_{ILD}	Digital Input Low Voltage	ADn, $\overline{RESET}$, $\overline{MSD}$, CFGn, AUTO, $\overline{4PVALID}$ (Note 6)	●			0.8	V
	I^2C Input Low Voltage	SCL, SDAIN (Note 6)	●			1	V
V_{IHD}	Digital Input High Voltage	(Note 6)	●	2.2			V
	Digital Output Low Voltage	I_{SDAOUT} = 3mA, $I_{\overline{INT}}$ = 3mA	●			0.4	V
		I_{SDAOUT} = 5mA, $I_{\overline{INT}}$ = 5mA	●			0.7	V
	Internal Pull-Up to V_{DD}	AD*n*, $\overline{RESET}$, $\overline{MSD}$, CFG2			50		kΩ
	Internal Pull-Down to DGND	AUTO, $\overline{4PVALID}$, CFG0			50		kΩ
	EXT3 Pull-Down to V_{EE}				50		kΩ
	IDn Internal Pull-Up to CAP4	IDn = 0V			5		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSE Timing Characteristics (Note 7)							
t_{DET}	Detection Time	Beginning to End of Detection	●		380	500	ms
t_{CLASS_RESET}	Classification Reset Duration		●	15			ms
t_{CEV}	Class Event Duration		●	6	15	20	ms
t_{CEVON}	Class Event Turn On Duration	C_{PORT} = 0.6µF	●			0.1	ms
t_{LCE}	Long Class Event Duration		●	88		105	ms
t_{CLASS}	Class Event I_{CLASS} Measurement Timing		●	6			ms
t_{CLASS_LCE}	Long Class Event I_{CLASS} Measurement Timing		●	6		75	ms
t_{CLASS_ACS}	Autoclass I_{CLASS} Measurement Timing		●	88		105	ms
t_{ME1}	Mark Event Duration (Except Last Mark Event)	(Note 11)	●	6	9.6	12	ms
t_{ME2}	Last Mark Event Duration	(Note 11)	●	6	20		ms
t_{PON}	Power On Delay, Auto Mode	From End of Valid Detect to End of Valid Inrush (Note 14)	●			400	ms
t_{AUTO_PSE1}	Autoclass Power Measurement Start	From End of Inrush to Beginning of Autoclass Power Measurement	●	1.4		1.6	s
t_{AUTO_PSE2}	Autoclass Power Measurement End	From End of Inrush to End of Autoclass Power Measurement	●	3.1		3.5	s
t_{AUTO_WINDOW}	Autoclass Average Power Sliding Window		●	0.15	0.23	0.3	s
t_{ED}	Fault Delay	From Power On Fault to Next Detect	●	1.0	1.3	1.8	s
t_{START}	Maximum Current Limit Duration During Inrush		●	50	60	75	ms
t_{CUT}	Maximum Overcurrent Duration After Inrush		●	50	65	75	ms
	Maximum Overcurrent Duty Cycle		●	5.8	6.3	6.7	%
t_{LIM}	Maximum Current Limit Duration After Inrush	(Note 12) Type 3, t_{LIMn} = 0x8 Type 4, t_{LIMn} = 0x5	 ● ●	 10 6	 15 11	 22 17	 ms ms
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Note 8)	●			6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	(Note 5)	●	320	370	400	ms
$t_{\overline{MSD}}$	Masked Shut Down Delay					6.5	µs
	I^2C Watchdog Timer Duration		●	1.5	2	3	s
	Minimum Pulse Width for Masked Shut Down		●	3			µs
	Minimum Pulse Width for $\overline{RESET}$		●	4.5			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I^2C Timing (Note 7)							
f_{SCLK}	Clock Frequency		●			1	MHz
t_1	Bus Free Time	Figure 5 (Note 9)	●	480			ns
t_2	Start Hold Time	Figure 5 (Note 9)	●	240			ns
t_3	SCL Low Time	Figure 5 (Note 9)	●	480			ns
t_4	SCL High Time	Figure 5 (Note 9)	●	240			ns
t_5	SDAIN Data Hold Time	Figure 5 (Note 9)	●	60			ns
	Data Clock to SDAOUT Valid	Figure 5 (Note 9)	●			250	ns
t_6	Data Set-Up Time	Figure 5 (Note 9)	●	80			ns
t_7	Start Set-Up Time	Figure 5 (Note 9)	●	240			ns
t_8	Stop Set-Up Time	Figure 5 (Note 9)	●	240			ns
t_r	SCL, SDAIN Rise Time	Figure 5 (Note 9)	●			120	ns
t_f	SCL, SDAIN Fall Time	Figure 5 (Note 9)	●			60	ns
	Fault Present to $\overline{INT}$ Pin Low	(Notes 9, 10)	●			150	ns
	Stop Condition to $\overline{INT}$ Pin Low	(Notes 9, 10)	●			1.5	µs
	ARA to $\overline{INT}$ Pin High Time	(Note 9)	●			1.5	µs
	SCL Fall to ACK Low	(Note 9)	●			250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifespan.

Note 2: This chipset includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 140°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC9102/LTC9103 operates with a negative supply voltage (with respect to AGND). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3.

Note 6: The LTC9101-1 digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

Note 7: Guaranteed by design, not subject to test.

Note 8: The IEEE 802.3 defines MPS as the set of minimum PSE and PD input current requirements to maintain power. An LTC9101-1/LTC9102/LTC9103 port resets its MPS timer when V_{SENSEn} – VSSKn ≥ $V_{HOLD-2P}$ for t_{MPS} and removes port power when V_{SENSEn} – VSSKn ≥ $V_{HOLD-2P}$ for a period longer than t_{DIS}. See Disconnect section.

Note 9: Values Measured at V_{IHD}.

Note 10: If a fault condition occurs during an I^2C transaction, the $\overline{INT}$ pin will not be pulled down until a stop condition is present on the I^2C bus.

Note 11: Load characteristics of the LTC9102/LTC9103 during Mark: 7V < (AGND – V_{OUTn}) < 10V.

Note 12: See the LTC9101-1 Software Programming documentation for information on serial bus usage and device configuration and status registers.

Note 13: Do not source or sink current from CAP1, CAP2, CAP3 and CAP4.

Note 14: For single-signature PDs, t_{PON} is measured from end of valid detect on either power channel. For dual-signature PDs, t_{PON} is measured from the end of valid detect on the same power channel.

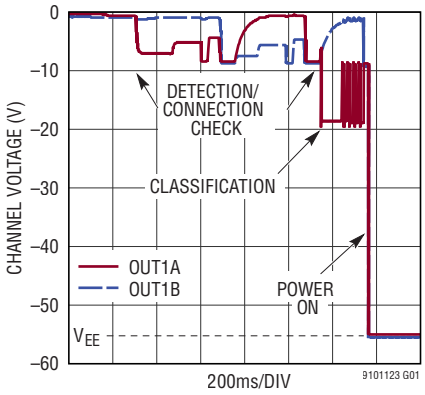
Note 15: Port current and port power measurements depend on sense resistor value (0.1Ω typical). See External Component Selection for details.

Note 16: See Inrush Control for details on inrush threshold selection.

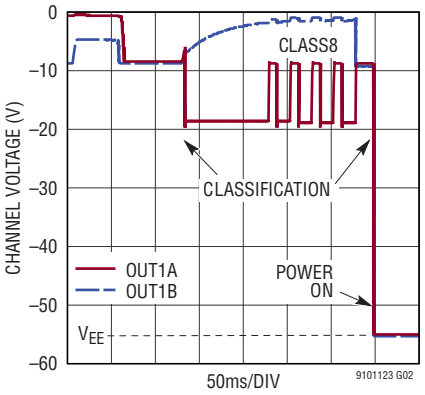
Note 17: ADC characteristics and typical performance are described in terms of LTC9102/LTC9103 hardware capability. Measurements from LTC9102/LTC9103 are processed and synthesized by LTC9101-1 to maintain backwards compatibility with LTC4291 software interface. See LTC9101-1 Software Interface for register descriptions and LSB weights (port current, port power, V_{EE} voltage, and system temperature).

TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

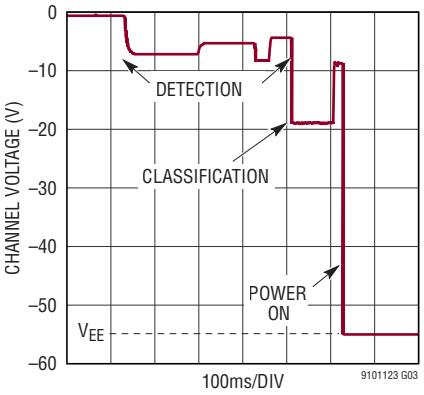
802.3bt Single-Signature Power-On Sequence, 4-Pair



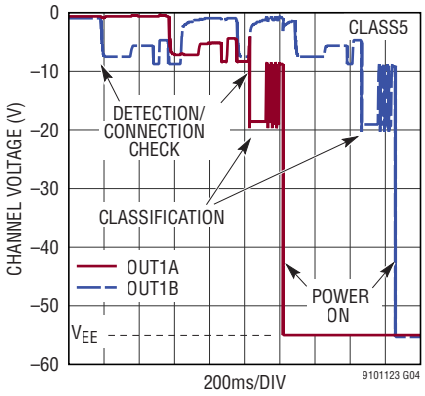
802.3bt Single-Signature Classification and Power-On, 4-Pair



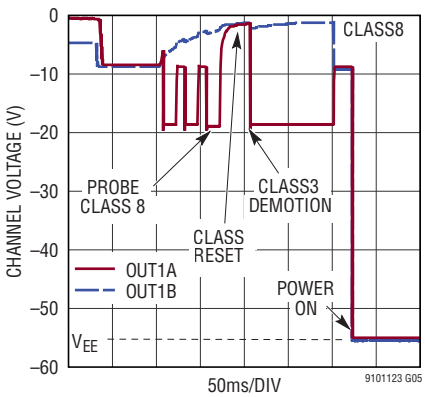
802.3bt Single-Signature Power-On Sequence, 2-Pair



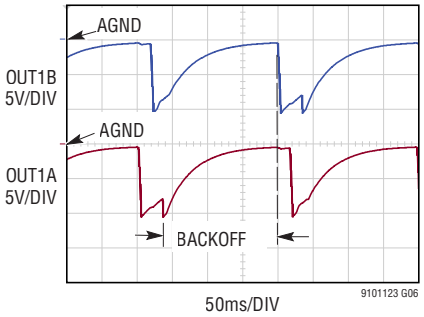
802.3bt Dual-Signature Power-On Sequence



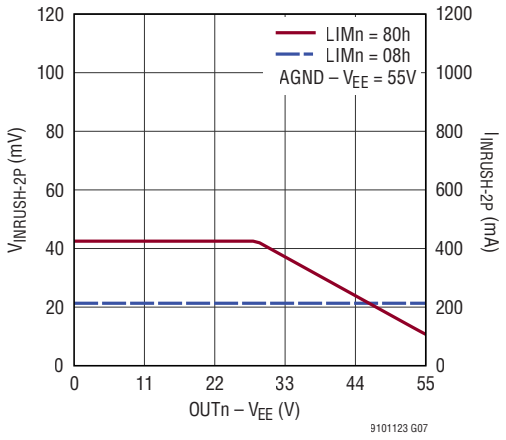
802.3bt Single-Signature Class Probe and Demotion



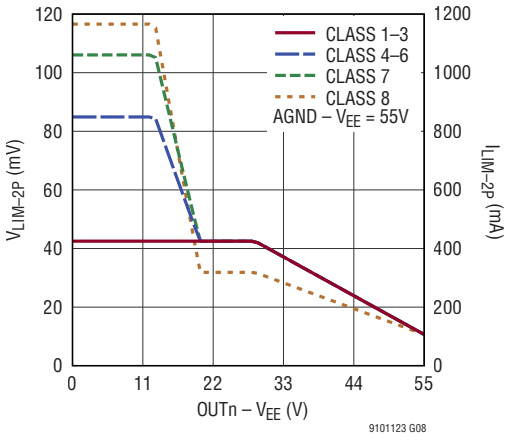
Open Circuit Detection



Inrush Current Limit (Note 16)

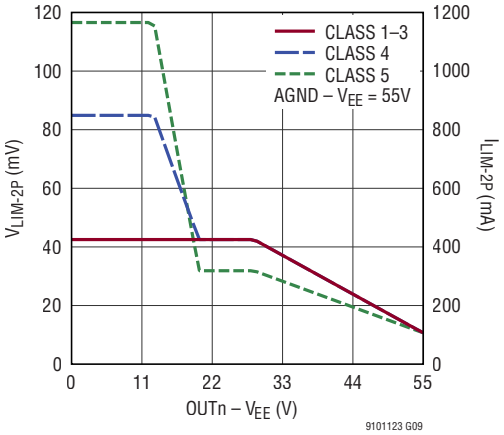


Power-On Current Limits Single-Signature

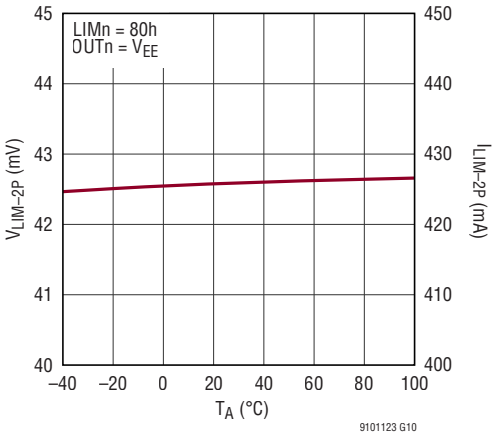


TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

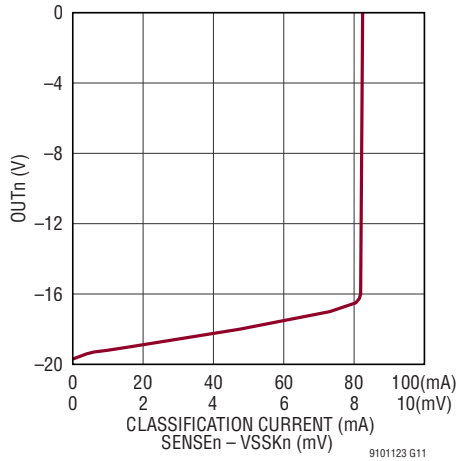
Power-On Current Limits Dual-Signature



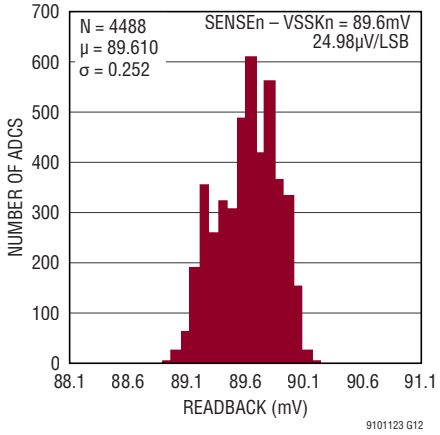
I_{LIM-2P} vs Temperature



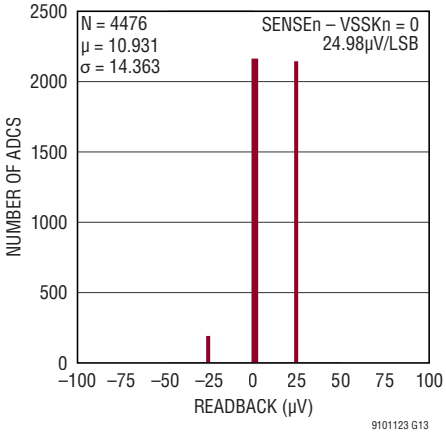
Classification Current Compliance



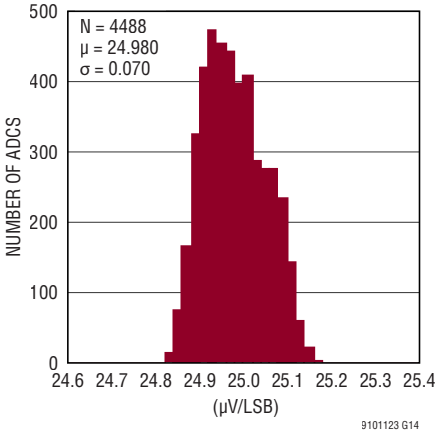
Port Current Readback



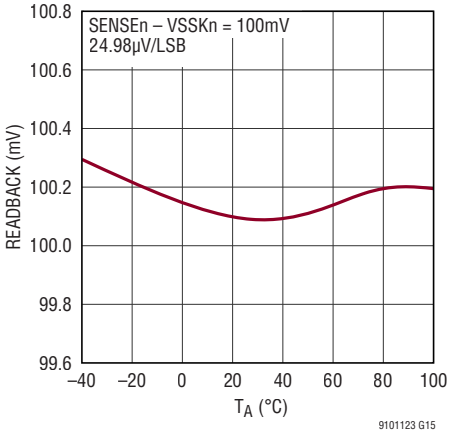
Port Current Readback Offset



Port Current Readback LSB

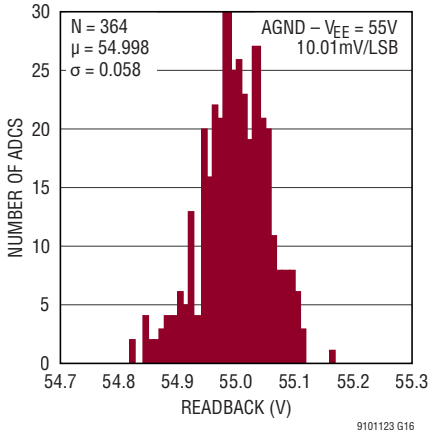


Port Current Readback vs Temperature

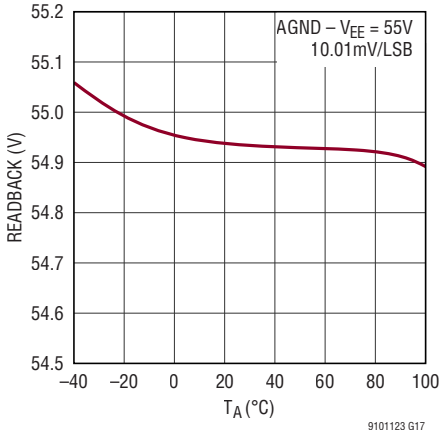


TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

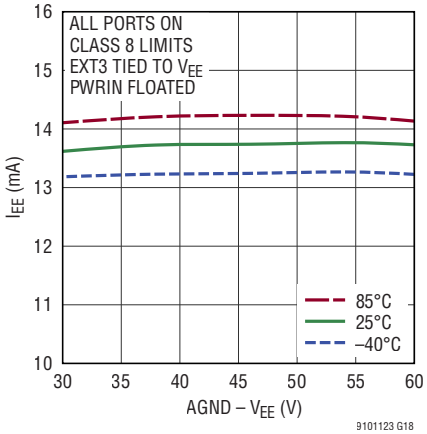
V_{EE} Readback



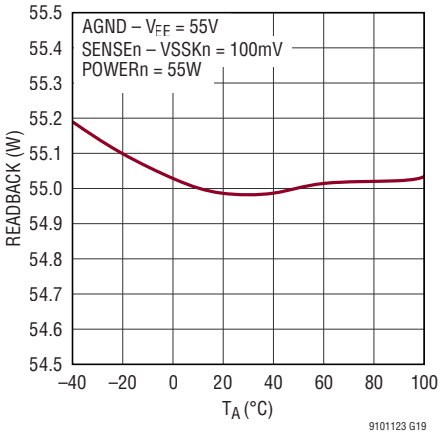
V_{EE} Readback vs Temperature



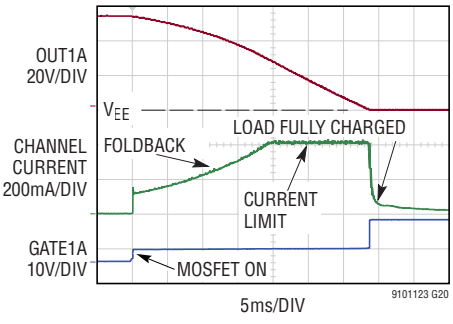
V_{EE} Supply Current vs Voltage and Temperature



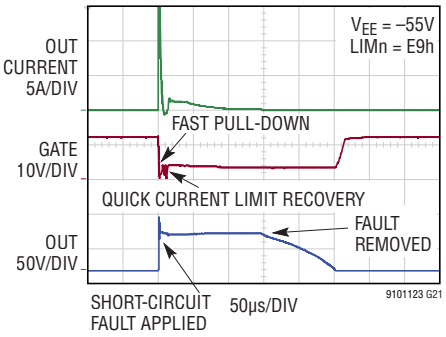
Port Power Readback vs Temperature



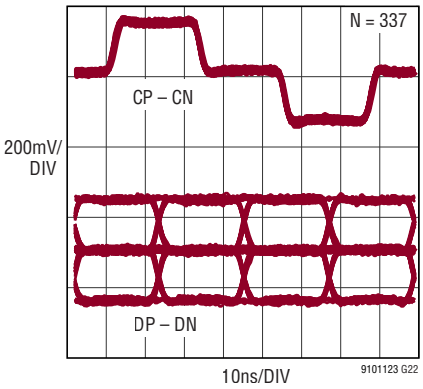
Powering Up into 180μF



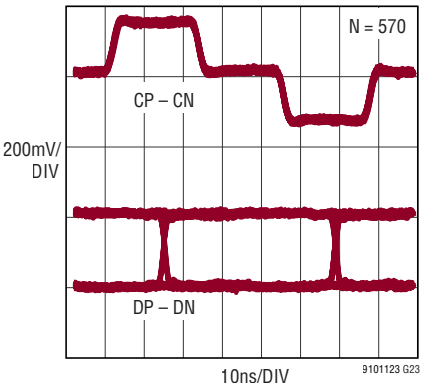
Short Circuit Recovery



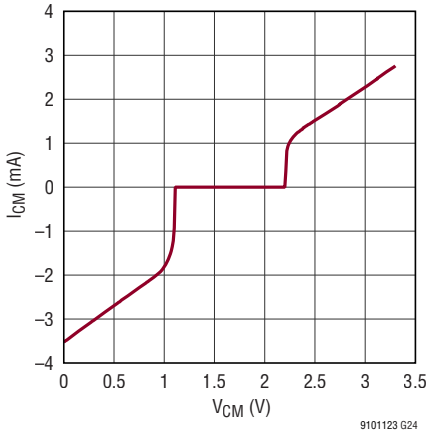
CLOCK and DATA WRITE EYE DIAGRAM



CLOCK and DATA READ EYE DIAGRAM

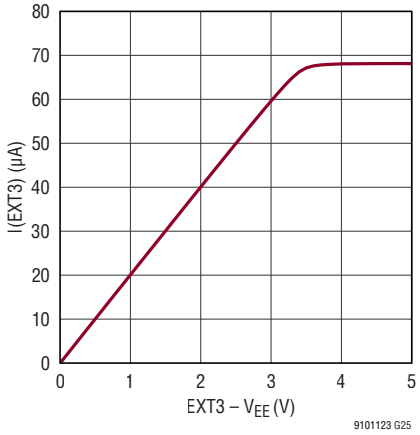


LTC9102/LTC9103 CP/CN and DP/DN Common Mode Correction Current

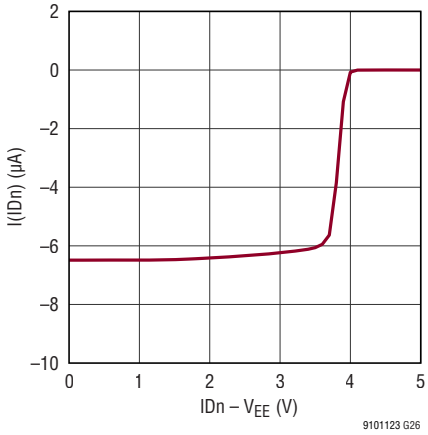


TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

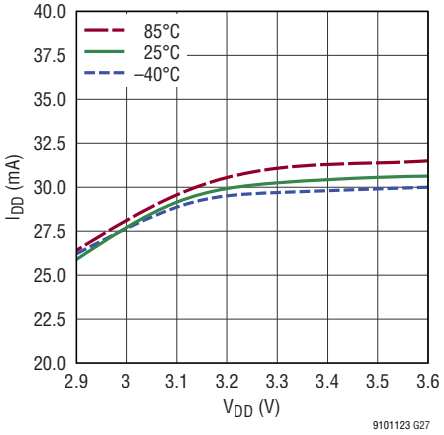
EXT3 Pin Current vs Voltage



IDn Pin Current vs Voltage



LTC9101-1 V_{DD} Supply Current vs Voltage and Temperature



TEST TIMING DIAGRAMS

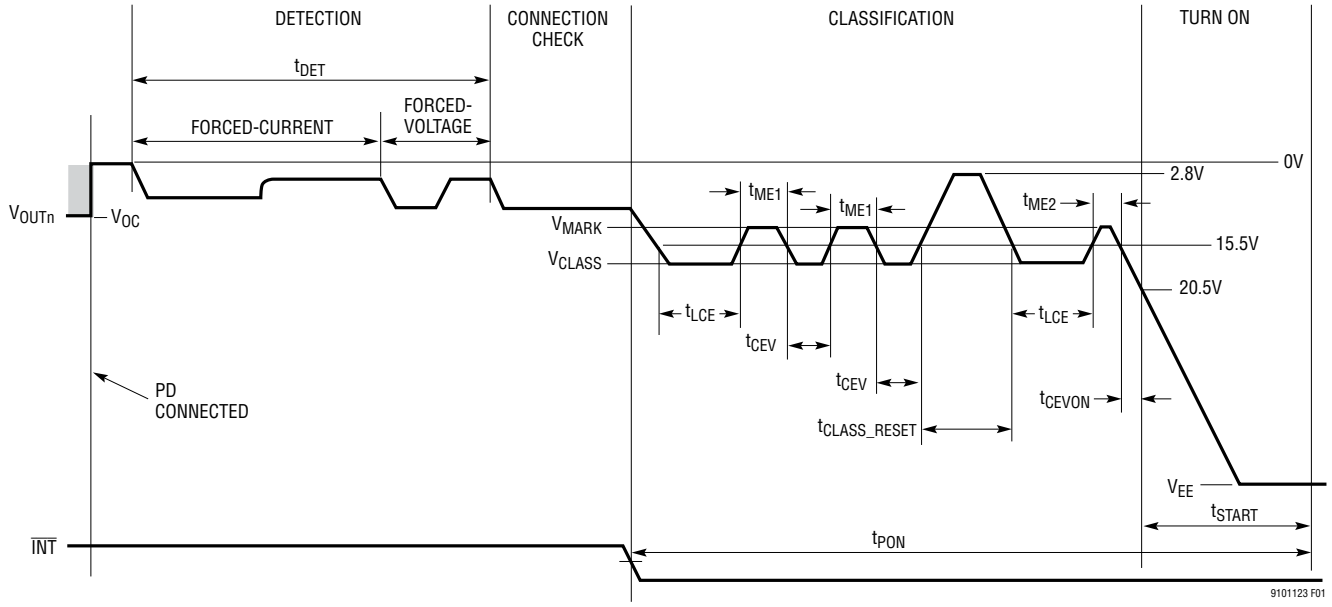
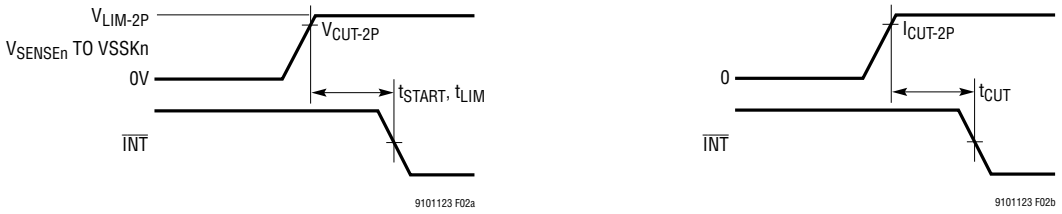


Figure 1. Detect, Class and Turn-On Timing, 4-Pair Port, Primary Alternative, Auto or Semi-Auto Mode

TEST TIMING DIAGRAMS



(a) Current Limit Timing

(b) Current Cutoff Timing

Figure 2. Current Timings

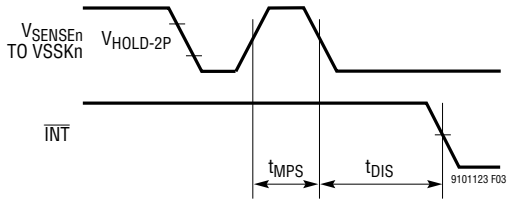


Figure 3. DC Disconnect Timing, 2-Pair System

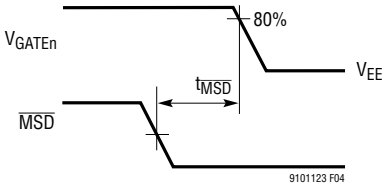


Figure 4. Shut Down Delay Timing

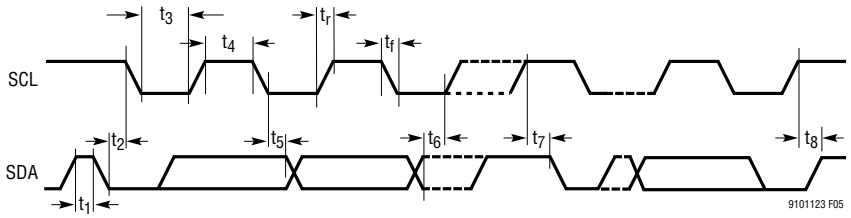


Figure 5. I²C Interface Timing

I²C TIMING DIAGRAMS

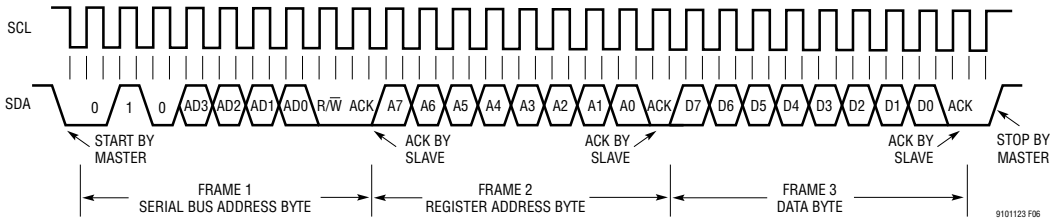


Figure 6. Writing to a Register

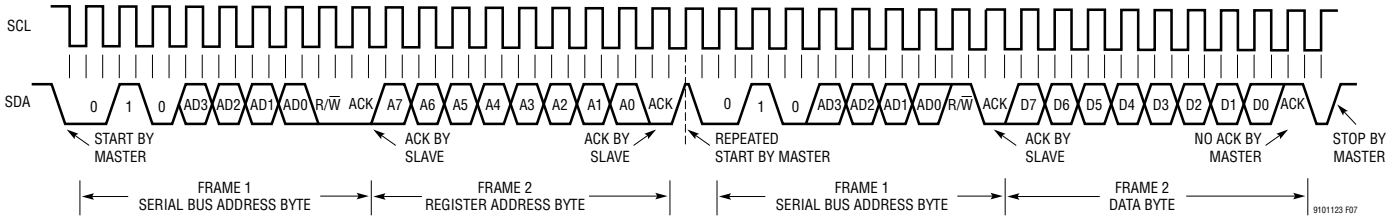


Figure 7. Reading from a Register

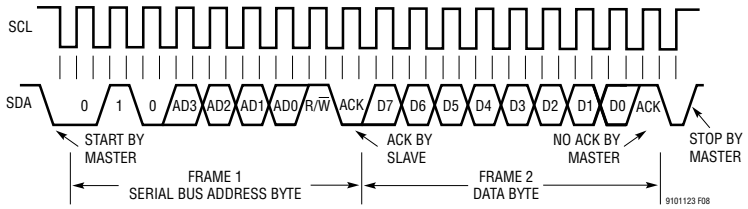


Figure 8. Reading the Interrupt Register (Short Form)

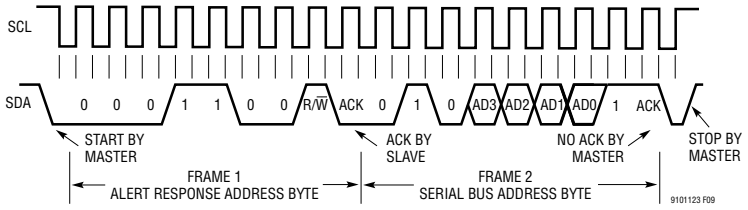


Figure 9. Reading from Alert Response Address

PIN FUNCTIONS

LTC9101-1

CFG[2:0] (Pins 3, 2, 1 Respectively): Device Configuration Inputs. Tie the configuration pins high or low to set number of ports, channels per port, and number of connected LTC9102/LTC9103s. See Device Configuration for details. CFG[0] is ignored when a custom configuration package is present. See Stored Configurations for details.

AD[3:2] (Pins 6, 5 Respectively): I^2C Address Bits 3 to 2. Tie the address pins high or low to set the base I^2C serial address. The base address will be $(010A_3A_200)b$. Internally pulled up to V_{DD}. See Bus Addressing for details.

CAP[2:1] (Pins 7, 23 Respectively): Core Power Supply Bypass Capacitors. Connect each pin to a 1µF capacitance to DGND for the internal 1.2V regulator bypass. Do not use other capacitor values. Do not source or sink current from this pin.

CPD (Pin 8): Clock Transceiver Positive Input Output (Digital). Connect to CPA through a data transformer.

CND (Pin 9): Clock Transceiver Negative Input Output (Digital). Connect to CNA through a data transformer.

DPD (Pin 10): Data Transceiver Positive Input Output (Digital). Connect to DPA through a data transformer.

DND (Pin 11): Data Transceiver Negative Input Output (Digital). Connect to DNA through a data transformer.

V_{DD} (Pins 12, 19, 24): V_{DD} IO Power Supply. Connect to a 3.3V power supply relative to DGND. Each V_{DD} pin must be locally bypassed with at least a 0.1µF capacitor. A 10µF bulk capacitor must be connected across V_{DD} for increased surge immunity.

$\overline{\text{4PVALID}}$ (Pin 13): 4-Pair Valid Input, Active Low. When low, the LTC9101-1/LTC9102/LTC9103 will not apply power to a port unless both pairsets present a valid signature. When high, the LTC9101-1/LTC9102/LTC9103 will power any pairset presenting a valid signature, regardless of the other pairset. Ports in 2-pair or AT mode are unaffected by 4-Pair Valid setting. Internally pulled down to DGND. $\overline{\text{4PVALID}}$ pin is ignored when a custom configuration package is present. See Stored Configurations for details.

$\overline{\text{RESET}}$ (Pin 14): Reset Input, Active Low. When $\overline{\text{RESET}}$ is low, the LTC9101-1/LTC9102/LTC9103 is held inactive with all ports off and all internal registers reset. When $\overline{\text{RESET}}$ is pulled high, the LTC9101-1/LTC9102/LTC9103 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of $\overline{\text{RESET}}$ prevents glitches less than 1µs wide from resetting the LTC9101-1/LTC9102/LTC9103. Internally pulled up to VDD.

$\overline{\text{INT}}$ (Pin 15): Interrupt Output, Open Drain. $\overline{\text{INT}}$ will pull low when any one of several events occur in the LTC9101-1. It will return to a high impedance state when bits 6 or 7 are set in the Reset PB register (0x1A). The $\overline{\text{INT}}$ signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual $\overline{\text{INT}}$ events can be disabled using the Int Mask register (0x01). See LTC9101-1 Software Programming documentation for more information. $\overline{\text{INT}}$ is only updated between I^2C transactions.

SDAOUT (Pin 16): Serial Data Output, Open Drain Data Output for the I^2C Serial Interface Bus. The LTC9101-1 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SDAIN (Pin 17): Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC9101-1 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SCL (Pin 18): Serial Clock Input. High impedance clock input for the I^2C serial interface bus. The SCL pin should be connected directly to the I^2C SCL bus line. SCL must be tied high if the I^2C serial interface bus is not used.

PIN FUNCTIONS

AUTO (Pin 20): Auto Mode Input, Active High. Auto mode allows the LTC9101-1 to detect, classify, and power up valid PDs without host interaction. AUTO determines the state of the internal registers when the LTC9101-1 is reset or comes out of UVLO (see LTC9101-1 Software Programming documentation). See Auto Mode Maximum PSE Power for details. The state of these register bits can subsequently be changed via the I^2C interface. Internally pulled down to DGND. The AUTO pin is ignored when a custom configuration package is present. See Stored Configurations for details.

$\overline{\text{MSD}}$ (Pin 21): Maskable Shutdown Input, Active Low. When pulled low, all ports that have their corresponding mask bit set in the mconf register (0x17) will be reset. Internal filtering of $\overline{\text{MSD}}$ prevents glitches less than 1µs wide from resetting ports. The $\overline{\text{MSD}}$ Pin Mode register can configure $\overline{\text{MSD}}$ polarity. Internally pulled up to V_{DD}.

DGND (Pins 22, 25): Digital Ground. DGND should be connected to the return from the V_{DD} supply.

LTC9102/LTC9103 COMMON

CAP3 (Pin 1): Analog Internal 3.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. A 3.3V power supply may be connected to this pin to improve power supply efficiency. The EXT3 pin must be pulled to CAP3 to shut off the internal 3.3V regulator if power is supplied externally. Do not source or sink current from this pin. Do not connect to CAP3 except as explicitly instructed in ADI documentation (e.g., strapping LTC9102/LTC9103 pins and terminating the serial interface).

EXT3 (Pin 2): External 3.3V Enable. Connect the EXT3 pin to CAP3 to shut off the internal 3.3V regulator when power is supplied externally. Float or connect to V_{EE} for internal regulator operation.

ID[1:0] (Pins 52, 51 respectively): Transceiver ID. Sets the address of the LTC9102/LTC9103 on the multidrop high-speed data interface. ID numbering must start at 00b. Tie high by connecting to CAP3. Tie low by connecting to V_{EE}. See Device Configuration section for details.

PWRIN (Pin 55): Startup Regulator Bypass and External Low Voltage Supply Input. Power for the internal 4.3V and 3.3V internal supplies. An internal regulator maintains the voltage of this pin above 6V. An external resistor or supply may be connected to this node to improve the power efficiency of the LTC9102/LTC9103. Connect a 1µF capacitor between this pin and V_{EE}.

AGND (Pin 56): Analog Ground.

PWRMD[1:0] (Pins 57, 58 Respectively): Maximum Power Mode Input. Connect PWRMD0 of the LTC9102/LTC9103 with ID[1:0] = 00b to V_{EE} with configuration resistor R_{PWRMD}. When the LTC9101-1 is reset with AUTO pin high, R_{PWRMD} selects initial maximum power allocation values for every port in the chipset; the system power supply must be sized to support all ports outputting up to R_{PWRMD}. When auto mode is enabled, the chipset runs independently as a PoE PSE. The chipset will detect and class all ports and grant power to each port up to R_{PWRMD} setting. The PWRMD0 pin of LTC9102/LTC9103s with ID pins set to 01b, 10b, and 11b must be left floating. The PWRMD1 pin of all LTC9102/LTC9103s must be left floating. See Auto Mode Maximum PSE Power for R_{PWRMD} options and details. The PWRMD pins are ignored when a custom configuration package is present. See Stored Configurations for details.

CAP4 (Pin 59): Analog Internal 4.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. Do not source or sink current from this pin.

V_{EE} (Pins 60, 65): Main PoE Supply Input. Connect to a –51V to –57V supply, relative to AGND. Voltage depends on PSE Type (Type 3 or 4).

DNA (Pin 61): Data Transceiver Negative Input Output (Analog). Connect to DND through a data transformer.

DPA (Pin 62): Data Transceiver Positive Input Output (Analog). Connect to DPD through a data transformer.

CNA (Pin 63): Clock Transceiver Negative Input Output (Analog). Connect to CND through a data transformer.

CPA (Pin 64): Clock Transceiver Positive Input Output (Analog). Connect to CPD through a data transformer.

PIN FUNCTIONS

LTC9102 EXCLUSIVE

VSSK[12:1] (Pins 47, 46, 39, 38, 31, 30, 23, 22, 15, 14, 7, 6 Respectively): Kelvin Sense to V_{EE}. Connect to V_{EE} side of sense resistor for channel n through a 0.1Ω resistor. Do not connect directly to V_{EE} plane. See Kelvin Sense layout requirements.

SENSE[12:1] (Pins 48, 45, 40, 37, 32, 29, 24, 21, 16, 13, 8, 5 Respectively): Current Sense Input, channel n. SENSEn monitors the external MOSFET current via a 0.1Ω sense resistor between SENSEn and VSSKn. If the voltage across the sense resistor reaches the current limit threshold I_{LIM-2P}, the GATEn pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the channel is unused, tie SENSEn to V_{EE}.

OUT[12:1] (Pins 49, 44, 41, 36, 33, 28, 25, 20, 17, 12, 9, 4 Respectively): Output Voltage Monitor, channel n. Connect OUTn to the output channel. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. A port power good event is raised when the voltage from OUTn to V_{EE} drops below 2.4V (typ). A 500k resistor is connected internally from OUTn to AGND when the channel is idle. If the channel is unused, the OUTn pin must float.

GATE[12:1] (Pins 50, 43, 42, 35, 34, 27, 26, 19, 18, 11, 10, 3 Respectively): Gate Drive, channel n. Connect GATEn to the gate of the external MOSFET for channel n. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATEn will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATEn is pulled down, turning the MOSFET off and raising a port fault event. If the channel is unused, the GATEn pin must float.

LTC9103 EXCLUSIVE

VSSK[8:1] (Pins 47, 46, 39, 38, 15, 14, 7, 6 Respectively): See LTC9102 VSSK[12:1].

SENSE[8:1] (Pins 48, 45, 40, 37, 16, 13, 8, 5 Respectively): See LTC9102 SENSE[12:1].

OUT[8:1] (Pins 49, 44, 41, 36, 17, 12, 9, 4 Respectively): See LTC9102 OUT[12:1].

GATE[8:1] (Pins 50, 43, 42, 35, 18, 11, 10, 3 Respectively): See LTC9102 GATE[12:1].

COMMON PINS

NC, DNC (LTC9101-1 Pin 4; LTC9102 Pins 53, 54; LTC9103 Pins 19–34, 53, 54): All pins identified with “NC” or “DNC” must be left unconnected.

APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE standard, known as 802.3af, allowed for 48V DC power at up to 13W. 802.3af was widely popular, but 13W was not adequate for some applications. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25.5W of delivered power. IEEE 802.3af and 802.3at are commonly known as PoE 1. In 2018, the IEEE released the latest PoE standard, known as 802.3bt or PoE 2. 802.3bt maximizes PD delivered power at 71.3W.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: endpoints (typically network switches or routers), which provide data and power; and midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices.

PoE++ Evolution

Even during the development of the IEEE 802.3at (PoE 1) 25.5W standard, it became clear there was a significant and increasing need for more than 25.5W of delivered power. In 2013, the 802.3bt task force was formed to develop a standard capable of increasing delivered PD power.

The primary objective of the task force is to use all four pairs of the Ethernet cable as opposed to the two pair power utilized by 802.3at. Using all four pairs allows for at least twice the delivered power over existing Ethernet cables. Further, the amount of current per two pairs (known as a pairset) has been increased while maintaining the Ethernet data signal integrity. 802.3bt increases PD delivered power from 25.5W to 71.3W, enabling IEEE-compliant high power PD applications.

The LTC9101-1/LTC9102/LTC9103 delivers power over one or two power channels when configured in 2-pair or 4-pair mode, respectively. Each pairset is driven by a dedicated power channel. In this data sheet, the term “channel” refers to the PSE circuitry assigned to a corresponding pairset. For the purposes of this document, the terms channel and pairset may be considered interchangeable.

In addition, IEEE 802.3bt enables substantially lower Maintain Power Signature (MPS) currents, resulting in significantly lower standby power consumption. This allows new and emerging government or industry standby regulations to be met using standard PoE components.

LTC9101-1/LTC9102/LTC9103 Product Overview

The LTC9101-1/LTC9102/LTC9103 is a sixth generation PSE controller that implements up to 24 (71.3W) 4-pair or 48 (25.5W) 2-pair PSE ports in either an endpoint or midspan application. Virtually all necessary circuitry is included to implement an IEEE 802.3bt compliant PSE design, requiring a pair of external power MOSFETs and sense resistors per port; these minimize power loss compared to alternative designs with onboard MOSFETs, and increase system reliability.

The LTC9101-1/LTC9102/LTC9103 chipset implements a proprietary isolation scheme for inter-chip communication. This architecture substantially reduces BOM cost by replacing expensive opto-isolators and isolated power supplies with a single low-cost transformer. A single LTC9101-1 is capable of controlling a bus of up to 4 LTC9102s/LTC9103s over this transformer-isolated interface. Direct connection of the LTC9101-1 and the associated LTC9102s/LTC9103s is also possible.

The LTC9101-1/LTC9102/LTC9103 offers configurable interrupt signal triggered by per-port events, per-channel power on control and fault telemetry, per-port current monitoring, V_{EE} monitoring, and one second rolling current, voltage and port power averaging.

The LTC9101-1/LTC9102/LTC9103 also offers advanced sixth-generation PSE features including internal eFlash for storage of firmware updates and custom user configuration packages, 2-pair operation in 802.3at-compliant or 802.3bt-compliant mode, I^2C quad virtualization for full

APPLICATIONS INFORMATION

backwards-compatibility with LTC4291 drivers, ultralow 100mΩ sense resistors, +80V/–20V tolerant port-facing pins, and improvements to cable surge ride through.

Each LTC9102/LTC9103 power channel is implemented with dedicated detection and classification hardware. This allows all ports and channels to detect, classify and power on simultaneously, drastically reducing power on latency across a switch. Other less advanced PSEs are subject to visible delays as PDs, e.g. LED lights, power on a port-by-port basis.

V_{EE} and port current measurements are performed simultaneously, enabling coherent and precise per-port power monitoring.

2-PAIR VS 4-PAIR MODE

The LTC9101-1 includes up to 12 groups of four identical ports. Each group of four ports is referred to as a quad. In the LTC9101-1 architecture, each quad contains register configuration and status for exactly four ports, regardless of whether the ports are in 2-pair mode or 4-pair mode.

In LTC9101-1 2-pair mode, exactly one LTC9102/LTC9103 channel is associated with each port in a quad. As such it is required that the LTC9102/LTC9103 power channel is connected to either Alternative A or Alternative B of the associated RJ45 connector. (See Figure 10)

In 2-pair mode the IEEE 802.3bt standard limits delivered power to 25.5W and supports PD Classes 0 to 4.

In LTC9101-1 4-pair mode, two LTC9102/LTC9103 channels are associated with each port. As such it is required that power channels are connected to Alternative A and Alternative B, respectively (see Figure 11). In 4-pair mode the host is responsible for deciding if both power channels will be utilized to power a given PD. Thus 2-pair powering in 4-pair mode can be used to power single-signature Class 0 to 4 PDs. For higher power Class 5 to 8 PDs and for all dual-signature PDs, both power channels must be utilized, also referred to as 4-pair power (see Figure 12).

In 4-pair mode the IEEE 802.3bt standard supports delivered power to 71.3W, supporting all existing single-signature PD Classes 0 to 8 and dual-signature PD Classes 1 to 5.

Mixes of 2-pair and 4-pair quads are available using a configuration package. See Stored Configurations for details.

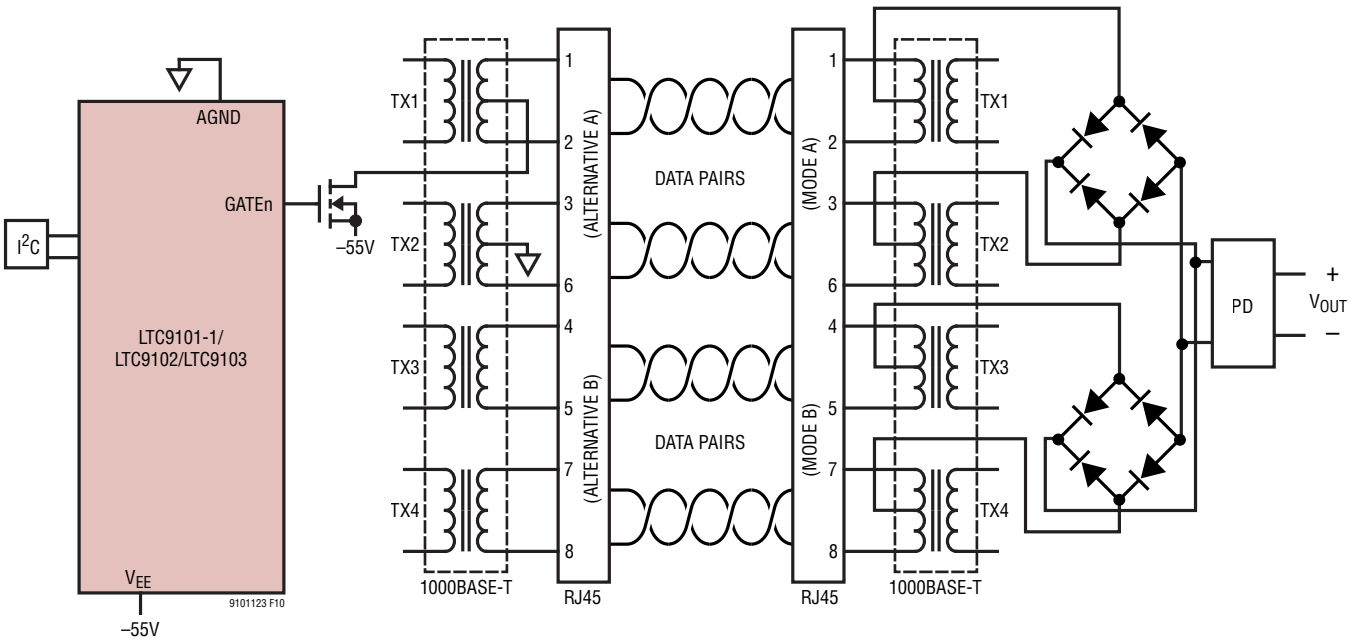


Figure 10. 2-Pair, Alternative A (Endpoint), Power over Ethernet Single-Signature PD System Diagram

APPLICATIONS INFORMATION

802.3at Mode

The LTC9101-1/LTC9102/LTC9103 may be configured as a 2-pair (802.3at or 802.3bt) or 4-pair 802.3bt PSE. All 802.3bt-compliant PSEs are fully backwards compatible with existing 802.3at Type 1 and Type 2 PDs as shown in Table 1. In addition to full compatibility, 802.3bt PSEs extend support for lower standby power, enhanced current limit timing, and dynamic power management to all PD Types (as supported by the PD application).

Table 1. PSE Maximum Delivered Power, Per-Port

DEVICE			PSE			
	STANDARD		802.3at		802.3bt	
		TYPE	1	2	3	4
PD	802.3at	1	13W	13W	13W	13W
		2	13W*	25.5W	25.5W	25.5W
	802.3bt	3	13W*	25.5W*	51W	51W
		4	13W*	25.5W*	51W*	71.3W

*Indicates PD allocated less power than requested.

The LTC9101-1 supports operation as an 802.3at compliant PSE. This feature is available in both 2-pair and 4-pair modes.

Note that an 802.3at PSE will not pass an 802.3bt PSE compliance test, and an 802.3bt PSE will not pass an 802.3at PSE compliance test. This is by design of the respective standards. 802.3at and 802.3bt devices are designed to be interoperable.

Table 2. 802.3at vs 802.3bt Features

FEATURE	802.3at	802.3bt
First Class Event	Short	Long
First Mark Event (15W Mode)	No	Yes
Limit Timer	No (Uses Cutoff Timer)	Yes
Connection Check	No	Yes
Active Alternative(s)	A	2-Pair: A 4-Pair: A and B
Maximum Class Events	2	5
Maximum Available Power	Class 4	2-Pair: Class 4 4-Pair: Class 8
Short MPS	No	Yes
Autoclass	No	Yes

PoE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as Ethernet cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 11 and Figure 12 show high level PoE system schematics.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE standard defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common-mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and applies power. When the PD is later disconnected, the PSE senses the open circuit and removes power. The PSE also removes power in the event of a current fault or short circuit.

When a PD is detected, the PSE looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to allocate power among several ports, to police the current consumption of the PD, or to reject a PD that will draw more power than the PSE has available.

New in 802.3bt

The 802.3bt specification introduces several new features:

- Type 3 and Type 4 PSEs may provide power over all four pairs (both pairsets), depending on connected PD characteristics.
- Type 3 and Type 4 PDs are required to be capable of receiving power over all four pairs (both pairsets).
- Type 3 and 4 PDs can be formed as either a single-signature PD or dual-signature PD. A single-signature PD presents the same valid signature resistor to both pairsets simultaneously (see Figure 11). A dual-signature PD presents two fully independent valid detection signatures, one to each pairset (see Figure 12).

APPLICATIONS INFORMATION

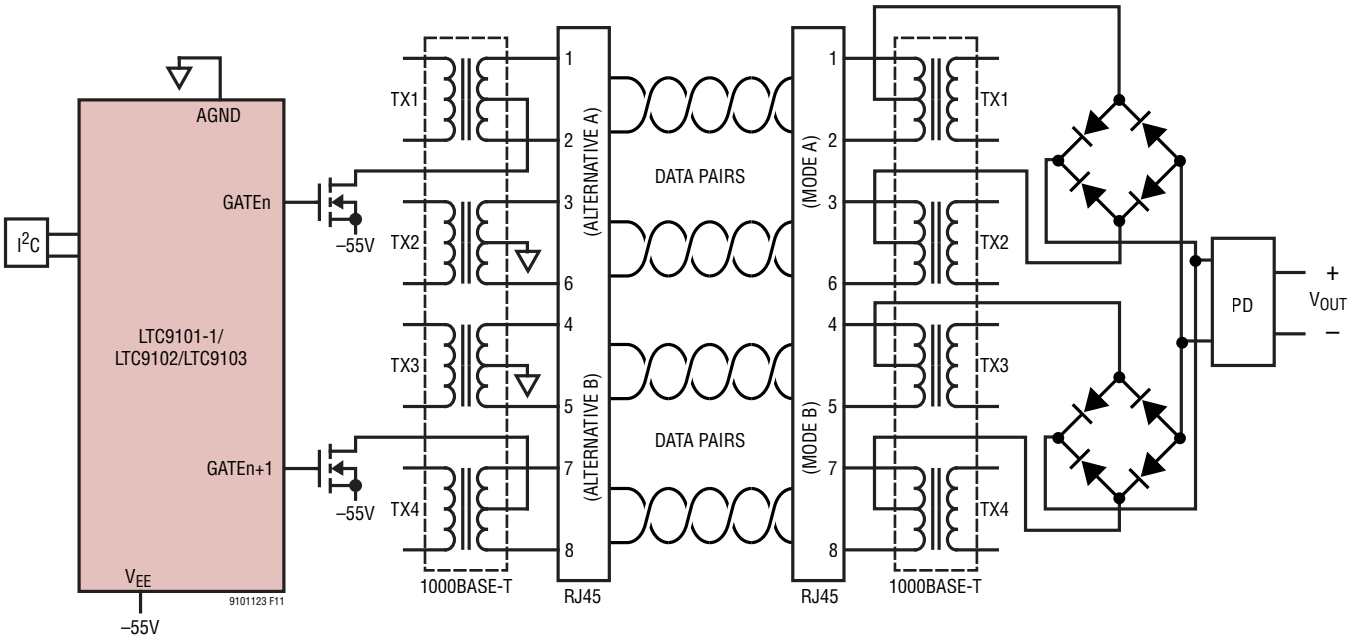


Figure 11. 4-Pair Power over Ethernet Single-Signature PD System Diagram

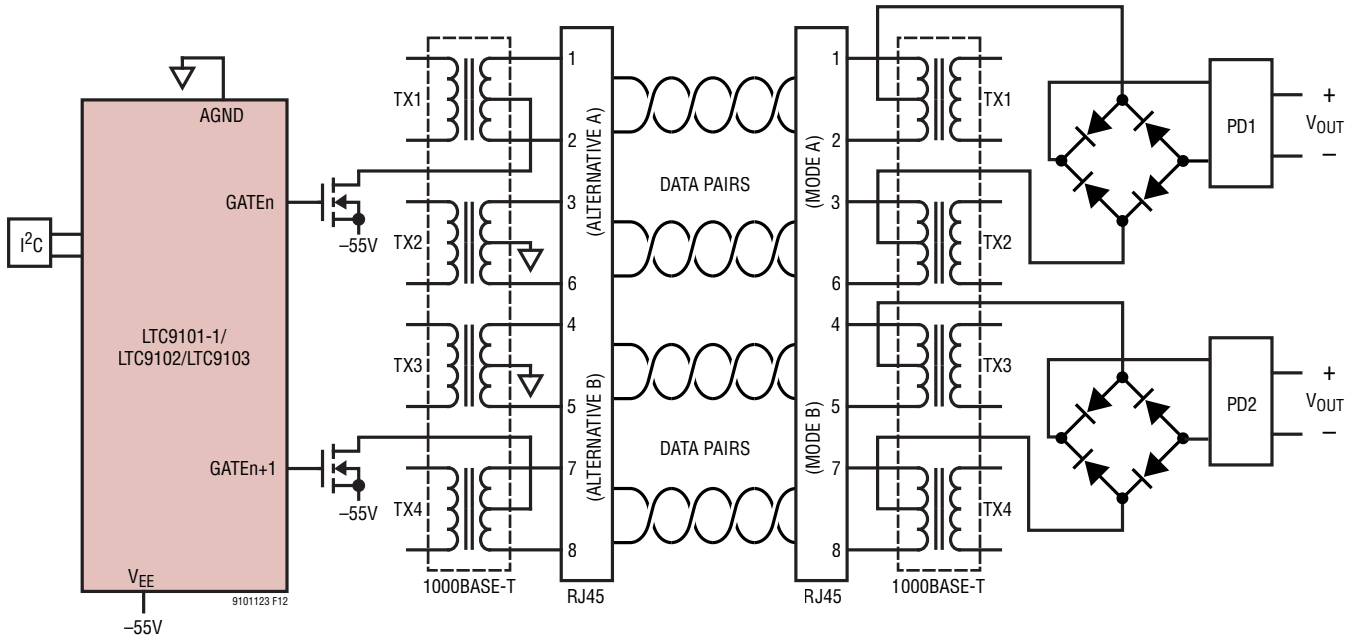


Figure 12. 4-Pair Power over Ethernet Dual-Signature PD System Diagram

APPLICATIONS INFORMATION

- Type 3 single-signature PDs request exactly one of six possible power levels: 3.84W, 6.49W, 13W, 25.5W, 40W, or 51W.
- Type 3 dual-signature PDs request exactly one of four possible power levels on each pairset: 3.84W, 6.49W, 13W, or 25.5W. The total PD requested power is the sum of the requested power on both pairsets.
- Type 3 PD Classes overlap with Type 1 and 2 Classes in order to provide additional Type 3 feature sets at lower power levels.
- Type 4 single-signature PDs request exactly one of two possible power levels: 62W or 71.3W.
- Type 4 dual-signature PDs request exactly 35.6W on at least one pairset and one of five possible power levels on the other pairset: 3.84W, 6.49W, 13W, 25.5W, or 35.6W. The total PD requested power is the sum of the requested power on both pairsets.
- Classification is extended to a possible maximum of five class events. The additional events allow for unique identification of existing and new PD Classes.
- Type 3 and 4 PSEs issue a long first class event to advertise Type 3 and 4 feature support to attached PDs.
- Lower standby power is enabled by shortening the length of the maintain power signature pulse (short MPS). The PD duty cycle drops from ~23% to ~2%. A PD is allowed to present short MPS if the PSE issues a long first class event.
- Power management is augmented by Autoclass, an optional feature for 802.3bt PSEs and PDs. In an Autoclass system the maximum PD power is measured and reported to the PSE host, enabling the PSE to reclaim output power not used by the PD application and losses in the Ethernet cabling (Table 3). See Autoclass section and LTC9101-1 Software Programming documentation for details.

Table 3. IEEE-Specified Power Allocations, Single-Signature PD

PD CLASS	PSE OUTPUT POWER	ALLOCATED CABLING LOSS	PD INPUT POWER
1	4W	0.16W	3.84W
2	6.7W	0.21W	6.49W
3	14W	1W	13W
4	30W	4.5W	25.5W
5	45W	5W	40W
6	60W	9W	51W
7	75W	13W	62W
8	90W	18.7W	71.3W

REGISTER MAP BACKWARD COMPATIBILITY

Software register map compatibility with LTC4266, LTC4271 and LTC4291-based PSEs has been maintained to the extent possible. LTC4291-based PSEs utilize two channels to control a single PSE port. LTC9101-based PSEs can be configured to utilize either a single power channel, delivering up to 25.5W, or as two channels, delivering up to 71.3W.

For register map details please contact Analog Devices to request the LTC9101-1 Software Programming documentation.

Special Compatibility Mode Notes

- As with prior generations, each I^2C address provides status and control for four PoE ports.
- In 4-pair mode, each port register slice provides port control and status as well as channel A vs B control and status.
- In 2-pair mode, each port register slice provides port control and status via channel A control and status. In this mode channel B control and status fields are ignored.
- Certain status registers, e.g. Port Status and Power Status, relate to a channel state, as opposed to port state and are split into three copies; a generalized port state, channel A state and channel B state.
- Certain command registers, e.g., Power-on pushbutton, likewise are bifurcated to allow per-channel control.

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DEVICE CONFIGURATION

An LTC9101-1 can control between one and four LTC9102/LTC9103. Each LTC9102 controls 12 power channels while each LTC9103 controls 8 channels. Thus, each LTC9101-1 can control up to 48 power channels configured in either 2-pair or 4-pair mode.

Large port count switch implementation may require a mix of 2-pair (25.5W) ports and 4-pair (up to 71.3W) ports. LTC9101-1 channels may be configured in an arbitrary combination of 2-pair or 4-pair quads by storing a custom configuration package. See Stored Configurations for details.

As described later in Bus Addressing, each group of four ports occupies a single I^2C address, regardless of 2-pair (2P) or 4-pair (4P) configuration. Using the CFG pins and a default configuration package, a LTC9101-1 can control either all 2-pair ports or can control all 4-pair ports (see Table 4).

Table 4. Device Configuration Options

		DEVICE COUNT		NUMBER OF PORTS			I^2C ADDRESS OFFSET															
CFG [2:0]		LTC9102	LTC9103	4P	2P	TOTAL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	000	1	0	0	12	12	2P	2P	2P													
0	000	0	1	0	8	8	2P	2P														
1	001	0	1	4	0	4	4P															
2	010	2	0	0	24	24	2P	2P	2P		2P	2P	2P									
2	010	1	1	0	20	20	2P	2P	2P		2P	2P										
2	010	0	2	0	16	16	2P	2P	2P		2P											
3	011	2	0	12	0	12	4P	4P	4P													
3	011	0	2	8	0	8	4P	4P														
4	100	3	0	0	36	36	2P	2P	2P		2P	2P	2P		2P	2P	2P					
4	100	2	1	0	32	32	2P	2P	2P		2P	2P	2P		2P	2P						
4	100	1	2	0	28	28	2P	2P	2P		2P	2P	2P		2P							
4	100	0	3	0	24	24	2P	2P	2P		2P	2P	2P									
5	101	2	1	16	0	16	4P	4P	4P		4P											
5	101	0	3	12	0	12	4P	4P	4P													
6	110	4	0	0	48	48	2P	2P	2P		2P	2P	2P		2P	2P	2P		2P	2P	2P	
6	110	3	1	0	44	44	2P	2P	2P		2P	2P	2P		2P	2P	2P		2P	2P		
6	110	2	2	0	40	40	2P	2P	2P		2P	2P	2P		2P	2P	2P		2P			
6	110	1	3	0	36	36	2P	2P	2P		2P	2P	2P		2P	2P	2P					
6	110	0	4	0	32	32	2P	2P	2P		2P	2P	2P		2P	2P						
7	111	4	0	24	0	24	4P	4P	4P		4P	4P	4P									
7	111	2	2	20	0	20	4P	4P	4P		4P	4P										
7	111	0	4	16	0	16	4P	4P	4P		4P											

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OPERATING MODES

The LTC9101-1/LTC9102/LTC9103 includes up to 48 independent ports, each of which can operate in one of three modes: manual, semi-auto, or auto. A fourth mode, shutdown, disables the port (see Table 5).

Table 5. Operating Modes

MODE	AUTO PIN	OPMD REGISTER	DETECT/ CLASS	POWER-UP	AUTOMATIC THRESHOLD ASSIGNMENT
Auto	1	11b	Enabled at Reset	Automatically	Yes
	0	11b	Host Enabled	Automatically	Yes
Semi-Auto	0	10b	Host Enabled	Upon Request	No
Manual	0	01b	Once Upon Request	Upon Request	No
Shutdown	0	00b	Disabled	Disabled	No

In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection, or detection and classification cycle when commanded to by the host, and reports the result in its Port Status register. The host system can command the port to apply or remove power at any time.

In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status of these attempts back to the host, and waits for a command from the host before applying power to the port. The host must enable detection and classification.

Auto mode operates the same as semi-auto mode except it will automatically apply power to the port if detection and classification are successful. Auto mode will autonomously set the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} values based on the Class result. This operational mode may be entered by setting AUTO high at reset or by changing the OPMD state to Auto (11b). See AUTO pin description and the Auto Mode Maximum PSE Power section.

In shutdown mode the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the LTC9101-1/LTC9102/LTC9103 will remove power automatically from any port or channel, as appropriate, that generates a fault. It will also automatically remove power from any port/channel that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

Reset and the AUTO Pin

The initial LTC9101-1/LTC9102/LTC9103 configuration depends on the state of AUTO during reset. Reset occurs at power-up, whenever $\overline{\text{RESET}}$ is pulled low, or when the global Reset All bit is set. Changing the state of AUTO after power-up will not change the port behavior of the LTC9101-1/LTC9102/LTC9103 until a reset occurs.

With AUTO high, each port will detect and classify repeatedly until a PD is discovered, set I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} according to the PSE assigned Class, apply power to valid PDs, and remove power when a PD is disconnected.

Table 6 and Table 7 show the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} values that will be automatically set in auto mode, based on the PSE assigned Class.

Table 6. Typical Auto Mode Power On Thresholds, Single-Signature PD**

PSE ASSIGNED CLASS	PER-CHANNEL		PER-PORT
	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-4P}
1	94mA	425mA	4.86W
2	150mA	425mA	7.56W
3	338mA	425mA	16.2W
4	638mA	850mA	32.4W
5	581mA	850mA	48.1W
6	731mA	850mA	64.3W
7	825mA	1063mA	80.5W
8	975mA	1167mA	96.1W

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Table 7. Typical Auto Mode Power On Thresholds, Dual-Signature PD**

PSE ASSIGNED CLASS	PER-CHANNEL		
	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-2P}*
1	94mA	425mA	4.86W
2	150mA	425mA	7.56W
3	338mA	425mA	16.2W
4	638mA	850mA	32.4W
5	975mA	1167mA	48.1W

*A per-port P_{CUT-4P} threshold holds the sum of P_{CUT-2P} for each powered channel.

**R_{SENSE} = 0.1Ω.

CONNECTION CHECK

Connection Check Overview

IEEE 802.3bt introduces a new detection subroutine known as connection check. A connection check is required to determine whether the attached PD is a single-signature PD, a dual-signature PD or an invalid result.

In 802.3at, only one PD configuration was described; this is known as a single-signature PD and is shown in Figure 11. A single-signature PD presents the same 25k detection resistor to both the pairsets in parallel.

New in 802.3bt is the dual-signature PD as shown in Figure 12. A dual-signature PD presents two fully independent 25k detection signature resistors, one to each pairset.

The PD configuration (single or dual) determines how the PD is managed during subsequent detection, classification and power on procedures. Throughout this data sheet attention will be called to the different treatment of single-signature and dual-signature PDs.

Connection check is performed with two current measurements, at the same forced voltage, on the first channel. The second channel is tested for aggressor behavior by introducing a forced current on the second channel during the second measurement. Comparison of the two resulting current measurements on the first channel allows for the connected device to be categorized as a single-signature PD, a dual-signature PD, or an invalid result.

An invalid connection check result is reported when a device is added or removed during connection check.

Connection check only affects operation in 4-pair mode. In 4-pair mode a detection cycle always includes a connection check unless the port is in AT mode. See Figure 1.

In 2-pair mode connection check is not enabled (intrinsically a 4-pair only operation) and all PDs are reported as single-signature regardless of the PD's actual signature configuration.

DETECTION

Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a valid PD before applying power. The IEEE 802.3 specification requires that a valid PD has a common-mode resistance of 25k ±5% at any channel voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 13). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer Network Interface Cards (NICs), many of which have 150Ω common-mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 13).

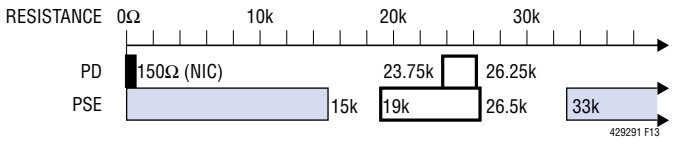

Figure 13. IEEE 802.3 Signature Resistance Ranges

APPLICATIONS INFORMATION

Multipoint Detection

The LTC9101-1/LTC9102/LTC9103 uses a multipoint method to detect PDs. False-positive detections are minimized by checking for signature resistance with both forced current and forced voltage measurements.

Initially, two test currents are forced onto the channel (via the OUTn pin) and the resulting voltages are measured. The detection circuitry subtracts the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 14). If the forced current detection yields a valid signature resistance, two test voltages are then forced onto the channel and the resulting currents are measured and subtracted. Both methods must report valid resistances to report a valid detection. PD signature resistances between 17k and 29k (typically) are detected as valid and reported as Detect Good in the corresponding Port Status register or Channel Status register, as appropriate. Values outside this range, including open and short circuits, are also reported. If the channel measures less than 1V during any forced current test, the detection cycle will abort and Short Circuit will be reported. Table 8 and Table 9 show the possible detection results.

Detection is enabled in both 2-pair and 4-pair modes. Detection is always performed on a per-channel basis.

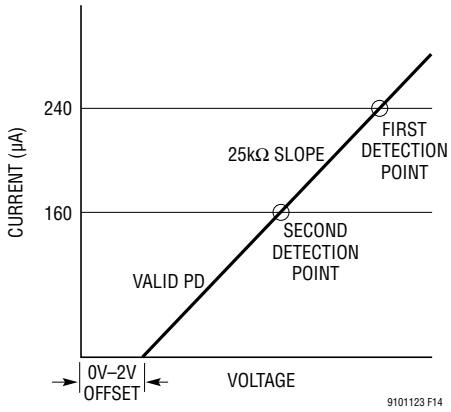

Figure 14. PD Detection

Table 8. Port Detection Status

MEASURED PD SIGNATURE (TYPICAL)	PORT DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
V_{PD} < 1V	Short Circuit
R_{PD} < 17k	R_{SIG} Too Low
17k < R_{PD} < 29k	Detect Good, Single-Signature PD
R_{PD} > 29k	R_{SIG} Too High
R_{PD} > 50k	Open Circuit
V_{PD} > 10V	Port Voltage Outside Detect Range
Connection Check = INVALID	Connection Check Invalid
Connection Check = DUAL or Channel Detection Results Differ	Refer to Channel Detect Results

Table 9. Channel Detection Status

MEASURED PD SIGNATURE (TYPICAL)	CHANNEL DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
V_{PD} < 1V	Short Circuit
C_{PD} > 2.7µF	C_{PD} Too High
R_{PD} < 17k	R_{SIG} Too Low
17k < R_{PD} < 29k	Detect Good, Dual-Signature PD
R_{PD} > 29k	R_{SIG} Too High
R_{PD} > 50k	Open Circuit
V_{PD} > 10V	Channel Voltage Outside Detect Range
Connection Check = INVALID	Connection Check Invalid
Connection Check = SINGLE or Channel Detection Results Match	Refer to Port Detect Result

More on Operating Modes

The port's operating mode determines when the LTC9101-1/LTC9102/LTC9103 runs a detection cycle. In manual mode, the port will idle until the host orders a detect cycle. It will then run detection, report the result, and return to idle to wait for another command.

In semi-auto mode the LTC9101-1/LTC9102/LTC9103 autonomously polls a port for PDs, but it will not apply power until commanded to do so by the host. The Detection/Classification Status registers are updated at the end of each detection/classification cycle.

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In semi-auto mode, if a valid signature resistance is detected and classification is enabled, the port will classify the PD and report that result as well. The port will then wait for at least 100ms, and will repeat the detection cycle to refresh the data in the Port Status registers.

The port will not turn on in response to a power-on command unless the current detect result is Detect Valid. Any other detect result will generate a t_{START} fault if a power-on command is received.

Behavior in Auto mode is similar to semi-auto; however, after Detect Valid is reported and the port is classified, it is automatically powered on without host intervention. In auto mode the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} thresholds are automatically set; see the Reset and the AUTO Pin section for more information.

Detection is disabled for a port when the LTC9101-1/ LTC9102/LTC9103 is initially powered up with AUTO low, when the port is in shutdown mode, or when the corresponding Detect Enable bit is cleared.

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy PDs. One type of legacy PD uses a large common-mode capacitance (>10µF) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that powers legacy PDs is noncompliant with the IEEE standard. The LTC9101-1/LTC9102/LTC9103 can be configured to detect this type of legacy PD. Legacy detection is disabled by default, but can be manually enabled on a per-port basis. When enabled, the port will report Detect Good when it detects either a valid IEEE PD or a high-capacitance legacy PD. With legacy mode disabled, only valid IEEE PDs will be recognized.

If a nonstandard PD presents an invalid detection signature not included by legacy detection, the LTC9101-1/ LTC9102/LTC9103 may be configured to perform classification and/or apply power regardless of detection result. To accomplish this, the LTC9101-1/LTC9102/LTC9103 introduces per-port Force Power and Class Event overrides. These overrides intentionally defeat compliance checks. See the LTC9101-1 Software Programming documentation for details.

CLASSIFICATION

802.3af Classification

A PD may optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V) as shown in Figure 16, with the current level indicating one of five possible PD signatures. Figure 15 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range. Table 10 shows the possible classification values.

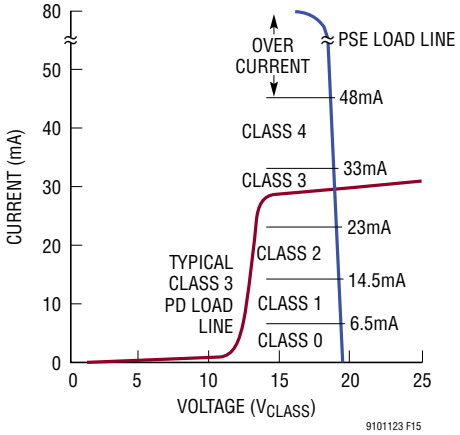

Figure 15. PD Classification

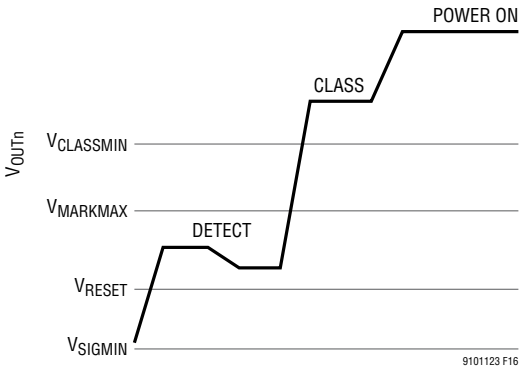

Figure 16. Type 1 or 2 PSE, 1-Event Class Sequence

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Table 10. Type 1 and Type 2 PD Classification Values

CLASS	RESULT
Class 0	No Class Signature Present; Treat Like Class 3
Class 1	3.84W
Class 2	6.49W
Class 3	13W
Class 4	25.5W (Type 2)

If classification is enabled, the PSE will classify the PD immediately after a successful detection cycle. The PSE measures the PD classification signature by applying V_{CLASS} to the port via OUTn and measuring the resulting current; it then reports the discovered class in the Port Status or Channel Status register, as appropriate. If the LTC9101-1/LTC9102/LTC9103 is in auto mode, it will additionally use the classification result to set the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} thresholds.

Classification is disabled for a port when the LTC9101-1/LTC9102/LTC9103 is initially powered up with the AUTO pin low, when the port is in shutdown mode, or when the corresponding Class Enable bit is cleared.

LLDP Classification

Introduced in 802.3at and extended by 802.3bt, the PoE specification defines a Link Layer Discovery Protocol (LLDP) method of classification. The LLDP method adds extra fields to the Ethernet LLDP data protocol.

Although the LTC9101-1/LTC9102/LTC9103 is compatible with this classification method, it cannot perform LLDP classification directly since it does not have access to the data path. LLDP classification allows the host to perform LLDP communication with the PD and update the PD's power allocation. The LTC9101-1/LTC9102/LTC9103 supports changing the I_{LIM-2P}, I_{CUT-2P}, and P_{CUT-4P} levels dynamically, enabling system-level LLDP support.

802.3at 2-Event Classification

In 802.3at, 802.3af classification is named Type 1 classification. The 802.3at standard introduces an extension of Type 1 classification: Type 2 (2-event) classification. Type 2 PSEs are required to perform classification.

A Type 2 PD requesting 25.5W presents class signature 4 during all class events. If a Type 2 PSE with 25.5W of available power measures class signature 4 during the first class event, it forces the PD to V_{MARK} (9V typical), pauses briefly, and issues a second class event as shown in Figure 17. The second class event informs the PD that the PSE has allocated 25.5W.

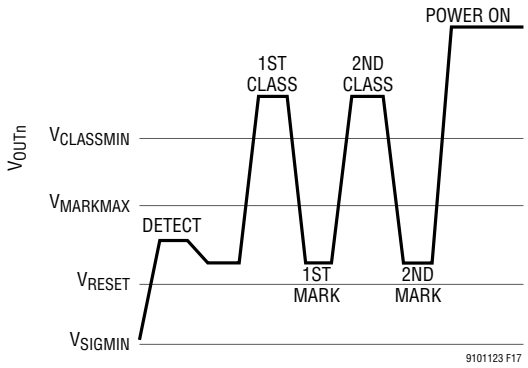

Figure 17. Type 2 PSE, 2-Event Class Sequence

Note that the second classification event only runs if required by the IEEE classification procedure. For example, a single-signature Class 0 to 3 PD will only be issued a single class event as shown in Figure 16.

The concept of demotion is introduced in 802.3at. A Type 2 PD may be connected to a PSE only capable of delivering 13W, perhaps due to power management limitations. In this case, the PSE will perform a single classification event as shown in Figure 16, and note that 25.5W is requested. Due to the limited power availability, the PSE will not issue a second event and proceeds directly to power on the PD. The presence of a single class event informs the Type 2 PD it has been demoted to 13W. If demoted, the PD is subject to power limitations and may operate in a reduced power mode.

802.3bt Multi-Event Classification

The LTC9101-1/LTC9102/LTC9103 implements Type 3 and Type 4 classification as required by 802.3bt. Type 3 and Type 4 classification are backwards-compatible with Type 1 and Type 2 PDs.

While Type 2 (802.3at) classification extends Type 1 (802.3af) classification, Type 3 and Type 4 (802.3bt)

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classification supersede Type 1 and Type 2 classification. Type 1 and Type 2 classification are described in the preceding sections as a historical reference and to define common terminology such as power demotion, class events, mark events, and electrical parameters.

IEEE 802.3bt defines eight PD Classes for single-signature PDs and five PD Classes for dual-signature PDs, as shown in Table 11.

Classification treatment of single-signature and dual-signature PDs differs. The following sections explain the Physical Layer classification of each PD configuration separately.

Table 11. Type 3 and Type 4 PD Classifications by PD Configuration

SINGLE-SIGNATURE PDs		DUAL-SIGNATURE PDs	
CLASS	PD AVAILABLE POWER	CLASS	CHANNEL AVAILABLE POWER*
Class 1	3.84W	Class 1	3.84W
Class 2	6.49W	Class 2	6.49W
Class 3	13W	Class 3	13W
Class 4	25.5W	Class 4	25.5W
Class 5	40W	Class 5	35.6W
Class 6	51W		
Class 7	62W		
Class 8	71.3W		

*Dual-signature PD total available power is the sum of both channels available power. Class signatures may differ between channels of a port, e.g., Class 3 + Class 4 = 13W + 25.5W = 38.5W.

802.3bt Classification of Single-Signature PDs

Type 3 and Type 4 PSEs issue a single classification event (see Figure 18) to Class 0 through 3 single-signature (SS) PDs. A Class 0 through 3 SS PD presents its class signature to the PSE and is then powered on if sufficient power is available. Power limited 802.3bt PSEs may also issue a single classification event to Class 4 and higher SS PDs in order to demote those PDs to 13W. See Figure 18.

Type 3 and 4 PSEs present three classification events to Class 4 SS PDs (see Figure 19) if sufficient power is available. Class 4 SS PDs present class signature 4 on all events. The third event differentiates a Class 4 SS PD from a higher Class SS PD. Power limited IEEE 802.3bt PSEs may issue three classification events to Class 5 and higher SS PDs in order to demote those PDs to 25.5W.

Type 3 and 4 PSEs present four classification events (see Figure 20) to Class 5 and 6 SS PDs if sufficient power is available. Class 5 and 6 SS PDs present class signature 4 on the first two events. Class 5 and 6 SS PDs present class signature 0 or 1, respectively, on the subsequent events. Power limited PSEs may issue four events to Class 7 and 8 SS PDs in order to demote those PDs to 51W.

Type 4 PSEs present five classification events (see Figure 21) to Class 7 and 8 SS PDs if sufficient power is available. Class 7 and 8 PDs present class signature 4 on the first two events. Class 7 and 8 SS PDs present class signature 2 or 3, respectively, on the subsequent events.

802.3bt Classification of Dual-Signature PDs

Classification and power allocations to each pairset of a dual-signature (DS) PD are fully independent. For example, a DS PD may request Class 1 (3.84W) on one pairset and a Class 4 (25.5W) on the second pairset for a total PD requested power of 29.3W. As such, all classification is performed to the pairset entity as opposed to the PD. The terms should be considered interchangeable for the remainder of this section.

Type 3 and Type 4 PSEs issue three classification events (see Figure 19) to all Class 1 through 4 DS PDs.

Power limited Type 3 and Type 4 PSEs may issue a class reset to Class 4 and 5 DS PDs in order to demote those PDs to 13W (see Understanding 4PID section).

Power limited Type 3 and Type 4 PSEs may issue only three events to Class 5 DS PDs in order to demote those PDs to 25.5W.

Type 4 PSEs present four classification events (see Figure 20) to Class 5 DS PDs if sufficient power is available. Class 5 DS PDs present class signature 4 on the first two events and class signature 3 on subsequent events.

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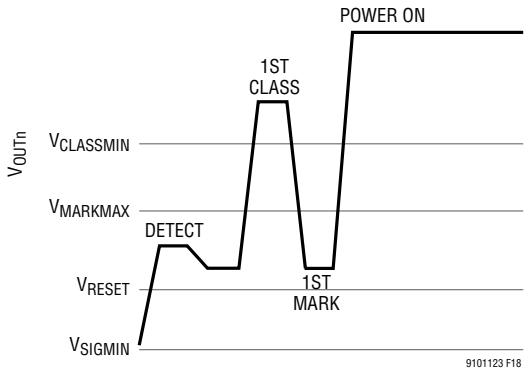

Figure 18. Type 3 or 4 PSE, 1-Event Class Sequence

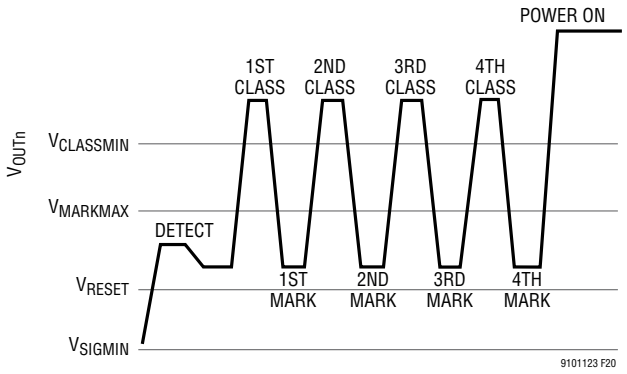

Figure 20. Type 3 or 4 PSE, 4-Event Class Sequence

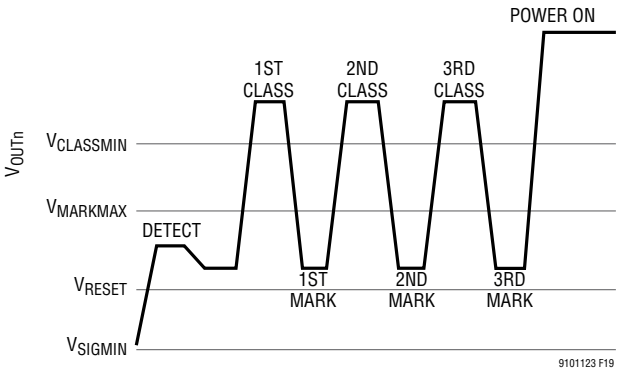

Figure 19. Type 3 or 4 PSE, 3-Event Class Sequence

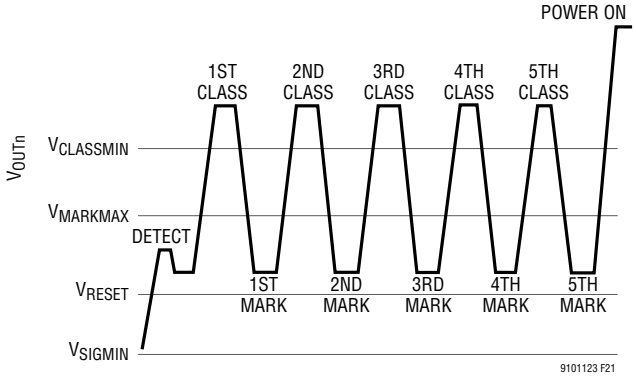

Figure 21. Type 4 PSE, 5-Event Class Sequence

Understanding 4PID

4-pair identification (4PID) refers to a set of conditions for determining whether a PD is capable of receiving power over both pairsets simultaneously.

The PSE may apply 4-pair power if the PD presents a valid detection signature on both pairsets and one or more of the following conditions are met:

- The port is in 4-pair mode.
- The PD is single-signature configuration.
- The PD is Type 3 or Type 4.
- The PD presents a valid detection signature on an unpowered pairset when power is applied over the other pairset.

Although PD signature configuration is not defined for Type 1 and Type 2 PDs, a Type 3 or Type 4 PSE may identify such a PD as single-signature or dual-signature. Single-signature PDs may receive 4-pair power regardless of PD Type. Certain pre-802.3bt “dual-signature” PDs may be damaged by 4-pair power.

Type 3 and Type 4 dual-signature PDs are required to present a unique classification response from pre-802.3bt dual-signature PDs of the same Class. For dual-signature PDs, the LTC9101-1/LTC9102/LTC9103 determines and reports both PD Class and PD Type during classification.

Type 3, Type 4, and pre-802.3bt Class 1 through Class 4 dual-signature PDs present class signature 1 through 4, respectively, during the first and second class events. Type 3 and Type 4 dual-signature PDs present class signature 0 for all subsequent class events. Thus, a PSE can conclusively determine PD Type by the third class event for all dual-signature PDs.

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Class Reset

An issue arises when a Class 4 or Class 5 dual-signature PD is connected. In order to determine PD Type, three class events are issued. Based on the class event count, the PD has been allocated 25.5W. If the PSE desires to both determine PD Type (3 events) and demote to 13W (1 event), a class reset event must be issued as shown in Figure 22.

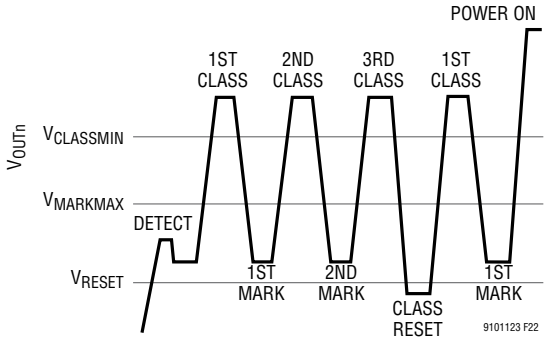

Figure 22. Class Reset Event Between Class Sequences

A class reset event is issued by maintaining the channel voltage below 2.8V for at least t_{CLASS_RESET}. The subsequent single event classification is used to demote the PD to 13W.

In auto mode the 4PID information and the state of $\overline{4PVALID}$ are used to automatically determine the number of powered channels.

LLDP signaling may, at some time later, determine the pre-bt PD is actually four pair capable and the LTC9101-1/LTC9102/LTC9103 may be instructed to deliver 4-pair power.

Invalid Multi-Event Classification Combinations

The 802.3bt specification defines a set of valid class signature combinations. All PDs return the same classification signature on the first two class events. Type 3 and 4 PDs modify the classification signature on all subsequent class events. For example, a single-signature Class 5 PD will respond to the class events 1, 2, 3, and 4 with a class signature of 4, 4, 0, and 0, respectively.

Any individual class signature that exceeds the class current limit is flagged as an invalid classification result. Any sequence of class signatures that does not represent a legal sequence based on PD configuration will likewise be flagged as an invalid classification result.

Auto Mode Maximum PSE Power

In auto mode the LTC9101-1/LTC9102/LTC9103 automatically detects, classifies and powers all connected valid PDs. In order to do this, each port must be configured for its maximum power allocation. Select the resistor R_{PWRMD} from Table 12 that reflects each port's maximum power delivery capability.

Connect the PWRMD0 pin of the LTC9102/LTC9103 at ID address 00b to V_{EE} through R_{PWRMD}. The PWRMD0 pin of the LTC9102/LTC9103 at ID address 01b, 10b, and 11b must be left floating. The PWRMD1 pin of each LTC9102/LTC9103 must be left floating. The PWRMD resistor is measured at reset.

The maximum power allocation is a reflection of the power supply and power path capability. The PWRMD resistor setting is applied to every port in this chipset, across all quads and ICs. Accordingly, the PWRMD resistor must be set with consideration for each port's power path capability and for the system's power supply capability.

When AUTO is low the PWRMD0 pin setting is ignored.

Table 12. Auto Mode Maximum Delivered Power Capabilities

	2-PAIR MODE	4-PAIR MODE	
R_{PWRMD}	MAX PORT POWER	MAX PORT POWER SINGLE-SIGNATURE PD	MAX PORT POWER DUAL-SIGNATURE PD*
Open	Class 3: 13.0W	Class 3: 13.0W	Class 3: 13.0W
24.3k		Class 4: 25.5W	Class 4: 25.5W
18.7k	Class 4: 25.5W		
14.3k		Class 5: 40.0W	Class 3: 13.0W
11.0k		Class 6: 51.0W	Class 4: 25.5W
8.45k		Class 7: 62.0W	Class 4: 25.5W
6.49k		Class 8: 71.3W	Class 5: 40.0W

*In auto mode, total port power allocation is double this value, reflecting the two halves of a dual-signature PD.

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POWER CONTROL

The primary function of the LTC9101-1/LTC9102/LTC9103 is to control power delivery to the PSE port. With the LTC9101-1/LTC9102/LTC9103, a PSE port is composed of either one or two power channels; each power channel controls power delivery over a pairset. Within this section, operation of 4-pair configured ports is defined per channel. When configured for 2-pair operation, only a single power channel is present per port.

The LTC9101-1/LTC9102/LTC9103 delivers power by controlling the gate drive voltage of an external power MOSFET while monitoring the current (through an external sense resistor) and the output voltage (across the OUT pin).

The LTC9101-1/LTC9102/LTC9103 connects the V_{EE} power supply to the PSE port in a controlled manner, meeting the power demands of the PD while minimizing power dissipation in the external MOSFET and disturbances to the V_{EE} backplane.

Inrush Control

When commanded to apply power to a port, the LTC9101-1/LTC9102/LTC9103 ramps up the GATE pin of one or both channels (as commanded), raising the external MOSFET gate voltage in a controlled manner.

During a typical inrush, the MOSFET gate voltage will rise until the external MOSFET is fully enhanced or the channel reaches the inrush current limit ($I_{INRUSH-2P}$). $I_{INRUSH-2P}$ is set automatically by the PSE. When the PSE is applying 4-pair power to a single-signature PD assigned Class 0 to Class 4, $I_{INRUSH-2P}$ is 212.5mA (typical) per channel. Otherwise, $I_{INRUSH-2P}$ is 425mA (typical) per channel.

The GATE pin will be servoed if channel current exceeds $I_{INRUSH-2P}$, actively limiting current to $I_{INRUSH-2P}$. When the GATE pin is not being servoed, the final V_{GS} is 12V (typical).

During inrush, each powered channel runs a timer (t_{START}). Each powered channel stays in inrush until t_{START} expires. When t_{START} expires, the PSE inspects channel voltage and current. When the PSE is applying power to a PD, inrush is successful if the channel(s) are drawing current below $I_{INRUSH-2P}$, as appropriate per the PD configuration and Class.

If inrush is not successful, power is removed and the corresponding t_{START} faults are set. Otherwise, the port or channel, as appropriate, advances to power on and the programmed current limiting thresholds are used as described in the Current Cutoff and Limit section.

Port Power Policing

The power policing threshold (P_{CUT-4P}) is monitored on a per-port basis, up to 128W in 0.5W increments (typical). When the total output power over a one second moving average exceeds the specified threshold, power is removed from the port and the corresponding t_{CUT} faults are set.

In particular, the port policing feature may be used to ensure delivery of PD Class power while staying below 100W Limited Power Source (LPS) requirements.

Current Cutoff and Limit

Each LTC9101-1/LTC9102/LTC9103 port includes two current limiting thresholds (I_{CUT-2P} and I_{LIM-2P}), each with a corresponding timer (t_{CUT} and t_{LIM}). Setting the I_{CUT-2P} and I_{LIM-2P} thresholds depends on several factors: the PD assigned Class, the main supply voltage (V_{EE}), the PSE Type (Type 3 or 4), and the MOSFET SOA.

A single set of programmable port I_{CUT-2P} and I_{LIM-2P} thresholds is shared by both channels. The thresholds should be set based on the classification result as shown in Table 6 and Table 7. For a dual-signature PD assigned unequal Classes, the highest Class is used to set the thresholds. For example, a dual-signature PD assigned Class 1 and Class 5 would enforce I_{CUT-2P} and I_{LIM-2P} based on Class 5.

Per the IEEE specification, the LTC9101-1/LTC9102/LTC9103 will allow the channel current to exceed I_{CUT-2P} for a limited period of time before removing power from the port, or channel, as appropriate whereas it will actively control the MOSFET gate drive to keep the channel current below I_{LIM-2P}. The channel does not take any action to limit the current when only the I_{CUT-2P} threshold is exceeded, but does start the t_{CUT} timer. If the current

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drops below the I_{CUT-2P} threshold before its timer expires, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. If the t_{CUT} timer reaches 65ms (typical), the port or channel, as appropriate, is turned off and the corresponding t_{CUT} faults are set. This allows the channel to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will remove power from the port or channel, as appropriate.

The I_{LIM-2P} current limiting circuit is always enabled and actively limiting channel current. The t_{LIM} timer is enabled only when the t_{LIM} Timer Configuration field is set to a non-zero value. This allows t_{LIM} to be set to a shorter value than t_{CUT} to provide more aggressive MOSFET protection and turn off a port before MOSFET damage can occur. The t_{LIM} timer starts when the I_{LIM-2P} threshold is exceeded. When the t_{LIM} timer reaches 1.9ms (typical) times the value in the t_{LIM} Timer Configuration field, the port or channel, as appropriate, is turned off and the appropriate t_{LIM} faults are set. When the t_{LIM} Timer Configuration field is set to 0, t_{LIM} behaviors are tracked by the t_{CUT} timer, which counts up during both I_{LIM-2P} and I_{CUT-2P} events. To maintain IEEE compliance, the programmed t_{LIM} Timer Configuration field should be set as shown in the LTC9101-1 Software Programming documentation.

I_{CUT-2P} is typically set to a lower value than I_{LIM-2P}, allowing the port to tolerate minor faults without current limiting.

To maintain IEEE compliance, I_{LIM-2P} should be set as shown in Table 6 and Table 7. The programmed I_{LIM-2P} setting is automatically applied following the completion of inrush.

The t_{CUT} and t_{LIM} timers are maintained on a per channel basis. When a t_{CUT} or t_{LIM} fault occurs a determination is made to turn off one or both channels. See the Port Fault vs Channel Fault section for details.

I_{LIM-2P} Foldback

The LTC9101-1/LTC9102/LTC9103 I_{LIM-2P} threshold is implemented as a two-stage foldback circuit that reduces the channel current if the channel voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels. Current limit and foldback behavior are programmable on a per-port basis.

The LTC9101-1/LTC9102/LTC9103 supports current levels well beyond the maximum values in the 802.3bt specification. Large values of I_{LIM-2P} may require larger external MOSFETs, additional heat sinking, and setting the t_{LIM} Timer Configuration field to a lower value.

MOSFET Fault Detection

LTC9101-1/LTC9102/LTC9103 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for an external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing SENSE to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing GATE to rise to an abnormally high voltage. OUT, SENSE and GATE are designed to tolerate up to 80V faults without damage.

If the LTC9101-1/LTC9102/LTC9103 detects any of these conditions for more than 3.8ms, it disables all port functionality, reduces the gate drive pull-down current for the port and reports a FET Bad fault. This is typically a permanent fault, but the host can attempt to recover by resetting the port, or by resetting the entire chip if a port reset fails to clear the fault. If the MOSFET is in fact bad, the fault will quickly return, and the port will disable itself again. The remaining ports of the LTC9101-1/LTC9102/LTC9103 are unaffected.

An open or missing MOSFET will not trigger a FET Bad fault, but will cause a t_{START} fault if the LTC9101-1/LTC9102/LTC9103 attempts to turn on the port.

Disconnect

The LTC9101-1/LTC9102/LTC9103 monitors powered channels to ensure the PD continues to draw the minimum specified current. The $I_{HOLD-2P}$ threshold, monitored as the $V_{HOLD-2P}$ threshold across the 0.1Ω sense resistor, is used to determine if a PD has been disconnected.

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The $I_{HOLD-2P}$ threshold is set automatically in auto mode and is set by the user in semi-auto and manual modes. When powering a single-signature PD assigned Class 0 to Class 4 over a single channel, set the $I_{HOLD-2P}$ threshold to 7.5mA (typ) via the Disconnect Configuration bit. In all other cases, set the $I_{HOLD-2P}$ threshold to 3.5mA (typ).

A disconnect timer (t_{DIS}) counts up whenever channel current is below the $I_{HOLD-2P}$ threshold, indicating that the PD has been disconnected. If the appropriate t_{DIS} timer(s) expire, the port or channel (Table 13) will be turned off and the corresponding t_{DIS} faults are set. If the current increases above $I_{HOLD-2P}$ before the t_{DIS} timer expires, the timer(s) reset. As long as the PD exceeds the minimum current level before t_{DIS} expires, it will remain powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding DC Disconnect Enable bits. Disabling the DC disconnect feature forces the LTC9101-1/LTC9102/LTC9103 out of compliance with the IEEE standard. A powered port will stay powered after the PD is removed; the still-powered port may be subsequently connected to a non-PoE data device, potentially causing damage.

The LTC9101-1/LTC9102/LTC9103 does not include AC disconnect circuitry. AC disconnect is not a supported feature of 802.3bt.

Fast Surge Recovery

High reliability systems demand excellent surge recovery. It is increasingly important for a PSE to minimize power disruption to the PDs during extreme power transients. Furthermore, PDs that do not meet minimum bulk capacitance requirements are particularly vulnerable to power brownouts with traditional PSE solutions. The LTC9101-1/LTC9102/LTC9103 provides an improved hot swap responsiveness with excellent recovery from surge events.

During a surge event, the LTC9102/LTC9103 GATE pin quickly turns off the external MOSFET current flow to protect the PSE, the MOSFET, and downstream circuitry. As the surge dissipates, the LTC9102/LTC9103 quickly turns the MOSFET back on in a safe, current limited manner while minimizing power disruption to the PD. The LTC9102/LTC9103 fast MOSFET turn off and power recovery better support both IEEE compliant PDs and PDs with lower bulk capacitance in high reliability applications.

Port Fault vs Channel Fault

The t_{CUT}, t_{LIM} and t_{DIS} timers are maintained on a per-channel basis. When any channel timer expires, a determination is made to remove power from both, one, or neither channel of the port.

Optional behavior is allowed by the 802.3bt standard when faults occur on single-signature PDs. This option allows a single-signature PD to remain powered on pairset X, even if a fault occurs on pairset Y. The `fault2Pn` bit, when set, enables this optional behavior. This behavior is not recommended for normal operation, as a fault in the PD or cabling is indicative of imminent PD or cable failure.

In 2-pair mode `fault2Pn` has no effect.

Table 13. Channel Fault Effect on Port/Channel State

PD CONFIGURATION	`fault2Pn` BIT	FAULT RESULT: TURN OFF PORT OR CHANNEL		
		t_{CUT}**	t_{LIM}	t_{DIS}
Single	0	Port	Port	Port*
	1	Channel	Channel	
Dual	x	Channel	Channel	Channel

*If t_{DIS} Expires on Both Channels

**Port power policing (P_{CUT-4P}) raises a t_{CUT} event. When enabled, port power policing removes power from the port regardless of `fault2Pn` configuration.

Fault Telemetry

As discussed in the preceding sections, faults may occur on one or both channels, resulting in power removal on one or both channels. The fault event registers have traditionally been implemented at the port level. In order to trace faults to the offending channel, a second layer of fault registers have been added to the LTC9101-1/

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LTC9102/LTC9103: the Fault Telemetry registers. See the LTC9101-1 Software Programming documentation for additional information.

Autoclass

IEEE 802.3bt introduces a new optional feature, Autoclass. Autoclass enables the PSE to reclaim power budget from single-signature PDs requesting more power than needed under worst-case operating conditions. 802.3bt does not specify Autoclass for dual-signature PDs. The LTC9101-1/ LTC9102/LTC9103 fully supports Autoclass.

Prior versions of the 802.3 PoE standard specify minimum PSE output power for worst-case IR drop across the Ethernet cable and minimum PSE output voltage. However, a method for the PSE to reclaim over-allocated power is not specified. When a shorter Ethernet cable is used, or when the guaranteed PSE output voltage is above the specified minimum, the specified minimum PSE output power substantially over-allocates power to the PD.

An example PoE system is shown in two versions. Figure 23 shows a 100W four port PSE servicing three 25.5W PDs over 100meter cables. Such a system requires the PSE to allocate 25.5W per PD and a further 4.5W for each 100m cable's IR drop.

The total power allocation is:

3 Ports • (4.5W + 25.5W) = 90W

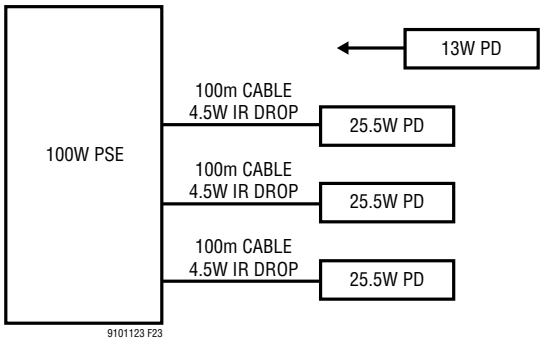

Figure 23. 100W PoE System with 100m Cables

If an additional 13W PD is plugged into the fourth PSE port, only 10W is available and the PD cannot be powered.

Figure 24 shows a 100W four port PSE servicing three 25.5W PDs over 10m cables. Such a system requires the PSE to allocate 25.5W per PD and a further ~0.5W for each 10m cable's IR drop.

Without Autoclass, the total power allocation is:

3 ports • (4.5W + 25.5W) = 90W

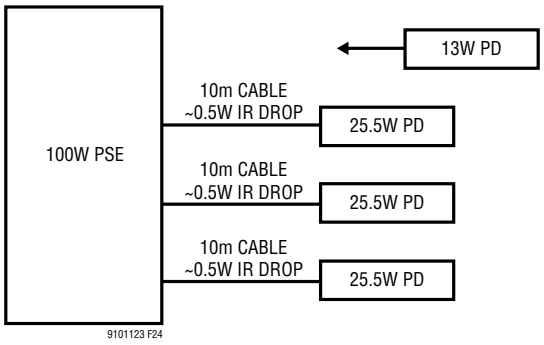

Figure 24. 100W PoE System with 10m Cables

If an additional 13W PD is plugged into the fourth PSE port, only 10W is available and the PD cannot be powered even though the IR drop is much less than in the prior example.

Assuming the system in Figure 24 is Autoclass-enabled, the recovered power budget can be used to power additional ports. During classification, the PSE observes the PD's Autoclass request. After power on is completed, the PD draws its maximum power while the PSE performs an Autoclass measurement, as specified by 802.3bt. The PSE in Figure 24 will measure and report 26W of power consumption for each of the three 25.5W PDs. This result allows the host to revise the PSE available power budget.

With Autoclass, the total power allocation for Figure 24 is:

3 Ports • 26W (Measured) = 78W

If an additional 13W PD is plugged into the fourth PSE port, a full 22W is now available and the PD can be successfully powered.

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Autoclass Negotiation Procedure

A PSE may receive an Autoclass request from the PD by Physical Layer classification or LLDP (by way of the PSE host). For Physical Layer requests, the Autoclass negotiation procedure listed below is shown in Figure 25.

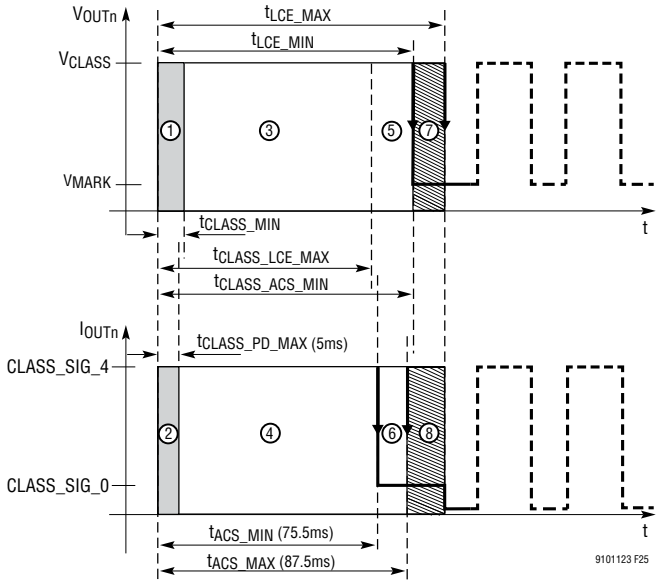


Figure 25. Autoclass Negotiation, Voltage and Current

1. PSE begins issuing the long first class event. The PD class signature is allowed to settle during this time.
2. The PD responds with a class signature corresponding to its Class. The class signature during this time period is unrelated to the Autoclass negotiation.
3. The PSE measures the PD class signature during this time and uses the result for the normal Multi-event Classification.
4. The PD continues presenting its class signature.
5. The PSE continues the long class event and does not measure the class signature current at this time.
6. The PD, if requesting Autoclass, transitions to class signature 0. If the PD is not requesting Autoclass it continues presenting its class signature.
7. The PSE measures the Autoclass response of the PD. If class signature 0 is measured, the PD is requesting Autoclass. When the measurement is complete the first class event is ended.
8. The PD continues holding the class signature selected in step 6 until the end of the first class event.

Following the Autoclass negotiation procedure, PSE and PD continue Physical Layer classification and power up as normal. Regardless of Autoclass, the PD is required to operate below the negotiated power allocation corresponding to PD assigned Class.

Autoclass Measurement Procedure

Autoclass measurements may be requested by the PD through Physical Layer classification or, following power on, through LLDP. Although the LTC9101-1/LTC9102/LTC9103 is compatible with LLDP-based Autoclass requests, it cannot receive LLDP Autoclass requests directly since it does not have access to the data path.

If the PSE is commanded to perform an Autoclass measurement following a Physical Layer request, the measurement typically begins t_{AUTO_PSE1} (1.5s typical) after port inrush is successfully completed. For LLDP-based Autoclass requests, the measurement begins immediately.

The Autoclass measurement period is $t_{AUTO\_PSE2} – t_{AUTO\_PSE1}$ (1.8s typical) using a sliding window of t_{AUTO_WINDOW} (0.23s typical). During the Autoclass measurement period, the PSE continuously monitors I_{PORT} and V_{EE}, calculating maximum average power. Following the Autoclass measurement period, the Autoclass measurements are reported in the Port Parametric registers.

See the LTC9101-1 Software Programming documentation for details on enabling Autoclass, the status of the Autoclass negotiation, reading Autoclass measurement results and dynamically requesting an Autoclass measurement.

APPLICATIONS INFORMATION

Port Current Readback

The LTC9101-1/LTC9102/LTC9103 measures the current at each power channel with per-channel A/D converters. Channel current is only valid when at least one power channel of a port is on and reads zero at all other times. The converter has two modes:

- 100ms mode: Samples are taken continuously and the measured value is updated every 100ms
- 1s mode: Samples are taken continuously; a moving 1 second average is updated every 100ms

V_{EE} Readback

The LTC9101-1/LTC9102/LTC9103 continuously measures the V_{EE} voltage with a dedicated A/D converter. This global V_{EE} measurement is fully synchronized to all port current measurements and can monitor down to the LTC9102/LTC9103 UVLO threshold.

Temperature Readback

In addition to the over temperature fault in the supply event register, the LTC9101-1 also reports die temperature of each corresponding LTC9102/LTC9103.

Overtemperature Protection

Overtemperature protection automatically removes power from affected ports when LTC9102/LTC9103 temperature exceeds a preset threshold (150°C, typ). Ports are prevented from resuming operation until the die temperature drops below a preset recovery threshold (125°C, typ). See LTC9101-1 Software Interface guide for details.

Port Power Readback

The LTC9101-1/LTC9102/LTC9103 provides fully continuous and synchronized port power measurements. The LTC9101-1/LTC9102/LTC9103 calculates the port power by multiplying the port current and V_{EE} measurements.

$$P_{PORT} = I_{PORT} \bullet V_{EE}$$

The Port Power measurements replace the Port Voltage measurements provided in prior ADI PSEs. Port voltage may be characterized and extrapolated from the V_{EE} measurement in a user-defined manner.

Masked Shutdown

The LTC9101-1/LTC9102/LTC9103 provides a low latency port shedding feature to quickly reduce the system load when required. By allowing a pre-determined set of ports to be turned off, the current on an overloaded main power supply can be reduced rapidly while keeping high priority devices powered. Each port can be configured to high or low priority; all low-priority ports will shut down within 6.5µs after $\overline{MSD}$ is pulled low, high priority ports will remain powered. If a port is turned off via $\overline{MSD}$, the corresponding Detection and Classification Enable bits are cleared, so the port will remain off until the host explicitly re-enables detection.

In the LTC9101-1/LTC9102/LTC9103 chipset, the active level of $\overline{MSD}$ is register configurable as active high or low. The default behavior is active low.

4-Pair Valid

The IEEE 802.3bt standard leaves room for interpretation in the single-signature and dual-signature PD definitions. Strictly speaking the 802.3bt standard defines only single-signature and dual-signature PDs.

A strict interpretation limits valid PDs to single-and dual-signature PDs which are connected to both PSE pairsets. PDs which do not have valid detection signatures on both pairsets are treated as invalid PDs. To enable a port's 4-Pair Valid mode, set $\overline{4PVALID}$ low or set the port's 4-Pair Valid configuration register. With 4-Pair Valid mode enabled, a port will only apply power if there is a valid detection signature on both pairsets. See Table 14.

Table 14. 4-Pair Valid Enabled

PAIRSET DETECTION SIGNATURE	ALTERNATIVE A INVALID	ALTERNATIVE A VALID
ALTERNATIVE B INVALID	Port Unpowered	Port Unpowered
ALTERNATIVE B VALID	Port Unpowered	Power A and B

APPLICATIONS INFORMATION

A second interpretation is more liberal and allows PDs which only present valid detection signatures on one pairset to be powered on the corresponding pairset, regardless of the detection result on the other pairset. To disable a port's 4-Pair Valid mode, set $\overline{4PVALID}$ high or clear the port's 4-Pair Valid configuration register. With 4-Pair Valid mode disabled, a port will power a pairset with a valid signature regardless of the valid or invalid signature on the other pairset. See Table 15.

Table 15. 4-Pair Valid Disabled

PAIRSET DETECTION SIGNATURE	ALTERNATIVE A INVALID	ALTERNATIVE A VALID
ALTERNATIVE B INVALID	Port Unpowered	Power A
ALTERNATIVE B VALID	Power B	Power A and B

Any PD powered with a valid detection signature on one pairset is treated as a dual-signature PD with one pairset unpowered.

Code Download

LTC9101-1 firmware is field-upgradable by downloading and executing firmware images.

Contact Analog Devices for code download procedures and firmware images.

Firmware images are stored in a dedicated flash partition. A fully-compliant IEEE 802.3at/bt firmware image is preconfigured on the LTC9101-1. The firmware image may be overwritten by the user.

Two complete copies of firmware images are maintained under separate ECC and CRC protection for maximum data protection.

Stored Configurations

Custom I^2C register map initial values may optionally be stored in a dedicated flash partition (configuration package). When shipped from the factory, the LTC9101-1 contains a default configuration package where register map initial values are as specified in the LTC9101-1 Software Interface. These initial values are subject to the state of pins, such as the AUTO and $\overline{4PVALID}$ pins. Register map default configurations may be stored during manufacturing bring up or field-updated via configuration package download and will be auto-loaded at boot.

In addition to configuring register map initial values, configuration packages enable port definition as either 2-pair or 4-pair ports. Ports are configured as 2-pair or 4-pair at the quad level (groups of 4 ports).

Contact ADI applications support for assistance in generating custom configuration packages. Configuration packages are downloaded using normal code download mechanisms. Package headers ensure configuration packages are identified and stored in the appropriate flash partition.

If a stored configuration is utilized, the state of the AUTO, CFG[0], PWRMD[1:0] and $\overline{4PVALID}$ pins can be overwritten by a configuration package. CFG[2:1] are still required to inform the LTC9101-1 how many LTC9102/LTC9103 are attached. AD[3:2] are still required to inform the LTC9101-1 of the base I^2C chip address.

Two identical copies of the configuration image are maintained under separate ECC and CRC protection for maximum data protection.

SERIAL DIGITAL INTERFACE

Overview

The LTC9101-1 communicates with the host using a standard SMBus/I^2C 2-wire interface. The LTC9101-1 is a slave-only device, and communicates with the host master using standard SMBus protocols. Interrupts are signaled to the host via $\overline{INT}$. The timing diagrams (Figure 5 through Figure 9) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at www.smbus.org.

The LTC9101-1 requires both the V_{DD} and V_{EE} supply rails to be present for the serial interface to function.

APPLICATIONS INFORMATION

Bus Addressing

The LTC9101-1's primary 7-bit serial bus address is $010A_3A_200b$, with bits 3:2 set by AD3:AD2 respectively. In Figure 6 through Figure 9, AD3:AD2 are set by LTC9101-1 pins and AD1:AD0 are inferred by device configuration. See Table 4 for device configuration options. Depending on device configuration, up to 12 I^2C addresses will be populated from the I^2C base address upwards. All LTC9101-1s also respond to the broadcast address 0110000b, allowing the host to write the same command (typically configuration commands) to multiple LTC9101-1s in a single transaction. If the LTC9101-1 is asserting $\overline{INT}$, it will also respond to the alert response address (0001100b) per the SMBus specification.

Each LTC9101-1/LTC9102/LTC9103 is logically composed of multiple four port groups, known as quads, each packed into a single I^2C address. See Device Configuration section for details. For example, if CFG[2:0] is set to 000, an LTC9101-1 is configured as an 8-port or 12-port device when attached to an LTC9102 or an LTC9103, respectively (see Table 4). This configuration requires two or three consecutive I^2C addresses, with quad offset 0 starting at the I^2C base address.

Note that any individual quad I^2C address greater than or equal to 0x30 (the broadcast address) will be automatically disabled.

Interrupts and SMBAlert

Most port events can be configured to trigger an interrupt, asserting $\overline{INT}$ and alerting the host to the event. This removes the need for the host to poll the LTC9101-1, minimizing serial bus traffic and conserving host CPU cycles. Multiple LTC9101-1s can share a common $\overline{INT}$ line, with the host using the SMBAlert protocol (ARA) to determine which LTC9101-1 caused an interrupt.

Register Description

For information on serial bus usage and device configuration and status, refer to the LTC9101-1 Software Interface guide. Contact Analog Devices to request this document.

ISOLATION REQUIREMENTS

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

If the PSE is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the PoE subsystem must be electrically isolated from the rest of the system.

The LTC9101-1/LTC9102/LTC9103 chipset simplifies PSE isolation by allowing the LTC9101-1 chip to reside on the non-isolated side. There it can receive power from the main logic supply and connect directly to the I^2C/SMBus bus. In this case, the SDAIN and SDAOUT pins can be tied together and will act as a standard I^2C/SMBus SDA pin. Isolation between the LTC9101-1 and LTC9102/LTC9103 is implemented using a proprietary transformer-based communication protocol. Additional details are provided in the High-Speed Data Isolation section of this data sheet.

For simple devices, such as unmanaged PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. The LTC9101-1 may directly connect to the LTC9102s/LTC9103s in the above circumstances, or if the system already provides isolation.

EXTERNAL COMPONENT SELECTION

Power Supplies

The LTC9101-1/LTC9102/LTC9103 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) relative to DGND. V_{EE} requires a negative voltage of between –51V to –57V for Type 2 and 3 PSEs, or –53V to –57V for Type 4 PSEs, relative to AGND.

APPLICATIONS INFORMATION

Digital Power Supply

V_{DD} provides digital power for the LTC9101-1 processor. A ceramic decoupling cap of at least 0.1µF should be placed from each V_{DD} to DGND, as close as practical to each LTC9101-1. In addition, each LTC9101-1 must include a bulk cap of 10µF for robust surge immunity. A 1.2V core voltage supply is generated internally and requires a 1µF ceramic decoupling cap between the CAP1 pin and DGND and between CAP2 and DGND.

In systems using ADI's proprietary isolation, V_{DD} should be delivered by the host controller's non-isolated 3.3V supply. To maintain required isolation, LTC9102/LTC9103 AGND and LTC9101-1 DGND must not be connected. If using the direct connection scheme, the LTC9101-1 DGND must be connected to LTC9102/LTC9103 V_{EE}.

Main PoE Power Supply

V_{EE} is the main isolated PoE supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V), leaving enough margin to account for transient over or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

A bypass capacitor and a transient voltage suppressor(TVS) between each LTC9102/LTC9103 AGND and V_{EE} are very important for reliable operation. If a short circuit occurs at one of the output ports it can take as long as 1µs for the LTC9102/LTC9103 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit; a high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC9101-1/LTC9102/LTC9103 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor and a SMAJ58A near each LTC9102/LTC9103 are recommended to minimize spurious resets. An electrolytic bulk capacitor of at least 47µF, 100V and a bulk TVS are also recommended per system.

LTC9102/LTC9103 Low Voltage Power Supplies

The LTC9102/LTC9103 includes internal voltage regulators that generate low voltage supplies directly from the main PoE power supply. At startup, an internal regulator generates 6V at PWRIN, drawing power from AGND. Internal 4.3V and 3.3V rails are sub-regulated from PWRIN. The PWRIN pin requires a local 1µF, 100V bypass capacitor.

Pull-up resistors can be connected from PWRIN to AGND to dissipate heat outside the LTC9102/LTC9103 package. Optionally, an external power supply can be connected to PWRIN to override the startup regulator and reduce power dissipation.

Figure 26 shows a pull-up resistor configuration with the internal 3.3V regulator. Bypass resistors R1, R2, R3, and R4 draw heat away from the LTC9102s/LTC9103s. Note that the voltage of the PWRIN pin changes based on the LTC9102/LTC9103 operating mode and its corresponding current consumption. If more current is consumed than the bypass resistors provide, the startup regulator maintains the voltage at 6V typical. The LTC9102 can operate without the pull-up resistors in space-constrained applications.

In applications with an external PWRIN supply, a 6.5V regulator provides an optimum voltage to override the internal 6V start-up regulator, while minimizing the LTC9102 device heating. The external supply may be shared across multiple LTC9102s/LTC9103s.

A 3.3V power supply can be connected directly to the CAP3 pin, as shown in Figure 27. This provides the most power efficient sleep mode. When supplying external 3.3V power, tie the EXT3 pin to CAP3. This will disable the internal 3.3V regulator and prevent power back-feed. The 3.3V regulator must power up within $t_{CAP3EXT}$ specified in the electrical characteristics table.

APPLICATIONS INFORMATION

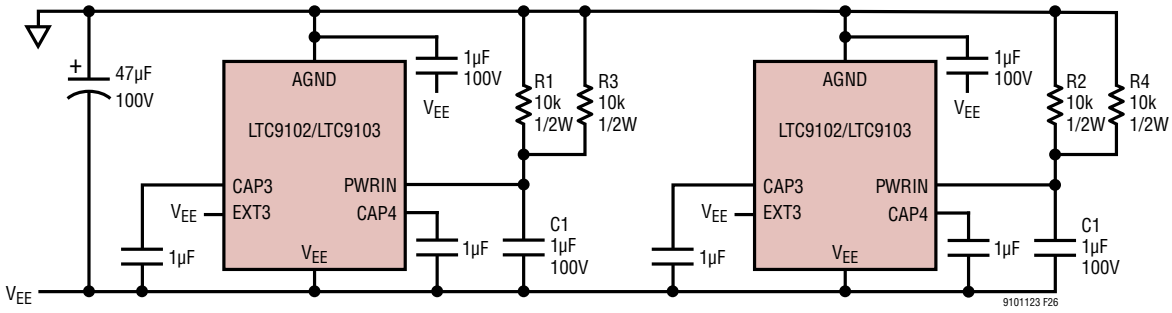


Figure 26. Power Supply Configuration with Internal 3.3V Supply

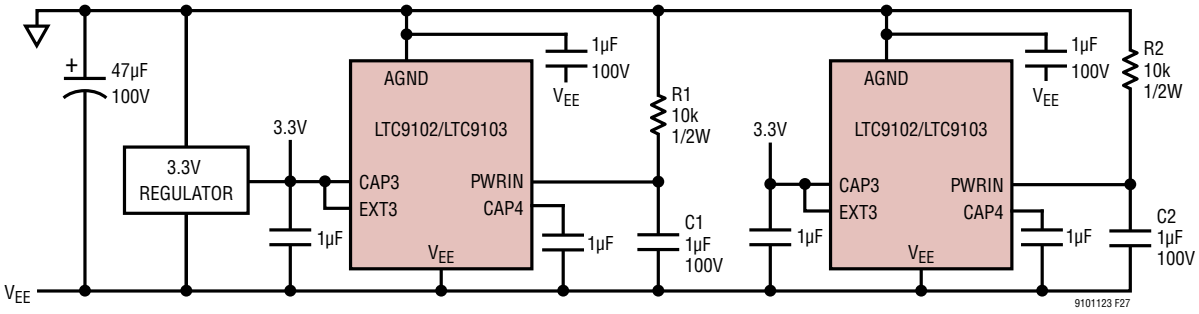


Figure 27. Power Supply Configuration with External 3.3V Regulators

If using the direct connection scheme, the 3.3V regulator that supplies the LTC9101-1 can also supply the LTC9102s/LTC9103s. This is the preferred option when the LTC9101-1 and LTC9102/LTC9103 are on the same side of the system isolation barrier.

High-Speed Data Isolation

The LTC9101-1/LTC9102/LTC9103 chipset can either provide proprietary isolation or rely on existing system isolation. Significant BOM cost reductions can be achieved using the proprietary isolation scheme.

In the proprietary isolation scheme, the LTC9101-1/LTC9102/LTC9103 chipset uses transformers to isolate the LTC9101-1 from one to four LTC9102s/LTC9103s (see Figure 28). In this case, the SDAIN and SDAOUT pins can be shorted to each other and tied directly to the I^2C/SMBus bus. The transformers should be 10BASE-T or 10/100BASE-T with a 1:1 turns ratio. Optimally, the selected transformers do not have common-mode chokes. These transformers typically provide 1500V of isolation between the LTC9101-1 and the LTC9102s/LTC9103s. For proper operation, strict layout guidelines must be met.

In the direct connection scheme, the LTC9101-1/LTC9102/LTC9103 chipset relies on pre-existing system isolation. In this scheme, the LTC9101-1 connects directly to one or more LTC9102s/LTC9103s using a proprietary communication protocol (see Figure 29).

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. Choosing a MOSFET requires extensive analysis and testing of the MOSFET SOA curve against the various PSE current limit conditions. ADI recommends the PSMN075-100MSE for PSEs configured to deliver up to 51W maximum port power (single-signature) or 25.5W maximum pairset power (dual-signature). For PSEs configured to power up to 71.3W maximum port power (single-signature) or 35.6W maximum pairset power (dual-signature), ADI recommends the PSMN040-100MSE. These MOSFETs are selected for their proven reliability in PoE applications. Contact ADI Applications before using a MOSFET other than one of these recommended parts.

APPLICATIONS INFORMATION

Sense Resistors

The LTC9101-1/LTC9102/LTC9103 is designed for a low 0.1Ω current sense resistance per channel, laid out as shown in the Layout Requirements section, Figure 31. In order to meet the $I_{HOLD-2P}$, I_{CUT-2P}, and I_{LIM-2P} accuracy required by the IEEE specification, the sense resistors should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient.

Port Output Cap

Each port requires a 0.1µF cap across OUTn to AGND (see Figure 30) to keep the LTC9102/LTC9103 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the LTC9102/LTC9103.

Surge Protection

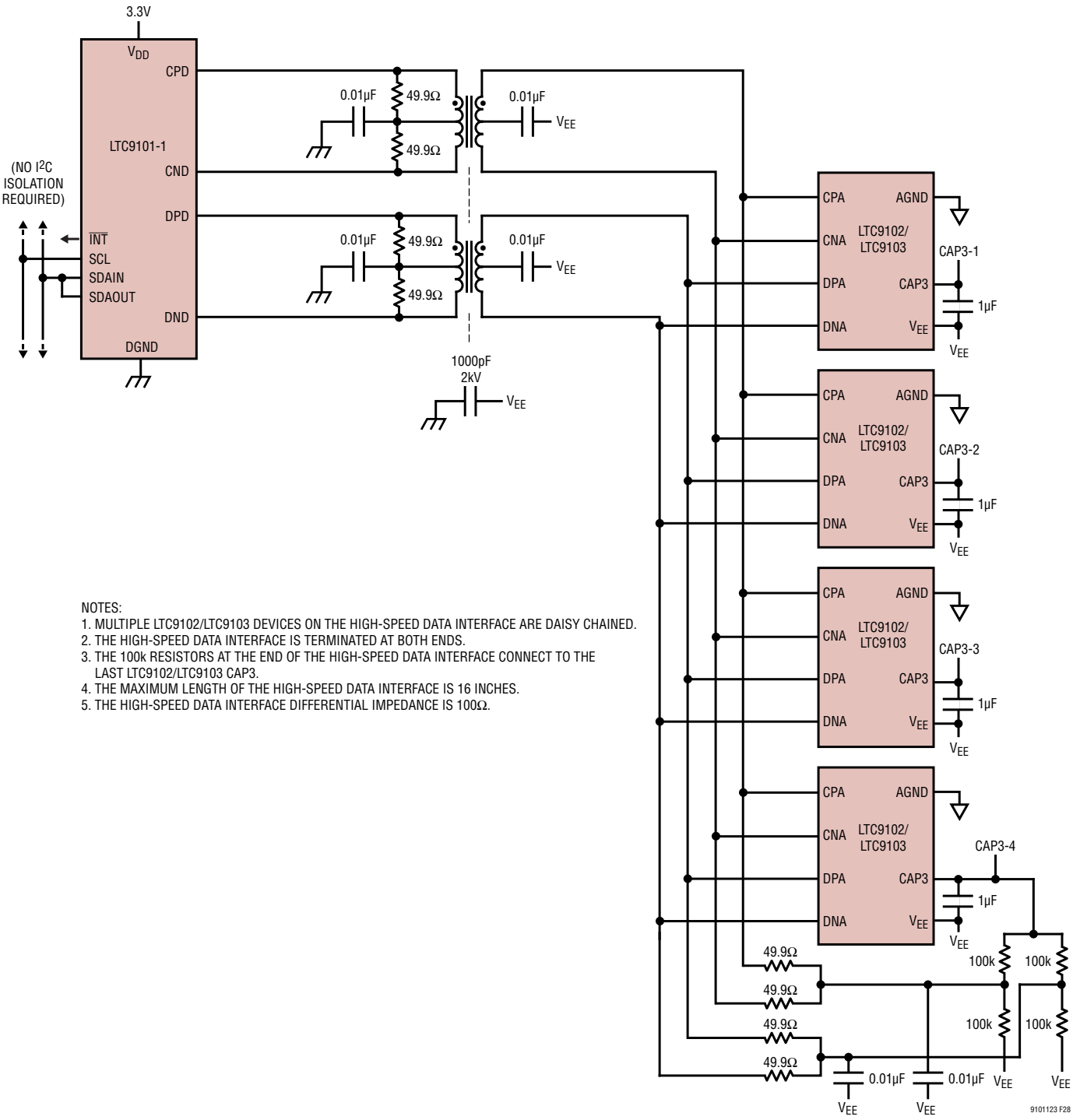
Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 30, are required at the main supply, at the LTC9102/LTC9103 supply pins, and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Across each LTC9102/LTC9103 AGND pin and V_{EE} pin is a SMAJ58A 58V TVS (D1) and a 1µF, 100V bypass capacitor (C1). These components must be placed close to the LTC9102/LTC9103 pins.

Each port requires an S1B clamp diode from OUTn to supply AGND. This diode steers harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

APPLICATIONS INFORMATION



NOTES:
1. MULTIPLE LTC9102/LTC9103 DEVICES ON THE HIGH-SPEED DATA INTERFACE ARE DAISY CHAINED.
2. THE HIGH-SPEED DATA INTERFACE IS TERMINATED AT BOTH ENDS.
3. THE 100k RESISTORS AT THE END OF THE HIGH-SPEED DATA INTERFACE CONNECT TO THE LAST LTC9102/LTC9103 CAP3.
4. THE MAXIMUM LENGTH OF THE HIGH-SPEED DATA INTERFACE IS 16 INCHES.
5. THE HIGH-SPEED DATA INTERFACE DIFFERENTIAL IMPEDANCE IS 100Ω.

Figure 28. LTC9101-1/LTC9102/LTC9103 Proprietary Isolation Scheme

APPLICATIONS INFORMATION

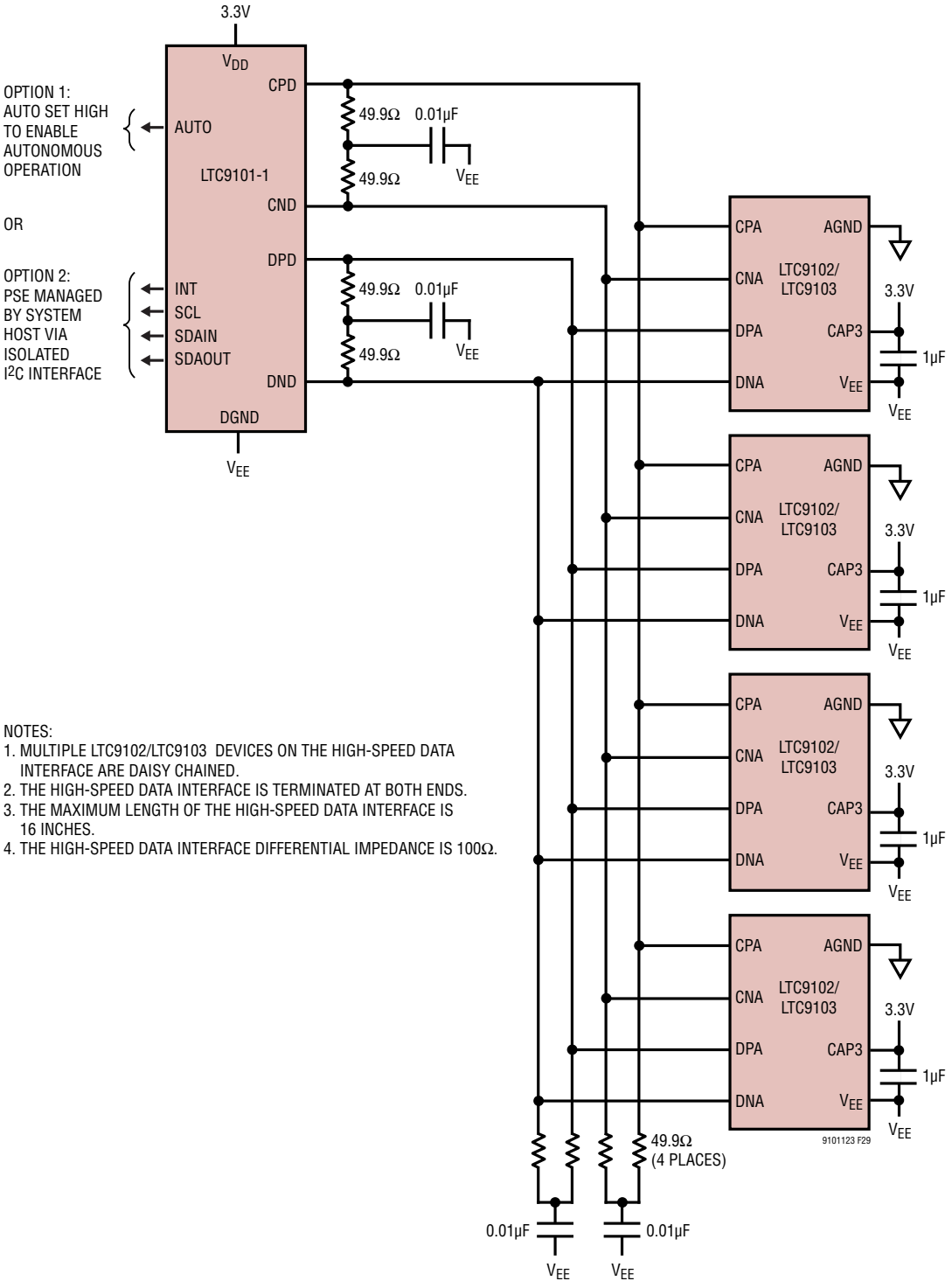


Figure 29. LTC9101-1/LTC9102/LTC9103 Proprietary Direct Connection Scheme

APPLICATIONS INFORMATION

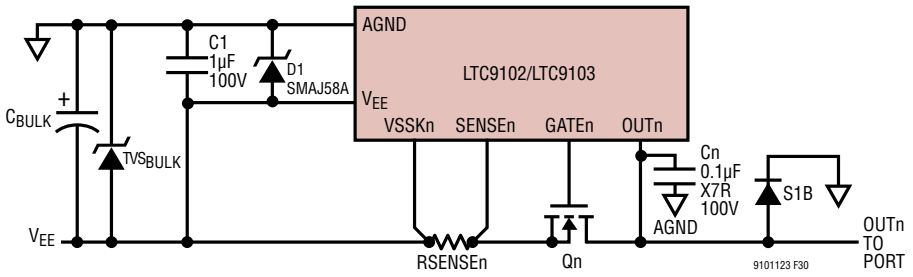


Figure 30. LTC9102/LTC9103 Surge Protection

Table 16. Component Selection for PSE Maximum Class

PSE CLASS	SENSE RESISTOR	HOT SWAP MOSFET	FUSE	ETHERNET TRANSFORMER
Class 3	100mΩ, 1%, 50mW	PSMN075-100MSE	SF-0603HI075F-2	7490220120
Class 4	100mΩ, 1%, 100mW	PSMN075-100MSE	SF-0603HI100F-2	7490220121
Class 6	100mΩ, 1%, 100mW	PSMN040-100MSE	SF-0603HI100F-2	7490220121
Class 8	100mΩ, 1%, 200mW	PSMN040-100MSE	SF-0603HI150F-2	7490220122

LAYOUT REQUIREMENTS

Strict adherence to board layout, parts placement and routing requirements is critical for IEEE compliance, parametric measurement accuracy, system robustness and thermal dissipation. Refer to the DC3160A-KIT demo kit for example layout references.

Kelvin Sense

Proper connection of the port current Kelvin sense lines is important for current threshold accuracy and IEEE compliance. Refer to Figure 31 for an example layout of these Kelvin sense lines. The LTC9102/LTC9103 VSSKn pin is Kelvin connected to the sense resistor (V_{EE} side) pad and is not otherwise connected to V_{EE} copper areas. Similarly, the LTC9102/LTC9103 SENSEn pin is Kelvin connected to the sense resistor (SENSEn side) pad and is not otherwise connected in the power path. Figure 31 shows the two Kelvin traces from the LTC9102/LTC9103 to the sense resistor (R_{SENSEn}).

High-Speed Data Interface

The LTC9101-1/LTC9102/LTC9103 chipset communicates across a proprietary high-speed, multi-drop data interface. This allows for a single LTC9101-1 to control up to four LTC9102s/LTC9103s.

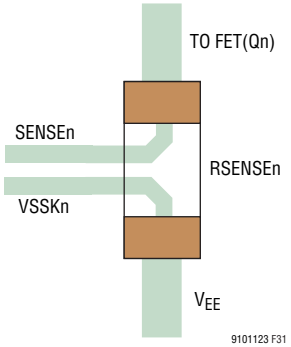


Figure 31. R_{SENSE} Kelvin Connections

The data-lines require impedance matched traces to each LTC9102/LTC9103. The data bus termination resistors must be located at the LTC9102/LTC9103 farthest away from the isolation transformers. For isolated applications, the DC biasing resistors must connect to the LTC9102/LTC9103 CAP3 pin, farthest away from the isolation transformers. As shown in Figure 28 and Figure 29, design the interface with 100Ω differential transmission lines, and terminate 100Ωs differentially. Limit the high-speed data interface line length to 16 inches. Minimize the transmission stubs between the LTC9102s/LTC9103s and the high-speed data interface.

TYPICAL APPLICATIONS

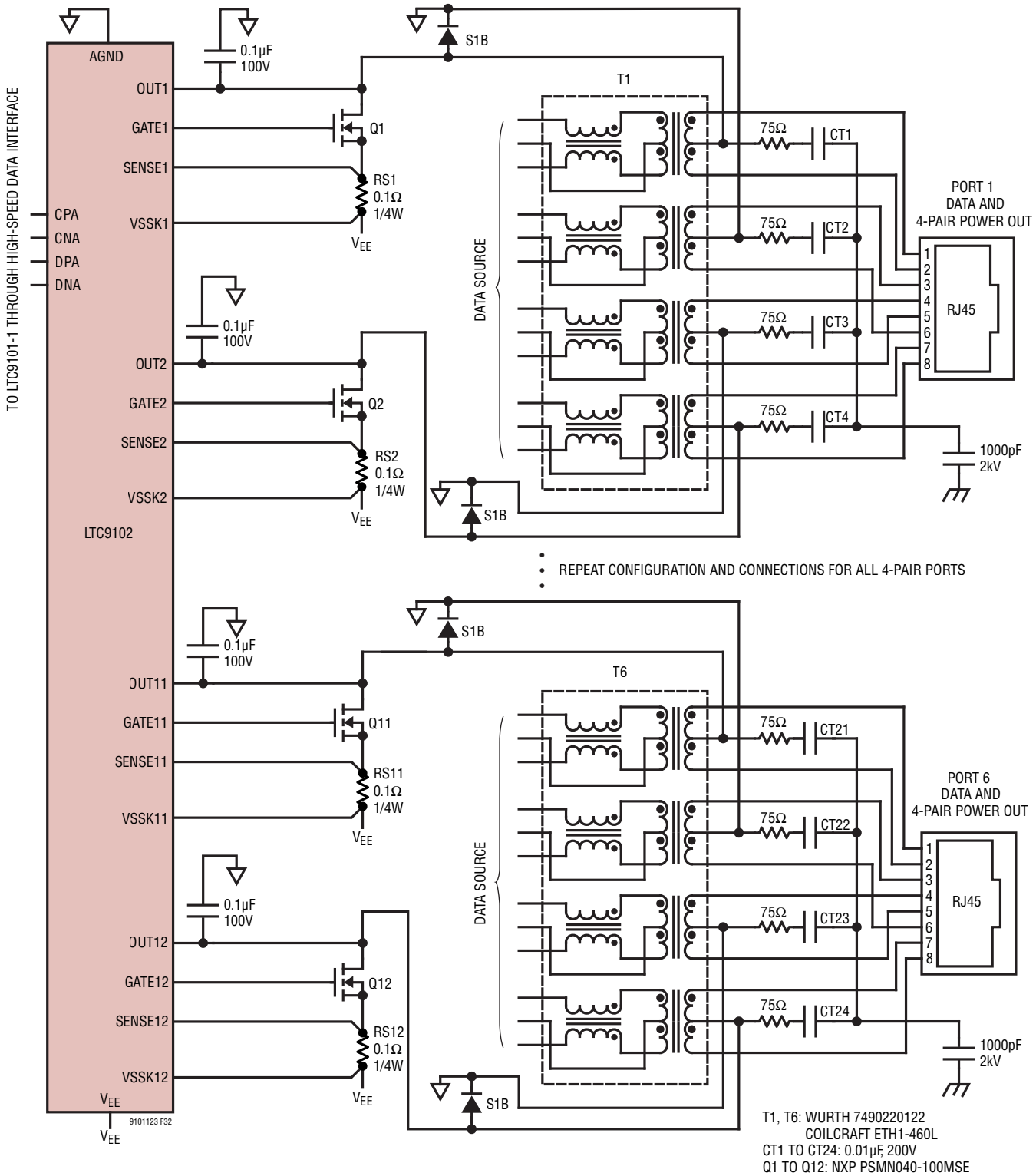


Figure 32. Alternative A (MDI-X) and B (S), 4-Pair, 1000BASE-T, IEEE 802.3bt, Type 3 or Type 4 PSE, Ports 1 and 6 Shown

TYPICAL APPLICATIONS

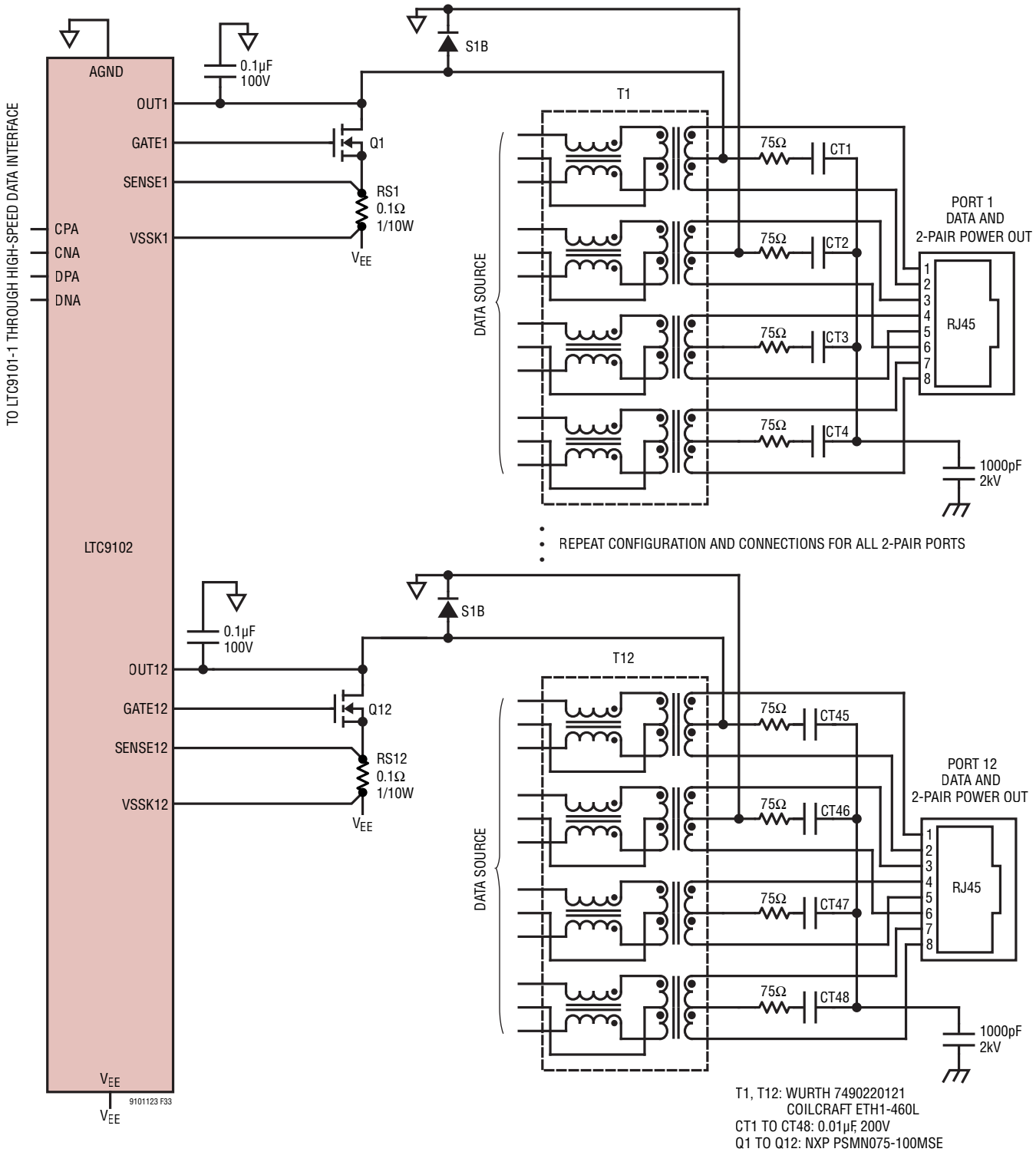


Figure 33. Alternative A (MDI-X), 2-Pair, 1000BASE-T, IEEE 802.3bt or IEEE 802.3at PSE, Ports 1 and 12 Shown

TYPICAL APPLICATIONS

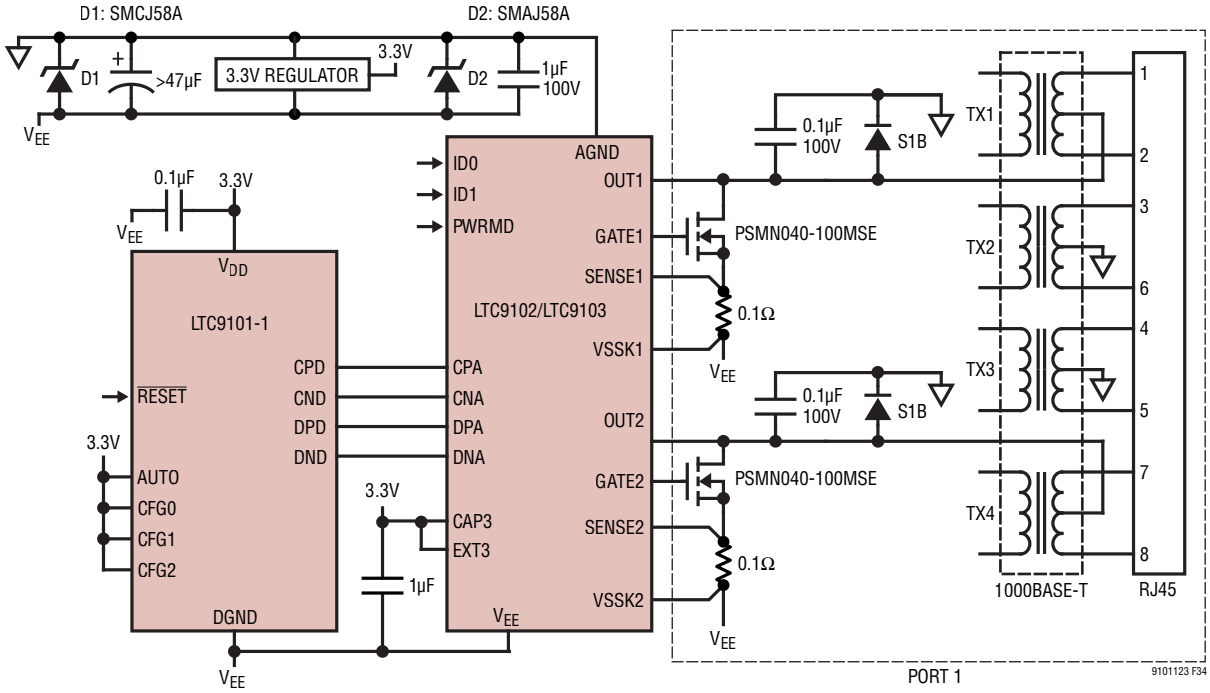
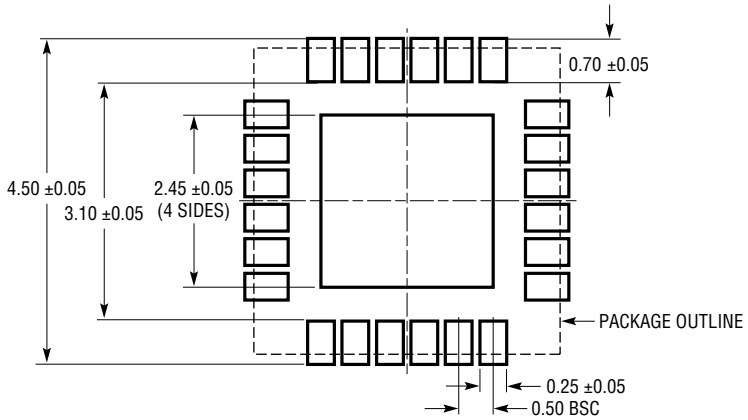


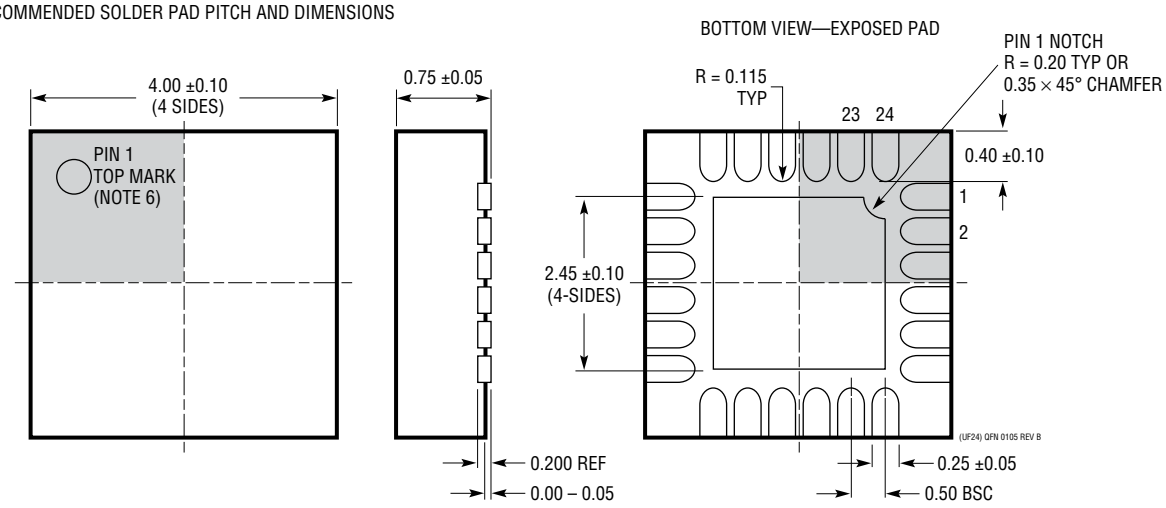
Figure 34. Autonomous IEEE 802.3bt 4-Pair PSE, Type 3 or Type 4, Alternative A (MDI-X) and B(S), 1000BASE-T, 1 Port Shown

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



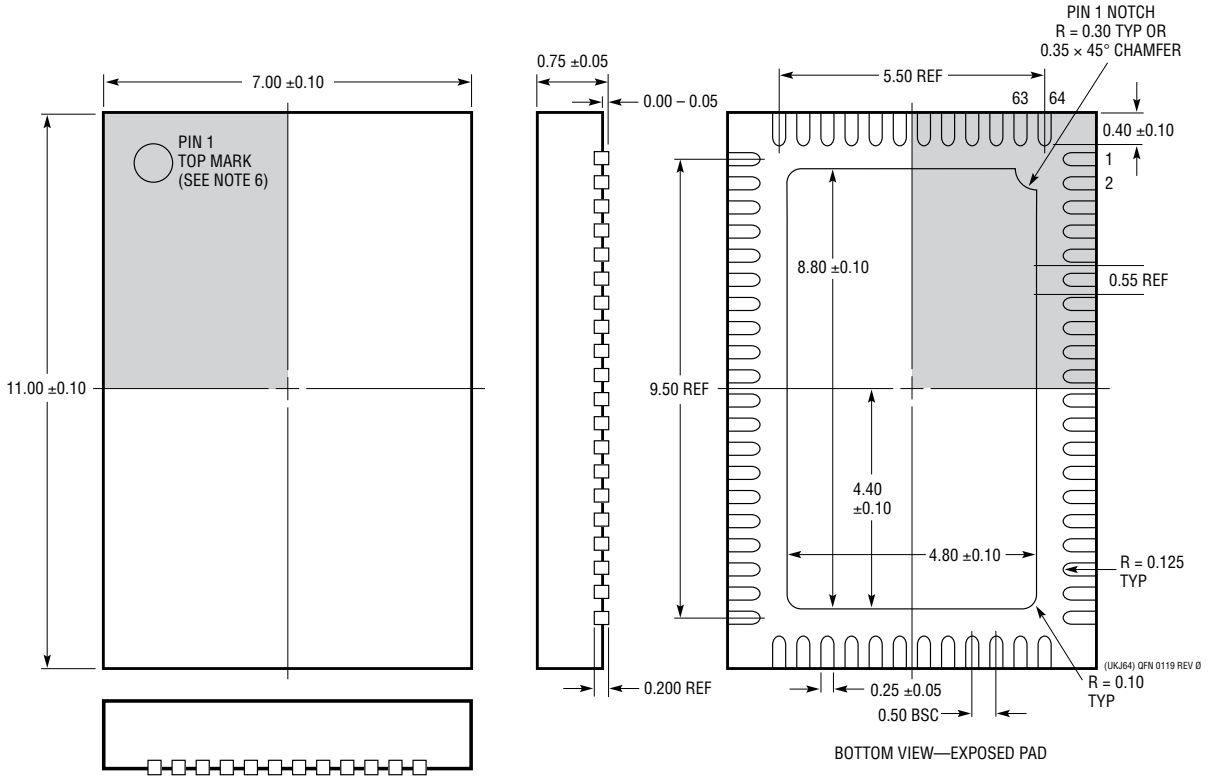
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



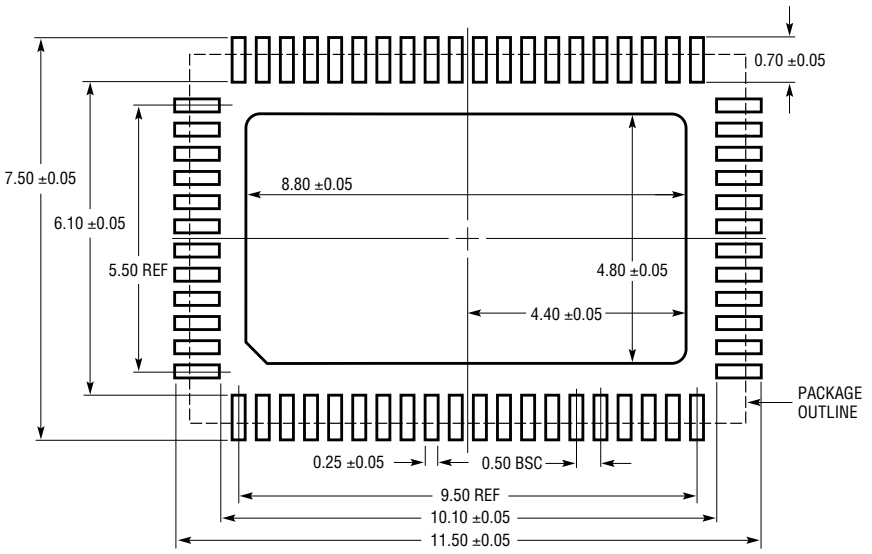
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

UKJ Package
64-Lead Plastic QFN (7mm × 11mm)
(Reference LTC DWG # 05-08-1780 Rev 0)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Rev. 0