

7.5kV_{RMS} SPI/Digital or I²C μModule Isolator with Transformer Driver

FEATURES

- 6-Channel Logic Isolator: 7500V_{RMS} for 1 Minute
- 16.2mm Creepage
- CSA (IEC/UL) Approved, File #255632
- 3V to 5.5V Supply Operation
- Transformer Driver with Integrated Isolated Side LDO
- SPI/Digital (LTM2810-S) or I²C (LTM2810-I) Options
- High Common Mode Transient Immunity: 50kV/μs
- High Speed Operation:
 - 10MHz Digital Isolation
 - 4MHz/8MHz SPI Isolation
 - 400kHz I²C Isolation
- Operation Up to 125°C (H-Grade)
- 1.62V to 5.5V Logic Supplies for Flexible Digital Interfacing
- ±25kV ESD HBM Across the Isolation Barrier
- Maximum Continuous Working Voltage: 1kV_{RMS}, 1.6kV_{DC}
- Low Current Shutdown Mode (<10μA)
- 22mm × 6.25mm × 2.06mm BGA Package

APPLICATIONS

- EV/HEV Systems
- Industrial and Metering Systems
- Test and Measurement Equipment
- Medical Equipment

DESCRIPTION

The LTM[®]2810 is a complete galvanic digital μModule[®] (micromodule) isolator. No external components are required. Individual 3V to 5.5V supplies power each side of the digital isolator. Separate logic supply pins allow easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

Module options are available with compatibility to SPI (LTM2810-S) and I²C (LTM2810-I), master mode only, specifications.

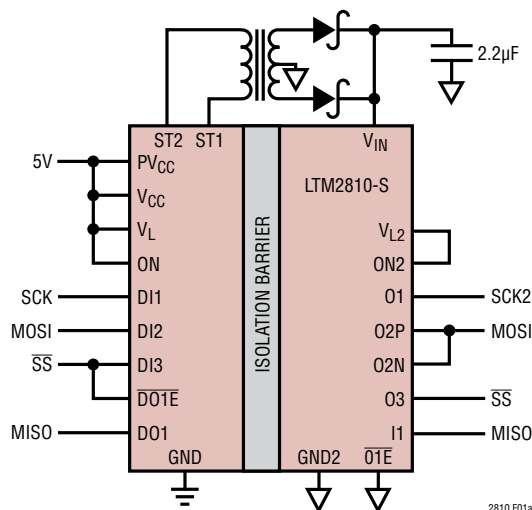
The module includes an integrated transformer driver on the logic side and an LDO on the isolated side to regulate the rectified transformer output. The LDO output is nominally 5V but may be overdriven.

Coupled inductors provide 7500V_{RMS} of isolation between the input and output logic interface. This device is ideal for systems with different ground potentials, allowing uninterrupted communication through large common mode transients faster than 50kV/μs.

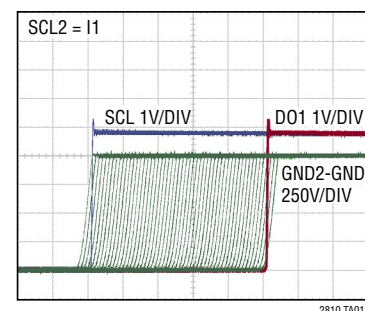
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TYPICAL APPLICATION

Isolated 4MHz SPI Interface



LTM2810-I Operating Through 70kV/μs CM Transients



LTM2810

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages

PV_{CC} to GND	-0.3V to 6V
V_{CC} to GND	-0.3V to 6V
V_L to GND	-0.3V to 6V

Isolated Supply Voltages

V_{IN} to GND2	-0.3V to 45V
V_{L2} to GND2	-0.3V to 6V

Logic Signals

DI1, DI2, DI3, DO1, $\overline{DO1E}$, DO2P, DO3, ON, SCL, ST1, ST2	GND - 0.3V to $V_L + 0.3V$
DO2N, SDA	GND - 0.3V to 6.3V

Isolated Signals

AV_{L2} , I1, I2, I3, O1, $\overline{O1E}$, O2P, O3, ON2, SCL2, SDA2	GND2 - 0.3V to $V_{L2} + 0.3V$
O2N	GND2 - 0.3V to 6.3V

Operating Temperature Range (Note 4)

LTM2810C	0°C to 70°C
LTM2810I	-40°C to 85°C
LTM2810H	-40°C to 125°C

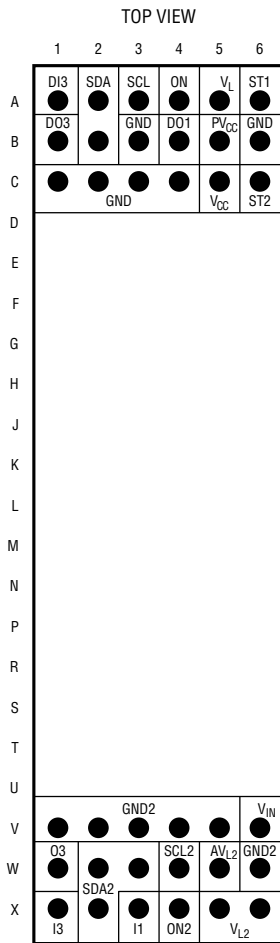
Maximum Internal Operating Temperature..... 125°C

Storage Temperature Range

Peak Body Reflow Temperature

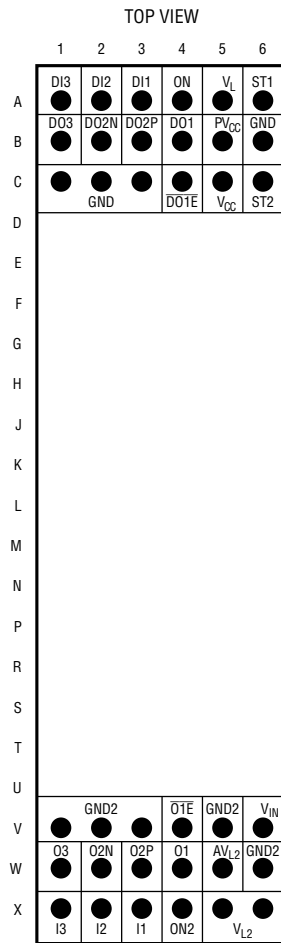
PIN CONFIGURATION

LTM2810-I



BGA PACKAGE
36-PIN (22mm × 6.25mm × 2.06mm)
 $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 49.6^{\circ}C/W$, $\theta_{JCBOTOM} = 34^{\circ}C/W$,
 $\theta_{JCTOP} = 26^{\circ}C/W$, $\theta_{JB} = 33.7^{\circ}C/W$
 θ VALUES DETERMINED PER JESD51-9, WEIGHT = 0.5g

LTM2810-S



BGA PACKAGE
36-PIN (22mm × 6.25mm × 2.06mm)
 $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 49.6^{\circ}C/W$, $\theta_{JCBOTOM} = 34^{\circ}C/W$,
 $\theta_{JCTOP} = 26^{\circ}C/W$, $\theta_{JB} = 33.7^{\circ}C/W$
 θ VALUES DETERMINED PER JESD51-9, WEIGHT = 0.5g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM2810CY-I#PBF	LTM2810CY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	0°C to 70°C
LTM2810IY-I#PBF	LTM2810IY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	-40°C to 85°C
LTM2810HY-I#PBF	LTM2810HY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	-40°C to 125°C
LTM2810CY-S#PBF	LTM2810CY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	0°C to 70°C
LTM2810IY-S#PBF	LTM2810IY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	-40°C to 85°C
LTM2810HY-S#PBF	LTM2810HY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	-40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to [Recommended BGA PCB Assembly and Manufacturing Procedures](#).

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $PV_{CC} = V_{CC} = 5\text{V}$, $V_L = V_{L2} = 3.3\text{V}$, $V_{IN} = \text{GND} = \text{GND2} = 0\text{V}$, $\text{ON} = V_L$, and $\text{ON2} = V_{L2}$ unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Supplies							
	Operating Voltage Range	V_{CC} , PV_{CC} , V_L (LTM2810-I), V_{L2} V_L (LTM2810-S) V_{IN}	● ● ●	3.0 1.62 3.6	5.5 5.5 38	V V V	
V_{L2}	Output Variation (Note 7)	$V_{L2} + 1\text{V} \leq V_{IN} \leq 38\text{V}$, $I_{LOAD} = 0$ to 100mA	●	-0.2	0.2	V	
AV_{L2}	Adjust Pin Voltage (Note 7)	$V_{L2} + 1\text{V} \leq V_{IN} \leq 38\text{V}$, $I_{LOAD} = 0$ to 100mA	●	580	600	620	mV
	Supply Current	I_{CC} , PI_{CC} , I_L , $\text{ON} = \text{ON2} = 0\text{V}$ I_{VIN} , $V_{IN} = 6\text{V}$, $\text{ON2} = 0\text{V}$ I_{CC} , PI_{CC} I_{VIN} , $V_{IN} = 5\text{V}$, V_{L2} Adjusted to 3V I_L (LTM2810-S) I_L (LTM2810-I)	● ● ● ● ●	0 40 3.2 3.6	10 80 5 6	μA μA mA mA	
	V_{L2} Current Limit	$V_{IN} = 7\text{V}$, $V_{L2} = 0\text{V}$ $V_{IN} = V_{L2(\text{NOMINAL})} + 1\text{V}$, $\Delta V_{L2} = -5\%$	●	110	200	mA mA	
	ST1, ST2 Output Current	(Note 2)		400		mA	
Logic – DI1, DI2, DI3, DO1, $\overline{\text{DO1E}}$, DO2N, DO2P, DO3, I1, I2, I3, O1, $\overline{\text{O1E}}$, O2N, O2P, O3, ON, ON2 ($V_L = V_L$ or V_{L2})							
V_{ITH}	Input Threshold Voltage	$1.62\text{V} \leq V_L < 2.35$	●	$0.25 \cdot V_L$	$0.75 \cdot V_L$	V	
		$2.35\text{V} \leq V_L$	●	$0.33 \cdot V_L$	$0.67 \cdot V_L$	V	
I_{IN}	Input Current		●	0	± 5	μA	
V_O	Output Voltage	$I_{LOAD} = 1\text{mA}$, $1.62\text{V} \leq V_L < 3\text{V}$ $I_{LOAD} = 4\text{mA}$, $3\text{V} \leq V_L$ DO1 (LTM2810-I), $I_{LOAD} = 2\text{mA}$, $3\text{V} \leq V_L$ DO2N, $I_{LOAD} = 1\text{mA}$, $1.62\text{V} \leq V_L < 3\text{V}$ DO2N, O2N, $I_{LOAD} = 4\text{mA}$, $3\text{V} \leq V_L$ DO2P, $I_{LOAD} = 1\text{mA}$, $1.62\text{V} \leq V_L < 3\text{V}$ DO2P, O2P, $I_{LOAD} = 4\text{mA}$, $3\text{V} \leq V_L$	● ● ● ● ● ● ●	0.4 0.4 0.4 0.4 0.4	$V_L - 0.4$ $V_L - 0.4$ $V_L - 0.4$ $V_L - 0.4$ $V_L - 0.4$ $V_L - 0.4$	V V V V V V V	
	Output High Resistance	(Note 3)		40		Ω	
	Output Low Resistance	(Note 3)		40		Ω	

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I²C – SCL, SCL2, SDA, SDA2 (LTM2810-I) ($V_L = V_L$ or V_{L2})						
V_{ITH}	Input Threshold Voltage	$3\text{V} \leq V_L \leq 5.5\text{V}$	●	$0.3 \cdot V_L$	$0.7 \cdot V_L$	V
V_{HYS}	Input Hysteresis	$3\text{V} \leq V_L \leq 5.5\text{V}$		$0.05 \cdot V_L$		V
I_{IN}	Input Current		●	0	±5	μA
V_{O}	Output Voltage	SCL2, $I_{\text{LOAD}} = 2\text{mA}$, $3\text{V} \leq V_L \leq 5.5\text{V}$	●	0.4	$V_L - 0.4$	V
V_{OL}	Output Low Voltage	SDA, $I_{\text{LOAD}} = 3\text{mA}$	●		0.4	V
		SDA2 = No Load, SDA = 0V, $4.5\text{V} \leq V_L < 5.5\text{V}$	●		0.45	V
		SDA2 = No Load, SDA = 0V, $3\text{V} \leq V_L < 4.5\text{V}$	●	0.3	0.55	V
	SDA, SDA2 Slew Rate		●	1		V/μs
I_{SC}	Short-Circuit Current	SDA2 = 0, SDA = V_L	●		100	mA
		$0\text{V} \leq \text{SCL2} \leq V_L$		±30		mA
		SDA = 0, SDA2 = V_L		6		mA
		SDA = V_L , SDA2 = 0		-1.8		mA
ESD (HBM) (Note 2)						
	Isolation Boundary	(V_{IN} , V_{L2} , GND2) to (PV_{CC} , V_{CC} , V_L , GND) in Any Combination		±25		kV

SWITCHING CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $PV_{CC} = V_{CC} = 5\text{V}$, $V_L = V_{L2} = 3.3\text{V}$, $V_{IN} = \text{GND} = \text{GND2} = 0\text{V}$, $\text{ON} = V_L$, and $\text{ON2} = V_{L2}$ unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Driver – ST1, ST2							
	Drive Frequency			2		MHz	
	Duty Cycle		49	50	51	%	
Power Supply Generator							
	V_{L2} Supply Start-Up Time	$V_{\text{IN}} \uparrow$ to $V_{L2} > 4.75\text{V}$		50		ms	
Logic Timing							
	Maximum Data Rate	Input → Output, $C_L = 15\text{pF}$ (Note 3) Bidirectional SPI Communication Unidirectional SPI Communication	● ● ●	10 4 8		MHz MHz MHz	
t_{PHL} , t_{PLH}	Propagation Delay	Input → Output, $C_L = 15\text{pF}$ (Figure 1)	●	30	45	100	ns
t_{PZH} , t_{PZL}	DO1, O1 Enable Time (Figure 2)	$\overline{\text{xO1E}} = \downarrow$ to xO1 High, $R_{\text{PD}} = 1\text{k}\Omega$, xI1 = High	●			50	ns
	ONx Enable Time (Figure 4)	ONx = \uparrow to xOx High, $R_{\text{PD}} = 1\text{k}\Omega$, xI1 = High	●			60	μs
t_{PHZ} , t_{PLZ}	DO1, O1 Disable Time (Figure 2)	$\overline{\text{xO1E}} = \uparrow$ to xO1 Low, $R_{\text{PD}} = 1\text{k}\Omega$, xI1 = High	●			50	ns
	ONx Disable Time (Figure 4)	ONx = \downarrow to xOx Low, $R_{\text{PD}} = 1\text{k}\Omega$, xI1 = High	●			100	ns
I²C Timing							
	Maximum Data Rate	(Note 3)	●	400		kHz	
t_{PHL} , t_{PLH}	Propagation Delay (Figure 3)	SCL → SCL2	●		150	250	ns
		SDA → SDA2	●		150	300	ns
		SDA2 → SDA, $R_{\text{PU}} = 1\text{k}\Omega$	●		300	500	ns
t_{R}	Rise Time (30% to 70%) (Figure 3)	SDA2, $C_L = 200\text{pF}$	●	40		350	ns
		SDA, $R_{\text{PU}} = 1\text{k}\Omega$, $C_L = 200\text{pF}$	●	40		350	ns
		SCL2, $C_L = 200\text{pF}$	●			250	ns
t_{F}	Fall Time (70% to 30%) (Figure 3)	SDA2, $C_L = 200\text{pF}$	●	40		250	ns
		SDA, $R_{\text{PU}} = 1\text{k}\Omega$, $C_L = 200\text{pF}$	●	40		250	ns
		SCL2, $C_L = 200\text{pF}$	●			250	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PZH} , t_{PZL}	ONx Enable Time	ON = \uparrow to SDA Low, $R_{PU} = 1\text{k}\Omega$, SDA2 = 0V	●		60	μs
		ON2 = \uparrow to (SCL2, SDA2) Low, (SCL, SDA) = 0V	●		60	μs
t_{PHZ} , t_{PLZ}	ONx Disable Time	ON = \downarrow to SDA High, $R_{PU} = 1\text{k}\Omega$, SDA2 = 0V	●		80	ns
		ON2 = \downarrow to SCL2 High, SCL = 0V	●		80	ns
		ON2 = \downarrow to SDA2 High, SDA = 0V	●		225	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0	50	ns

ISOLATION CHARACTERISTICS $T_A = 25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test	7500			V_{RMS}
		1 Second (Notes 5, 6)	9000			V_{RMS}
	Common Mode Transient Immunity	$PV_{CC} = V_{CC} = V_L = \text{ON} = 5\text{V}$, $V_{L2} = \text{ON2} = 5\text{V}$ $V_{CM} = 1\text{KV}$, $\Delta t = 20\text{ns}$ (Note 2)	50	75		$\text{kV}/\mu\text{s}$
V_{IORM}	Maximum Continuous Working Voltage	(Notes 2, 5)	1600			V_{DC}
			1000			V_{RMS}
	Partial Discharge	$V_{PD} = 2650V_{PEAK}$ (Note 5)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2), Material Group I	600			V_{RMS}
		Depth of Erosion		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.2		mm
		Input to Output Resistance	(Notes 2, 5)	1	5	$\text{T}\Omega$
	Input to Output Capacitance	(Notes 2, 5)		2		pF
	Creepage Distance	(Note 2)		16.2		mm

REGULATORY INFORMATION

CSA (Note 8)

CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1 +A2:

Basic Insulation at $1600V_{RMS}$

Reinforced Insulation at $800V_{RMS}$

CSA 62368-1-14 and IEC 62368-1-14:2014, second edition:

Basic Insulation at $1600V_{RMS}$

Reinforced Insulation at $800V_{RMS}$

CSA 60601-1:14 and IEC 60601-1, third edition, +A1:

Two means of patient protection (2 MOPP) at $500V_{RMS}$

UL 1577-2015:

Single Protection, $7500V_{RMS}$ Isolation Voltage

File 255632

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Guaranteed by other measured parameters and is not tested directly.

Note 4: This μ Module isolator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 5: Device is considered a 2-terminal device. Pin group A1 through C6 shorted together and pin group V1 through X6 shorted together.

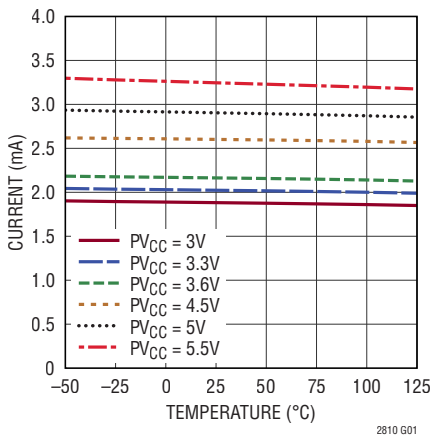
Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 7: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at the maximum input-to-output voltage differential. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback will limit the maximum output current as a function of input-to-output voltage.

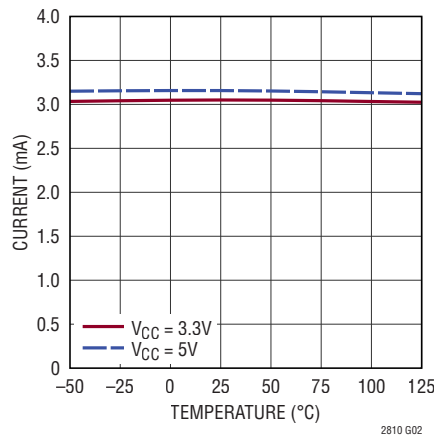
Note 8: Ratings are for pollution degree 2, material group 3 and overvoltage category II where applicable. Ratings for other environmental and electrical conditions to be determined from the appropriate safety standard.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $PV_{CC} = V_{CC} = 5\text{V}$, $V_L = V_{L2} = 3.3\text{V}$, $GND = GND2 = 0\text{V}$, $ON = V_L$, and $ON2 = V_{L2}$, unless otherwise noted.

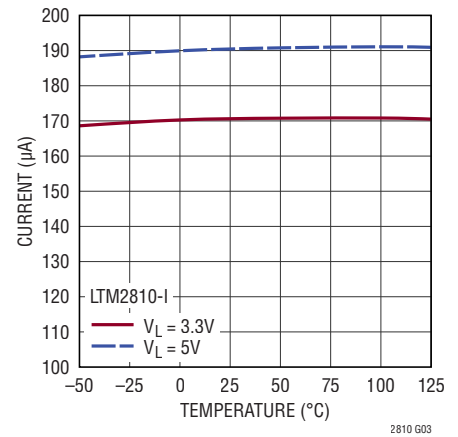
PV_{CC} Supply Current vs Temperature



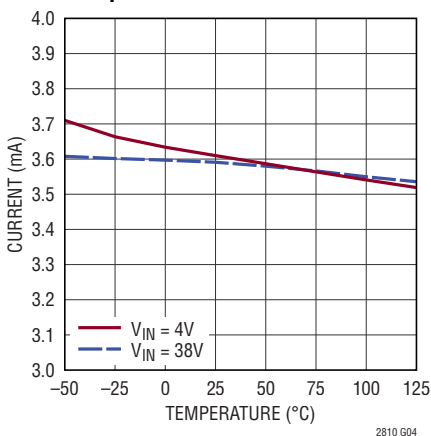
V_{CC} Supply Current vs Temperature



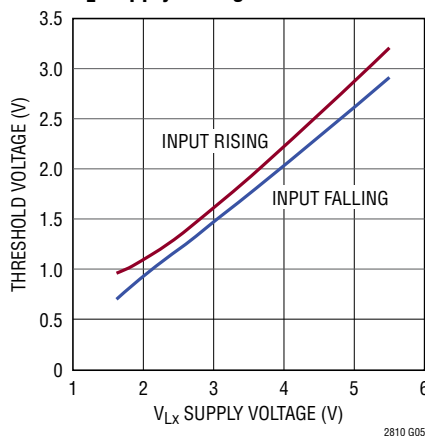
V_L Supply Current vs Temperature



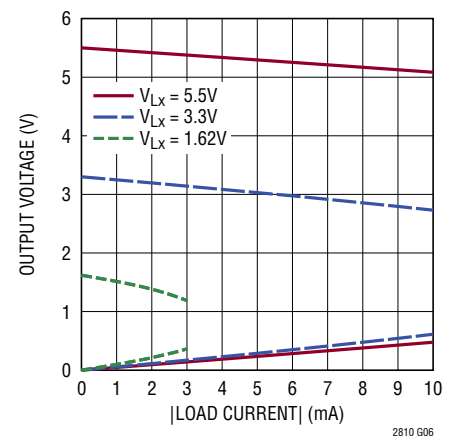
V_{IN} Supply Current vs Temperature



Logic Input Threshold vs V_L Supply Voltage



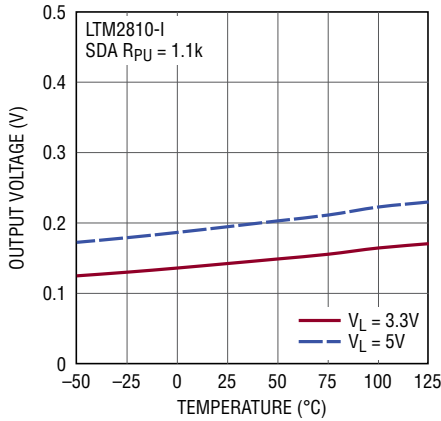
Logic Output Voltage vs Load Current



TYPICAL PERFORMANCE CHARACTERISTICS

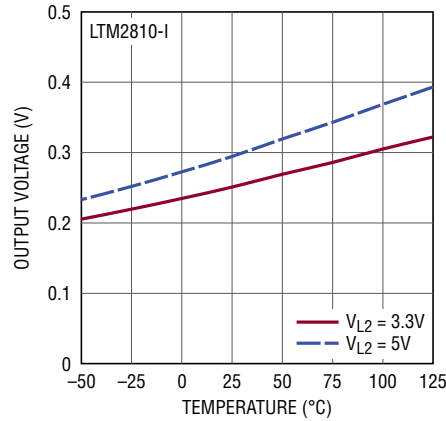
$T_A = 25^\circ\text{C}$, $PV_{CC} = V_{CC} = 5\text{V}$, $V_L = V_{L2} = 3.3\text{V}$,
 $GND = GND2 = 0\text{V}$, $ON = V_L$, and $ON2 = V_{L2}$, unless otherwise noted.

SDA Low Level Output Voltage vs Temperature



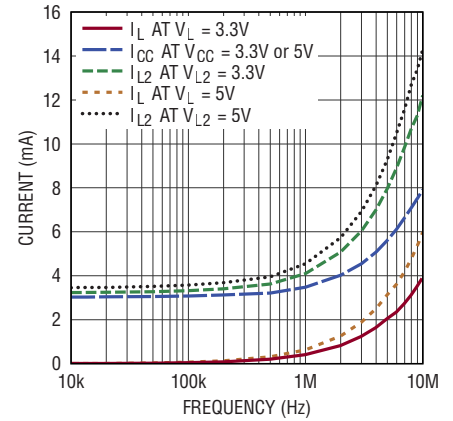
2810 G07

SDA2 Low Level Output Voltage vs Temperature



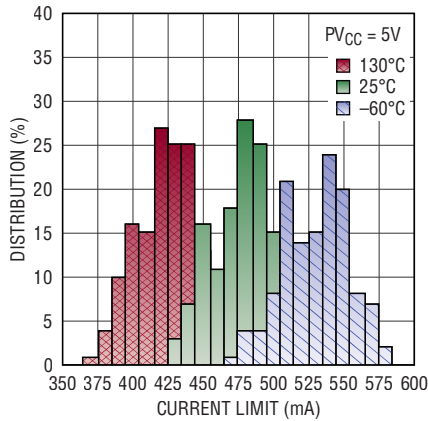
2810 G08

Supply Current vs Data Rate, All Channels



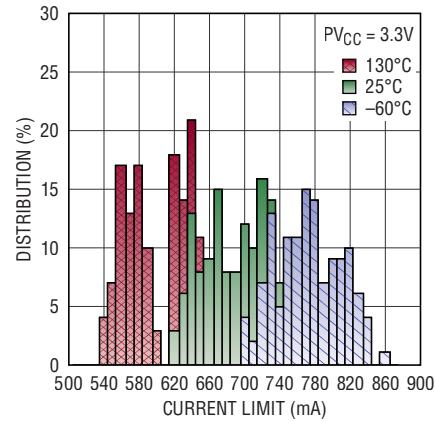
2810 G09

ST1 and ST2 Current Limit vs Temperature Histogram



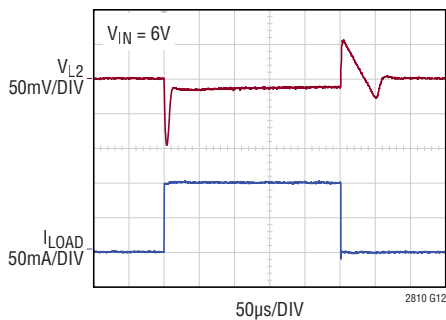
2810 G10

ST1 and ST2 Current Limit vs Temperature Histogram



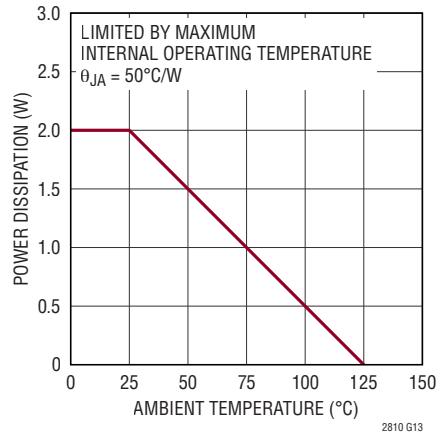
2810 G11

V_{L2} Transient Response



2810 G12

Thermal Derating



2810 G13

PIN FUNCTIONS

LTM2810-S, Logic Side

DI3 (A1): Digital Input, Referenced to V_L and GND. Logic input connected to O3 through the isolation barrier. The logic state on DI3 translates to the same logic state on O3. Connect to GND or V_L if not used.

DI2 (A2): Digital Input, Referenced to V_L and GND. Logic input connected to O2N and O2P through the isolation barrier. The logic state on DI2 translates to the same logic state on O2N and O2P. Connect to GND or V_L if not used.

DI1 (A3): Digital Input, Referenced to V_L and GND. Logic input connected to O1 through the isolation barrier. The logic state on DI1 translates to the same logic state on O1. Connect to GND or V_L if not used.

ON (A4): Enable, Referenced to V_L and GND. Enables data communication through the isolation barrier. If ON is high the part is enabled and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_L if not driven.

V_L (A5): Logic Supply. Interface supply voltage for pins DI1, DI2, DI3, DO1, DO2P, DO3, $\overline{DO1E}$, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed with 1 μ F.

ST1, ST2 (A6, C6): Bridge Driver Outputs, Referenced to PV_{CC} and GND. Each output runs at 50% duty cycle, ST1 is 180 degrees out of phase with ST2. Operating frequency is 2MHz. Bridge driver is enabled when PV_{CC} is between 3V to 5.5V and ON is high.

DO3 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I3 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO2N (B2): Open Drain Pull-Down Output to GND. Logic output connected to I2 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO2P (B3): Open Drain Pull-Up Output to V_L . Logic output connected to I2 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO1 (B4): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

PV_{CC} (B5): Bridge Driver Supply Voltage. Operating voltage is 3V to 5.5V, connect to GND to disable bridge driver. Internally bypassed with 2.2 μ F.

$\overline{DO1E}$ (C4): Digital Output Enable, Referenced to V_L and GND. A logic high on $\overline{DO1E}$ places the logic side DO1 pin in a high impedance state, a logic low enables the output. Connect to GND or V_L if not used.

V_{CC} (C5): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1 μ F.

GND (B6, C1 to C3): Circuit Ground.

LTM2810-S, Isolated Side

$\overline{O1E}$ (V4): Digital Output Enable, Referenced to V_{L2} and GND2. A logic high on $\overline{O1E}$ places the isolated side O1 pin in a high impedance state, a logic low enables the output. Connect to GND2 or V_{L2} if not used.

V_{IN} (V6): Internal LDO Input Voltage. Operating voltage is 3.6V to 38V. Internally bypassed with 0.1 μ F.

O3 (W1): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI3 through the isolation barrier. Under the condition of an isolation communication failure O3 defaults to a high state.

O2N (W2): Open Drain Pull-Down Output to GND2. Logic output connected to DI2 through the isolation barrier. Under the condition of an isolation communication failure O2N defaults to a low state.

O2P (W3): Open Drain Pull-Up Output to V_{L2} . Logic output connected to DI2 through the isolation barrier. Under the condition of an isolation communication failure O2P defaults to a low state.

O1 (W4): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI1 through the isolation barrier. Under the condition of an isolation communication failure O1 defaults to a low state.

AV_{L2} (W5): V_{L2} LDO Adjust Pin.

PIN FUNCTIONS

I3 (X1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO3 through the isolation barrier. The logic state on I3 translates to the same logic state on DO3. Connect to GND2 or V_{L2} if not used.

I2 (X2): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO2N and DO2P through the isolation barrier. The logic state on I2 translates to the same logic state on DO2N and DO2P. Connect to GND2 or V_{L2} if not used.

I1 (X3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO1 through the isolation barrier. The logic state on I1 translates to the same logic state on DO1. Connect to GND2 or V_{L2} if not used.

ON2 (X4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, O1, O2N and O2P are in a low state, and O3 is in a high state. Connect to V_{L2} if not driven.

V_{L2} (X5, X6): Logic Supply, Referred to GND2. Interface supply voltage for pins O1, O2P, O3, I1, I2, I3, $\overline{O1E}$, and ON2. Operating voltage is 3V to 5.5V. Internally bypassed with 6.6 μ F.

GND2 (V1 to V3, V5, W6): Isolated Ground.

LTM2810-I, Logic Side

DI3 (A1): Digital Input, Referenced to V_L and GND. Logic input connected to O3 through the isolation barrier. The logic state on DI3 translates to the same logic state on O3. Connect to GND or V_L if not used.

SDA (A2, B2): Serial I²C Data Pins, Referenced to V_L and GND. Bidirectional logic pins connected to isolated side SDA2 pins through the isolation barrier. Under the condition of an isolation communication failure pins are in a high impedance state. Pull up to V_L if not used.

SCL (A3): Serial I²C Clock Input, Referenced to V_L and GND. Logic input connected to isolated side SCL2 pin through the isolation barrier. Clock is unidirectional from logic to isolated side. Pull up to V_L if not used.

ON (A4): Enable, Referenced to V_L and GND. Enables data communication through the isolation barrier. If ON is high the part is enabled and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_L if not driven.

V_L (A5): Logic Supply. Interface supply voltage for pins SCL, DI3, DO1, DO3, and ON. Operating voltage is 3V to 5.5V. Internally bypassed with 1 μ F.

ST1, ST2 (A6, C6): Bridge Driver Outputs, Referenced to PV_{CC} and GND. Each output runs at 50% duty cycle, ST1 is 180 degrees out of phase with ST2. Operating frequency is 2MHz. Bridge driver is enabled when PV_{CC} is between 3V to 5.5V and ON is high.

DO3 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I3 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO1 (B4): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

PV_{CC} (B5): Bridge Driver Supply Voltage. Operating voltage is 3V to 5.5V, connect to GND to disable bridge driver. Internally bypassed with 2.2 μ F.

V_{CC} (C5): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1 μ F.

GND (B3, B6, C1 to C4): Circuit Ground.

LTM2810-I, Isolated Side

V_{IN} (V6): Internal LDO Input Voltage. Operating voltage is 3.6V to 38V. Bypassed with 0.1 μ F.

O3 (W1): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI3 through the isolation barrier. Under the condition of an isolation communication failure O3 defaults to a high state.

SDA2 (W2, W3, X2): Serial I²C Data Pins, Referenced to V_{L2} and GND2. Bidirectional logic pins connected to logic side SDA pins through the isolation barrier. Output is biased high by a 1.8mA current source. Do not connect

PIN FUNCTIONS

an external pull-up device to SDA2. Under the condition of an isolation communication failure outputs default to a high state. Pins connected internally.

SCL2 (W4): Serial I²C Clock Output, Referenced to V_{L2} and GND2. Logic output connected to logic side SCL pin through the isolation barrier. Clock is unidirectional from logic to isolated side. SCL2 has a push-pull output stage; do not connect an external pull-up device. Under the condition of an isolation communication failure this output defaults to a high state.

AV_{L2} (W5): V_{L2} LDO Adjust Pin.

I3 (X1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO3 through the isolation barrier. The logic state on I3 translates to the same logic state on DO3. Connect to GND2 or V_{L2} if not used.

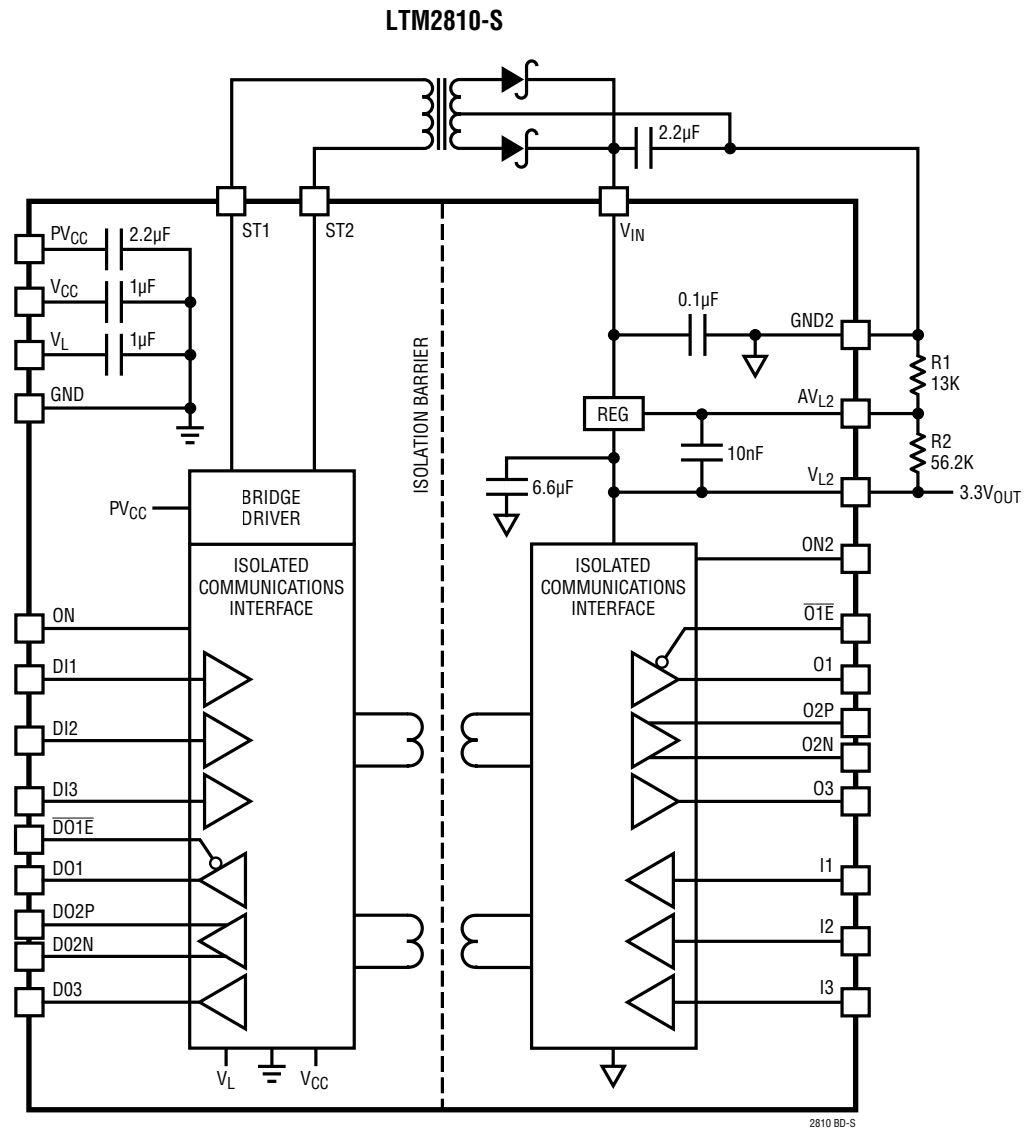
I1 (X3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO1 through the isolation barrier. The logic state on I1 translates to the same logic state on DO1. Connect to GND2 or V_{L2} if not used.

ON2 (X4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, all digital outputs are in a high state. Connect to V_{L2} if not driven.

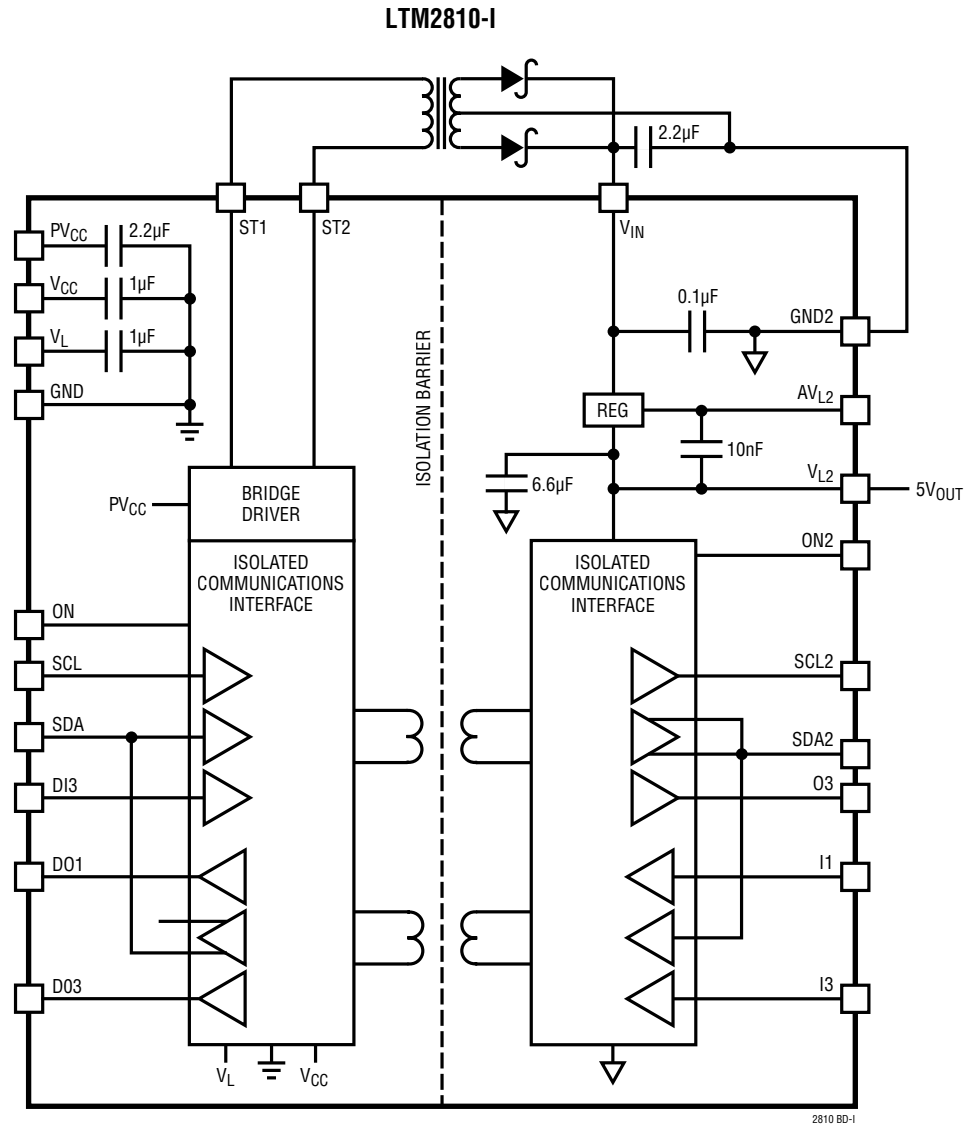
V_{L2} (X5, X6): Logic Supply, Referred to GND2. Interface supply voltage for pins SCL2, SDA2, I1, I3, O3, and ON2. Operating voltage is 3V to 5.5V. Internally bypassed with 6.6μF.

GND2 (W6, V1 to V5): Isolated Ground.

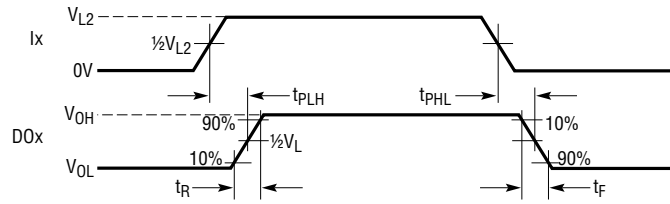
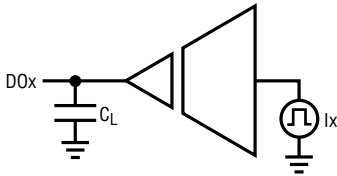
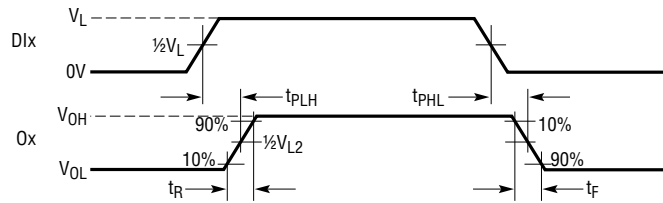
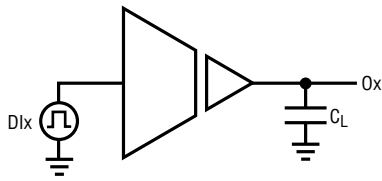
BLOCK DIAGRAM



BLOCK DIAGRAM

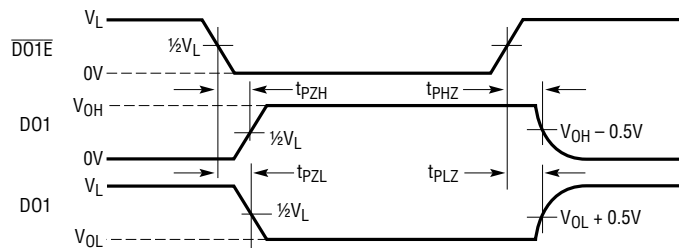
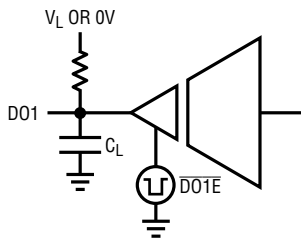
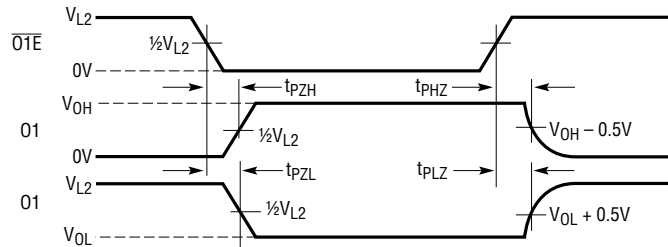
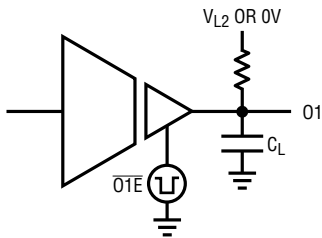


TEST CIRCUIT



2810 F01

Figure 1. Logic Timing Measurements



2810 F02

Figure 2. Logic Enable/Disable Time

TEST CIRCUIT

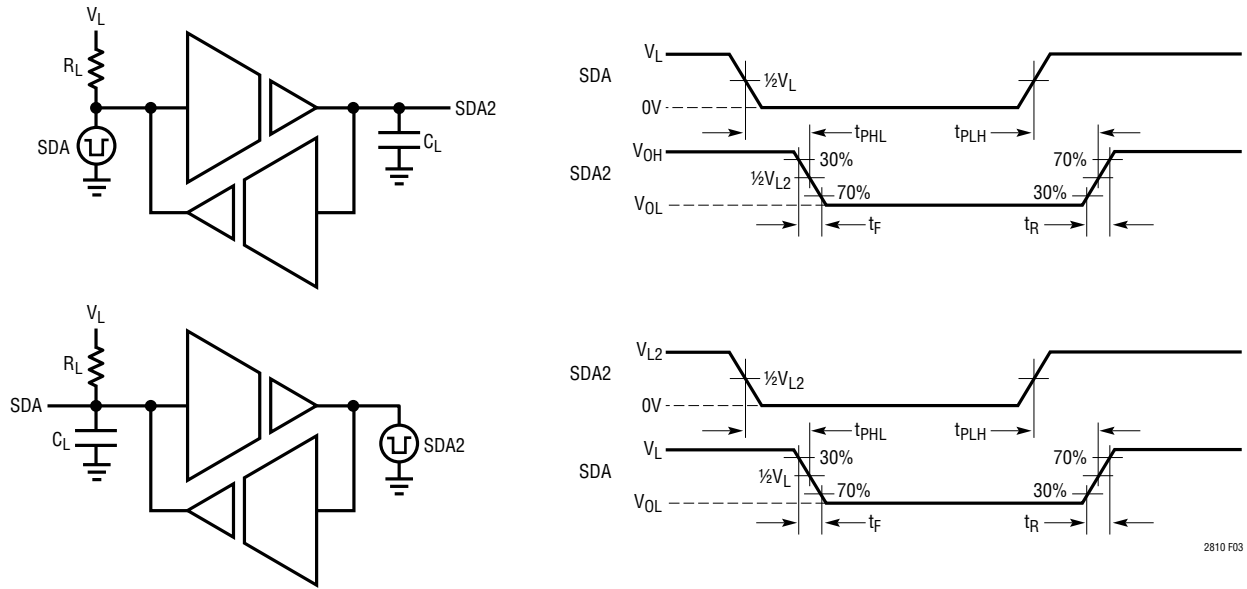


Figure 3. I²C Timing Measurements

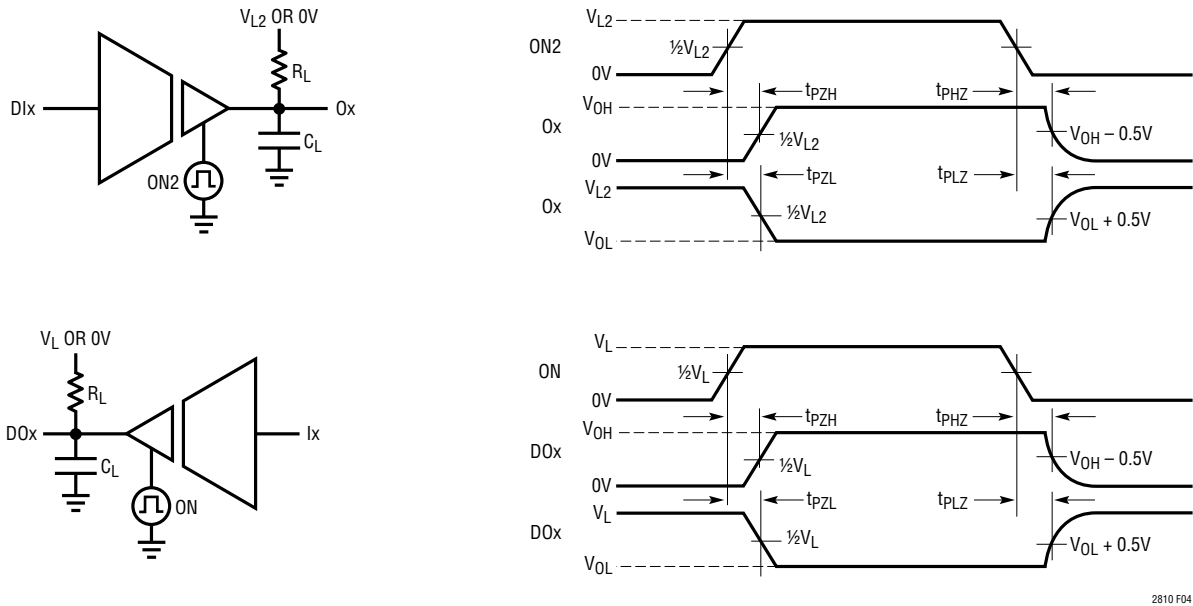


Figure 4. ONx Enable/Disable Time

APPLICATIONS INFORMATION

Overview

The LTM2810 digital μ Module isolator provides a galvanically-isolated robust logic interface, complete with decoupling capacitors. The LTM2810 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2810 blocks high voltage differences and eliminates ground loops, and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events as fast as 50kV/ μ s providing excellent noise isolation.

Input Supply (V_{CC})

The LTM2810 is powered by a 3V to 5.5V supply on the logic side of the isolation interface. The input supply provides power to the internal isolated communications interface and is completely independent of either the logic power supply or bridge driver supply. V_{CC} is bypassed internally with a 1 μ F ceramic capacitor.

Bridge Driver Supply (PV_{CC})

The integrated bridge driver is powered by a 3V to 5.5V supply on the logic side of the isolation interface. The bridge driver may be disabled by tying PV_{CC} to GND. PV_{CC} is bypassed internally with a 2.2 μ F ceramic capacitor.

LDO Input Supply (V_{IN})

The isolated side includes an integrated LDO powered by V_{IN} , with a nominal output voltage of 5V on V_{L2} . Input operating range is 4V to 38V. V_{IN} is bypassed internally with a 0.1 μ F ceramic capacitor. V_{IN} may be grounded or left unconnected if V_{L2} is driven by an external supply.

Logic Supplies (V_L , V_{L2})

Separate logic supply pins, V_L and V_{L2} , allow the LTM2810 to interface with any logic signal from 1.62V to 5.5V on the logic side of the SPI/Digital version, 3V to 5.5V for the logic and isolated sides of the I²C version and isolated side of the SPI/Digital version, as shown in Figure 5.

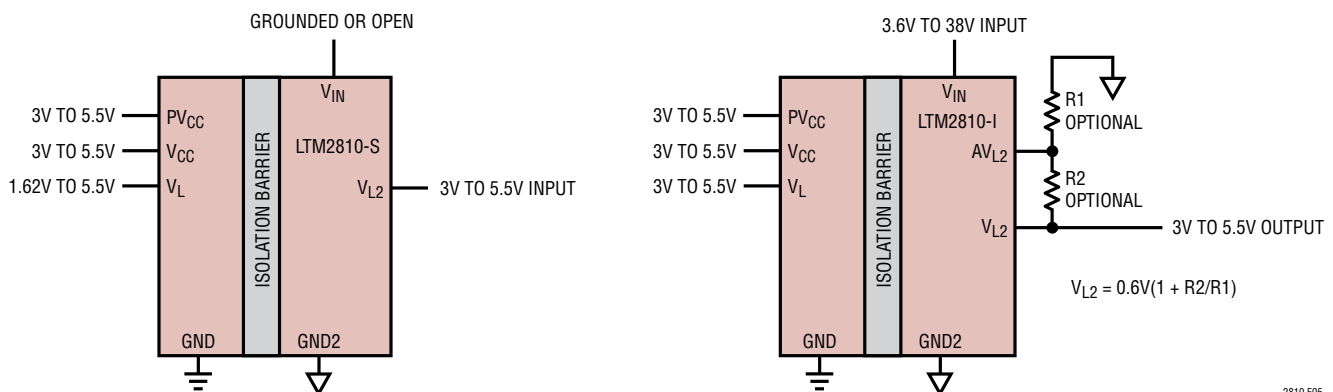


Figure 5. Supplies are Independent

2810 F05

APPLICATIONS INFORMATION

With V_{IN} driven, the V_{L2} output may be adjusted from the nominal 5V by connecting a voltage divider to the AV_{L2} pin as shown in Figure 5. Select the voltage divider ratio so that the AV_{L2} voltage is 0.6V. The value of R1 should be no greater than 13k Ω to minimize errors in the output voltage caused by the adjust pin bias current and internal voltage divider.

There is no interdependency between V_{CC} , V_L , and PV_{CC} . They may simultaneously operate at any voltage within their specified operating ranges and may sequence in any order. V_L is bypassed internally with a 1 μ F ceramic capacitor and V_{L2} is bypassed internally by a 6.6 μ F ceramic capacitor.

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2810's power supplies, V_{CC} , PV_{CC} , V_L , or V_{L2} due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high-Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2810. Refer to Application Note 88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion and mitigation of this phenomenon.

Isolation Transformer

Because of the wide voltage range for V_{IN} , there are many options for the isolation transformer and rectifier topology. The selected transformer should meet the application's isolation requirements, have a minimum volt-second rating greater than $0.5 \cdot PV_{CC}$ μ Vs and a current rating sufficient for the LTM2810's I_{VIN} plus any application load. Different winding configurations and turns ratios allow the accommodation of different input or isolated output voltages as illustrated by Figures 14 to 18.

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals in each direction are assembled as serial packets and transferred across the isolation barrier. The time required to transfer all three bits is 100ns maximum, and sets the limit for how often a signal can change on the opposite side of the barrier. Encoding and transmission is independent for each data direction. The technique used assigns DI1(-S) or SCL(-I) on the logic side, and I1(-S or -I) on the isolated side, the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ± 6 ns, but may vary up to ± 44 ns if the low priority channels are not encoded within the same high priority serial packet.

Serial Peripheral Interface (SPI) Bus

The LTM2810-S provides an SPI compatible isolated interface. The maximum data rate is a function of the inherent channel propagation delays, channel to channel pulse width uncertainty, and data direction requirements. Channel timing is detailed in Figures 6 through 9, Table 2, and Table 3. The SPI protocol supports four unique timing configurations defined by the clock polarity (CPOL) and clock phase (CPHA) summarized in Table 1.

Table 1. SPI Mode

CPOL	CPHA	DATA TO (CLOCK) RELATIONSHIP	
0	0	Sample (Rising)	Setup (Falling)
0	1	Setup (Rising)	Sample (Falling)
1	0	Sample (Falling)	Setup (Rising)
1	1	Setup (Falling)	Sample (Rising)

APPLICATIONS INFORMATION

The maximum data rate for bidirectional communication is 4MHz, based on a synchronous system, as detailed in the timing waveforms. Slightly higher data rates may be achieved by skewing the clock duty cycle and minimizing the DO1 (SDO) to DI1 (SCK) setup time, however the clock rate is still dominated by the system propagation delays. A discussion of the critical timing paths relative to Figure 6 and Figure 7 follows. For SPI communication DI1 = SCK, DI2 = SDI, DI3 = CS, DO1 = SDO, O1 = SCK2, O2N and O2P = SDI2, O3 = CS2, and I1 = SDO2.

- CS to SCK (master sample SDO, 1st SDO valid)
 - $t_0 \rightarrow t_1 \approx 50\text{ns}$, CS to CS2 propagation delay
 - $t_1 \rightarrow t_{1+}$ Isolated slave device propagation (response time), asserts SDO2
 - $t_1 \rightarrow t_3 \approx 50\text{ns}$, SDO2 to SDO propagation delay
 - $t_3 \rightarrow t_5$ Setup time for master SDO to SCK
- SDI to SCK (master data write to slave)
 - $t_2 \rightarrow t_4 \approx 50\text{ns}$, SDI to SDI2 propagation delay
 - $t_5 \rightarrow t_6 \approx 50\text{ns}$, SCK to SCK2 propagation delay
 - $t_2 \rightarrow t_5 \geq 50\text{ns}$, SDI to SCK, separate packet non-zero setup time
 - $t_4 \rightarrow t_6 \geq 50\text{ns}$, SDI2 to SCK2, separate packet non-zero setup time

- SDO to SCK (master sample SDO, subsequent SDO valid)

t_8 Setup data transition SDI and SCK

$t_8 \rightarrow t_{10} \approx 50\text{ns}$, SDI to SDI2 and SCK to SCK2 propagation delay

t_{10} SDO2 data transition in response to SCK2

$t_{10} \rightarrow t_{11} \approx 50\text{ns}$, SDO2 to SDO propagation delay

$t_{11} \rightarrow t_{12}$ Setup time for master SDO to SCK

Maximum data rate for single direction communication, master to slave, is 8MHz, limited by the systems encoding/decoding scheme or propagation delay. Timing details for both variations of clock phase are shown in Figure 8, Figure 9, and Table 3.

Additional requirements to insure maximum data rate are:

- CS is transmitted prior to (asynchronous) or within the same (synchronous) data packet as SDI
- SDI and SCK setup data transition occur within the same data packet. Referencing Figure 6, SDI can precede SCK by up to 13ns ($t_7 \rightarrow t_8$) or lag SCK by 3ns ($t_8 \rightarrow t_9$) and not violate this requirement. Similarly in Figure 8, SDI can precede SCK by up to 13ns ($t_4 \rightarrow t_5$) or lag SCK by 3ns ($t_5 \rightarrow t_6$).

APPLICATIONS INFORMATION

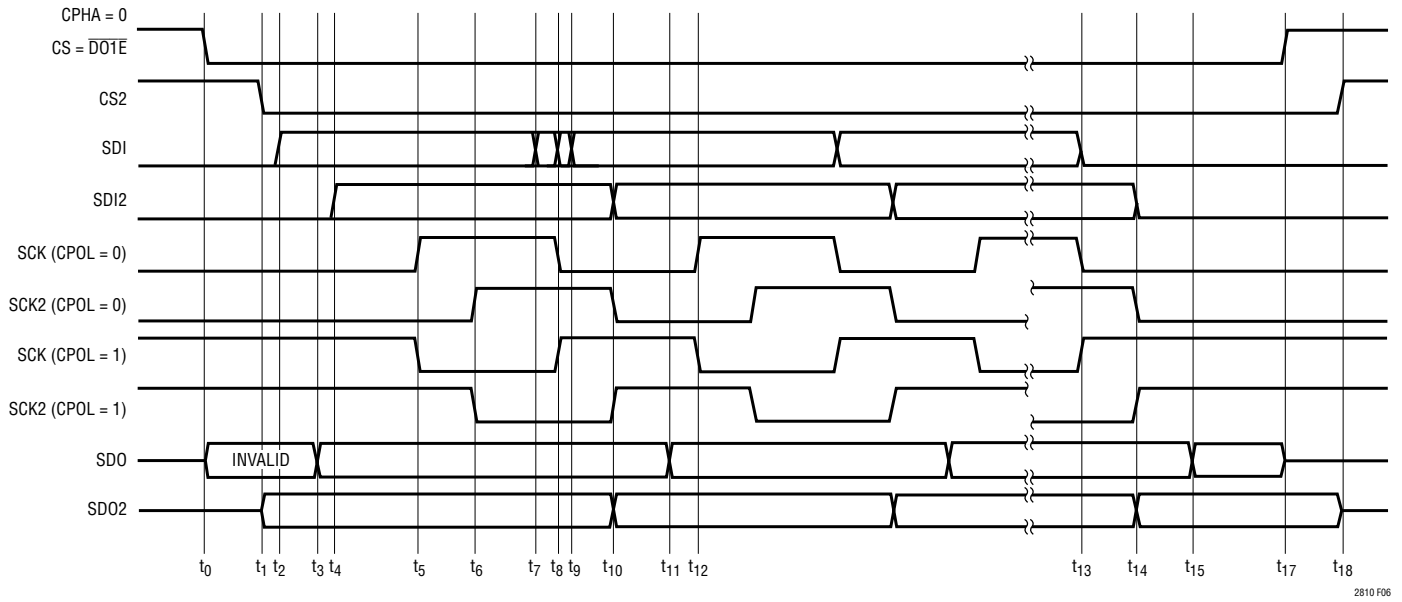


Figure 6. SPI Timing Bidirectional, CPHA = 0

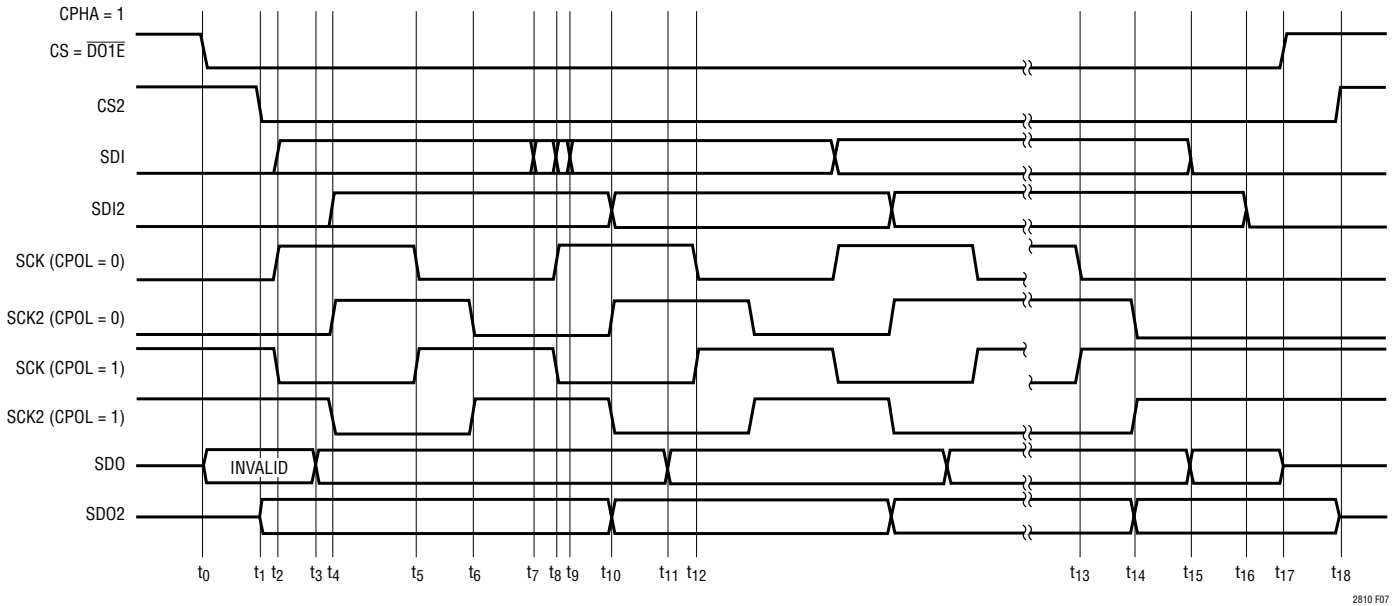


Figure 7. SPI Timing, Bidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 2. Bidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns. Logic side slave data output enabled, initial data is not equivalent to slave device data output.
t_0, t_1, t_{17}, t_{18}	0, 1	Propagation delay chip select, logic to isolated side, 50ns typical.
t_1	0, 1	Slave device chip select output data enable.
t_2	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within -13ns to 3ns of clock edge.
t_1 to t_3	0, 1	Propagation delay of slave data, isolated to logic side, 50ns typical.
t_3	0, 1	Slave data output valid, logic side.
t_2 to t_4	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t_5	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t_5, t_6	0, 1	Propagation delay of clock, logic to isolated side.
t_6	0, 1	Isolated side data sample time.
t_8	0, 1	Synchronous data and clock transition, logic side.
t_7, t_8	0, 1	Data to clock delay, must be ≤ 13 ns.
t_8, t_9	0, 1	Clock to data delay, must be ≤ 3 ns.
t_8, t_{10}	0, 1	Propagation delay clock and data, logic to isolated side.
t_{10}, t_{14}	0, 1	Slave device data transition.
$t_{10}, t_{11}, t_{14}, t_{15}$	0, 1	Propagation delay slave data, isolated to logic side.
t_{11}, t_{12}	0, 1	Slave data output to sample clock setup time.
t_{13}	0	Last data and clock transition logic side.
	1	Last sample clock transition logic side.
t_{13}, t_{14}	0	Propagation delay data and clock, logic to isolated side.
	1	Propagation delay clock, logic to isolated side.
t_{15}	0	Last slave data output transition logic side.
	1	Last slave data output and data transition, logic side.
t_{15}, t_{16}	1	Propagation delay data, logic to isolated side.
t_{17}	0, 1	Asynchronous chip select transition, end of transmission. Disable slave data output logic side.
t_{18}	0, 1	Chip select transition isolated side, slave data output disabled.

APPLICATIONS INFORMATION

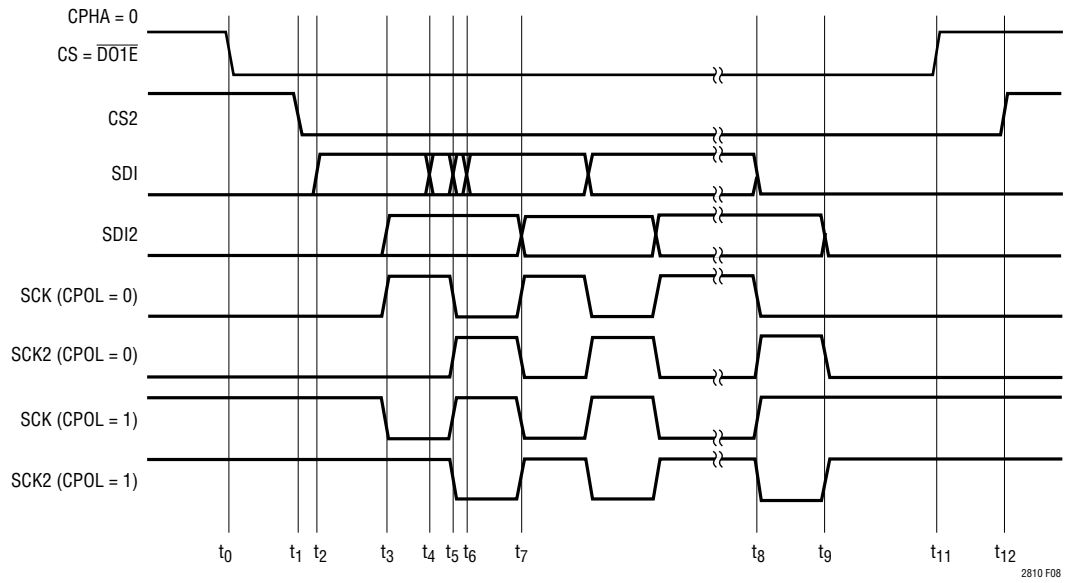


Figure 8. SPI Timing, Unidirectional, CPHA = 0

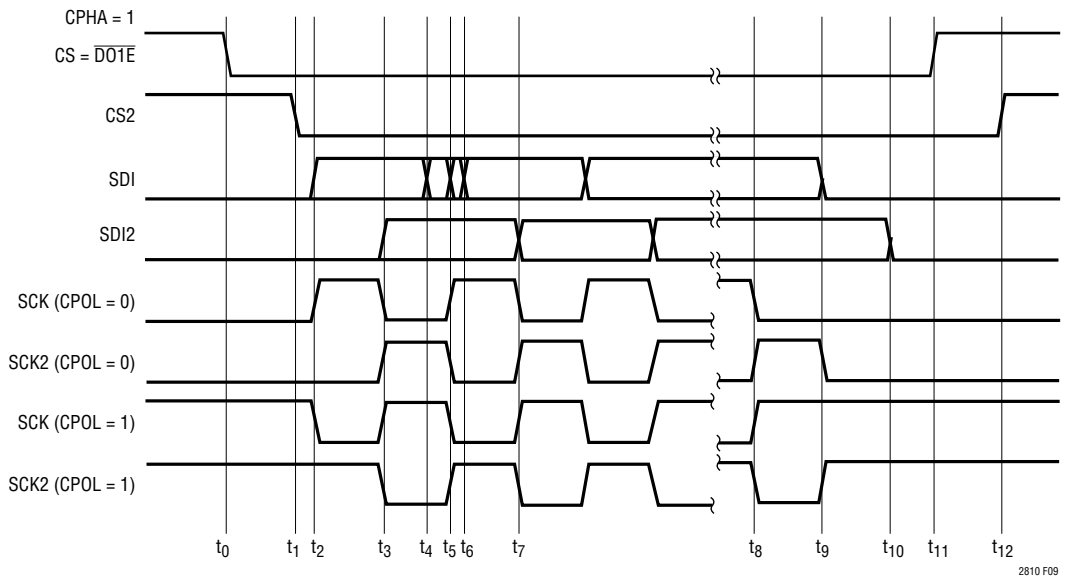


Figure 9. SPI Timing, Unidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 3. Unidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t ₀	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns.
t ₀ , t ₁	0, 1	Propagation delay chip select, logic to isolated side.
t ₂	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within –13ns to 3ns of clock edge.
t ₂ , t ₃	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t ₃	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t ₃ to t ₅	0, 1	Clock propagation delay, clock and data transition.
t ₄ , t ₅	0, 1	Data to clock delay, must be ≤ 13ns.
t ₅ , t ₆	0, 1	Clock to data delay, must be ≤ 3ns.
t ₅ to t ₇	0, 1	Data and clock propagation delay.
t ₈	0	Last clock and data transition.
	1	Last clock transition.
t ₈ , t ₉	0	Clock and data propagation delay.
	1	Clock propagation delay.
t ₉ , t ₁₀	1	Data propagation delay.
t ₁₁	0, 1	Asynchronous chip select transition, end of transmission.
t ₁₂	0, 1	Chip select transition isolated side.

APPLICATIONS INFORMATION

Inter-IC Communication (I²C) Bus

The LTM2810-I provides an isolated I²C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). The maximum data rate is 400kHz which supports fast-mode I²C. Timing is detailed in Figure 10. The data rate is limited by the slave acknowledge setup time ($t_{SU;ACK}$), consisting of the I²C standard minimum setup time ($t_{SU;DAT}$) of 100ns, maximum clock propagation delay of 225ns, glitch filter and isolated data delay of 500ns maximum, and the combined isolated and logic data fall time of 300ns at maximum bus loading. The total setup time reduces the I²C data hold time ($t_{HD;DAT}$) to a maximum of 175ns, guaranteeing sufficient data setup time ($t_{SU;ACK}$).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 11. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in fast mode and greater than 400pF in standard mode.

Additional proprietary circuitry monitors the slew rate on the SDA and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than 1V/ μ s for proper operation.

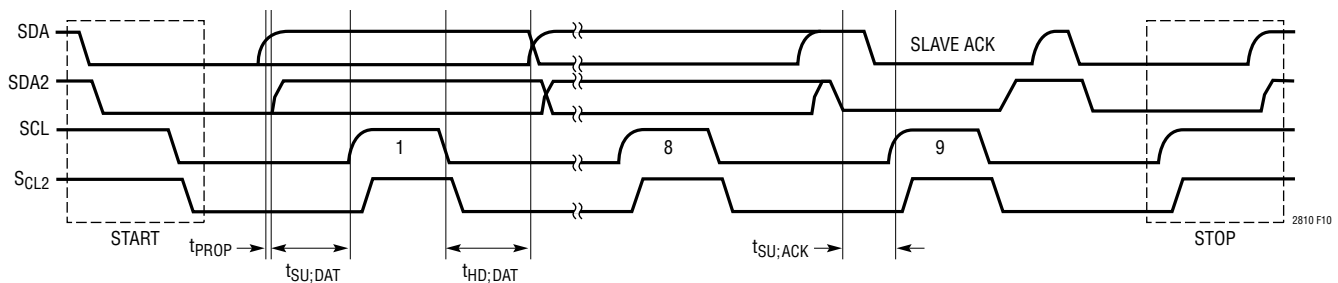


Figure 10. I²C Timing Diagram

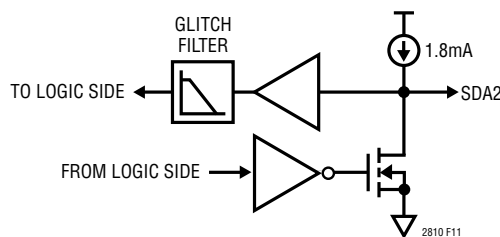


Figure 11. Isolated SDA2 Pin Schematic

APPLICATIONS INFORMATION

The logic side bidirectional serial data pin, SDA, requires a pull-up resistor or current source connected to V_L . Follow the requirements in Figure 12 and Figure 13 for the appropriate pull-up resistor on SDA that satisfies the desired rise time specifications and V_{OL} maximum limits for fast and standard modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.

The isolated side clock pin, SCL2, has a weak push-pull output driver; do not connect an external pull-up device. SCL2 is compatible with I²C devices without clock stretching. On lightly loaded connections, a 100pF capacitor

from SCL2 to GND2 or RC low pass filter ($R = 500\Omega$, $C = 100\text{pF}$) can be used to decrease the rise and fall times and minimize noise.

Some consideration must be given to signal coupling between SCL2 and SDA2. Separate these signals on a printed circuit board or route with ground between. If these signals are wired off board, twist SCL2 with V_{L2} and/or GND2 and SDA2 with GND2 and/or V_{L2} ; do not twist SCL2 and SDA2 together. If coupling between SCL2 and SDA2 is unavoidable, place the aforementioned RC filter at the SCL2 pin to reduce noise injection onto SDA2.

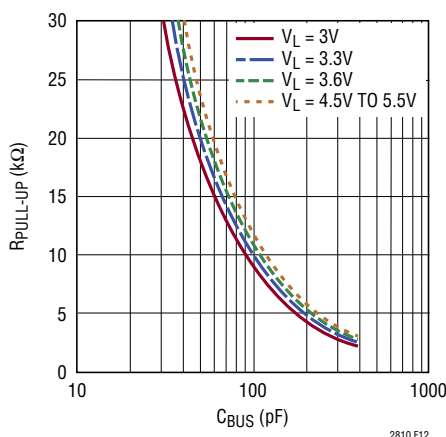


Figure 12. Maximum Standard Speed Pull-Up Resistance on SDA

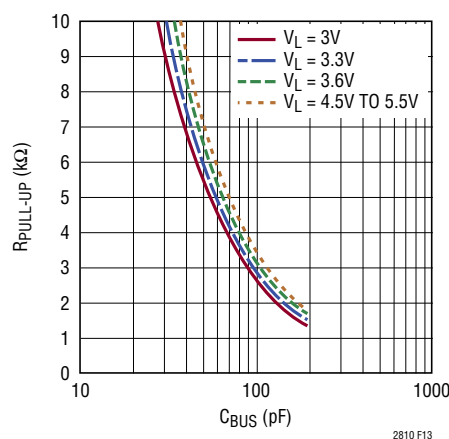


Figure 13. Maximum Fast Speed Pull-Up Resistance on SDA

APPLICATIONS INFORMATION

RF, Magnetic Field Immunity

The isolator μ Module technology used within the LTM2810 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity
EN 61000-4-8	Power frequency magnetic field immunity
EN 61000-4-9	Pulsed magnetic field immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 4.

Table 4. EMC Immunity Tests

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

* Non IEC method.

PCB Layout

The high integration of the LTM2810 makes PCB layout very simple. However, to optimize its electrical isolation characteristics and EMI performance, some layout considerations are necessary.

- Input and output supply decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8 μ F to 22 μ F with 1 Ω to 3 Ω of ESR is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1 μ F to 4.7 μ F, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, and minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used, it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (\leq 330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to ensure the voltage rating of the barrier is not compromised.
- In applications without an embedded PCB substrate capacitance, a slot may be added between the logic side and isolated side device pins. The slot extends the creepage path between terminals on the PCB side, and may reduce leakage caused by PCB contamination. The slot should be placed in the middle of the device and extend beyond the package perimeter.

TYPICAL APPLICATIONS

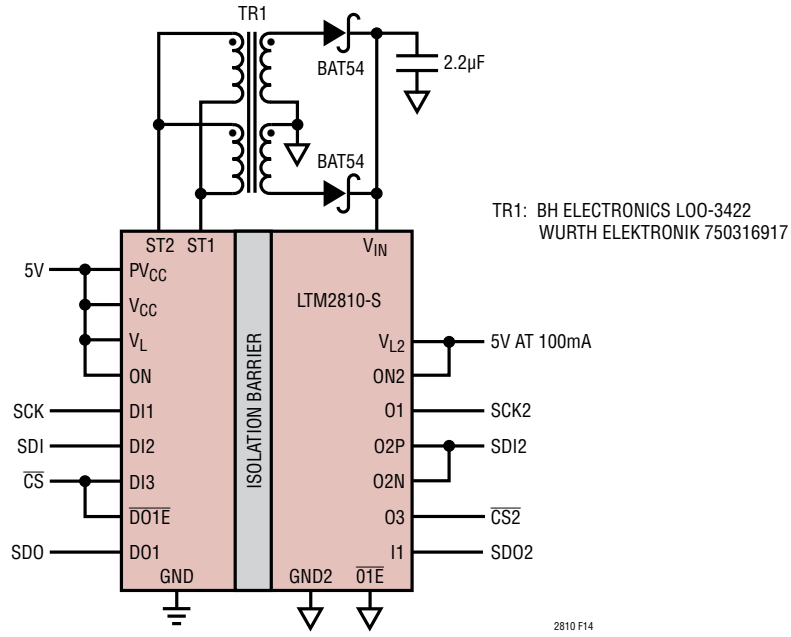


Figure 14. Isolated SPI with 5V Input and 5V Regulated Output

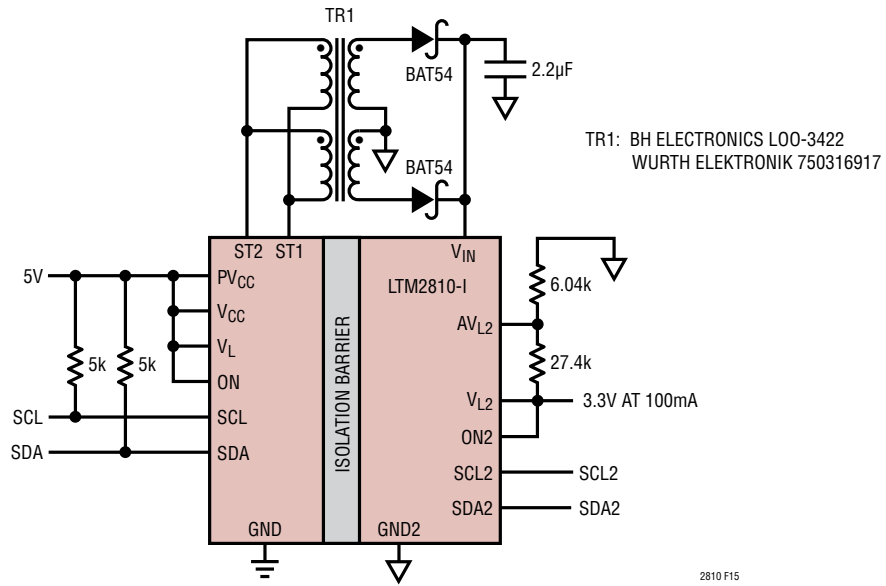


Figure 15. Isolated I²C with 5V Input and 3.3V Regulated Output

TYPICAL APPLICATIONS

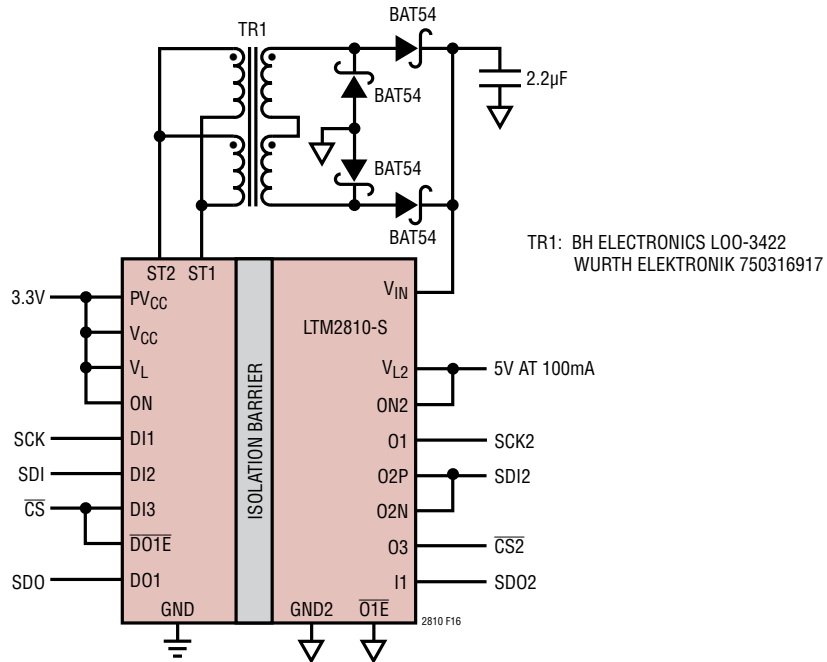


Figure 16. Isolated SPI with 3.3V Input and 5V Regulated Output

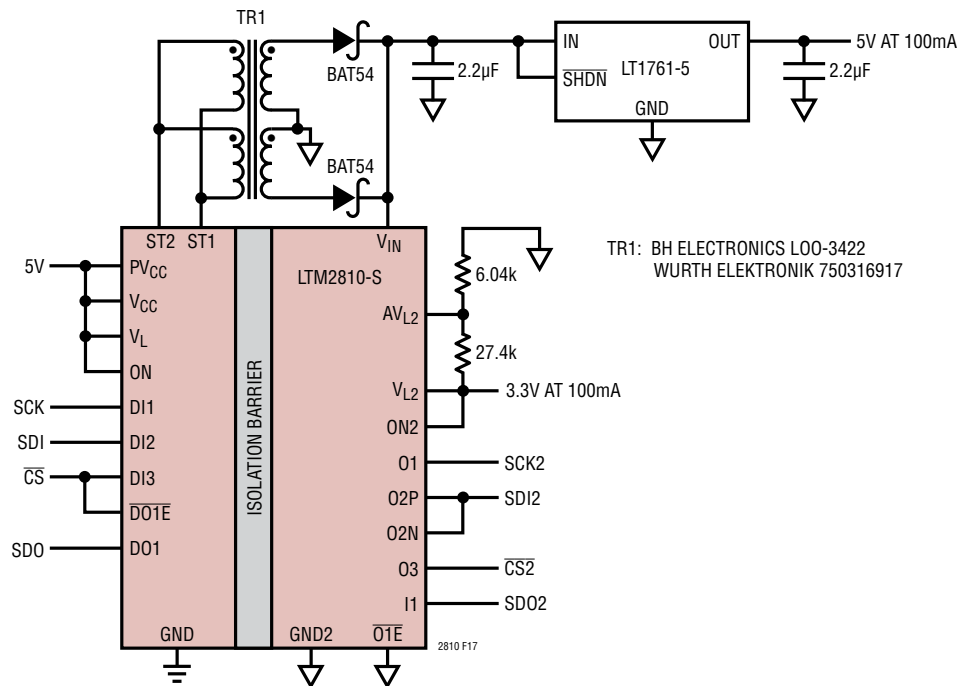
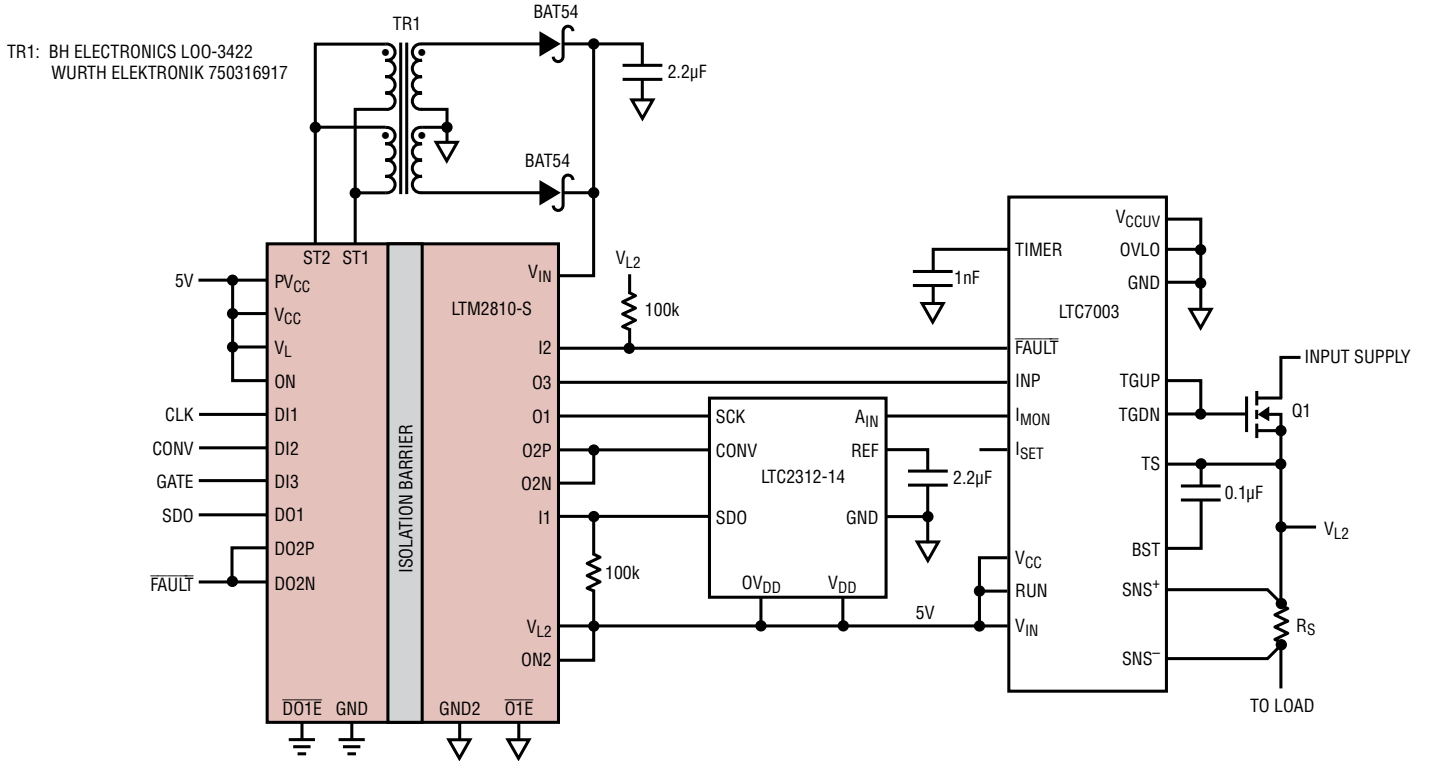


Figure 17. Isolated SPI with 3.3V Input with 3.3V and 5V Regulated Outputs

TYPICAL APPLICATIONS



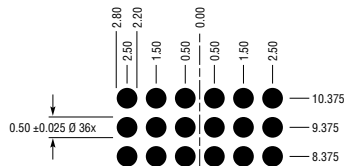
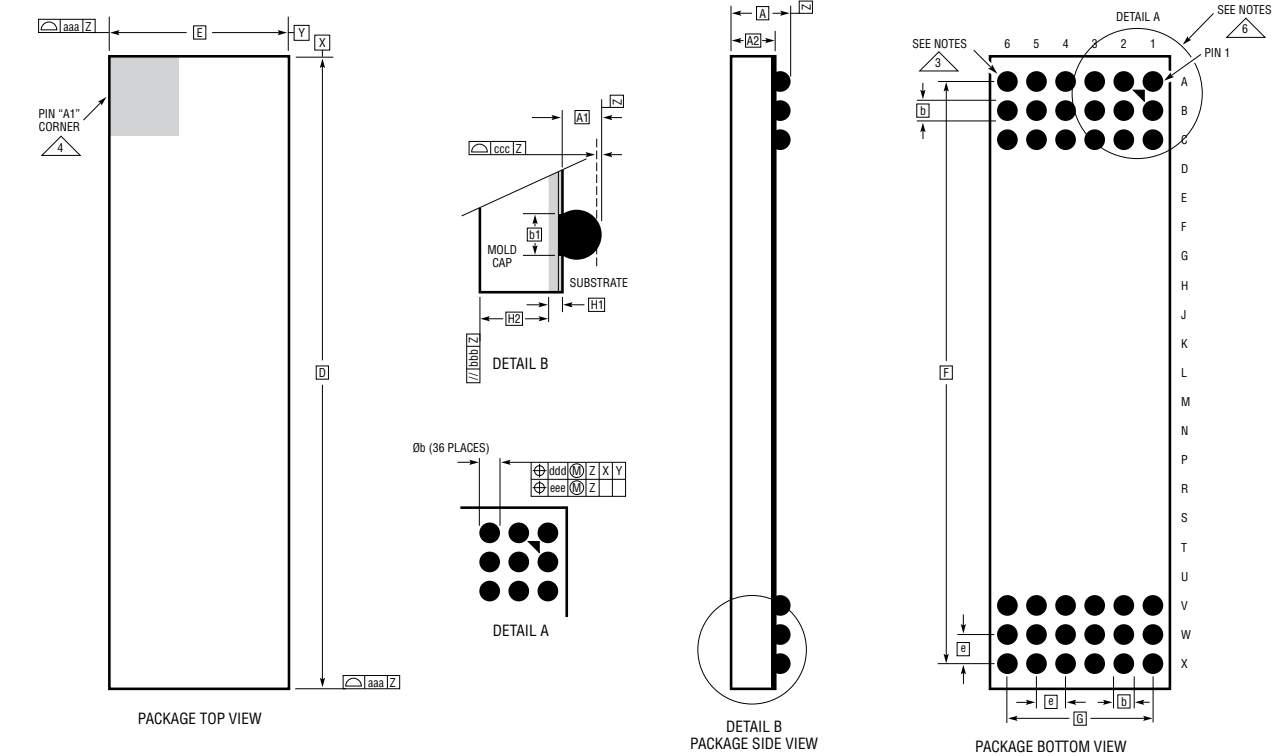
*NOTE: I_{MON} VALID WHEN INP (GATE) IS HIGH FOLLOWED BY 150µs OF BLANKING TIME.
TGUP – TS VOLTAGE IS APPROXIMATELY 7V.

2810 F18

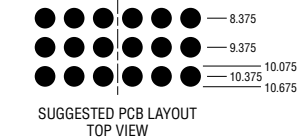
Figure 18. High Voltage Switch Controller with Current Readback

PACKAGE DESCRIPTION

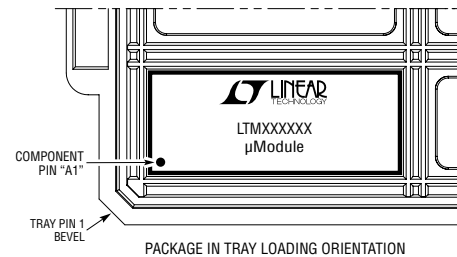
BGA Package
36-Lead (22mm × 6.25mm × 2.06mm)
 (Reference LTC DWG# 05-08-1588 Rev 0)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.81	2.06	2.31	
A1	0.40	0.50	0.60	BALL HT
A2	1.41	1.56	1.71	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		22.0		
E		6.25		
e		1.0		
F		20.75		
G		5.0		
H1	0.46	0.56	0.66	SUBSTRATE THK
H2	0.95	1.00	1.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 36				



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. BALL DESIGNATION PER JESD MS-028 AND JEP95
 4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
 5. PRIMARY DATUM -Z- IS SEATING PLANE
 6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG μModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



BGA 36 0817 REV 0

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/22	Added CSA (UL/IEC) Certifications.	1, 5