LTP5900-WHM

SmartMesh WirelessHART Node Wireless Mote Module

NETWORK FEATURES

- Complete **Radio Transceiver, Embedded Processor, and Networking Software** for Forming a Self-Healing Mesh Network
- Compliant to WirelessHART (IEC62591) Standard
- SmartMesh® Networks Incorporate:
  - Time Synchronized Network-Wide Scheduling
  - Per Transmission Frequency Hopping
  - Redundant Spatially Diverse Topologies
  - Network-Wide Reliability and Power Optimization
  - NIST Certified Security
- SmartMesh Networks Deliver:
  - >99.999% Network Reliability Achieved in the Most Challenging Dynamic RF Environments Often Found in Industrial Applications
  - Sub 50µA Routing Nodes

LTP5900-WHM FEATURES

- Industry-Leading Low Power Radio Technology with:
  - 4.5mA to Receive a Packet
  - 5.4mA to Transmit at 0dBm
  - 9.7mA to Transmit at 8dBm
- RF Modular Certifications Include USA, Canada, and EU
- 24mm × 39mm, 22-Pin PCB Assembly with MMCX Antenna Connector

DESCRIPTION

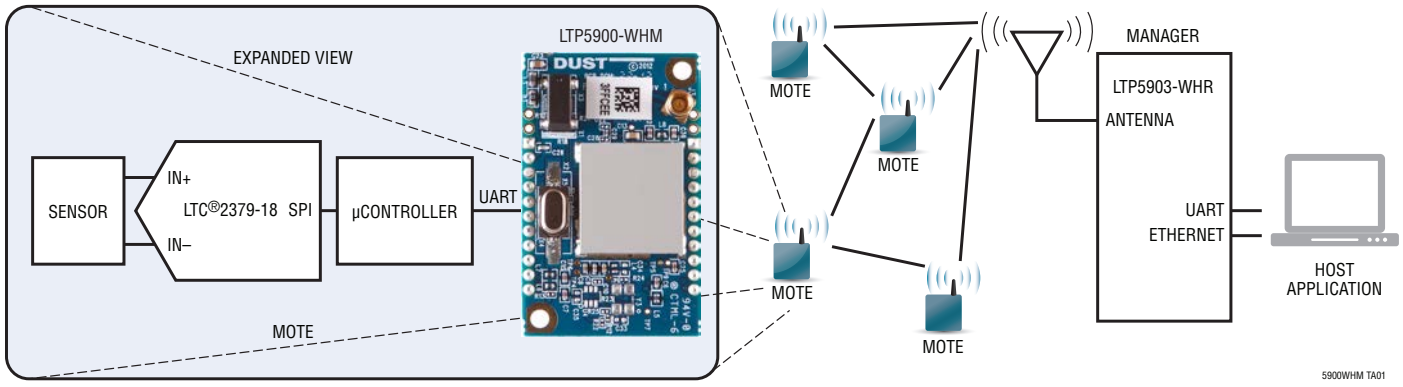
SmartMesh WirelessHART wireless sensor networks are self managing, low power networks built from wireless nodes called motes. The LTP™5900-WHM is the 22-pin WirelessHART mote product in the Eterna®* family of IEEE 802.15.4 printed circuit board assembly solutions, featuring a highly-integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh WirelessHART networking software. The LTP5900-WHM provides a forward compatible solution for customers using Dust Networks M2510 PCB module.

With Dust's time-synchronized WirelessHART networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation. The SmartMesh WirelessHART software provided with the LTP5900-WHM is fully tested and validated, and is readily configured via a software Application Programming Interface (API).

SmartMesh WirelessHART motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION

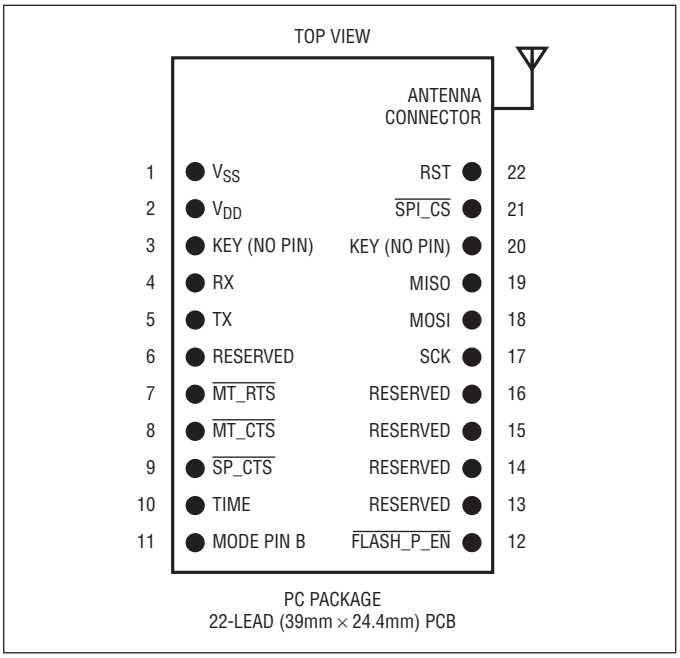


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD} to V_{SS}) ..... –0.3V to 4.20V
Voltage on Any Digital I/O Pin. V_{SS} – 0.3V to V_{DD} + 0.3V
Input RF Level, Input Power at Antenna Connector.....
10dBm
Storage Temperature Range ..... –55°C to 105°C
VSWR of Antenna 3:1
Operating Temperature Range .....–40°C to 85°C

PIN CONFIGURATION



PC PACKAGE
22-LEAD (39mm × 24.4mm) PCB

ORDER INFORMATION

LEAD FREE FINISH†	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTP5900IPC-WHMA#PBF	LTP5900IPC-WHMA#PBF	22-Lead (39mm × 24.4mm) PCB	–40°C to 85°C

†This product ships with the flash erased at the time of order. OEMs will need to program devices during development and manufacturing.
For legacy part numbers and ordering information, go to: http://www.linear.com/product/LTP5900-WHM#orderinfo

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C, V_{DD} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications					
Operational Supply Voltage Range (Between V_{DD} and V_{SS})	Including Noise and Load Regulation	2.75		3.76	V
Voltage Supply Noise	50Hz to 2MHz			250	mV_{P-P}
Voltage Supervisor Trip Point	Reset Trip Point		1.5		V
Supply Current, Peak	Searching for Network, Typically 150ms on and 2850ms in Doze (Note 2)		4.5		mA
Supply Current, Peak During Power on Reset	Maximum 750uS + V_{DD} Rise Time from 1V to 1.9V		12		mA
Supply Current, Peak Power Amplifier Enabled	TX, 5ms Maximum		9.7		mA
	TX, 5ms Maximum, 85°C (Note 7)			12	mA
Peak Current Power Amplifier Disabled	TX, 5ms Maximum		5.4		mA

ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C, V_{DD} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Allowed Temperature Ramp During Operation	–40°C to 85°C			8	°C/min
Operating Relative humidity	Non-Condensing	10		90	% RH
Current Consumption					
Supply Current, Transmit	Power Amplifier Enabled Power Amplifier Disabled		9.7 5.4		mA mA
Supply Current, Receive			4.5		mA
Device Load					
Total Capacitance	V_{DD} to V_{SS} (Note 7)			6	µF
Total Inductance	V_{DD} to V_{SS} (Note 7)			4.9	µH

Specifications are at –40°C to 85°C, V_{DD} = 3.6V unless otherwise noted.

PARAMETER	CONDITONS	MIN	TYP	MAX	UNITS
Digital Signals					
V_{IL} (Low Level Input Voltage)		–0.3		0.6	V
V_{IH} (High Level Input Voltage)		V_{DD} – 0.3		V_{DD} + 0.3	V
V_{OL} (Low Level Output Voltage)	$I_{OL(MAX)}$ = 1.2mA			0.4	V
V_{OH} (High Level Output Voltage)	$I_{OH(MAX)}$ = –1.8mA	V_{DD} – 0.3			V
Input Leakage Current	25°C		50		nA
Radio Specifications					
Operating Frequency	(Note 7)	2.4000		2.4835	GHz
Number of Channels			15		
Channel Separation			5		MHz
Occupied Channel Bandwidth	At –20dBc		2.7		MHz
Frequency Accuracy	(Note 7)	–40		40	ppm
Modulation	IEEE 802.15.4 DSSS				
Raw Data Rate			250		kbps
Receiver Operating Maximum Input Level			0		dBm
Receiver Sensitivity	At 50% PER, V_{DD} = 3V, 25°C At 1% PER, V_{DD} = 3V, 25°C		–95.0 –92.5		dBm dBm
Output Power, Conducted Power Amplifier Enabled Power Amplifier Disabled	 V_{DD} = 3.6V, 25°C V_{DD} = 3.6V, 25°C		 8 0		 dBm dBm
Range (Note 3) Power Amplifier Enabled: Indoor (Note 4) Outdoor (Note 4) Free space Power Amplifier Disabled: Indoor (Note 4) Outdoor (Note 4) Free space	25°C, 50% RH, 2dBi Omni-Directional Antenna, 2m above ground		 100 300 1200 25 200 350		 meters meters meters meters meters meters

ANTENNA SPECIFICATIONS

A MMCX-compatible male connector is provided on board for the antenna connection. The antenna must meet the following specifications. For a list of FCC-approved antennae, see the FCC-Approved Antennae section.

PARAMETER	VALUE
Frequency Range	2.4GHz to 2.4835GHz
Impedance	50Ω
Maximum VSWR	3:1
Connector	MMCX (Note 5)

When the mote is placed inside an enclosure, the antenna should be mounted such that the radiating portion of the antenna protrudes from the enclosure. The antenna should be connected using a MMCX connector on a coaxial cable. For optimum performance, the antenna should be positioned vertically when installed.

Note 1: The absolute maximum ratings shown should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to the LTP5900. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: The duration of doze time and "on" time is determined by the joinDutyCycle command in the mote serial API. Refer to the SmartMesh WirelessHART Mote Serial API Guide for details.

Note 4: Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance.

Note 5: 1 meter above ground.

Note 6: The LTP5900-WHM can accommodate the following RF mating connectors: MMCX straight connector such as Johnson 135-3402-001, or equivalent; MMCX right angle connector such as Tyco 1408149-1, or equivalent.

Note 7: Guaranteed by design. Not production tested.

PIN FUNCTIONS

V_{SS} (Pin 1): Ground. I/O type = power.

V_{DD} (Pin 2): Power. I/O type = power.

KEY (Pins 3, 20): No Pin.

RX (Pin 4): UART RX. I/O type = 1. Direction = In.

TX (Pin 5): UART TX. I/O type = 1. Direction = Out. Pin state in Deep Sleep = V_{DD}. Deep Sleep is the lowest possible power state, with V_{DD} and GND connected. The mote microprocessor and radio are inactive, and the mote must be awakened using the $\overline{RST}$ signal (for more information see the lowPowerSleep command in the WirelessHART Mote Serial API Guide).

Reserved (Pins 6, 13, 14, 15, 16): No Connection.

$\overline{MT\_RTS}$ (Pin 7): UART Active Low Mote Ready to Send. I/O type = 1. Direction = Out. Pin state in Deep Sleep = V_{DD}. Deep Sleep is the lowest possible power state, with V_{DD} and GND connected. The mote microprocessor and radio are inactive, and the mote must be awakened using the $\overline{RST}$ signal (for more information see the lowPowerSleep command in the WirelessHART Mote Serial API Guide).

$\overline{MT\_CTS}$ (Pin 8): UART Active Low External Processor Clear to Send. I/O type = 1. Direction = Out. Pin state in Deep Sleep = V_{DD}. Deep Sleep is the lowest possible power state, with V_{DD} and GND connected. The mote microprocessor and radio are inactive, and the mote must be awakened using the $\overline{RST}$ signal (for more information see the lowPowerSleep command in the WirelessHART Mote Serial API Guide).

$\overline{SP\_CTS}$ (Pin 9): UART Active Low Serial Peripheral Clear to Send. I/O type = 1. Direction = In.

$\overline{TIME}$ (Pin 10): Falling Edge Time Request. I/O type = 1. Direction = In. The $\overline{TIME}$ input pin is optional, and must either be driven or pulled up with a 5.1M resistor. Unless noted otherwise, all signals are active low.

MODE_PIN_B (Pin 11): Selects Between Mode 1 and Mode 3 Operation. I/O type = 1. Direction = In.

$\overline{FLASH\_P\_EN}$ (Pin 12): Active Low Flash Power Enable. I/O Type = 1. Direction = In.

SCK (Pin 17): SPI Clock. I/O type = 1. Direction = In.

PIN FUNCTIONS

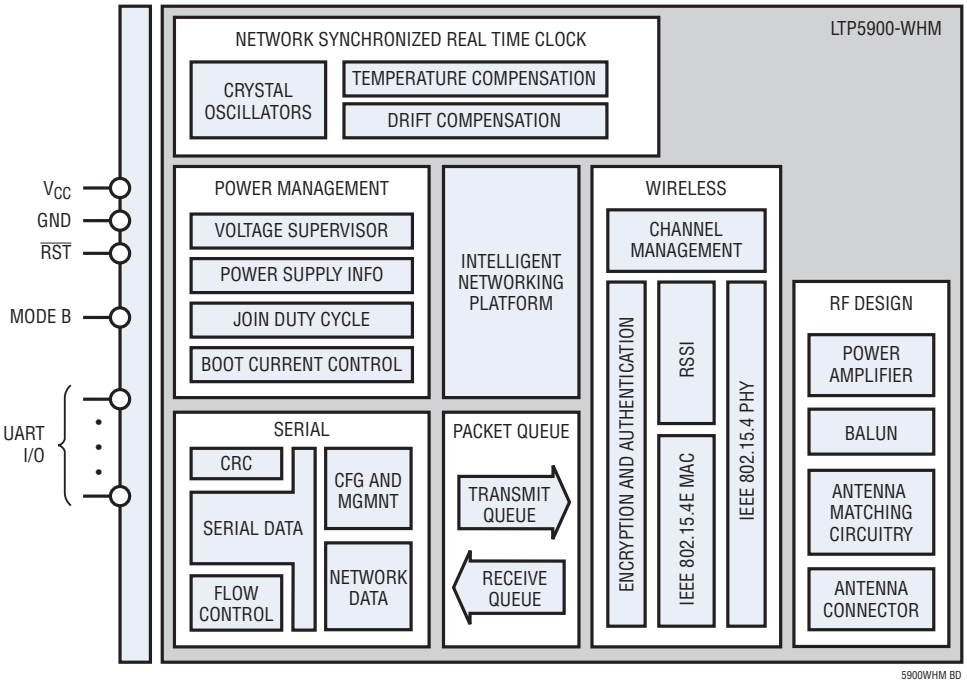
MOSI (Pin 18): SPI Master Out Slave In Serial Data. I/O type = 1. Direction = In.

MISO (Pin 19): SPI Master In Slave Out Serial Data. I/O type = 1. Direction = Out.

$\overline{\text{SPI\_CS}}$ (Pin 21): Active Low Flash Chip Select. I/O type = 1. Direction = In.

$\overline{\text{RST}}$ (Pin 22): Active Low Reset. I/O type = 1. Direction = In. The $\overline{\text{RST}}$ input pin is internally pulled up and connecting it is optional. When driven active low, the mote is hardware reset until the signal is de-asserted. Refer to the Power-On Sequence section for timing requirements on the $\overline{\text{RST}}$ pin. Note that the mote may also be reset using the mote serial command (see the SmartMesh WirelessHART Mote Serial API Guide).

BLOCK DIAGRAM



MOTE BOOT UP

POWER-ON SEQUENCE

The LTP5900-WHM has internal power-on reset circuits that ensure that the mote will properly boot. External resetting of the device is not required and not recommended.

Table 1. Power-On Sequence

PARAMETER	COMMENTS	MIN	TYP	MAX	UNITS
$\overline{RST}$ Pulse Width	Reset Timing	125			µs

INRUSH CURRENT

During power on, the mote can be modeled as a lumped impedance, as shown in Figure 1. With a source impedance (R_{SRC}) of 1Ω, the inrush current on the mote appears as shown in Figure 2.

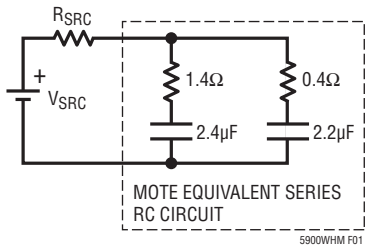


Figure 1. LTP5900-WHM Equivalent Series RC Circuit

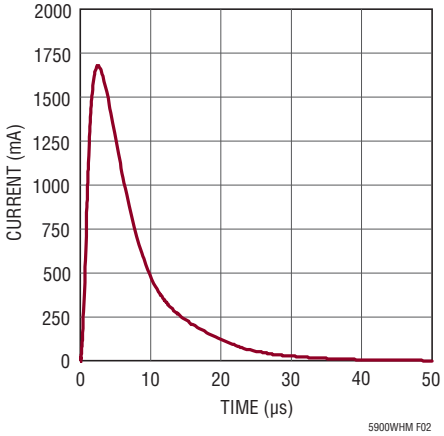


Figure 2. V_{DD} Inrush Current (Power-On with Supply Impedance of 1Ω)

MOTE BOOT SEQUENCE

Following the negation of $\overline{RST}$ the mote completes its boot-up process by loading the application image and loading the operating parameters. The LTP5900-WHM lowers average current consumption by spreading the boot operation over time. This method supports systems with supplies having a maximum DC current less than the peak current required by the LTP5900-WHM. These systems must store enough charge to maintain the supply through the LTP5900-WHM's peak current consumption. For more information, contact your Linear Technology applications engineer. The maximum average current consumption for the LTP5900-WHM is defined by the maximum total charge Q consumed over a sliding window in time, t_{WINDOW}.

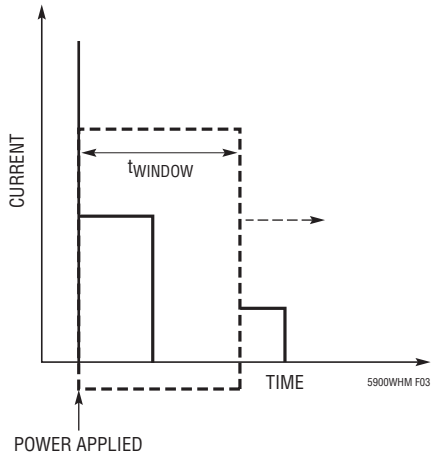


Figure 3. Boot Sequence

Table 2. Boot Sequence Parameters

PARAMETER	COMMENTS	MIN	TYP	MAX	UNITS
t_{BOOT_DELAY}	The time between mote power greater than 1.9V and serial interface availability		3	5	sec
Q	t_{WINDOW} = 0.56s			200	µC

SERIAL INTERFACE BOOT UP

LTP5900-WHM Serial Interface Boot Up

Upon LTP5900-WHM power up, the $\overline{MT\_CTS}$ line is high (inactive). The LTP5900-WHM serial interface boots within t_{BOOT_DELAY} (see the Mote Boot Sequence section) of the mote powering up, at which time the LTP5900-WHM will transmit an HDLC boot event packet. Note that full handshake is in effect and is required to receive this packet.

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RESET PIN

The $\overline{RST}$ input pin is internally pulled up. Connecting it is optional; however, in applications operating in the presence of EMI, $\overline{RST}$ should be actively driven high. When driven low, the mote hardware is in reset. Note that the mote may also be reset using the mote reset command (0×08). For requirements on reset timing, see the Mote Boot Up section.

The LTP5900-WHM is a highly sophisticated device and Linear Technology recommends doing resets gracefully. If the device is in the network, a disconnect command (0×07) should be issued before the $\overline{RST}$ signal is asserted. This will result in the device rebooting and sending the boot event.

The $\overline{RST}$ signal may then be asserted since the device is not in the network.

Refer to the LTP5900-WHM Integration Guide for recommendations on how to connect to the $\overline{RST}$ pin, including voltage supervision. For detailed information about mote serial commands, refer to the SmartMesh WirelessHART Mote Serial API Guide.

TIMESTAMPS

The LTP5900-WHM has the ability to deliver network-wide synchronized timestamps. The LTP5900-WHM sends a time packet (as described in the SmartMesh WirelessHART Mote Serial API Guide) through its serial interface when one of the following occurs:

- Mote receives an HDLC request to read time
- The $\overline{TIME}$ signal is asserted

The $\overline{TIME}$ pin is optional and has the advantage of being more accurate. The value of the timestamp is taken within approximately 1ms of receiving a $\overline{TIME}$ signal activation. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet. Refer to the SmartMesh WirelessHART Mote Serial API Guide for more information on timestamps.

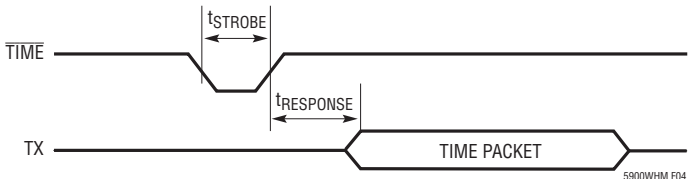

Figure 4. Operation of $\overline{TIME}$ Pin

Table 3. $\overline{TIME}$ Timing Values

VARIABLE	DESCRIPTION	MIN	MAX	UNITS
t_{STROBE}	$\overline{TIME}$ Strobe Pulse Width	125		µs
$t_{RESPONSE}$	Negation of Time Strobe to Start of Time Packet		100	ms

SETTABLE I/O MODES

The LTP5900-WHM offers a choice of two I/O modes. The functionality of the interface will be determined by the setting of Mode pin B whose pinout is described in the Pin Functions section.

Table 4. Mode Pin Settings

PIN	MODE 1	MODE 3
MODE_PIN_B	Externally Tied Low	Externally Tied High

All modes provide a means of transmitting and receiving serial data through the wireless network, as well as a command interface that provides synchronized time stamping, local configuration, and diagnostics.

Mode 1 implements an 8-bit, no parity, 9600bps baud three-, four- or five-signal serial interface with bidirectional packet-level flow control operating at 9600bps. In certain OEM designs, one or two of the serial handshake signals may be optional for reduced pin count, as described in Table 5.

Mode 3 implements an 8-bit, no parity, 115.2kbps baud five-signal serial interface with bidirectional packet-level flow control and byte-level flow control in the mote-to-microprocessor direction only.

Mode 1: Three/Four/Five-Signal Serial Interface (9600bps)

The LTP5900-WHM mode 1 provides a three-, four-, or five-signal serial interface that is optimized for low powered embedded applications (and in certain designs

INTERFACES

may provide a low pin count serial solution). The mode 1 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{\text{MT\_RTS}}$, $\overline{\text{MT\_CTS}}$, $\overline{\text{SP\_CTS}}$) used for bidirectional flow control. The $\overline{\text{MT\_RTS}}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). Refer to Table 5 for information on each handshake pin, including details on which pins are optional.

Table 5. Mode 1 Pin Usage

PIN	I/O	USAGE
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\overline{\text{MT\_RTS}}\text{ to }\overline{\text{SP\_CTS}}}$ timeout defined in the UART AC Timing section expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert , wait for $t_{\overline{\text{MT\_RTS}}}$ retry and then re-assert to attempt to send the serial packet again (see Figure 8). $\overline{\text{MT\_RTS}}$ may be ignored by the microprocessor only if always stays low.
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides packet-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. $\overline{\text{SP\_CTS}}$ may be externally tied low (reducing pin count) only if the microprocessor is always ready to receive a serial packet.
$\overline{\text{MT\_CTS}}$	Output	$\overline{\text{MT\_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT\_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT\_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT\_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT\_CTS}}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT\_CTS}}$ state. (For a list of local commands, see the SmartMesh WirelessHART Mote Serial API Guide.)
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

Table 6. Mode 3 Pin Usage

PIN	I/O	USAGE
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP\_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\overline{\text{MT\_RTS}}\text{ to }\overline{\text{SP\_CTS}}}$ timeout defined in the UART AC Timing section expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert $\overline{\text{MT\_RTS}}$, wait for $t_{\overline{\text{MT\_RTS}}}$ retry and then re-assert $\overline{\text{MT\_RTS}}$ to attempt to send the serial packet again (see Figure 8).
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides byte-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. In mode 3 byte-level flow control is achieved by having the microprocessor negate and then reassert the $\overline{\text{SP\_CTS}}$ signal following the receipt of each byte. The mote will begin transmission of the next byte after detecting the reassertion of $\overline{\text{SP\_CTS}}$.
$\overline{\text{MT\_CTS}}$	Output	$\overline{\text{MT\_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT\_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT\_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT\_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT\_CTS}}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT\_CTS}}$ state. For a list of local commands, see the SmartMesh WirelessHART Mote Serial API Guide.
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

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Mode 3: Five-Signal Serial Interface (115.2kbps)

The LTP5900-WHM mode 3 provides a five-signal serial interface with byte-level flow control on transfers from the mote to the microprocessor. The mode 3 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{MT\_RTS}$, $\overline{MT\_CTS}$, $\overline{SP\_CTS}$) used for bidirectional flow control. The $\overline{MT\_RTS}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet. Refer to Table 6 for information on each handshake pin, including details on which pins are optional.

UART AC Timing

Table 7. UART Timing Values (Note 7)

VARIABLE	DESCRIPTION	MIN	MAX	UNITS
t_{RX_BAUD}	Deviation from baud rate	–2	2	%
t_{RX_STOP}	Number of stop bits (9600bps)	1		bit period
t_{RX_STOP}	Number of stop bits (115.2kbps)	1.5		bit period
t_{TX_BAUD}	Deviation from baud rate	–1	1	%
t_{TX_STOP}	Number of stop bits	1		bit period
$t_{\overline{SP\_CTS}\ to\ \overline{MT\_RTS}}$	Assertion of $\overline{SP\_CTS}$ to negation of $\overline{MT\_RTS}$	0	10	ms
$t_{\overline{MT\_RTS}\ to\ \overline{SP\_CTS}}$	Assertion of $\overline{MT\_RTS}$ to assertion of $\overline{SP\_CTS}$		500	ms
$t_{\overline{MT\_RTS}\ RETRY}$	Time from a $\overline{MT\_RTS}$ timeout to the retry.		500	ms
$t_{\overline{SP\_CTS}\ to\ TX}$	Assertion of $\overline{SP\_CTS}$ to start of byte	0	10	ms
$t_{TX\ to\ \overline{SP\_CTS}}$	Start of byte to negation of $\overline{SP\_CTS}$	1		bit period
$t_{\overline{SP\_CTS}\ ACK\ PW}$	Negation pulse width of $\overline{SP\_CTS}$	500		ns
$t_{DIAG\_ACK\_TIMEOUT}$*	The mote responds to all requests within this time.		125	ms
$t_{INTERBYTE\_TIMEOUT}$	Falling edge of TX to falling edge of $\overline{SP\_CTS}$ (Mode 3 only)		7.1	ms
$t_{INTERPACKET\_DELAY}$	The sender of an HDLC packet must wait at least this amount of time before sending another packet	20		ms

* For more information about supported requests and details on when $t_{DIAG\_ACK\_TIMEOUT}$ applies, refer to the SmartMesh WirelessHART Mote Serial API Guide.

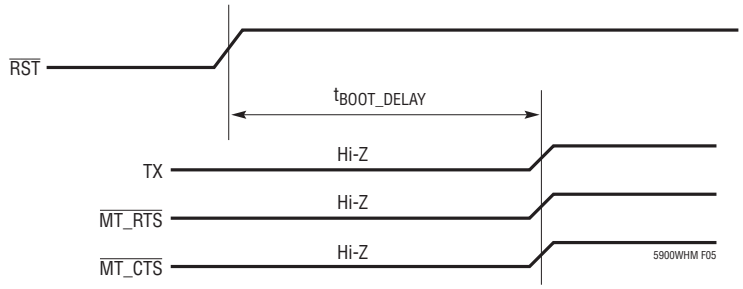


Figure 5. Power-On Sequence. See the Mote Boot Sequence Section for the Value of t_{BOOT_DELAY}

INTERFACES

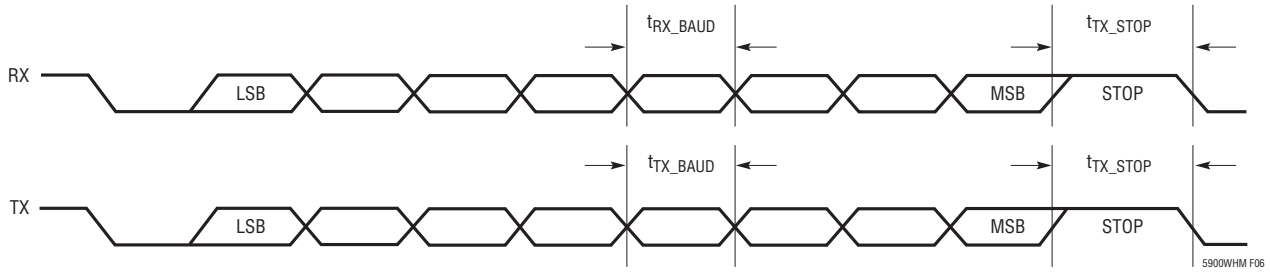


Figure 6. Byte-Level Timing

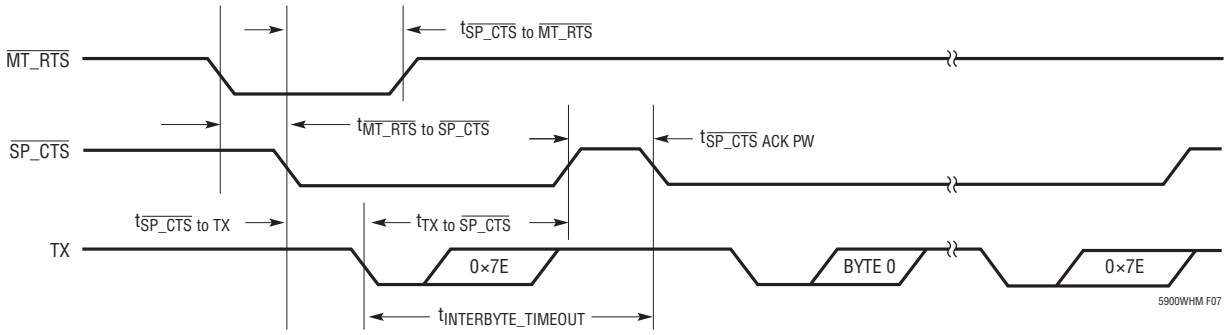


Figure 7. Flow Control Timing

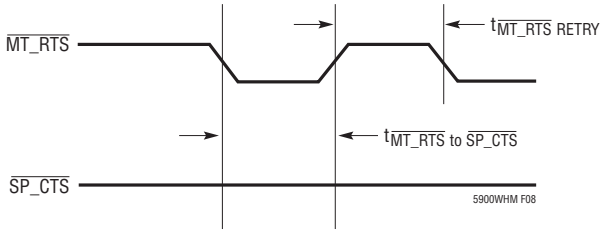
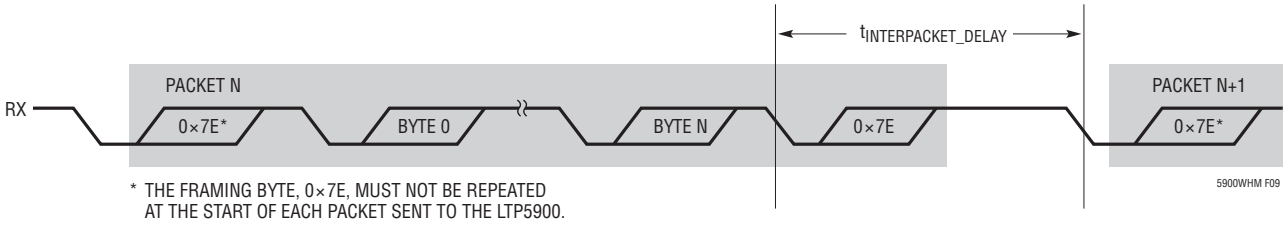


Figure 8. MT_RTS Timeout Behavior



* THE FRAMING BYTE, 0×7E, MUST NOT BE REPEATED AT THE START OF EACH PACKET SENT TO THE LTP5900.

Figure 9. Packet Timing

INTERFACES

MOTE SERIAL API

The LTP5900-WHM offers a comprehensive application programming interface (API) that provides full programmatic access to control the mote, monitor its status (such as battery charge and network status), and provide access to the wireless mesh network. Refer to the SmartMesh WirelessHART Mote Serial API Guide for more information.

TEMPERATURE SENSOR

The LTP5900-WHM has an onboard temperature sensor. The temperature readings are available locally through the mote serial API and through the network at the manager via the XML API. For more information, refer to the SmartMesh WirelessHART Mote Serial API Guide, SmartMesh WirelessHART Manager API Guide.

Table 8. Temperature Sensor

PARAMETER	MIN	TYP	MAX	UNITS
Sensor Input Range	–40		85	°C
Accuracy		±7		°C

SOFTWARE INSTALLATION

Devices are supplied with the flash erased, requiring programming as part of the OEMs manufacturing procedure. The US department of commerce places restrictions on export of systems and software supporting encryption. All of Linear/Dust product software produced to date contains encryption and is subject to export regulations and may be provided only via MyLinear, https://www.linear.com/mylinear. Customers purchasing SmartMesh products will receive a certificate containing a registration key and registration instructions with their order. After registering with the key, customers will be able to download SmartMesh software images from MyLinear. Once registered, customers will receive automated e-mail notifications as software updates are made available.

Linear Technology offers the DC9010, in circuit programmer for the Eterna based products. While the DC9010, is provided as a finished product, the design documents are provided as a reference for customers.

Once software has been loaded, devices can be configured via the API port. Configuration commands and settings are defined in SmartMesh WirelessHART Mote API Guide.

APPLICATIONS INFORMATION

REGULATORY AND STANDARDS COMPLIANCE

Radio Certification

The LTP5900 has been certified under a single modular certification, with the module name of ETERNA1. Following the regulatory requirements provided in the ETERNA1 User's Guide enables customers to ship products in the supported geographies, by simply completing an unintentional radiator scan of the finished product(s). The ETERNA1 User's Guide also provides the technical information needed to enable customers to further certify either the modules or products based upon the modules in geographies that have not or do not support modular certification.

Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances 2 (RoHS 2) is a directive that places maximum concentration limits on the use of certain hazardous substances in electrical and electronic equipment. Linear Technology is committed to meeting the requirements of the European Community directive 2011/65/EU.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2011/65/EU.

The RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Halogen-free mold compound
- RoHS-compliant and 245 °C re-flow compatible

Note: Customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2011/65/EU. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

SOLDERING INFORMATION

The LTP5900 is suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260°C. A more detailed description of layout recommendations, assembly procedures and design considerations is included in the LTP5900 Hardware Integration Guide.

INDUSTRIAL ENVIRONMENT OPERATION

The LTP5900-WHM is designed to meet the specifications of harsh industrial environments which includes:

- **Shock and Vibration**—The LTP5900-WHM complies with high vibration pipeline testing, as specified in IEC 61298-3.
- **Temperature Extremes**—The LTP5900-WHM is designed for industrial storage and operational temperature range of –40°C to 85°C.

ENCRYPTION CIPHER

The LTP5900-WHM's 128-bit Advanced Encryption Standard (AES) cipher has been certified compliant to the United States National Institute of Standards and Technology (NIST) FIPS-197 (NIST certificate number, AES: 1437). To view the FIPS-197 validation list, go to: http://csrc.nist.gov/groups/STM/cavp/documents/aes/aesval.html

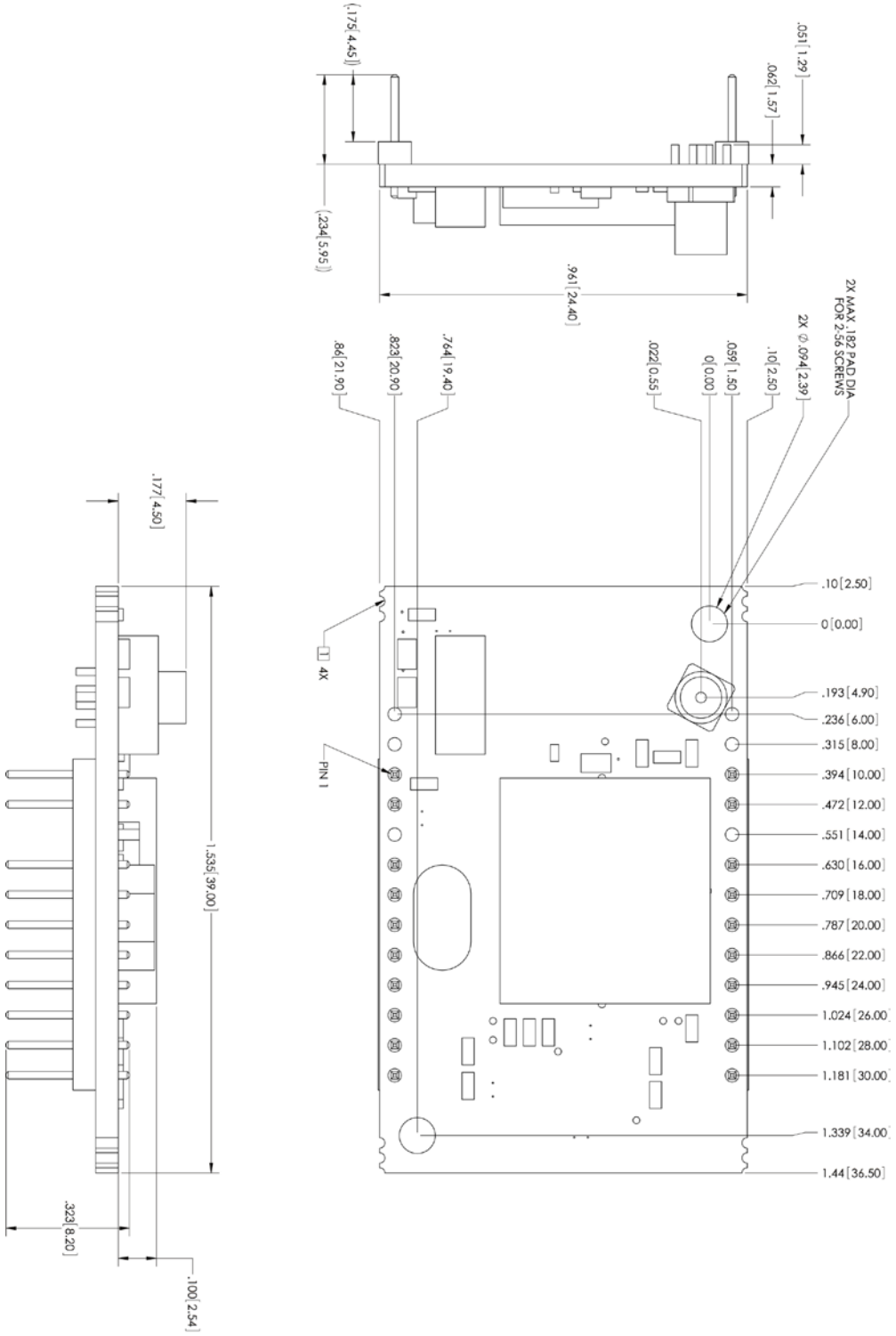
RELATED DOCUMENTATION

- LTP5900-WHM Integration Guide
- SmartMesh WirelessHART Mote Serial API Guide

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTP5900-WHM#packaging for the most recent package drawings.

PC Package
22-Lead (39mm × 24.4mm) PCB
(Reference LTC DWG # 05-08-1001 Rev D)



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/16	Added Software Installation section.	11