LTP5901-IPA/LTP5902-IPA

SmartMesh IP Access Point (AP) Mote
2.4GHz 802.15.4e Wireless AP Mote

NETWORK FEATURES

- Complete **Radio Transceiver, Embedded Processor**, and **Networking Software** for Forming a Self-Healing Mesh Network
- SmartMesh® Networks Incorporate:
  - Time Synchronized Network-Wide Scheduling
  - Per Transmission Frequency Hopping
  - Redundant Spatially Diverse Topologies
  - Network-Wide Reliability and Power Optimization
  - NIST Certified Security
- SmartMesh Networks Deliver:
  - >99.999% Network Reliability Achieved in the Most Challenging RF Environments
  - Sub 50µA Routing Nodes
- Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

LTP5901/2-IPA FEATURES

- Provides Network Access Point Radio Functions for SmartMesh VManager
- Supports Networks of Thousands of Nodes, in Combination with VManager Network Manager Software
- Enables Redundant Network Ingress/Egress with Automatic Failover
- RF Modular Certification Include USA, Canada, Japan, EU, Taiwan, Korea, India, Australia and New Zealand
- PCB Assembly with Chip Antenna (LTP5901-IPA) or with MMCX Antenna Connector (LTP5902-IPA)

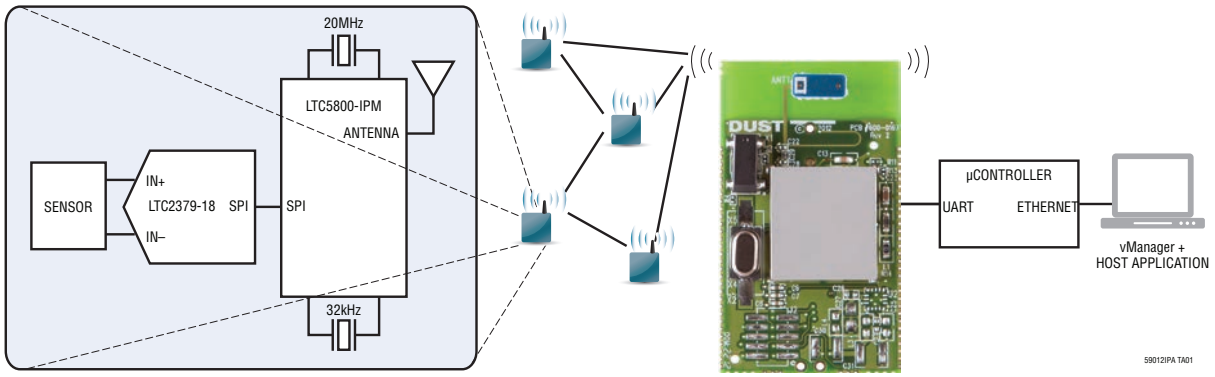
DESCRIPTION

SmartMesh IP™ wireless sensor networks are self managing, low power internet protocol (IP) networks built from wireless nodes called motes. The LTP™5901-IPA/LTP5902-IPA is the IP Access Point Mote™ (AP Mote™) in the Eterna®* family of IEEE 802.15.4e system-on-chip (SoC) solutions, featuring a highly integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software. SmartMesh IP software provided with the LTP5901/LTP5902-IPA is a fully tested and validated binary image.

Based on the IETF 6LoWPAN and IEEE-802.15.4e standards, the LTP5901/LTP5902-IPA, executing SmartMesh IP Access Point Mote software, provides a data ingress/egress point via a two wire UART interface. In combination with the VManager™ software the LTP5901/LTP5902-IPA enables very large scale networks with full redundancy and automatic failover, in addition to providing a means to scale network throughput. With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery-powered operation.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION



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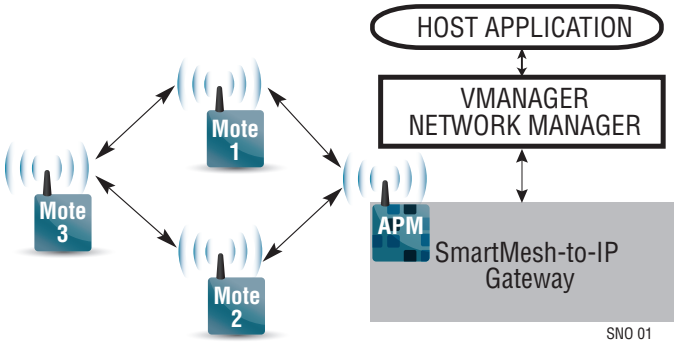
SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop, mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

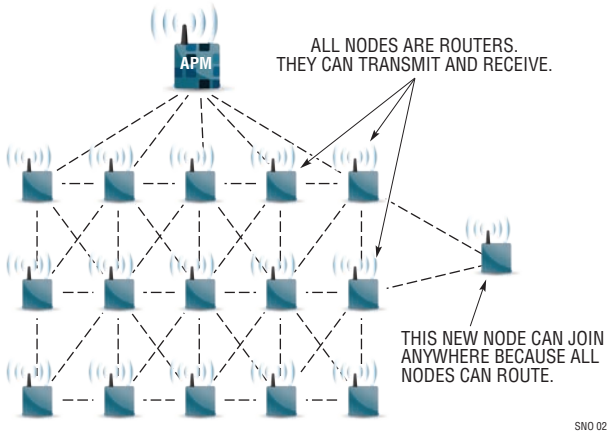
SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into time slots, which enable collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g., mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

A network begins to form when the network manager instructs its AP Mote to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.



An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g. quality of used paths, and lists of potential paths) and periodically sends that information to the network manager in packets called health reports. The network manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments.

The use of TSCH allows SmartMesh devices to sleep in-between scheduled communications and draw very little power in this state. Motes are only active in time slots where they are scheduled to transmit or receive, typically resulting in a duty cycle of <1%. The optimization software in the Network Manager coordinates this schedule automatically. When combined with the Eterna low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.



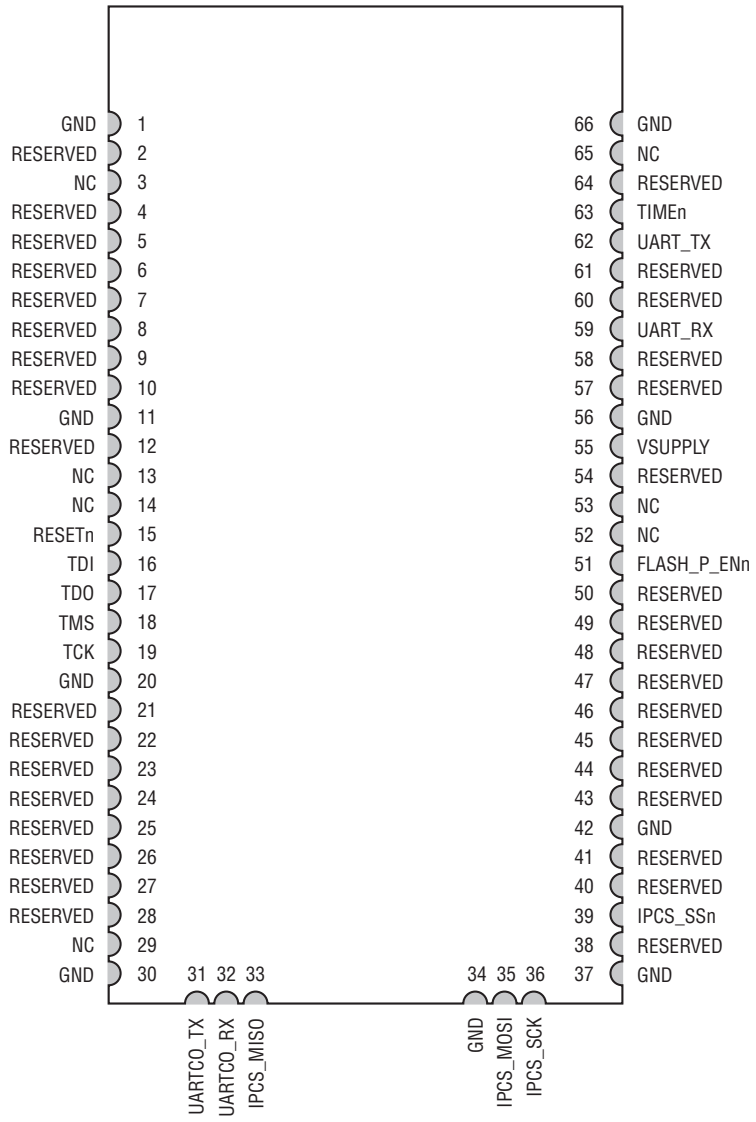
At the heart of SmartMesh motes and AP motes is the Eterna IEEE 802.15.4e system-on-chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of application programming interfaces (APIs) which allows a host application to interact with the network, e.g. to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed. For a complete description of the system, refer to the SmartMesh IP User's Guide.

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage on VSUPPLY.....4.20V
Voltage on Any Digital I/O Pin ....–0.3V to VSUPPLY + 0.3V
Input RF Level.....10dBm
Storage Temperature Range (Note 3).....–55°C to 105°C
Operating Temperature Range
LTP5901I/LPT5902I.....–40°C to 85°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTP5901/LTP5902-IPA.

PIN CONFIGURATION



PC PACKAGE
66-LEAD PCB

ORDER INFORMATION

http://www.linear.com/product/LTP5901-IPA#orderinfo

LEAD FREE FINISH†	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTP5901IPC-IPMA#PBF	LTP5901IPC-IPMA#PBF	66-Lead (42mm × 24mm × 5.5mm) PCB with Chip Antenna	–40°C to 85°C
LTP5902IPC-IPMA#PBF	LTP5902IPC-IPMA#PBF	66-Lead (37.5mm × 24mm × 5.5mm) PCB with MMCX Connector	–40°C to 85°C

† This product ships with the flash erased at the time of order. OEMs will need to program devices during development and manufacturing. Purchase of LTP5901IPC-IPMA#PBF or LTP5902IPC-IPMA#PBF components includes access to download IP Access Point Mote software via http://www.linear.com/mylinear. See the Software Installation section for details.

*The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VSUPPLY	Supply Voltage	Including Noise and Load Regulation	●	2.1		3.76	V
	Supply Noise	50Hz to 2MHz	●			250	mV
	Operating Relative Humidity	Non-Condensing	●	10		90	% RH
	Temperature Ramp Rate While Operating in Network		●	–8		8	°C/min

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

OPERATION/STATE	CONDITIONS		MIN	TYP	MAX	UNITS
Power-On Reset	During Power-On Reset, Maximum 750µs + VSUPPLY Rise Time from 1V to 1.9V			12		mA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK at 3.33MHz			20		mA
Peak Operating Current 0dBm 8dBm	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum Duration 4.33 ms.			 26 30		 mA mA
Active	ARM Cortex-M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 14.7456MHz, VCORE = 1.2V			2.6		mA
Flash Write	Single Bank Flash Write			3.7		mA
Flash Erase	Single Bank Page or Mass Erase			2.5		mA
Radio Tx 0dBm 8dBm	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 14.7456MHz.			 5.9 10.2		 mA mA
Radio Rx	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 14.7456MHz.			5.0		mA

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where k = 11 to 25, as Defined by IEEE.802.15.4	●		2405 + 5 • (k-11)		MHz
Raw Data Rate		●		250		kbps
Antenna Pin ESD Protection	HBM Per JEDEC JESD22-A114F (Note 2)			±6000		V
Range Indoor Outdoor Free Space	25°C, 50% RH, +2dBi Omnidirectional Antenna, Antenna 2m Above Ground (Note 4)			 100 300 1200		 m m m

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)			–93		dBm
Receiver Sensitivity	PER = 50%			–95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets			0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)			22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)			19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)			40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)			36		dBc
Second Alternate Channel Rejection	Desired Signal at –82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)			42		dBc
Co-Channel Rejection	Desired Signal at –82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%			–6		dBc
LO Feed Through				–55		dBm
Frequency Error Tolerance (Note 6)				±50		ppm
Symbol Error Tolerance				±50		ppm
Received Signal Strength Indicator (RSSI) Input Range				–90 to -10		dBm
RSSI Accuracy				±6		dB
RSSI Resolution				1		dB

RADIO TRANSMITTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	Delivered to a 50Ω Load					
High Calibrated Setting				8		dBm
Low Calibrated Setting				0		dBm
Spurious Emissions	Conducted Measurement with a 50Ω Single-Ended Load, 8dBm Output Power. All Measurements Made with Max Hold.					
30MHz to 1000MHz	R_{BW} = 120kHz, V_{BW} = 100Hz			< –70		dBm
1GHz to 12.75GHz	R_{BW} = 1MHz, V_{BW} = 3MHz			–45		dBm
2.4GHz ISM Upper Band Edge (Peak)	R_{BW} = 1MHz, V_{BW} = 3MHz			–37		dBm
2.4GHz ISM Upper Band Edge (Average)	R_{BW} = 1MHz, V_{BW} = 10Hz			–49		dBm
2.4GHz ISM Lower Band Edge	R_{BW} = 100kHz, V_{BW} = 100kHz			–45		dBc
Harmonic Emissions	Conducted Measurement Delivered to a 50Ω Load, 8dBm Output Power, Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz.					
2nd Harmonic				–50		dBm
3rd Harmonic				–45		dBm

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		●	–0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{OL(MAX)}$ = 1.2mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{OH(MAX)}$ = –0.8mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 2, Low Drive, $I_{OL(MAX)}$ = 2.2mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 2, Low Drive, $I_{OH(MAX)}$ = –1.6mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 2, High Drive, $I_{OL(MAX)}$ = 4.5mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 2, High Drive, $I_{OH(MAX)}$ = –3.2mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	Input Leakage Current	Input Driven to VSUPPLY or GND			50		nA
	Pull-Up/Pull-Down Resistance				50		kΩ

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C			±0.25		°C
Slope Error				±0.033		°C/°C

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	RESETn Pulse Width		●	125			µs
	Total Capacitance	Note 12	●			6	µF
	Total Inductance	Note 12	●			3	µH
	Network Upstream Throughput	Note 12	●			40	Pkts/s

UART AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
	Permitted Rx Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	–2		2	%
	Generated Tx Baud Rate Error	Both API and CLI UARTs	●	–1		1	%
$t_{RX\_INTERBYTE}$	Receive Inter-Byte Delay		●			1	Bit Period
$t_{TX\_INTERPACKET}$	Transmit Inter-Packet Delay		●	1			Bit Period

TIMEn PPS AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
	TIMEn PPS Period		●		1		s
	TIMEn PPS Error		●	-250		250	ns
	TIMEn Pulse Width (High or Low)		●	100			ms
$t_{RFT\_to\_ST}$	Time from receipt of readyForTime notification to completion of setParameter<time> command. **(Note 9)**		●			250	ms

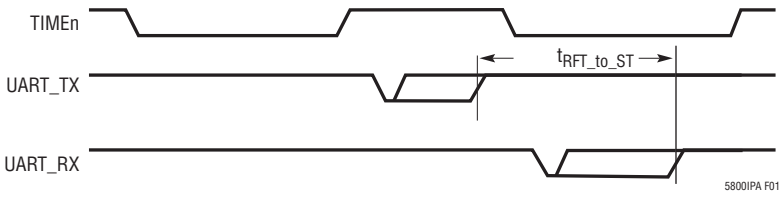


Figure 1. TIMEn PPS Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 10)		●			21	µs
t_{PAGE_ERASE}	Time to Erase a 2k Byte Page (Note 10)		●			21	ms
t_{MASS_ERASE}	Time to Erase 256k Byte Flash Bank (Note 10)		●			21	ms
	Data Retention	25°C 85°C 105°C		100 20 8			Years Years Years

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{FP\_EN\_to\_RESET}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0			ns
t_{FP_ENTER}	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125			µs
t_{FP_EXIT}	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn (Note 11)		●	10			µs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15			ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15			ns
t_{CK}	IPCS_SCK Period		●	300			ns
t_{DIS}	IPCS_MOSI Data Setup		●	15			ns
t_{DIH}	IPCS_MOSI Data Hold		●	5			ns
t_{DOV}	IPCS_MISO Data Valid		●	3			ns
t_{OFF}	IPCS_MISO Data Three-State		●	0		30	ns

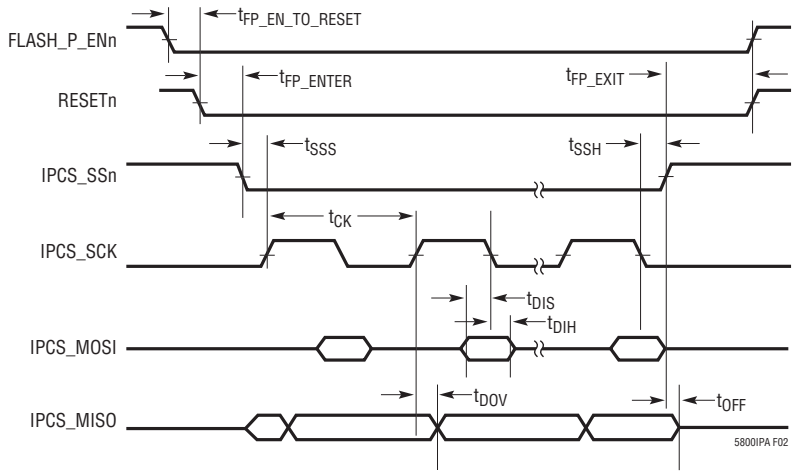


Figure 2. Flash Programming Interface Timing

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to Eterna. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data. See FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/findstds/standard/802.15.4-2011.html.

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than ±40ppm.

Note 7: Per pin I/O types are provided in the Pin Functions section.

Note 8: V_{IH} maximum voltage input must respect the VSUPPLY maximum voltage specification.

Note 9: See the SmartMesh IP User's Guide for the readyForTime notification to completion of setParameter<time> command definitions.

Note 10: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 11: Following erase or write transfers, the IPCS SPI slave status register, 0xD7 must be polled to determine the completion time of the erase or write operation prior to negating either FLASH_P_ENn or RESETn.

Note 12: Guaranteed by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

In mesh networks data can propagate from the manager to the motes, downstream, or from the motes to the manager, upstream, via a sequence of transmissions from one device to the next. As shown in Figure 4, data originating from mote P1 may propagate to the manager directly or through P2. As mote P1 may directly communicate with the manager, mote P1 is referred to as a 1-hop mote. Data originating from mote D1, must propagate through at least one other mote, P2 or P1, and as a result is referred to as a 2-hop mote. The fewest number of hops from a mote to the AP Mote determines the hop depth.

Eterna provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the AP Mote and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was thus affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between –40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for 8 hours, followed by rapid cycling between –5°C and 45°C for 8 hours, and lastly, rapid cycling between –40°C and 15°C for 8 hours.

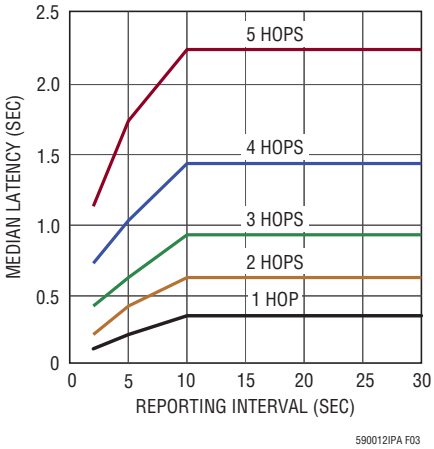


Figure 3. Packet Latency vs Reporting Interval

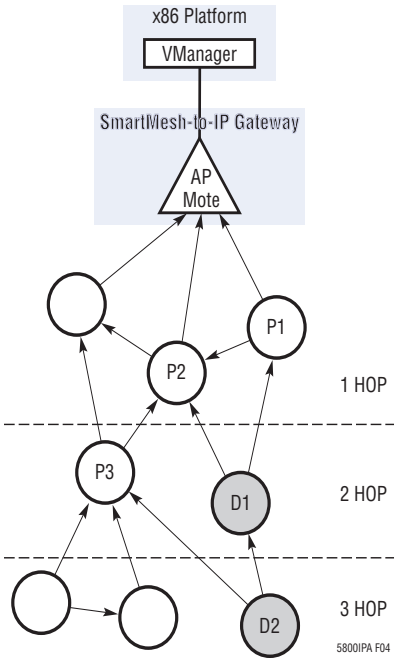
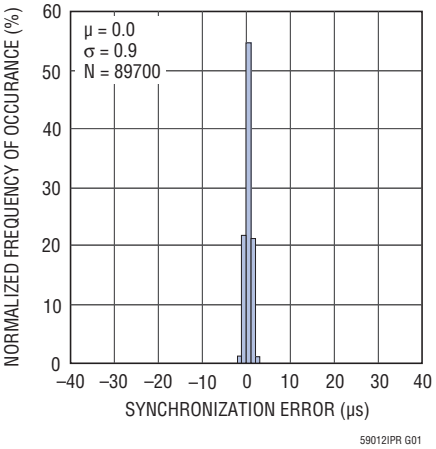


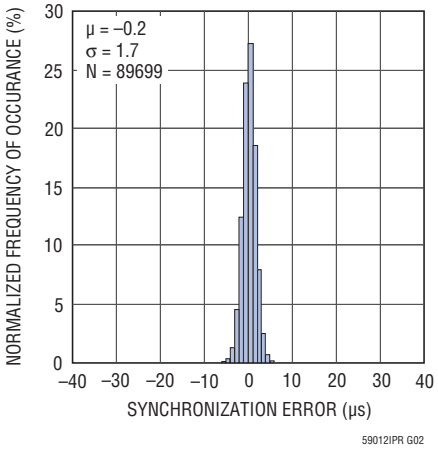
Figure 4. Example Network Graph

TYPICAL PERFORMANCE CHARACTERISTICS

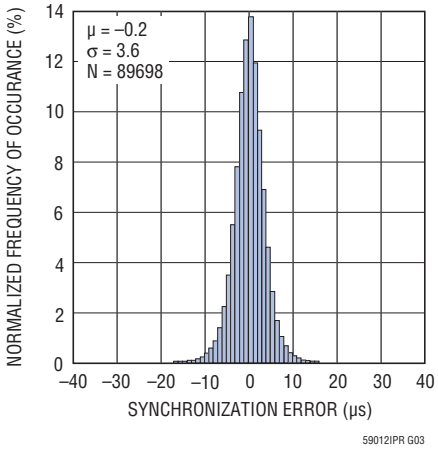
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, Room Temperature



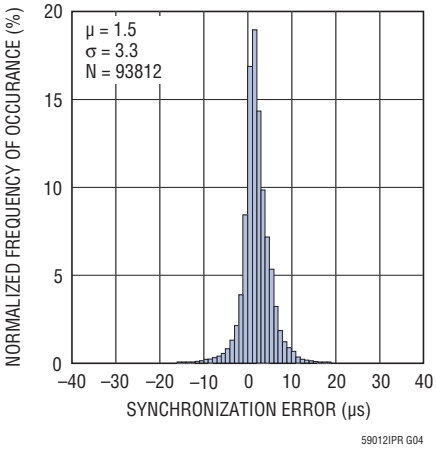
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, Room Temperature



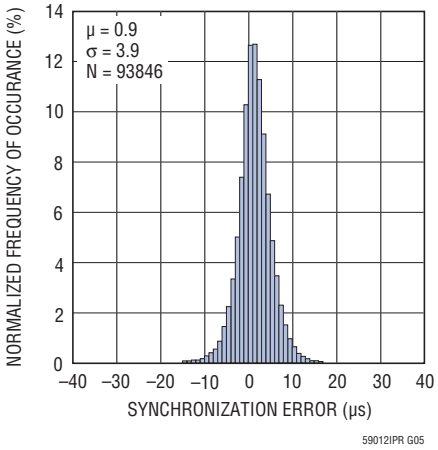
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, Room Temperature



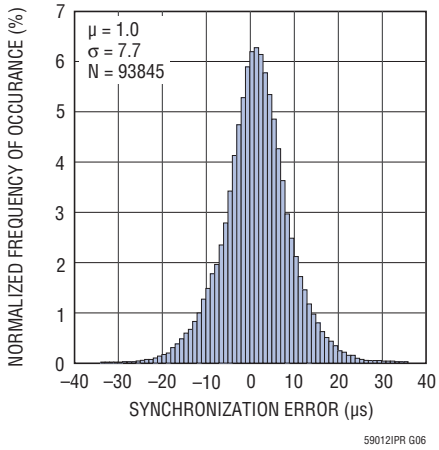
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 2°C/Min.



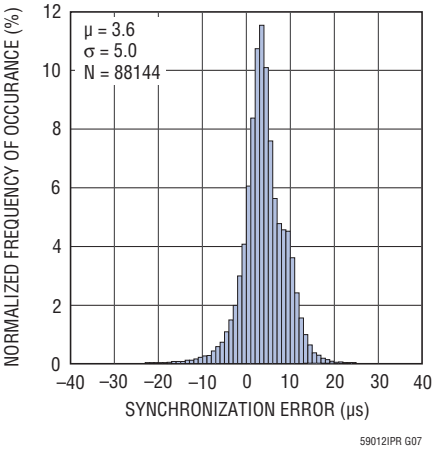
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 2°C/Min.



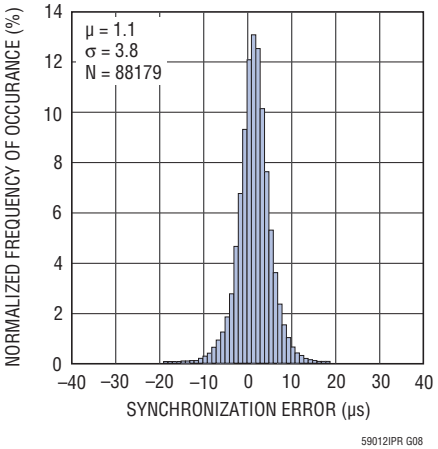
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 2°C/Min.



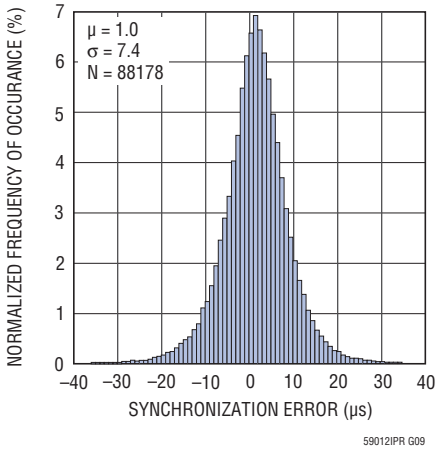
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 8°C/Min.



TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 8°C/Min.

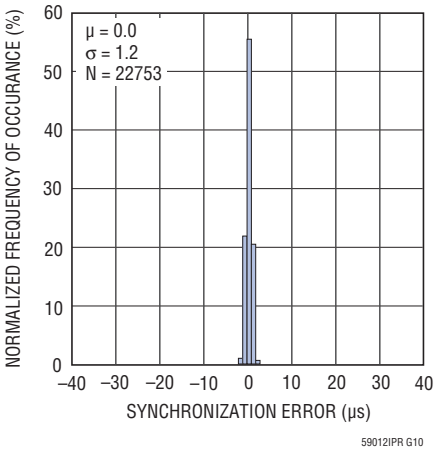


TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 8°C/Min.

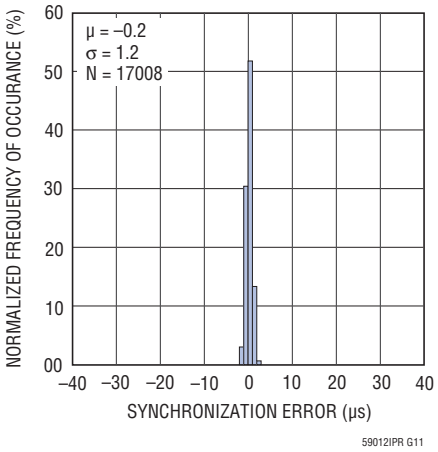


TYPICAL PERFORMANCE CHARACTERISTICS

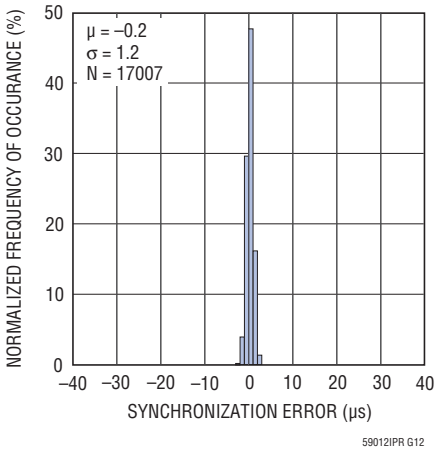
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, Room Temperature



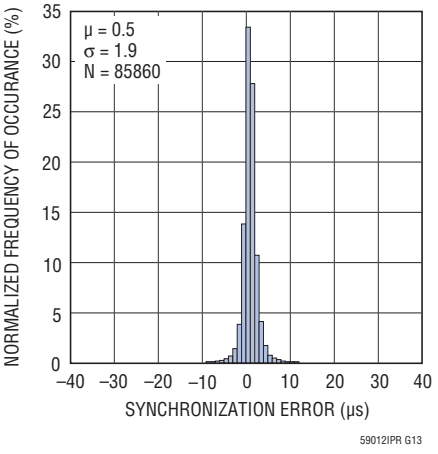
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, Room Temperature



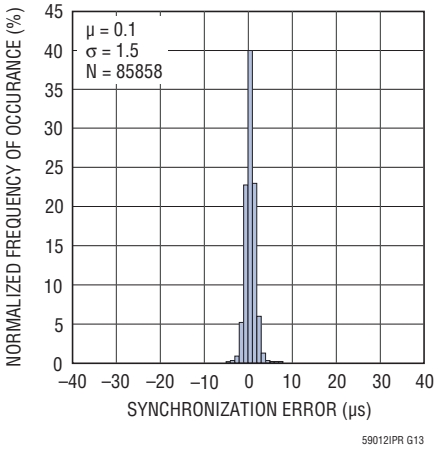
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, Room Temperature



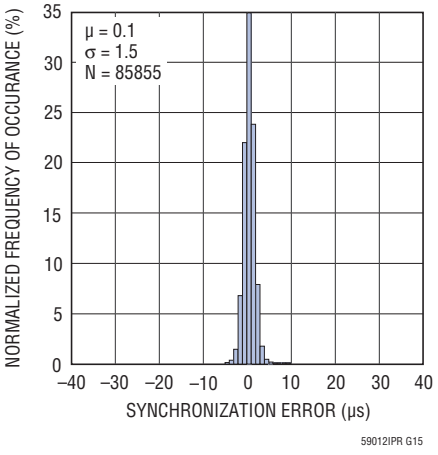
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 2°C/Min.



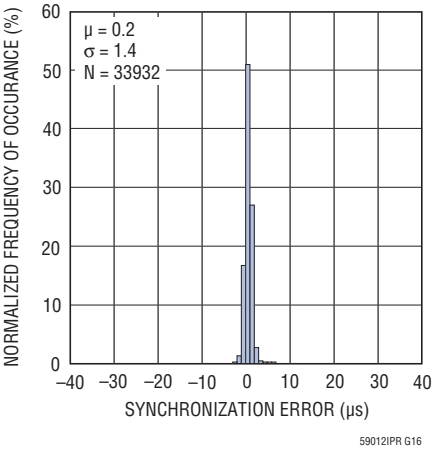
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 2°C/Min.



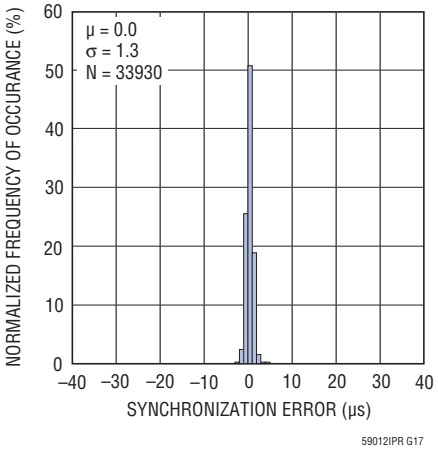
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 2°C/Min.



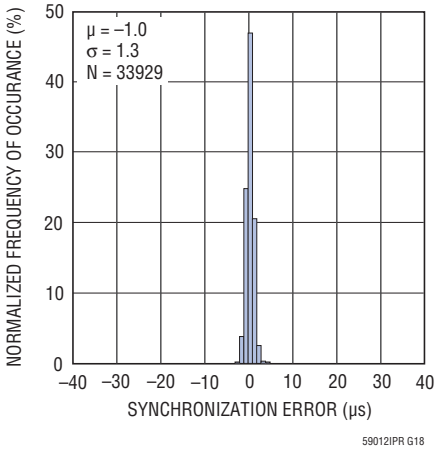
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 8°C/Min.



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 8°C/Min.



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 8°C/Min.



PIN FUNCTIONS

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **No** column provides the pin number. The second column lists the function. The **Type** column lists the I/O type. The **I/O** column lists the direction of the signal relative to Eterna. The **Pull** column shows which signals have a fixed passive pull-up or pull-down. The **Description** column provides a brief signal description.

NO	POWER SUPPLY	TYPE	I/O	PULL	DESCRIPTION
1	GND	Power	-	-	Ground Connection
11	GND	Power	-	-	Ground Connection
20	GND	Power	-	-	Ground Connection
30	GND	Power	-	-	Ground Connection
34	GND	Power	-	-	Ground Connection
37	GND	Power	-	-	Ground Connection
42	GND	Power	-	-	Ground Connection
56	GND	Power	-	-	Ground Connection
66	GND	Power	-	-	Ground Connection
55	VSUPPLY	Power	-	-	Power Supply Input to Eterna

NO	RADIO	TYPE	I/O	PULL	DESCRIPTION
-	ANTENNA	N/A	N/A	-	Chip Antenna (LTP5901) or MMCX Connector (LPT5902)

NO	RESET	TYPE	I/O	PULL	DESCRIPTION
15	RESETn	1	I	UP	Reset Input, Active Low

NO	JTAG	TYPE	I/O	PULL	DESCRIPTION
16	TDI	1	I	UP	JTAG Test Data In
17	TDO	1	O	-	JTAG Test Data Out
18	TMS	1	I	UP	JTAG Test Mode Select
19	TCK	1	I	DOWN	JTAG Test Clock

NO	SPECIAL PURPOSE	TYPE	I/O	PULL	DESCRIPTION
63	TIMEn	1 (Note 13)	I	-	Time Capture Request, Active Low

NO	IPCS SPI/FLASH PROGRAMMING (NOTE 14)	TYPE	I/O	PULL	DESCRIPTION
33	IPCS_MISO	2	O	-	SPI Flash Emulation (MISO) Master in Slave Out Port
35	IPCS_MOSI	1	I	-	SPI Flash Emulation (MOSI) Master Out Slave in Port
36	IPCS_SCK	1	I	-	SPI Flash Emulation (SCK) Serial Clock Port
39	IPCS_SSn	1	I	-	SPI Flash Emulation Slave Select, Active Low
51	FLASH_P_ENn	1	I	UP	Flash Program Enable, Active Low

NO	API UART	TYPE	I/O	PULL	DESCRIPTION
59	UART_RX	1 (Note 13)	I	-	UART Receive
62	UART_TX	2	O	-	UART Transmit

Note 13: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage.

Note 14: Embedded programming over the IPCS SPI bus is only available when RESETn is asserted.

PIN FUNCTIONS

VSUPPLY: System and I/O Power Supply. Provides power to the module. The digital-interface I/O voltages are also set by this voltage.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the MMCX connector should be 50Ω, single-ended with respect to ground.

RESETn: The asynchronous reset signal is internally pulled up. Resetting Eterna will result in the ARM Cortex-M3 rebooting and loss of network connectivity. Use of this signal for resetting Eterna is not recommended, except during power-on and in-circuit programming.

TMS, TCK, TDI, TDO: JTAG port supporting software debug and boundary scan.

UART_RX, UART_TX: The HDLC coded API UART interface provided the primary mechanism for communication between the SmartMesh-to-IP Gateway CPU and the LTP5901/2.

TIMEn: The rising edge of a Pulse Per Second (PPS) signal at the TIMEn input provides the AP Mote with the network timing reference. The use of a PPS input is optional - see the Access Point section of the SmartMesh IP User's Guide for details.

UARTC0_RX, UARTC0_TX: The CLI UART provides a mechanism for monitoring, configuration and control of Eterna during operation.

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The In-circuit programming control system (IPCS) bus enables in-circuit programming of Eterna's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

OPERATION

NETWORK MANAGEMENT OPTIONS

SmartMesh IP managers provide dynamic network optimization, deterministic power management, intelligent routing, and configurable bandwidth allocation while achieving carrier class data reliability and low power operation. Linear Technology offers two solutions to manage SmartMesh IP Networks: Embedded Manager products such as the LTP5902-IPR and VManager, a software solution, which operates in tandem with one or more Access Point Motes, such as the LTP5902-IPA. For a complete description of VManager please refer to the SmartMesh IP User's Guide.

VMANAGER + AP MOTE BENEFITS

While the SmartMesh IP Embedded Manager form factor provides convenience for many applications, it has some limitations due to resource constraints associated with a SoC. The VManager resolves many of the limitations of a single chip solution by moving the management function to a more powerful computing platform. With the "manager" running on a range of x86 hardware platforms in a Virtual Machine, customers have the flexibility to select from a broad range of existing third party hardware, while the VManager software has the resources needed to scale. The feature highlights of this larger scale manager are as follows:

- 100% compatible with all SmartMesh IP Motes
- Increased Management capability
  - Network scale to thousands of motes
  - Network throughput scales at 40 pkt/sec per AP Mote upstream - more than 12x the embedded manager
  - Downstream throughput scales up to 17 pkt/sec per AP - up to 96x the embedded manager
  - AP Mote and management function hot redundancy
- Optional GPS Integration
  - Locking of network time to real time
  - Support of discontinuous network segments in a single network
  - Shared sense of time across all network segments

AP MOTE / VMANAGER COMMUNICATION

VManager may be connected to an AP Mote over a TCP/IP socket or directly over a COM port. COM ports may be implemented as:

- Embedded UART(s) operating at LVTTL switching thresholds
- UART(s) over USB
- RS-485

A SmartMesh-to-IP Gateway typically provides the connection between the AP Mote the VManager via a TCP/IP Socket. The corresponding TCP/IP network can take many forms, including:

- Ethernet
- WiFi
- Cellular
- DSL
- Cable Modem

For detailed information on AP Mote implementation see the SmartMesh IP User's Guide.

AP MOTE TIME SYNCHRONIZATION

The SmartMesh IP network protocol establishes network wide timing synchronization of all wireless devices. To accomplish this, each network must have a single time base. The LTP5901/2-IPA supports operating from an internal time base, network time base or an external time base. See the Access Points section of the SmartMesh IP User's Guide for the engineering trade-offs with respect to AP Mote time base options.

OPERATION

The LTP5901/LTP5902 is the world's most energy-efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex-M3, best-in-class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 5, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low power states. Items in the gray shaded region labeled analog core correspond to the analog/RF components.

NETWORKING

The LTP5901/2-IPA access point mote provides the ingress/egress point at the mesh network boundary via the API UART interface. The mesh network management is handled by the VManager software, which also provides dynamic network optimization, deterministic power management, intelligent routing, and configurable bandwidth allocation while achieving carrier class data reliability and low power operation.

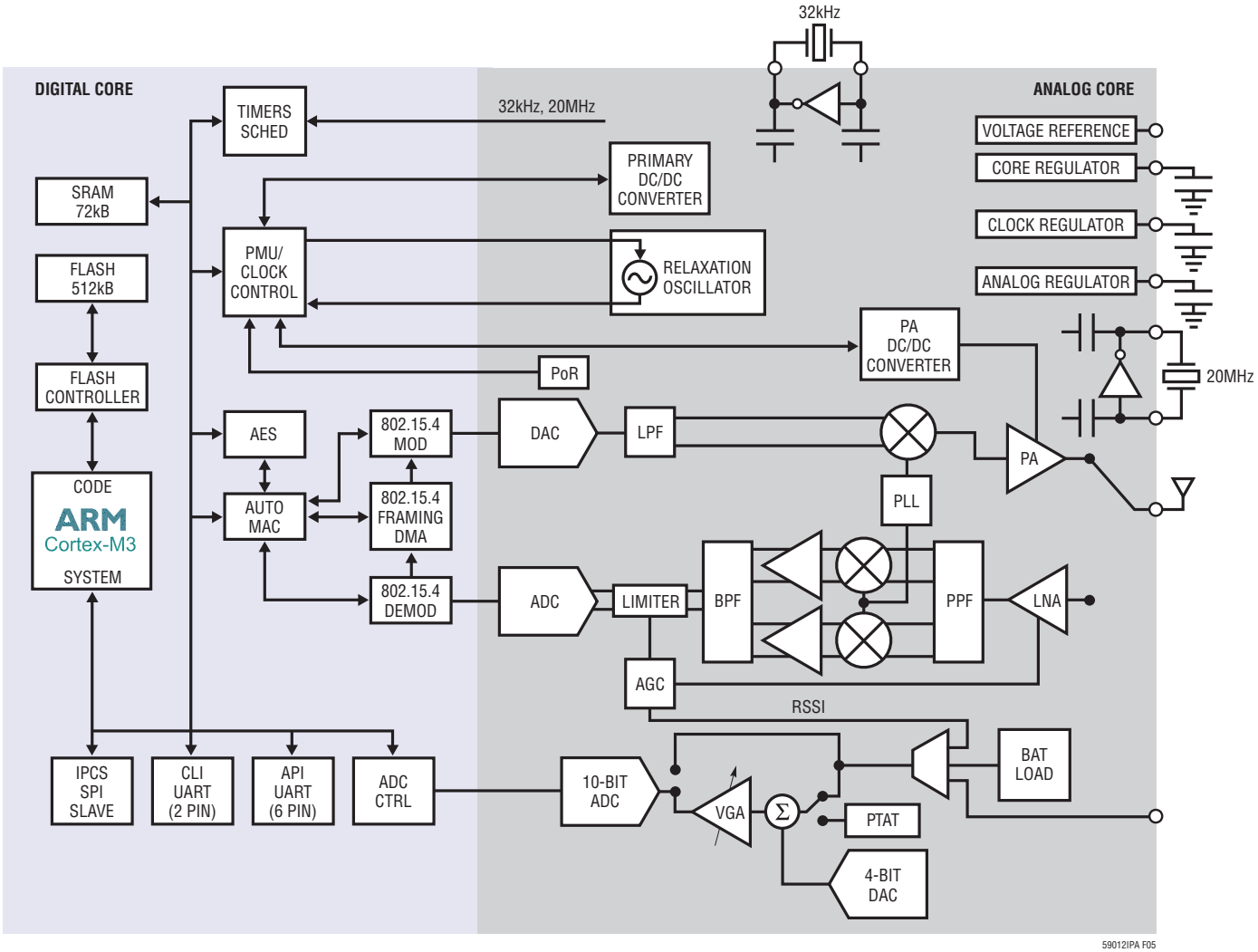


Figure 5. Eterna Block Diagram

OPERATION

CONFIGURABLE BANDWIDTH ALLOCATION

SmartMesh networks provide configurations that enable users to make bandwidth and latency versus power trade-offs both network wide and on a per device basis. This flexibility enables solutions to be tailored to the application requirements, such as request/response, fast file transfer, and alerting. Relevant configuration parameters are described in the SmartMesh IP User's Guide. The Design trade-offs between network performance and current consumption are illustrated via the SmartMesh Power and Performance Estimator.

POWER SUPPLY

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize Eterna's energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low power state. Eterna's integrated power supply conditioning architecture, including the two integrated DC/DC converters and three integrated low dropout regulators, provides excellent rejection of supply noise. Eterna's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride, Li-SOCl2, sources and wide enough to support battery operation over a broad temperature range.

SUPPLY MONITORING AND RESET

Eterna integrates a power-on-reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. Eterna includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. The integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust nonvolatile storage solution.

PRECISION TIMING

A major feature of Eterna over competing 802.15.4 product offerings is its low power dedicated timing hardware and timing algorithms. This functionality provides timing precision two to three orders of magnitude better than any other low power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

TIME REFERENCES

Eterna includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 14.3728MHz.

32.768kHz Crystal

Once Eterna is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational and is used as the timing basis. See the State Diagram section, for a description of Eterna's operational states.

20MHz Crystal

The 20MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed.

RADIO

Eterna includes the lowest power commercially available 2.4GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to section Radio Specifications, for power consumption numbers). Eterna's integrated power amplifier

OPERATION

is calibrated and temperature-compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, Eterna uniquely includes a hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and advanced encryption standard (AES) peripherals. The hardware-based autonomous media access controller (MAC) minimizes CPU activity, thereby further decreasing power consumption.

UARTS

The principal network interface is through the application programming interface (API) UART. A command-line interface (CLI) UART is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred over the port and then automatically returning to their lowest power state after the conclusion of a transfer. The definition for packet encoding on the API UART interface can be found in the SmartMesh IP User's Guide.

API UART PROTOCOL

Unlike the LTP5901/2-IPM or the LTP5901/2-IPR the LTP5901/2-IPA operates its API UART interface without flow control, requiring only the UART_TX and UART_RX signals. The API UART is configured at 961.6 kbaud, one stop bit and no parity.

CLI UART

The command line interface (CLI) UART port is a two wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one stop bit and no parity. The CLI UART interface is intended to support command line instructions and response activity.

SECURITY

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. SmartMesh IP system solutions provide a FIPS-197 validated encryption scheme that includes authentication and encryption at the MAC and network layers with separate keys for each mote. This not only yields end-to-end security, but if a mote is somehow compromised, communication from other motes is still secure. A mechanism for secure key exchange allows for key rotation. To prevent physical attacks, Eterna includes hardware support for electronically locking devices, thereby preventing access to Eterna's flash and RAM memory and thus the keys and code stored therein.

SOFTWARE INSTALLATION

Devices are supplied with the flash erased, requiring programming as part of the OEMs manufacturing procedure. The US Department of Commerce places restrictions on export of systems and software supporting encryption. All of Linear/Dust product software produced to date contains encryption and is subject to export regulations and may be provided only via MyLinear, www.linear.com/mylinear. Customers purchasing SmartMesh products will receive a certificate containing a registration key and registration instructions with their order. After registering with the key, customers will be able to download SmartMesh software images from MyLinear. Once registered, customers will receive automated e-mail notifications as software updates are made avaialbe.

Linear Technology offers the DC9010, in circuit programmer for the Eterna based products. While the DC9010, is provided as a finished product, the design documents are provided as a reference for customers.

Once software has been loaded, devices can be configured via either the CLI or API ports. Configuration commands and settings are defined in the SmartMesh IP User's Guide and the SmartMesh IP VManager CLI Guide.

OPERATION

FLASH DATA RETENTION

Eterna contains internal flash (non-volatile memory) to store calibration results, unique ID, configuration settings and software images. Flash retention is specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive storage outside the operating temperature range of –40°C to 85°C is possible; although, this may result in a degradation of retention characteristics.

The degradation in flash retention for temperatures exceeding specified temperatures can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 0.6eV

k = 8.625 • 10^{-5}eV/°K

T_{USE} = is the specified temperature retention in °C

T_{STRESS} = actual storage temperature in °C

Example: Calculate the effect on retention when storing at a temperature of 105°C.

T_{STRESS} = 105°C

T_{USE} = 85°C

AF = 2.8

So the overall retention of the flash would be degraded by a factor of 2.8, reducing data retention from 20 years at 85°C to 7.1 years at 105°C.

STATE DIAGRAM

In order to provide capabilities and flexibility, the AP Mote operates in various states, as shown in Figure 6, and described in this section. State transitions shown in red are not recommended.

Fuse Table

Eterna's Fuse Table is a 2kB page in flash that contains two data structures. One structure supports hardware configuration immediately following power-on reset or the assertion of RESETn. The second structure supports configuration of software board support parameters. Fuse Tables are generated via the Fuse Table application described in the Board Specific Configuration Guide. Hardware configuration of I/O immediately following power-on reset provides a method to minimize leakage due to floating nets prior to software configuration. I/O leakage can contribute hundreds of microamperes of leakage per input, potentially stressing current limited supplies. Examples of software board support parameters include setting of UART modes, clock sources and trim values. Fuse Tables are loaded into flash using the same software and in-circuit programmer used to load software images as described in the Eterna Serial Programmer Guide.

Start-Up

Start-up occurs as a result of either crossing the power-on reset threshold or asserting RESETn. After the completion of power-on reset or the falling edge of an internally synchronized RESETn, Eterna loads its fuse table which, as described in the previous section, includes setting I/O direction. In this state, Eterna checks the state of the FLASH_P_ENn and RESETn and enters the serial flash emulation mode if both signals are asserted. If the FLASH_P_ENn pin is not asserted but RESETn is asserted, Eterna automatically reduces its energy consumption to a minimum until RESETn is released. Once RESETn is de-asserted, Eterna goes through a boot sequence, and then enters the active state.

OPERATION

Serial Flash Emulation

When both RESETn and FLASH_P_ENn are asserted, Eterna disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed.

Operation

Once Eterna has completed start-up Eterna transitions to the Operational states with either the CPU active or inactive.

Active State

In the Active State, Eterna's relaxation oscillator is running and peripherals are enabled as needed.

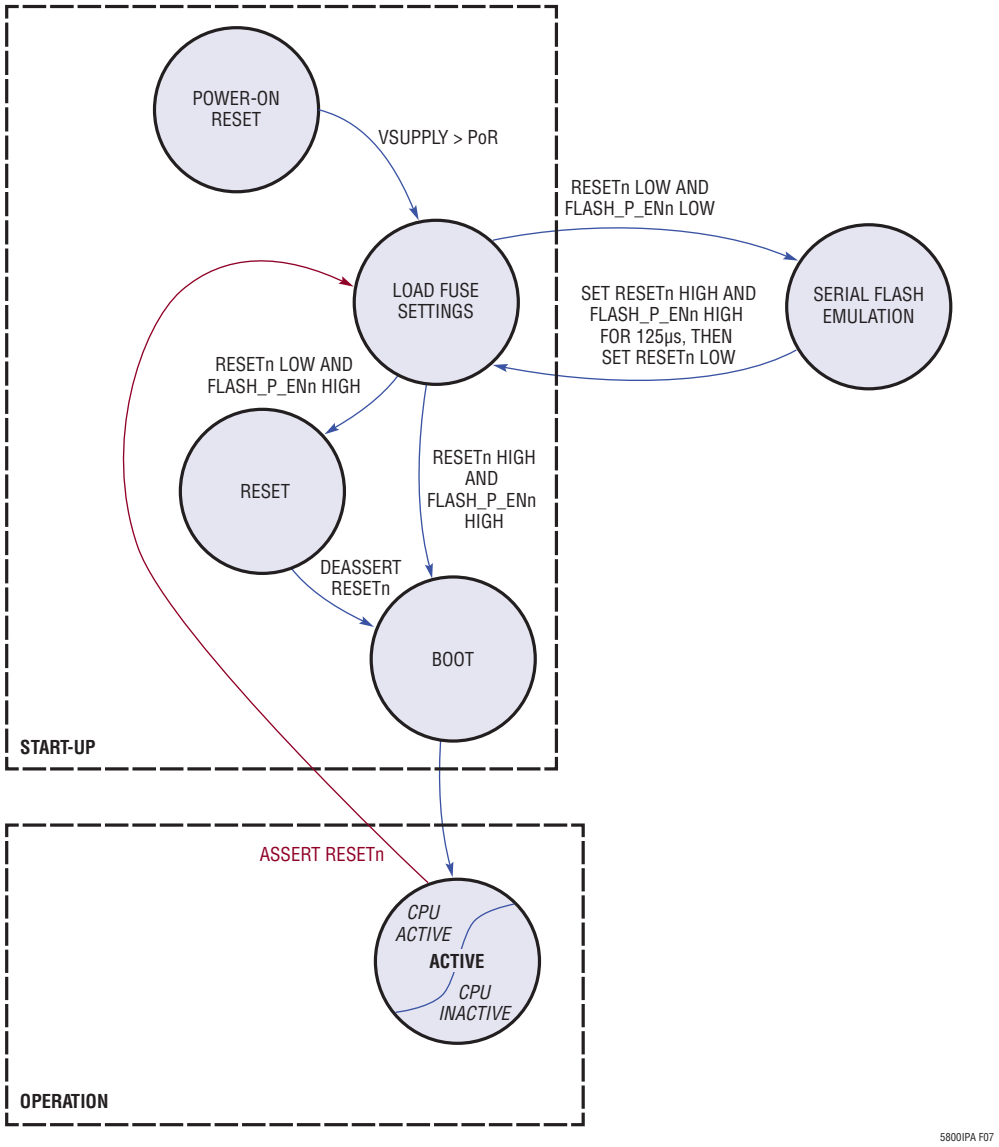


Figure 6. Eterna State Diagram

APPLICATIONS INFORMATION

REGULATORY AND STANDARDS COMPLIANCE

Radio Certification

The LTP5901 and LTP5902 have been certified under a single modular certification, with the module name of ETERNA2. Following the regulatory requirements provided in the ETERNA2 Users Guide can enable customers to ship products in the supported geographies, by simply completing an unintentional radiator scan of the finished product(s). The ETERNA2 Users Guide also provides the technical information needed to enable customers to further certify either the modules or products based upon the modules in geographies that have not or do not support modular certification.

Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of hazardous substances 2 (RoHS 2) is a directive that places maximum concentration limits on the use of certain hazardous substances in electrical and electronic equipment. Linear Technology is committed to meeting the requirements of the European Community directive 2011/65/EU.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2011/65/EU.

The RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Halogen-free mold compound
- RoHS-compliant and 245°C re-flow compatible

Note: Customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2011/65/EU. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

SOLDERING INFORMATION

The LTP5901 and LTP5902 are suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260°C. A more detailed description of layout recommendations, assembly procedures and design considerations is included in the LTP5901 and LTP5902 Hardware Integration Guide.

RELATED DOCUMENTATION

TITLE	LOCATION	DESCRIPTION
SmartMesh IP Users Guide	http://www.linear.com/docs/41880	Theory of operation for SmartMesh IP networks and motes
SmartMesh IP VManager API Guide	http://www.linear.com/docs/47487	Definitions of the applications interface commands available over the API UART
SmartMesh IP VManager CLI Guide	http://www.linear.com/docs/47486	Definitions of the command line interface commands available over the CLI UART
LTP5901 and LTP5902 Hardware Integration Guide	http://www.linear.com/docs/41877	Recommended practices for designing with the LTP5901 and LTP5902
ETERNA2 Users Guide	http://www.linear.com/docs/42916	The ETERNA2 module user's guide covering certification requirements for certified geographies and support documentation enabling customer certification in additional geographies for the LTP5901 and LTP5902

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTP5901-IPA#packaging for the most recent package drawings.

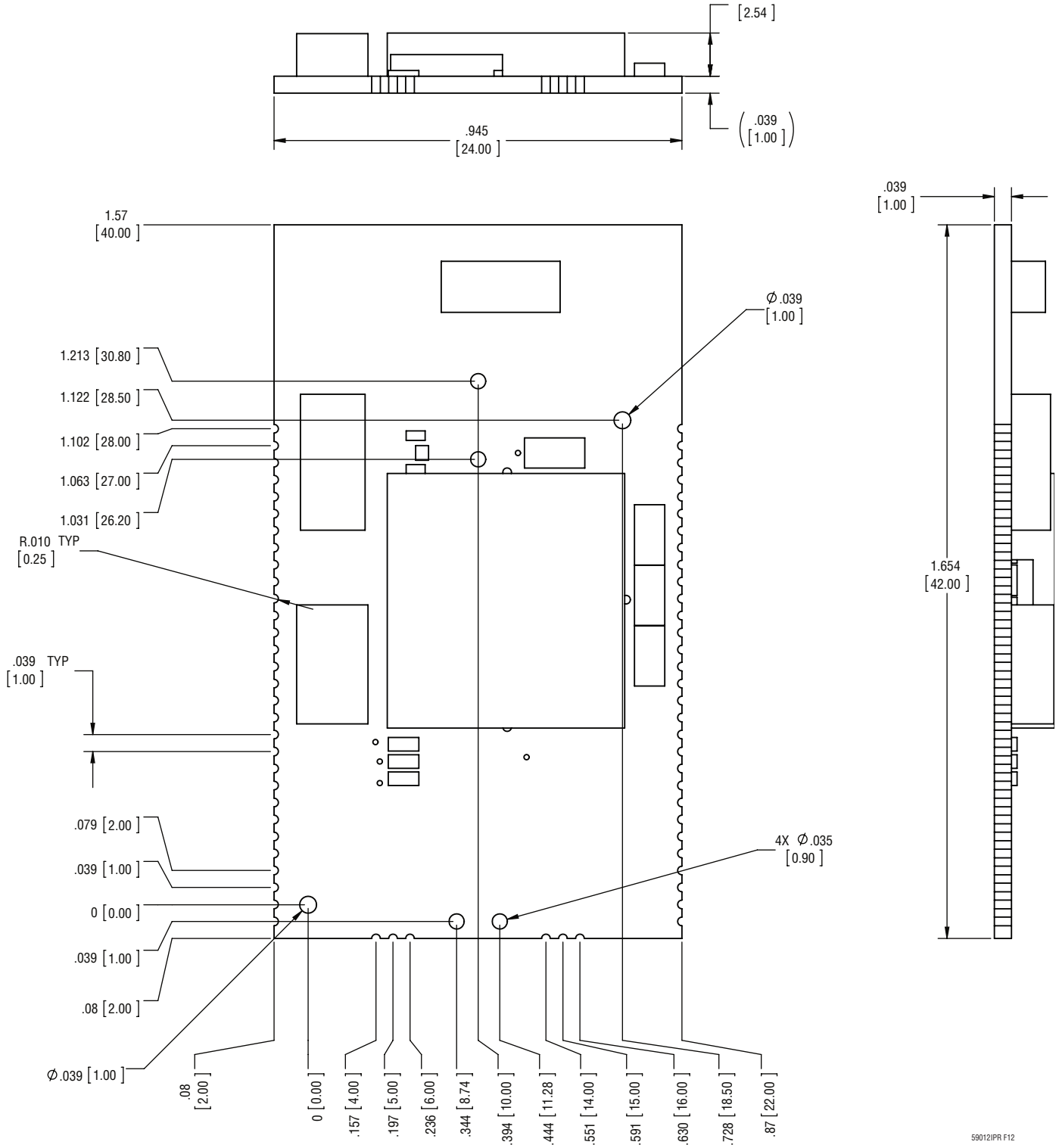


Figure 13. LTP5901 Mechanical Drawing

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTP5902-IPA#packaging for the most recent package drawings.

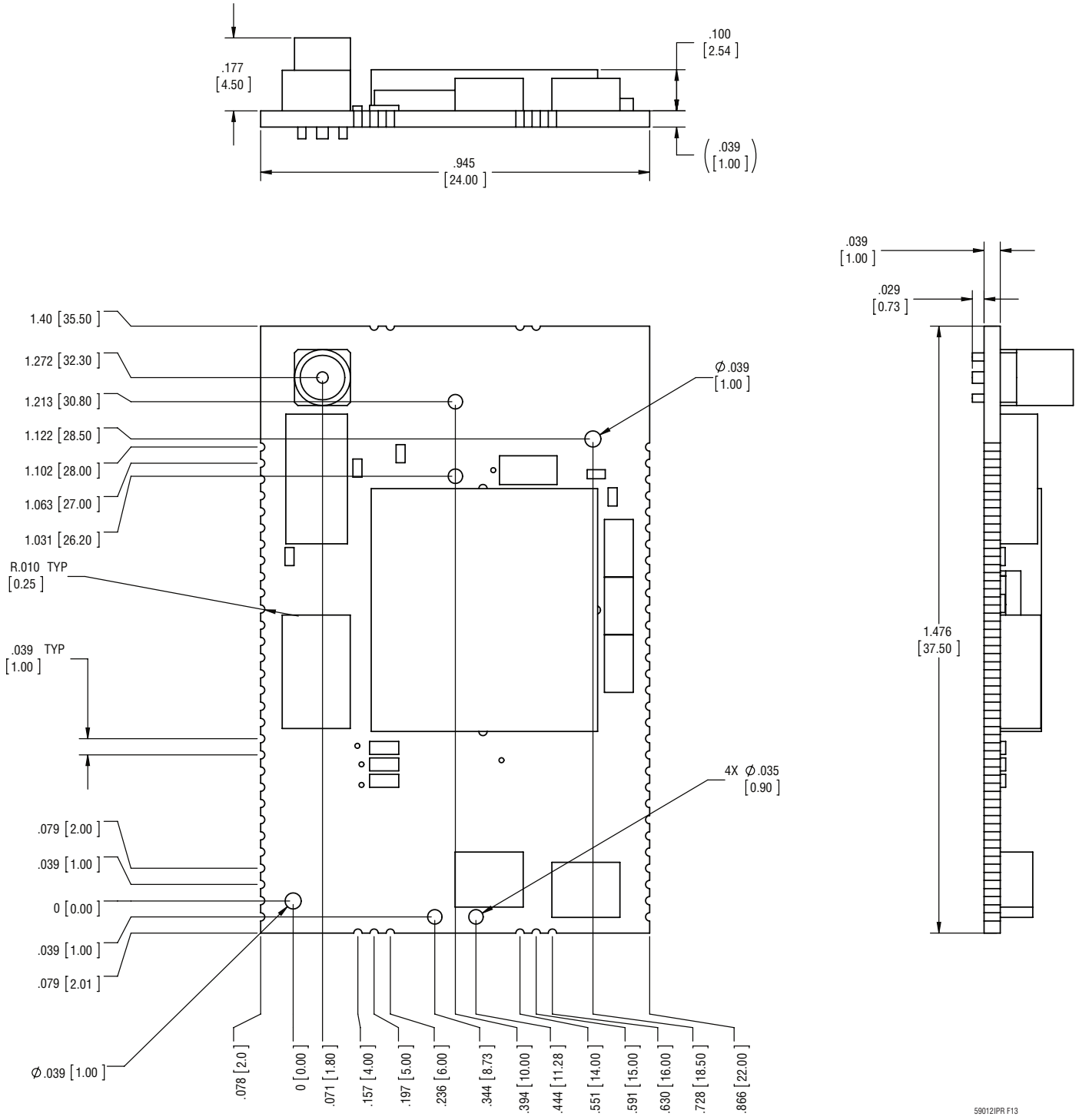


Figure 14. LTP5902 Mechanical Drawing