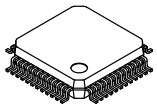
Multi-purpose Three-Phase BLDC Predriver

LV8968BBUW



SPQFP48
CASE 131AN

Overview

The LV8968BB is a multi−purpose three−phase BLDC predriver for automotive applications and developed in compliance with ISO 26262. This 3−phase peripheral predriver offers a BEMF (Back ElectroMotive Force) output and the wide operating voltage range and AEC−Q100 qualification make this device ideal for automotive applications. Six gate drivers provide 400 mA (typ) gate current to external power bridges allowing use of low resistance power FETs as well as logic level FETs. All FETs are protected against overcurrent, short−circuit, overtemperature and gate undervoltage. A multitude of protection and monitoring features make this device suitable for applications with functional safety (FuSa) requirements. Three independent low−side source pins allow multiple shunt measurement.

The device also includes a programmable linear regulator, a fast current sense amplifier and a window watchdog for microcontroller support. The SPI interface allows for real time parameter setup and diagnostics. Critical system parameters can be programmed into nonvolatile OTP memory.

Junction temperature tolerance up to 175°C and control via wide level WAKE and PWM signals make the LV8968BB an ideal motor predriver for a wide range of ISO 26262 related actuators, fans and pumps.

Features

- Full Drive Power from 8 V to 28 V Supply Voltage with Transient Tolerance from 4.5 V to 40 V
- Extended Voltage Range from 6 V to 33 V Using Logic Level Mode
- Up to 30 kHz Motor PWM with Individual Six Gate Control or Drive−3 Mode with Integrated Programmable Dead Time
- 5 V / 3.3 V Linear Regulator for External Loads up to 50 mA
- Extensive System Protection Features Including:
  - Drain−Source Short Detection for External FET
  - Overcurrent Shutoff
  - Low Gate Voltage Warning
  - Overtemperature Warning and Shutoff
  - Over / Undervoltage Protection
- SPI Interface for Parameter Setup and Diagnostic Access, Dynamic Access to Dead Time, Amplifier Gain, and Short−Circuit Levels
- Nonvolatile (OTP) Memory for Storing Critical System Parameters
- Wide Voltage Enable Line and PWM Interface
- Integrated Window Watchdog Timer Function
- AEC−Q100 Qualified and PPAP Capable
- Thermally Efficient Exposed Die 48 Pin SQFP Package for Transient Operation Up to 175°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM

MP = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LV8968BBUWR2G	SPQFP48K (Pb−Free / Halogen Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SAFETY DESIGN ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

Typical Applications

- Suspension, Park Brake, Transmission, Steering Pump, Vacuum Pump, Battery Pack Cooling, Sliding Door, Lift Gate etc.
- Robotics
- Light E−mobility and Motive Power
- Industrial Equipment
- White Goods

INTERNAL EQUIVALENT BLOCK DIAGRAM AND APPLICATION CIRCUIT

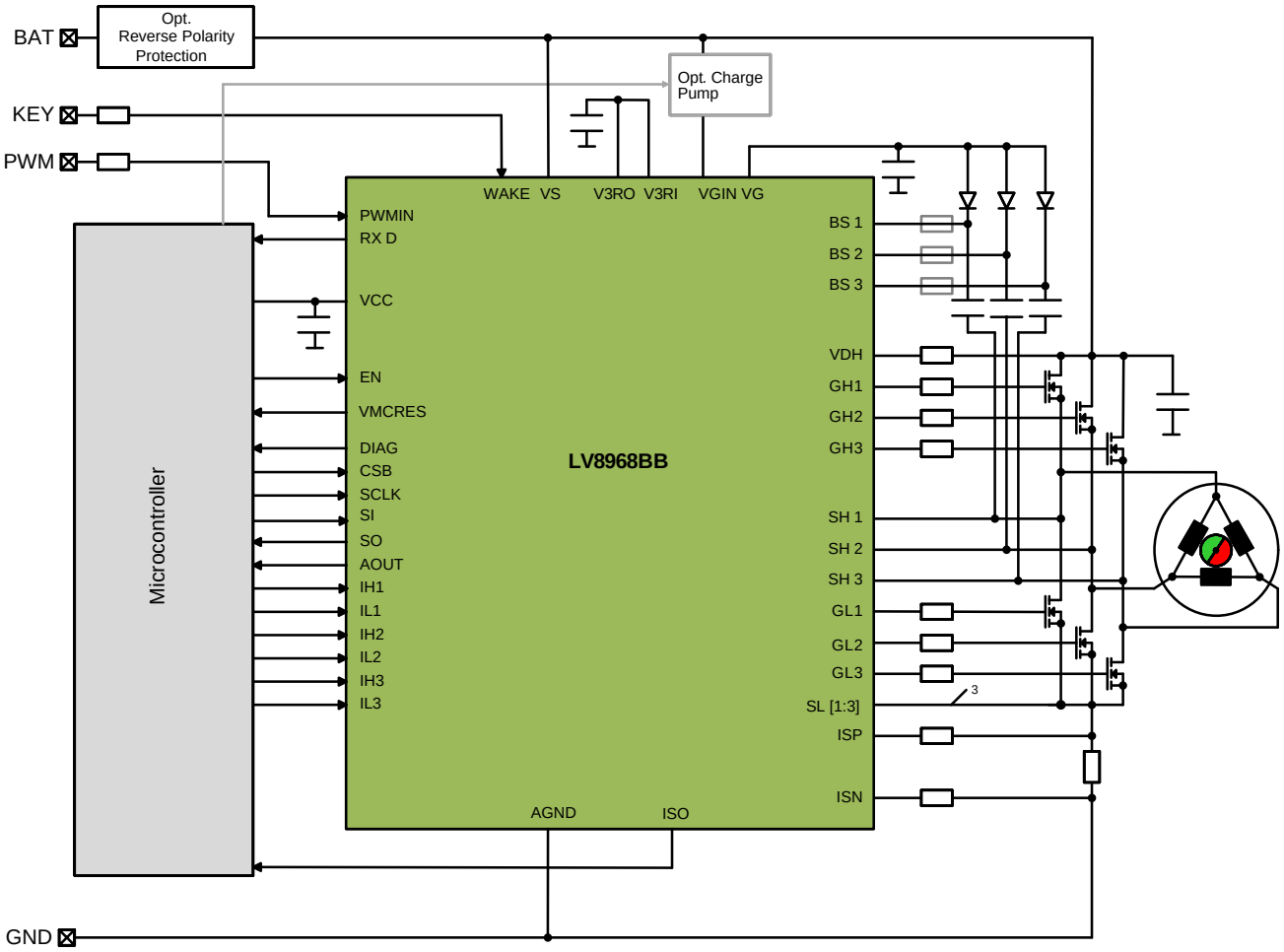


Figure 1. Typical Application Diagram

PIN ASSIGNMENT

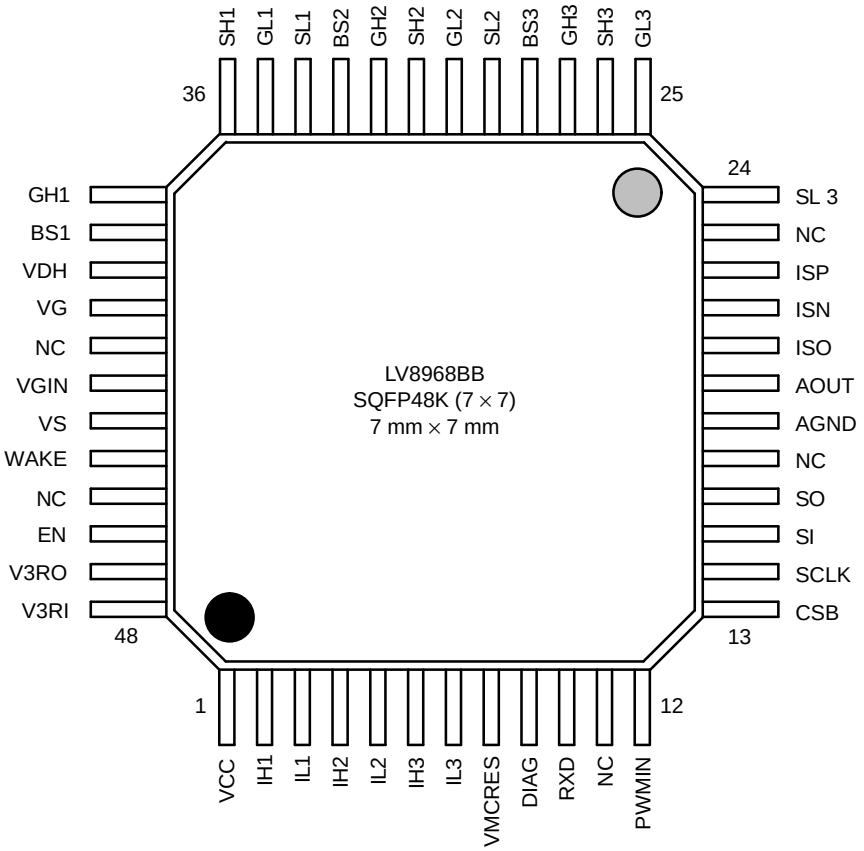


Figure 2. LV8968BB Pinout

Table 1. PIN ASSIGNMENTS & DESCRIPTION

Name	No.	Description
VCC	1	5 V or 3.3 V linear regulator output. (Selected by SPI register setting)
IH1	2	Active high, digital control input to activate GH1.
IL1	3	Active low, digital control input to activate GL1.
IH2	4	Active high, digital control input to activate GH2.
IL2	5	Active low, digital control input to activate GL2.
IH3	6	Active high, digital control input to activate GH3.
IL3	7	Active low, digital control input to activate GL3.
VMCRES	8	Open drain reset output for the microcontroller. Goes low for VCC undervoltage fault, optionally for watchdog reset and thermal shutdown.
DIAG	9	Open drain error or diagnostic output to be connected to microcontroller interrupt line. DIAG functionality is defined by internal register settings.
RXD	10	Open drain PWM data output to microcontroller.
NC	11	No connection.
PWMIN	12	Input for battery level control signal. The digital level of PWMIN appears on RXD.
CSB	13	High voltage level translator. Digital level is active low, digital SPI interface chip selection pin.
SCLK	14	SPI interface clock input pin. SI data is latched during the rising edge.

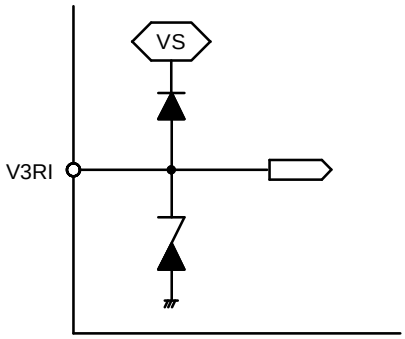
Table 1. PIN ASSIGNMENTS & DESCRIPTION (continued)

Name	No.	Description
SI	15	SPI interface serial data input pin.
SO	16	SPI interface serial data output pin. High level is pulled to VCC.
NC	17	No connection.
AGND	18	Ground pin.
AOUT	19	Output for various internal analog signals. Actual signal is selected via SPI register.
ISO	20	Output pin for current sense amplifier. Connect to AD converter input of the microcontroller for current sensing. Gain, reference, and overcurrent threshold is programmable via SPI register.
ISN	21	Current sense amp minus input pin. Connect this pin to the GND side of the shunt resistor with Kelvin leads.
ISP	22	Current sense amp plus input pin. Connect this through to top side of shunt resistor with Kelvin leads.
NC	23	No connection.
SL3	24	Low−side source connection of the power stage. Return path for gate current of GL3. Connect to source of FET controlled by IL3 or to common source of the power stage.
GL3	25	Gate driver output for low−side FETs. Switches voltage level between VG and SL3. Use at least 10 Ω gate resistors to protect against current spikes.
SH3	26	Connection for the motor phase terminal controlled by GH3 and GL3. Return path for high−side drivers and input for BEMF sensing.
GH3	27	Gate driver output for high−side FETs. Switches voltage level between BS3 and SH3. Use at least 10 Ω gate resistors to protect against current spikes.
BS3	28	Supply pin for high−side driver GH3. Needs a bootstrap capacitor to SH3 and a diode in reverse connection to VG.
SL2	29	Low−side source connection of the power stage. Return path for gate current of GL2. Connect to source of FET controlled by IL2 or to common source of the power stage.
GL2	30	Gate driver output for low−side FETs. Switches voltage level between VG and SL2. Use at least 10 Ω gate resistors to protect against current spikes.
SH2	31	Connection for the motor phase terminal controlled by GH2 and GL2. Return path for high−side drivers and input for BEMF sensing.
GH2	32	Gate driver output for high−side FETs. Switches voltage level between BS2 and SH2. Use at least 10 Ω gate resistors to protect against current spikes.
BS2	33	Supply pin for high−side driver GH2. Needs a bootstrap capacitor to SH2 and a diode in reverse connection to VG.
SL1	34	Low−side source connection of the power stage. Return path for gate current of GL1. Connect to source of FET controlled by IL1 or to common source of the power stage.
GL1	35	Gate driver output for low−side FETs. Switches voltage level between VG and SL1. Use at least 10 Ω gate resistors to protect against current spikes.
SH1	36	Connection for the motor phase terminal controlled by GH1 and GL1. Return path for high−side drivers and input for BEMF sensing.
GH1	37	Gate driver output for high−side FETs. Switches voltage level between BS1 and SH1. Use at least 10 Ω gate resistors to protect against current spikes.
BS1	38	Supply pin for high−side driver GH1. Needs a bootstrap capacitor to SH1 and a diode in reverse connection to VG.
VDH	39	Sense input for supply voltage and short−circuit detection of high−side power FETs. Connect through 100 Ω resistor to common drain of the power bridge.
VG	40	Power supply pin for low−side gate drive GL[1−3] directly and GH[1−3] through bootstrap circuit. Connect decoupling capacitor between VG and GND.
NC	41	No Connection.
VGIN	42	Gate supply input. Normally shorted to VS. Insert a charge pump circuit between VS and VGIN if low voltage operation is required.
VS	43	Power supply pin.

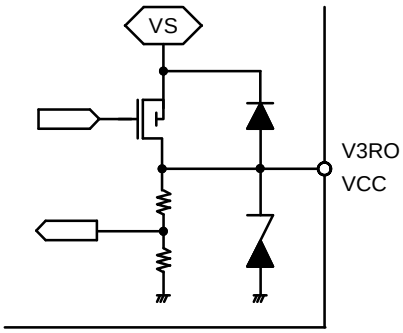
Table 1. PIN ASSIGNMENTS & DESCRIPTION (continued)

Name	No.	Description
WAKE	44	WAKE up pin for internal power supply. “H” => Operating mode, “L” or “Open” => Sleep mode.
NC	45	No connection.
EN	46	Active high digital input. A high on EN will activate the outputs. EN can be used as a hold input to allow an external microcontroller to keep the IC operating even if WAKE is low. A falling edge on EN clears the error flags.
V3RO	47	Internal regulator output pin. Connect capacitor between this pin and GND.
V3RI	48	Internal regulator feedback pin (Control circuit and Logic power supply). Connect to V3RO pin.

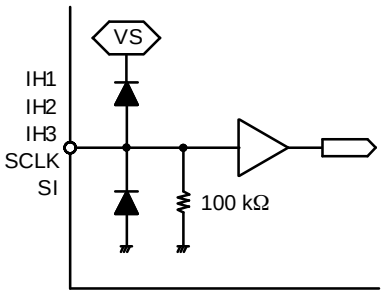
PIN FUNCTIONALITY



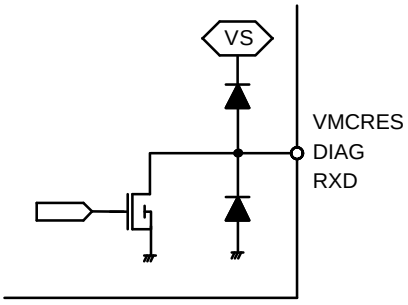
TYPE1: V3RI



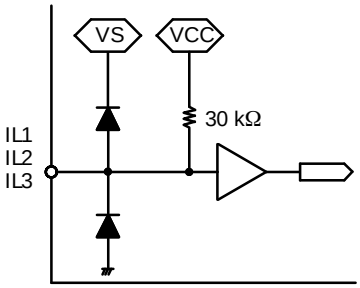
TYPE2: V3RO, VCC



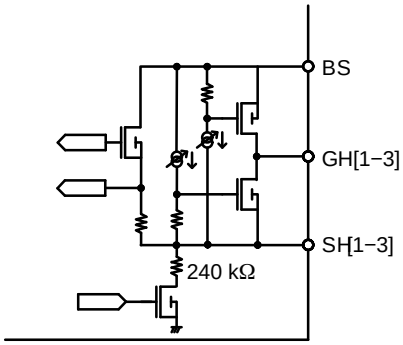
TYPE3: IH1, IH2, IH3, SCLK, SI, EN



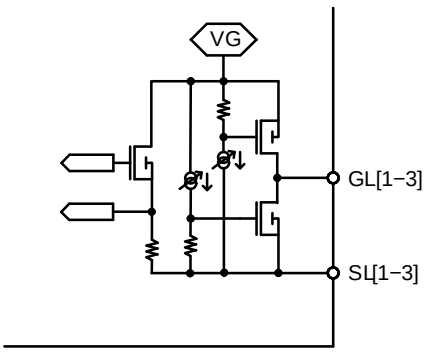
TYPE4: VMCRES, DIAG, RXD



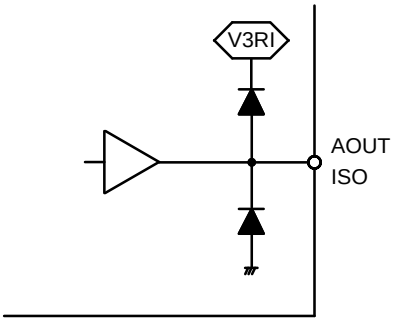
TYPE5: IL1, IL2, IL3, CSB



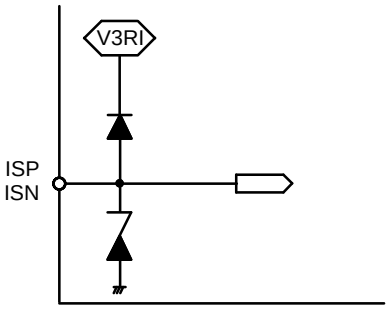
TYPE6: BS[1−3], GH[1−3], SH[1−3]



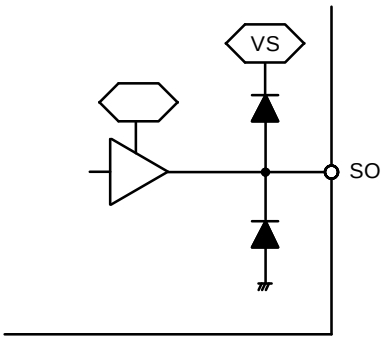
TYPE7: GL[1−3], SL[1−3]



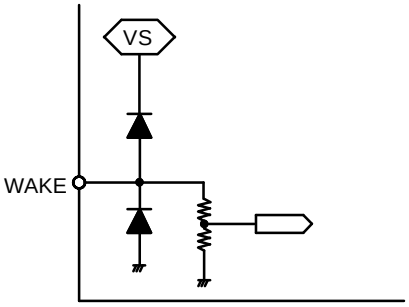
TYPE8: AOUT, ISO



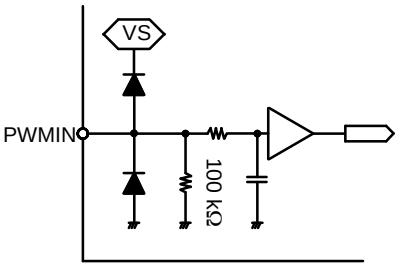
TYPE9: ISP, ISN



TYPE10: SO



TYPE11: WAKE



TYPE12: PWMIN

PIN FUNCTIONALITY (continued)

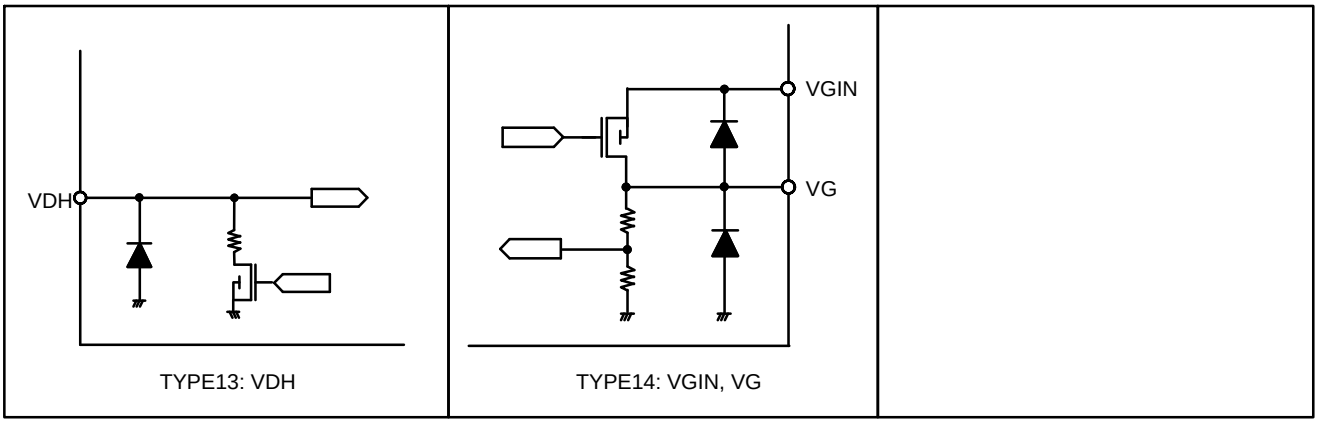


Figure 3. Pin Functionality

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Pins	Ratings	Unit
Supply Voltage	VS, VDH, VGIN	−0.3 to 40	V
Gate Voltage to GND	VG	−0.3 to 40	V
Bootstrap to GND	BS[1−3]	−0.3 to 40	V
Bootstrap to SH[1−3]	BS[1−3]	−0.3 to 40	V
Logic Power Supply	V3RI, V3RO	−0.3 to 3.6	V
3.3 V / 5 V Regulator Voltage	VCC	−0.3 to 5.5	V
VS Level Signal Voltage	WAKE, PWMIN	−0.3 to 40	V
Digital Inputs	CSB, EN, SCLK, SI, IH[1−3], IL[1−3]	−0.3 to 40	V
Open Drain Voltage	VMCRES, RXD, DIAG	−0.3 to 40	V
Digital Output Voltage	SO	−0.3 to V_{VCC}+0.3	V
Current Sense Input	ISP, ISN	−3 to V_{V3RI}+0.3	V
Analog Output	ISO, AOUT	−0.3 to V_{V3RO}+0.3	V
High−side Output to GND	GH[1−3]	−3 to 40	V
Motor Phase	SH[1−3]	−3 to 40	V
Low−side Output to GND	GL[1−3]	−3 to 40	V
Low−side Source Pin to GND	SL[1−3]]	−3 to 40	V
Voltage between HS Gate and Phase	GH[n] to SH[n] for n = {1,2,3}	−0.3 to 20	V
Allowable Power SQFP48K	at 70°C	2430	mW
Thermal Resistance (JESD51−7)	J_A = Junction Ambient	33	°C/W
	J_C = Junction Case	2	°C/W
Storage Temperature		−55 to 150	°C
Junction Temperature		−40 to 150	°C
	(Note 1)	150 to 175	°C
ESD Human Body Model	AEC Q100_002	2	kV
ESD Charge Device Model	AEC Q100_011	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Operation outside the Operating Junction temperature is not guaranteed. Operation above 150°C should not be considered without a written agreement from ON Semiconductor Engineering staff.

Table 3. ELECTRICAL CHARACTERISTICS

(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified. Typical values at 25°C and VS = 12 V unless specified otherwise)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY VS RELATED INPUTS						
VS supply voltage range	VSLOF	Full logic functionality	4.5		40 (Note 3)	V
	VSNO	Standard FET operation mode (VGVSEL = 0)	8		28 (Note 2)	V
	VSLO	Logic level FET operation mode (VGVSEL = 1)	6		33 (Note 2)	V
VS supply current	ISTBY	Standby mode, VS & VGIN shorted VS = 6 V ~ 25 V	7	11	16	mA
	ISLEEP	Sleep mode at 25°C, VS & VGIN shorted		25	50	μA
WAKE input voltage	VTHWKL	Low level	0		1.3	V
	VTHWKH	High level	2.7		VS	V
WAKE pulldown resistor	RPDWK		50	100	200	kΩ
WAKE up time for POR	TWTPOR	WAKE pin high			1	ms
VCC start−up time to active state	TVCSU				1.05	ms
VG start−up time to active state	TVGSU				1.05	ms
OTP download time	TDNLD	After POR			125	μs
PWMIN switching levels	VTHPIL	Low level	0		0.4×VS	V
	VTHPIH	High level	0.6×VS		VS	V
PWMIN pulldown resistor	RPDPI		50	100	200	kΩ
PWMIN frequency range	FPWMIN		0		30	kHz
INTERNAL REGULATOR						
V3RO output voltage	V3RO	V3RO only connect to V3RI	3.135	3.3	3.465	V
Max pull-up current Isource	IV3RO	Source, V3RO = V3RI			1	mA
VCC CONSTANT VOLTAGE OUTPUT						
Output voltage 5 V	VC5RO	VCVSEL = 1, No load	4.9	5.0	5.1	V
Output voltage 3.3 V	VC3RO	VCVSEL = 0, No load	3.23	3.3	3.37	V
	VC3RL	VS = 4.5 V, I_{VCC} =-50 mA	3.0			V
Voltage regulation	VCCVR				50	mV
Load regulation	VCCLR	Io = −5 mA to −50 mA			80	mV
Output current limit	VCCILIM		50		180	mA
GATE DRIVERS						
Low−side Rdson to SL[1−3]	RONLSSK	“L” level Io = 10 mA		6	15	Ω
Low−side Rdson to SH[1−3]	RONLSSC	“H” level Io = −10 mA		12	22	Ω
High−side Rdson to SH[1−3]	RONHSSK	“L” level Io = 10 mA		6	15	Ω
High−side Rdson to BS[1−3]	RONHSSC	“H” level Io = −10 mA		12	22	Ω
Propagation delay ON	PDON	50% IHx to 20% GHx. Cload = 0 nF			120	ns
Propagation delay OFF	PDOFF	50% IHx to 80% GHx. Cload = 0 nF			120	ns
Propagation delay ON Difference GH[1−3], GL[1−3]	DPDON	a.3 Phase difference of GH1,Gh2 and GH3. b.3 Phase difference of GL1,GL2 and GL3.	−20		20	ns
Propagation delay OFF Difference GH[1−3], GL[1−3]	DPDOFF	a.3 Phase difference of GH1,Gh2 and GH3. b.3 Phase difference of GL1,GL2 and GL3.	−20		20	ns
Output current limit	IGOLIM			400		mA
FDTI programmable dead time	TFDTI	0.2 μs step by FDTI register 4 bits (Note 4)	0.2		3.2	μs

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified.
Typical values at 25°C and VS = 12 V unless specified otherwise)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
BS PINS						
BS internal current	IBSC				800	μA
VG PIN						
VG output voltage	VGNO	Normal mode, VGVSEL = 0, IVG < 40 mA	7.0	11.0	12.0	V
	VGLO	Logic level mode, VGVSEL = 1	5	6	7	
	VGOL	VS = 6 V, IVG < 30 mA	5			
VG current limit	VGILIM		40		180	mA
ANALOG OUTPUT (AOUT)						
BEMF divider ratio	BEMFDR			1/16		
BEMF divider mismatch	BEMFDM		−2		2	%
BEMF divider settling time	BEMFST	for 20% to 80% step		0.5	2	μs
VDH divider ratio	VDHDR			1/32		
VDH divider settling time	VDHST	for 20% to 80% step		0.5	2	μs
Thermal voltage	VTMPH	Tj = 155°C (Note 4)		705		mV
Thermal slope	VTEMPSL	(Note 4)		+1.9		mV/°C
AOUT full scale range	AOFLSCR				2.1	V
AOUT output resistance	RONAO	IAOUT = ±100 μA			200	Ω
AOUT output current	IAO		−100		100	μA
CURRENT SENSING (ISP, ISN, ISO)						
ISP, ISN input current	IISP/N	−0.2V ≤ VISP, VISN ≤ 2 V	−50		50	μA
Reference voltage ISO	VRCSA0	CSOFEN = 0, GAIN = 30, ISP = ISN = 0.2 V	1.425	1.5	1.575	V
	VRCSA1	CSOFEN = 1, GAIN = 30, ISP = ISN = 0.2 V	0.125	0.2	0.275	V
Gain	CSAG00	CSGAIN = 00	6.53	7.5	8.63	
	CSAG01	CSGAIN = 01 (Note 4)		15		
	CSAG10	CSGAIN = 10 (Note 4)		22.5		
	CSAG11	CSGAIN = 11	26	30	34.3	
Common mode range	CSACMR		−0.2	1	2	V
ISN, ISP differential voltage	DVCSAIN		−200		200	mV
ISO full scale range	CSAFLSCR		0.1		2.9	V
Amplifier settling time (20% − 80% FSR)	CSAOST	Gain = 7.5, 0.25 V < V_{ISO} < 3 V			5400	ns
ISO output resistance	RCSAO	I_{ISO} = ±100 μA			200	Ω
ISO output current	ICSAO		−100		100	μA
Overcurrent voltage level V_{ISP}−V_{ISN}	VTHCSA00	OCDL = 00	180	200	220	mV
	VTHCSA01	OCDL = 01	130	150	170	mV
	VTHCSA1X	OCDL = 10,11	80	100	120	mV
OCMASK programmable Overcurrent Mask time	TOCMASK	0.2 μs step by OCMASK register 4 bits (Note 4)	0.2		3.2	μs
ACTIVE HIGH DIGITAL INPUTS (EN, SCLK, SI, IH[1−3])						
High−level input voltage	VTAHH		0.8×V3RO			V
Low−level input voltage	VTAHL				0.2×V3RO	V
Pull−down resistance	RPDAH		50	100	200	kΩ
ACTIVE LOW DIGITAL INPUTS (CSB, IL[1−3])						
High−level input voltage	VTALH		0.8×V3RO			V
Low−level input voltage	VTALL				0.2×V3RO	V
Pull−up resistance to VCC	RPDAL		15	30	60	kΩ

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 8.0 V ≤ VS ≤ 25 V unless otherwise specified.
Typical values at 25°C and VS = 12 V unless specified otherwise)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIGITAL OUTPUTS (SO)						
Output voltage	VSOH	Io = −1 mA	V_{VCC} −0.2			V
	VSOL	Io = 1 mA			0.2	V
OPEN DRAIN OUTPUTS (VMCRES, DIAG, RXD)						
Output voltage	VODL	Io = 1 mA			0.2	V
Pin leakage current	ILKOD	Vo = 5.5 V			10	μA
WARNING AND PROTECTION						
Thermal warning (Junction temperature)	TWT0	THTSEL = 0	125			°C
	TWT1	THTSEL = 1	150			°C
	HYSTW	Hysteresis		25		°C
Thermal shutdown (Junction temperature)	TSDT0	THTSEL = 0	150			°C
	TSDT1	THTSEL = 1	175			°C
	HYSTSD	Hysteresis		25		°C
VS voltage warning/protection	VSOVTH	VS high voltage detection, warning/protection response set by VSOVPS	16	17	18	V
	VSUVTH	VS low voltage detection, warning/protection response set by VSUVPS	7	7.5	8	V
VDH voltage warning/protection	VDHOVTH	VDH high voltage detection, warning/protection response set by VDOVPS	25	26.5	28	V
VG undervoltage	VGNUVTH	Normal mode, VGVSEL = 0	5	6	7	V
	VGLUVTH	Logic level mode, VGVSEL = 1	3.5	4	4.5	V
VCC undervoltage	VC3UVTH	VCVSEL = 0	2.3		2.7	V
	VC5UVTH	VCVSEL = 1	3.8		4.2	V
V3R Power on Reset	VPOR				2.7	V
FET short detection Level	VFSDL	100 mV step by FSDL register 4 bits (Note 4)	100		1600	mV
FET short Detection level	FSDL0000	FSDL = 0000	75	100	125	mV
	FSDL0010	FSDL = 0010	240	300	360	mV
	FSDL0100	FSDL = 0100	400	500	600	mV
	FSDL1000	FSDL = 1000	720	900	1080	mV
	FSDL1111	FSDL = 1111	1280	1600	1920	mV
FET short detection masking time	TFSDT	3.2 μs step by FSDT register 2 bits (Note 4)	3.2		12.8	μs
FET short detection debounce filter time,	TFSFT	0.8 μs step by FSFT register 2 bits (Note 4)	0.8		3.2	μs
WATCHDOG						
WD first open window	WDFOW	WDTWT[2:0] typical values	3.2		409.6	ms
WD closed window time	WDCW	WDTWT[2:0] typical values	0.8		102.4	ms
WD open window time	WDOW	WDTWT[2:0] typical values	1.6		204.8	ms
WD reset duration	WDRD			400		μs
SPI INTERFACE						
SPI clock frequency	FSPI				4.5	MHz
BS internal current	IBSC				800	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. VDH overvoltage warning will be issued for elevated VS supply voltage levels. See the specification of the VDH overvoltage warning threshold voltage VDHOVTH.
3. Valid for limited time duration of 400 ms (Load dump)
4. Not tested in production. Guaranteed by design and verified during qualification.

DETAILED FUNCTIONAL DESCRIPTION

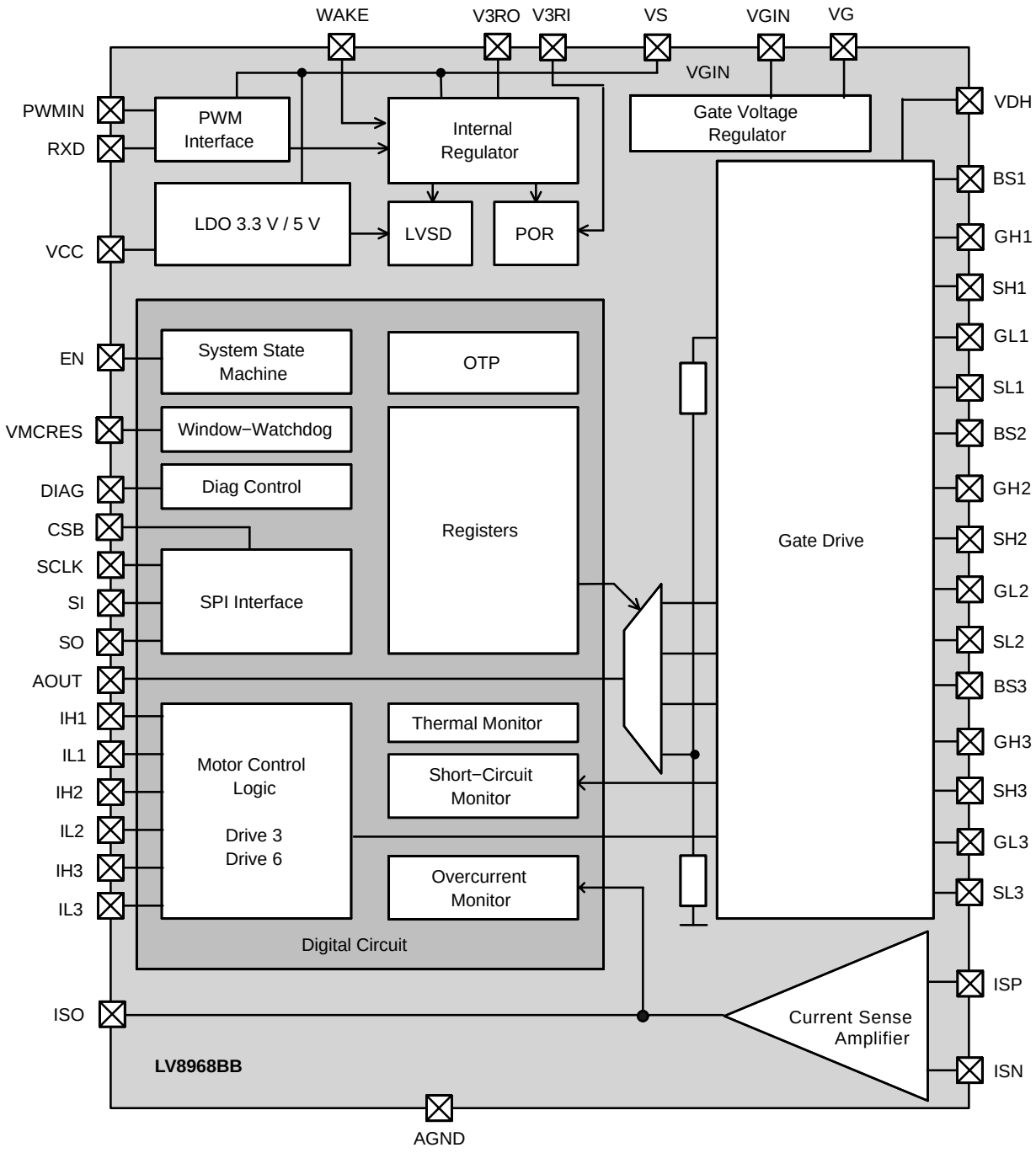


Figure 4. Block Diagram

Chip Activation, System States and Shutdown (EN, WAKE)

Once the supply voltage VS rises above VSLOF(Min.), the LV8968BB enters Sleep mode. In Sleep mode system states are controlled with pin WAKE.

Table 4. OPERATION MODES

Mode	WAKE	EN	V3RO	Logic	VCC	VG	SPI	Drivers
Sleep	L	NA	Disable	Reset	Disable	Disable	Disable	High−Z
Standby	H	L	Enable	Active	Enable	Enable	Enable	Low
Normal	NA	H	Enable	Active	Enable	Enable	Enable	Active

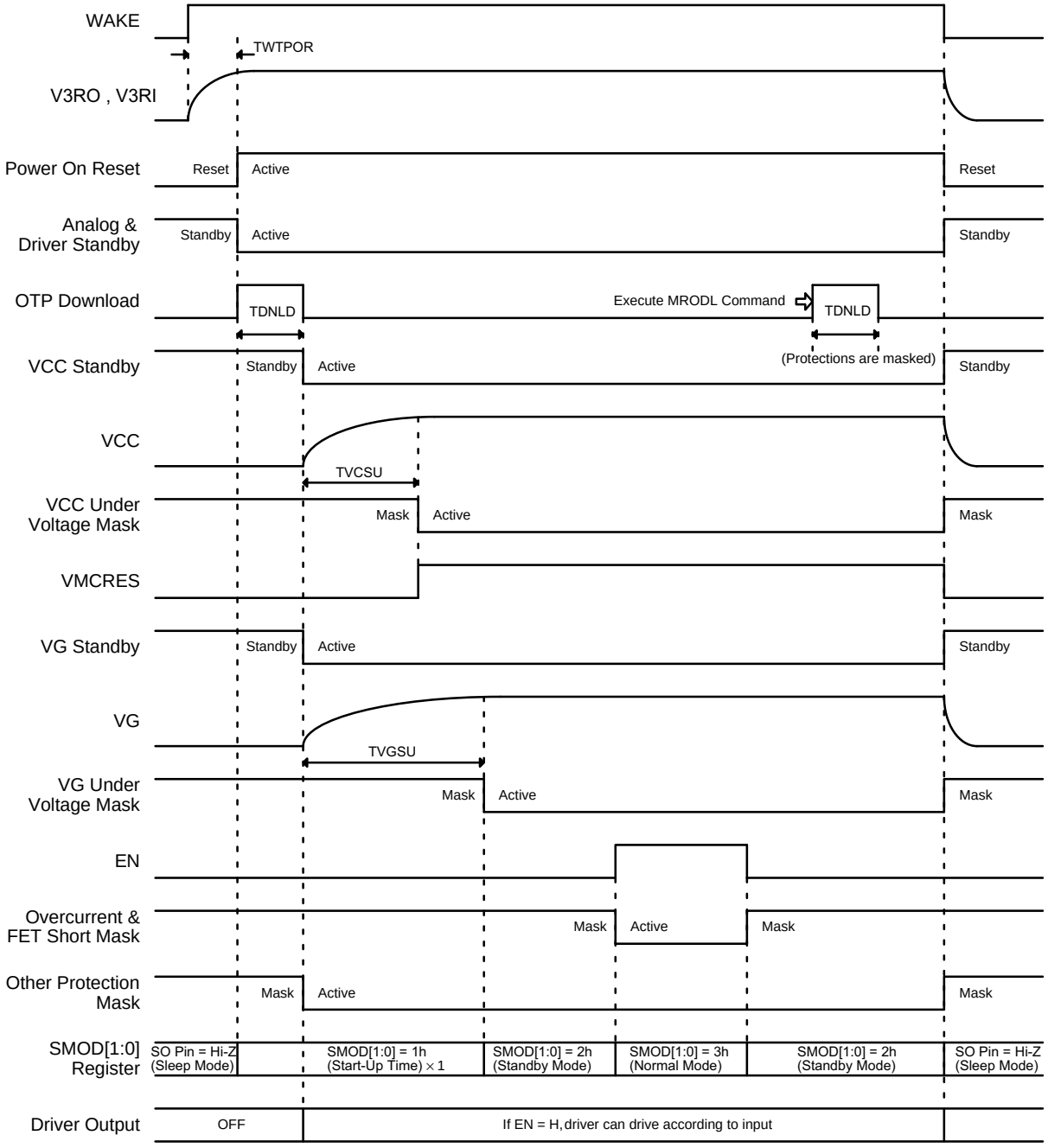
A high level on WAKE pin activates the IC from sleep mode and enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and releases the internal digital reset. OTP register contents are loaded into the system registers defining the power on state of the LV8968BB and the VCC regulator voltage.

VCC is powering up next, holding the CPU reset line VMCRES low until VCC passes its undervoltage level. During the entire wake−up sequence, DIAG is masked for VG undervoltage. After wake−up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.

Note that if the CPU watchdog was enabled via OTP, a VMCRES low will be asserted after the watchdog first open window (WDFOW) unless the watchdog is being triggered properly. See section “**Watchdog**”.

A high on EN takes the LV8968BB from Standby to Normal mode. Normal mode allows motor control and the IC accepts control inputs via the motor control pins IH[1−3], IL[1−3]. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.

The IC is shut down by taking WAKE pin low if EN is low. If EN is high, a low on WAKE will be ignored until the microcontroller pulls EN low.



NOTE: Even if EN = H, driver status is not changed to normal mode.

Figure 5. Powerup and Shutdown Timing

Operating Voltage Range

Normal operation with full functionality is guaranteed from 8 V to 25 V. The device will operate from 4.5 V to 40 V with limited performance:

Shutdown: VS < $VSLOF_{(min)}$
The IC will be off. Gate drivers are Hi−Z.

Undervoltage: $VSLOF_{(min)}$ < VS < VSUVTH
VS undervoltage warning/protection will be active according to VSUVPS. VG undervoltage warning may be asserted. If VCC is programmed to provide 3.3 V to the microcontroller, it will be supplied even if VS < $VSLO_{(min)}$. If motor operation is required during Undervoltage, see section below “Motor Operation during Undervoltage”.

Normal VS Drive Mode: VSUVTH < VS < VSOVTH
Normal operation.

VS High Voltage Operation: VSOVTH < VS < VDHOVTH
Normal operation: VS high voltage warning/protection might be active according to VSOVPS.

VDH High Voltage Operation:
VDHOVTH < VS < $VSLOF_{(max)}$
VDH high voltage warning/protection might be active according to VDOVPS. The driver stage can be programmed to let the motor freewheel to protect the bootstrap circuitry at BS[1−3] from overstress. This works if the motor is not operating in field weakening.

In case of active braking, or field weakening operation, the microcontroller will have to react to a VDH overvoltage warning by either disabling the driver stage or activating all low−side FETs to brake the motor. The maximum allowed VS level for motor operation depends on the driver FET type: VSNO(Max.) or VSLO(Max.). For additional protection add zener diodes to the bootstrap pins.

Motor Operation during Undervoltage
An undervoltage charge pump is not included into the LV8968BB to save cost. If undervoltage operation of the motor is desired either an external charge pump must be inserted between VS and VGIN, or it is possible to use the device in logic level mode by setting MRCONF0[1]. In the latter case logic level FETs must be used for the inverter stage.

System Power Supplies

Three power supplies are integrated into the LV8968BB, all are supplied by VS:

- An internal 3.3 V regulator which provides power to the digital and interface section
- A linear regulator to provide 5 V or 3.3 V for external loads such as a microcontroller
- The VG regulator for the gate voltages of the inverter stage

Internal Regulator (V3RO, V3RI)
The internal regulator provides 3.3 V at V3RO and takes its feedback from V3RI. V3RO and V3RI need to be connected externally and decoupled with capacitor to GND for stability.

LDO 3.3 / 5 V (VCC)
VCC becomes active during Start−Up, where after Standby mode is entered. The VCC voltage can be configured via registers to provide 5 V or 3.3 V. VMCRES low is asserted if the output voltage drops below the threshold levels. VCC may power external loads and must be decoupled to GND with an external capacitor. The voltage level is programmed in register VCVSEL with OTP backup.

Gate Voltage Regulator (VGIN,VG)
The gate voltage regulator is supplied by VGIN and regulates to either VGNO or VGLO at VG. The voltage level is programmed in register VGVSEL with OTP backup.

VG provides the drive voltage for the low−side drivers GL[1−3] directly and for the high−side drivers BS[1−3] through the bootstrap circuitry. The output is current limited to 40 mA(min). The output at VG should be decoupled with a capacitor C_{VG} to GND which should be at least 20 times the maximum gate charge of the power FETs.

Motor Control Inputs

Once the LV8968BB is in standby mode with the supplies running, a microcontroller can facilitate motor control via the inputs EN, IL[1−3], IH[1−3]. All are VS compatible.

PWM Interface (PWMIN, RXD)
The PWM interface translates a VS level signal with a threshold of 40% and 60% VS to a digital signal appearing at RXD. This RXD signal can be used for input PWM signal translation to the microcontroller.

Case of abnormal state such as PWMIN pin is Open or Short, RXD signal shows Low DC voltage level.

Additionally, PWMIN a supply level compatible level shifter can bring a high voltage control such as a PWM signal or a crash indicator to microcontroller supply level.

Drive Enable (EN)
Taking EN high enables the output drivers GH[1−3] and GL[1−3] for control by the microcontroller, taking EN low disables them by switching all of them to the sources of the corresponding external FETs. In addition, a high on EN will override a low on WAKE allowing the microcontroller to keep the motor running even after the WAKE line has gone low.

Motor Control (IL[1−3] IH[1−3])

The individual motor phases are controlled by inputs IL[1−3] and IH[1−3]. IH[1−3] are active high, while IL[1−3] are active low allowing for parallel control with only three PWM outputs using internal dead time. To control the driver stage with GH [1−3] and GL[1−3] EN has to be “high”. The LV8968BB will insert an adjustable dead time during output transitions to prevent short circuiting the FETs. Two drive modes exist:

Drive 6 Mode

In drive 6 mode, each input independently controls its corresponding output requiring 6 independent PWM channels in the microcontroller. A “high” on IH1 will result in a “high” on GH1. A “high” on IL1 will result in a “low” on GL1, and so forth. Trying to force a short by driving IH1 high and IL1 low will be ignored by the logic of the LV8968BB.

Table 5. DRIVE 6 MODE

Input		Output	
IH[1−3]	**IL[1−3]**	**GH[1−3]**	**GL[1−3]**
L	L	L	H
L	H	L	L
H	L	L	L
H	H	H	L

Drive 3 Mode

This mode is suitable for small microcontrollers which do not have 6 dedicated PWM control lines. IL[1−3] serve as enable signals for the phase drivers GH[1−3] and GL[1−3] while IH[1− 3] serve as their PWM inputs. Connect the microcontroller’s PWM line to IH[1−3] and the phase select lines to the individual IL inputs 1−3 respectively.

Table 6. DRIVE 3 MODE

Input		Output	
IH[1−3]	**IL[1−3]**	**GH[1−3]**	**GL[1−3]**
L	L	L	L
L	H	L	H
H	L	L	L
H	H	H	L

Gate Drive

The gate drive circuit of the LV8968BB includes 3 half−bridge drivers which control six external N−Channel FETs. The high−side gate drivers GH[1−3] switch their gate connection either to corresponding BS[1−3] pin or the respective phase connection SH[1−3]. The low−side gate drivers GL[1−3] are switched from VG to the corresponding source connection SL[1−3]. Both high− and low−side switches are hard switching, but saturate around IGOLIM for pullup/down currents. Slope control has to be implemented with gate resistors.

“Through Current Prevention Function”

Current shoot through protection of the bridge drivers is implemented by ignoring inputs at IH[n] and IL[n] that would result in turning on of both high−and low−side FET at the same time. In addition a dead time counter is implemented that begins counting after one driver has been turned off, and blocks the turning−on of the complementary driver for a programmable time t_{FDTI}.

Dead Time Counter

The dead time counter uses a fixed minimum dead time which can be programmed into 4bit parameter FDTILIM. The dead time is never allowed to fall below that value.
A dynamic dead time register FDTI allows dead time variation during motor operation. This register is uploaded at the beginning of every dead time measurement. Flag FDTIBSY is high when a dead time value has been written to register FDTI but was not uploaded to the counter, yet. Two consecutive writes to FDTI before a counter upload are flagged as an SPI error by setting bit SACF in the SPI status register GSDAT.

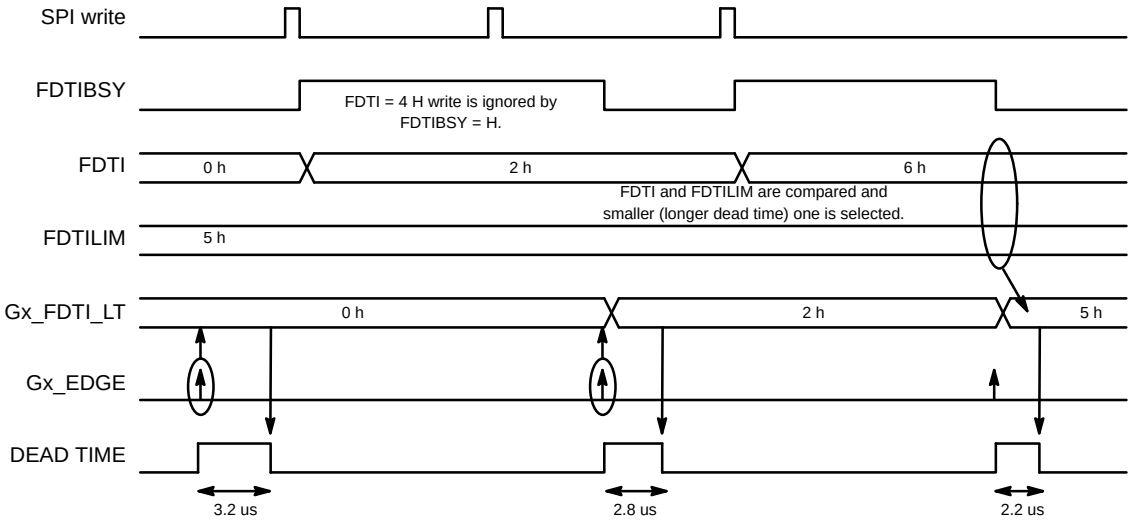


Figure 6. Dead Time Programming

Short Protection

To protect against FET shorts the drain−source voltage of the active external power FETs is monitored. The drain source voltage of the high−side FETs is monitored between VDH and the corresponding source SH[1−3]. While the low−side FETs are monitored between SH[1−3] and SL[1−3]. After activation of the FET the short detection is masked for time t_{FSFT} to allow for signal settling. If after the masking time t_{FSFT} the FET voltage exceeding V_{FSDL} continues for t_{FSDT}, a FET short error is flagged. For details see “System Errors and Warnings” on page 18.

Four bits register FSDL selects the FET short protection shutoff voltage VFSDL. The masking time TFSDT is set with bits FSDT[1:0] and a debounce filter time TFSFT is set with bits FSFT[1:0]. Both parameters residing in register MRCONF6. These registers are dynamic and FSDL can be changed during motor operation, though FSFT and FSDT can be changed when EN = L.

Current Sensing and Overcurrent Shutoff

Single shunt current sensing can be implemented with the integrated high speed sense amplifier. It amplifies the voltage across ISP – ISN with a programmable gain defined by register CSGAIN. Access to this register is dynamic, allowing gain adjustment during motor operation. The offset is determined by CSOFEN relative to an internal reference which can be either 200 mV(typ) for unidirectional current sensing, or 1.5 V(typ) for sensing current in both directions. The output of the current sense amplifier appears on the ISO pin.

Overcurrent Shutoff

A parallel path implements fast overcurrent shutoff of the driver stage. Overcurrent shutoff is triggered if the voltage across ISP − ISN exceeds a programmable level as defined by register OCDL. In overcurrent shutoff all gate drivers go to Hi−Z, turning the power FETs high impedance and letting the motor freewheel – this reaction is maskable. For more information on masking and recovery see section “System Errors and Warnings” on page 18.

To suppress switching transients, an overcurrent masking time can be programmed into register OCMASK.

Temperature Sensing

The LV8968BB monitors internal junction temperature T_j. The voltage representing this temperature (V_{PTAT}) can be sampled at AOUT as described below. Thermal warnings and errors are issued if T_J exceeds the levels defined by THTSEL:

Table 7. THERMAL THRESHOLDS

THTSEL	Thermal Warning	Thermal Shutoff
0	125°C	150°C
1	150°C	175°C

If thermal error shutoff is activated, VG and VCC turn off, and the driver stage goes high impedance. As a result VMCRES goes low and SPI communication is disabled as well. The exact failure modes and masks are described in section “System Errors and Warnings”.

BEMF and other Measurements

The LV8968BB includes a multiplexer for measuring the phase voltages, the motor voltage and the IC temperature. Depending on the state of AOUTSEL the following voltages appear on AOUT:

Table 8. AOUT SELECTION

MRAOSEL[2:0]	Pin	Formula	Comment
0	VDH	V_{VDH} = 32 V_{AOUT}	Motor Supply Voltage
1	SH1	V_{SH1} = 16 V_{AOUT}	Phase Voltage 1
2	SH2	V_{SH2} = 16 V_{AOUT}	Phase Voltage 2
3	SH3	V_{SH2} = 16 V_{AOUT}	Phase Voltage 3
4, 5	−	T_J (°C) = 0.53 x V_{AOUT} (mV) − 216	Internal junction temperature
6, 7	−	High Impendance	

Watchdog

The LV8968BB includes a window watchdog to monitor the microcontroller. The size of the watchdog window is defined by register WDTWT. For detailed timing information see Figure 7: Window Watchdog Timing. A write access to register MRRST during open window time resets the watchdog timer and it starts counting again. The watchdog will issue an error whenever MRRST is written to during closed window time or the watchdog time expires. Watchdog error effects can be customized. For detailed error behavior a masking see section “System Errors and Warnings”.

After a watchdog induced microcontroller reset, the error register contents of registers MRDIAG[0] remain conserved until an SPI read access. This helps the microcontroller identify the fault condition.

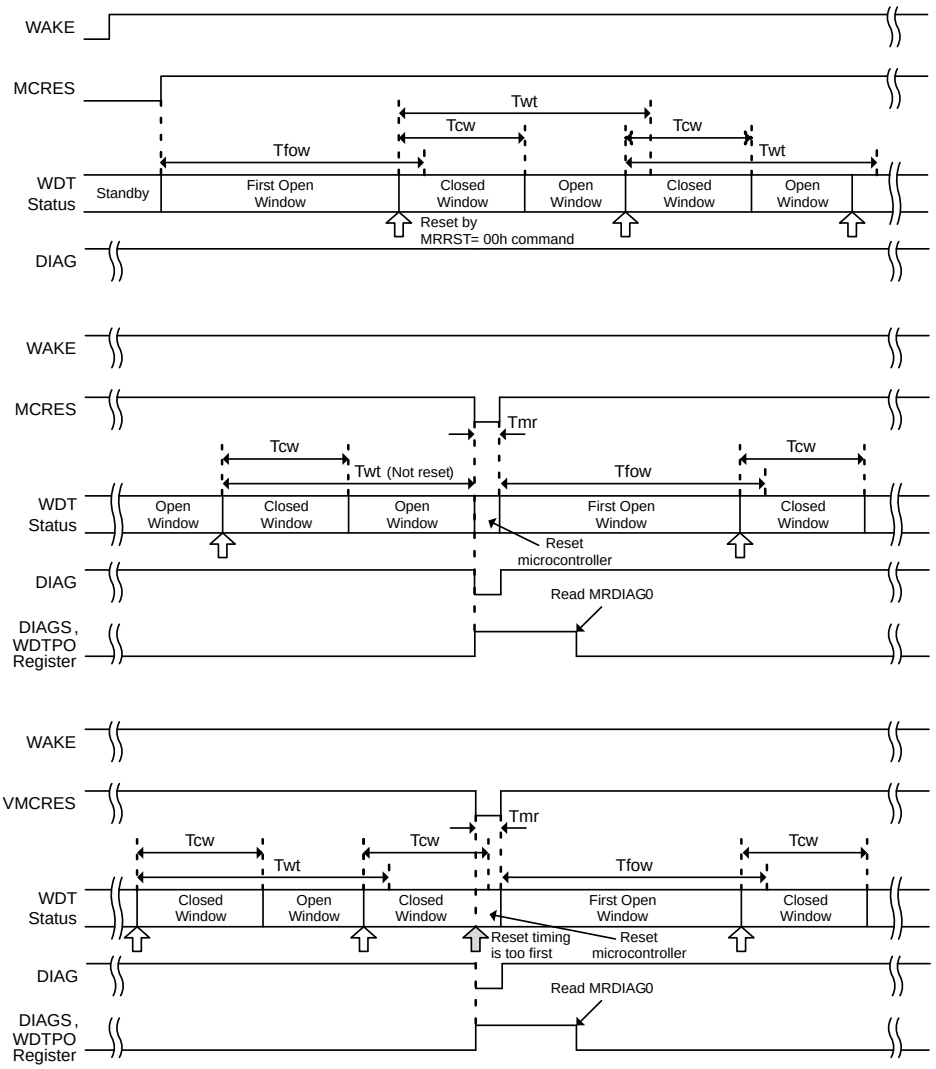


Figure 7. Window Watchdog Timing

Table 9. WINDOW WATCHDOG TIMING OPTIONS (T_J = −40 to 150 °C, VS = 4.5 to 40 V)

Symbol	Characteristic	Min	Typ	Max	Unit
T_{FOW}	WDT first open window time				ms
	WDTWT[2:0] = 0h	390.0	409.6	431.2	
	WDTWT[2:0] = 1h	195.0	204.8	215.6	
	: (1/2 step)	:	: (1/2 step)	:	
	WDTWT[2:0] = 7h	3.0	3.2	3.4	
T_{CW}	WDT closed window time				ms
	WDTWT[2:0] = 0h	97.4	102.4	107.8	
	WDTWT[2:0] = 1h	48.7	51.2	53.9	
	: (1/2 step)	:	:(1/2 step)	:	
	WDTWT[2:0] = 7h	0.7	0.8	0.9	
T_{WT}	WDT window time				ms
	WDTWT[2:0] = 0h	195.0	204.8	215.6	
	WDTWT[2:0] = 1h	97.4	102.4	107.8	
	: (1/2 step)	:	:(1/2 step)	:	
	WDTWT[2:0] = 7h	1.4	1.6	1.7	
T_{MR}	WDT microcontroller reset time	333	400	422	μs

System Errors and Warnings

System errors and warnings are always flagged in their corresponding register MRDIAG0 and MRDIAG1 and their presence is indicated in SPI status register GSDAT. The LV8968BB gives great flexibility in modifying the error response. Error response definition can be backed up into OTP.

All system errors and warnings can cause a transition on DIAG. The polarity of this transition is selected in bit DIAGPOL. DIAG should be connected to an interrupt input of the microcontroller. Errors that can cause serious damage such as short−circuit and overcurrent may be latched by enabling the corresponding latch bit in MRCONF7. In this case the LV8968BB will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset
- EN low
- SPI write of FFh to MRRST

Table 10 explains the error behaviour. “Error” names the type of error that is covered. “Reaction Settings Option” lists which options exists for this error and the corresponding register. ”Reaction names what happens if the error occurs. Some reactions depend on the “Setting Options” and are described in Notes below.

Table 10. SYSTEM ERROR AND WARNING RESPONSE MATRIX

	Reaction Setting Options					Reaction					
Error	Setup Register	Mask Error	Report on DIAG	Auto Recover	Latch Off	VG	DRV	VCC	MC RES	Recovery Condition	Protection Enabled
VS Under Voltage	VSUVPS [1:0]	Yes	Yes	Yes	No	ON	(Note 5)	ON	H	VS voltage recovers	After OTP download
VS Over Voltage	VSOVPS [1:0]	Yes	Yes	Yes	No	ON	(Note 5)	ON	H	VS voltage recovers	After OTP download
VDH Over Voltage	VDOVPS [1:0]	Yes	Yes	Yes	No	ON	(Note 5)	ON	H	VDH voltage recovers	After OTP download
VG Under Voltage	VGUVPS [1:0]	Yes	Yes	Yes	No	ON	(Note 5)	ON	H	VG voltage recovers	After VG start−up time
VCC Under Voltage	−	No	No	Yes	No	ON	OFF	ON	L	VCC voltage recovers	After VCC start−up time

Table 10. SYSTEM ERROR AND WARNING RESPONSE MATRIX

Error	Reaction Setting Options					Reaction				Recovery Condition	Protection Enabled
	Setup Register	Mask Error	Report on DIAG	Auto Recover	Latch Off	VG	DRV	VCC	MC RES		
Over Current	OCPS [1:0]	Yes	Yes	Yes	Yes	ON	(Note 5)	ON	H	[Latch Off] EN = L or execute MRRST = Ffh command [Auto Recover] EN = L or after ecovery time [Report] EN = L or motor current is down	EN = H (Normal mode)
FET Short	FSPS [1:0]	Yes	Yes	Yes	Yes	ON	(Note 5)	ON	H	[Latch Off] EN = L or execute MRRST = FFh command [Auto Recover] EN = L or after recovery time [Report] EN = L or FET short current is down	EN = H (Normal mode)
Thermal Warning	THWPS	Yes	Yes	No	No	ON	ON	ON	H	Temperature is down	After OTP download
Thermal Shutdown	THSPS	Yes	No	Yes	No	(Note 6)	(Note 6)	(Note 6)	(Note 7)	Temperature is down	After OTP download
Watchdog Timer	WDTPS	Yes	No	Yes	No	ON	(Note 6)	ON	(Note 8)	After output reset pulse from VMCRES pin	VMCRES = H

5. Report or Ignore = ON, Latch Off or Auto Recover = OFF
6. Ignore = ON, Auto Recover = OFF
7. Ignore = H, Auto Recover = L
8. Ignore = Fixed H, Auto Recover = Output L pulse

SPI Interface

In the LV8968BB the SPI Interface is used to perform general communications for status reporting, control and programming.

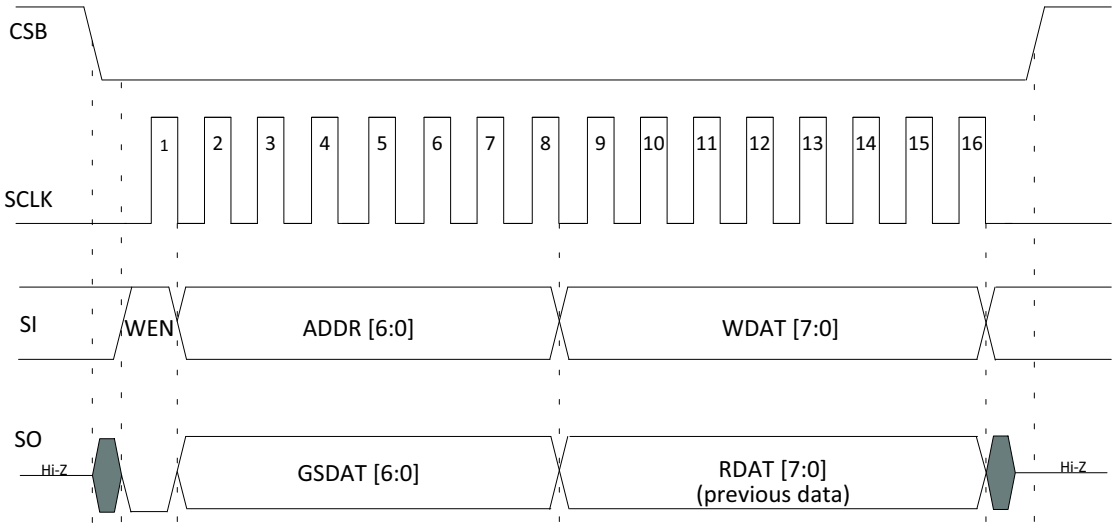


Figure 8. SPI Format in Write Mode

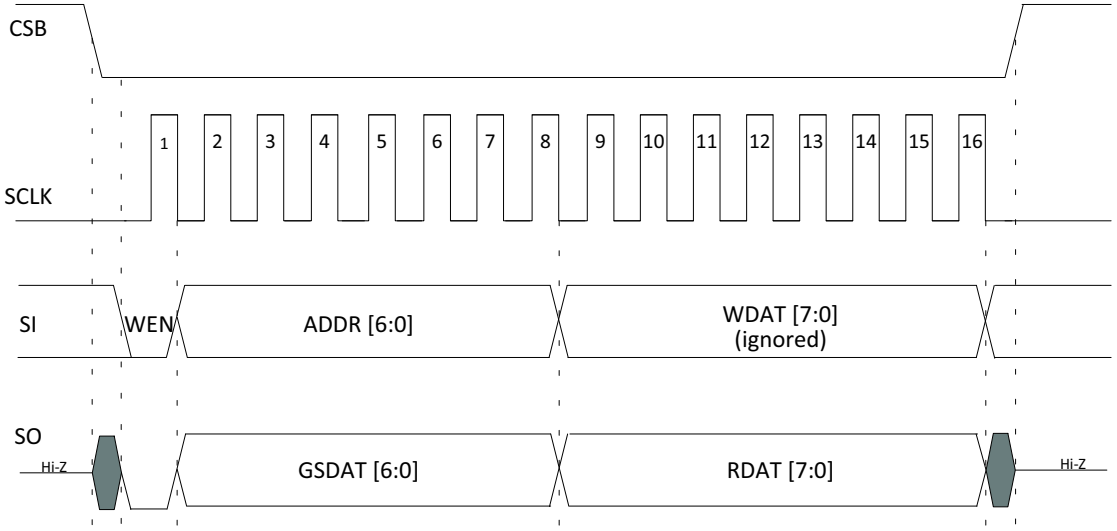


Figure 9. SPI Format in Read Mode

SPI communications with the LV8968BB follows established industry standard practices including the use of WEN and start and stop bits as shown above. Data is transferred MSB first and both clock and data are transferred as 'true' data with the higher level indicating a logical 1 or true state.

There are two items to be especially careful of with the general communication scheme:

- Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable
- It is important the system master have the clock and data polarities and phases as shown above. Both the clock and data on some systems can be inverted for various reasons but must arrive at the LV8968BB per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half a bit time exists to eliminate transmission delay hazards.

The first byte returned on all transactions is always the status register GSDAT, and contains information such as the busy flag during programming operations

Table 11.

GSDAT[7:0]								
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
0	ORBEN	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]		
NA	NA	NA	NA	NA	NA	NA	NA	Sleep mode
NA	NA	NA	NA	NA	NA	0	1	Device start−up time
NA	NA	NA	NA	NA	NA	1	0	Standby mode
NA	NA	NA	NA	NA	NA	1	1	Normal mode
NA	0	0	0	0	0	NA	NA	Normal Operation
NA	NA	NA	NA	NA	1	NA	NA	OTP download of default values
NA	NA	NA	NA	1	NA	NA	NA	Latched shutdown condition
NA	NA	NA	1	NA	NA	NA	NA	Failure Condition
NA	NA	1	NA	NA	NA	NA	NA	Last SPI access failed*
NA	1	NA	NA	NA	NA	NA	NA	OTP integrity test mode

The following SPI failures are detectable and reported collectively by a high on SACF in GSDAT[5] as general SPI failures:

- Any access to an address which is not assigned.
- The number of SCLK edges is not 16 within one word transfer
- Any access to MRCONF and ORCONF while OBSY = 1, (During write operations)
- Write access to MRODL register while OBSY = 1, (during write operations)
- Write access to any of the main registers after setting MSAENB = 1 (Implies Reg. address 04 h to 07 h are locked)
- Write access to any of the OTP registers after OSAENB = 1 (Implies Reg. address 40 h to 43 h are locked)
- Write access attempt to a read only or locked register
- SI signal changed at positive edge of SCLK (Incorrect data/sclk phase setup)
- Write access to dead time register FDTI while FDTIBSY is still high (last value has not been uploaded)

SPI Timing

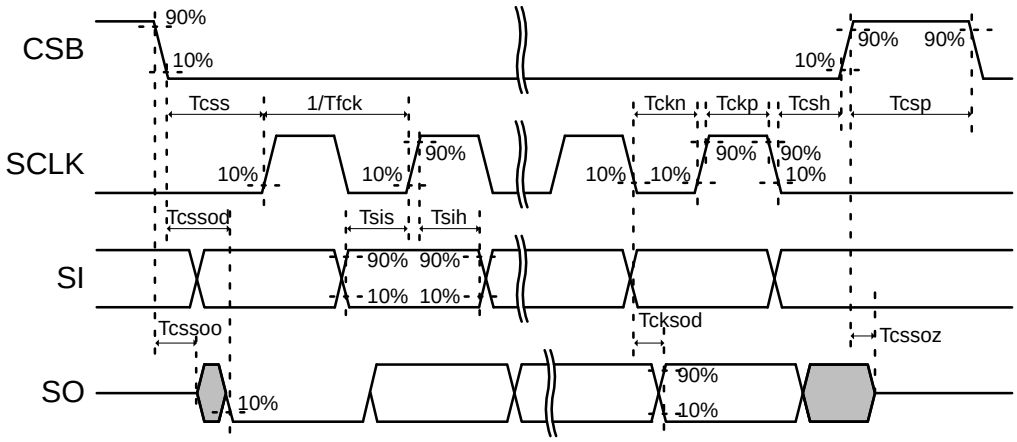


Figure 10. SPI Timing Diagram

Table 12. SPI TIMING (T_J = −40 to 150°C, VS = 4.5 to 40 V, SO load = 50 pF)

Symbol	Comment	Min	Typ	Max	Unit
T_{FCK}	SCLK Clock Frequency			4.5	MHz
T_{CKP}	SCLK High Pulse Width	90			ns
T_{CKN}	SCLK Low Pulse Width	90			ns
T_{CSS}	CSB Setup Time	90			ns
T_{CSH}	CSB Hold Time	0			ns
T_{CSP}	CSB High Pulse Width	90			ns
T_{SIS}	SI Setup Time	45			ns
T_{SIH}	SI Hold Time	45			ns
T_{CKSOD}	SCLK Fall Edge to SO Delay Time			75	ns
T_{CSSOD}	CSB Fall Edge to SO Delay Time			75	ns
T_{CSSOO}	CSB Fall Edge to SO Data Out Time	0			ns
T_{CSSOZ}	CSB Rise Edge to SO Hi−Z Out Time			75	ns

NOTE: SPI−Interface can be used after the data download of the OTP has been completed. However it can not be used during VMCRES = L.

OTP Programming

The OTP register data is typically transferred into the main registers at device start−up (From sleep to standby transition). This operation takes up to 125 μs. A high OBSY flag in the first returned byte during a SPI transaction indicates this.

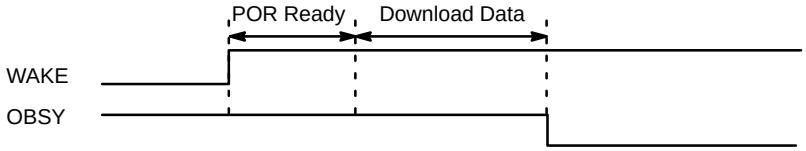


Figure 11. OTP Data Download Timing at Start−Up

An OTP download can also actively be initiated by writing 00h to register MRODL. This command requires monitoring the OBSY flag. Don't perform specific register access (MRCONF0 ~ 3, ORCONF0 ~ 3, MRORB, MRODL) until the OBSY flag is cleared.

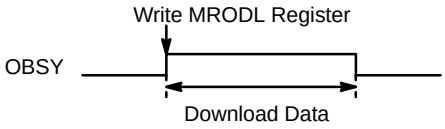


Figure 12. OTP Data Download Timing after an MRODL Command

OTP Programming Overall

Figure 13 shows overall of the OTP memory write and verify flow. It consists of preparation, write and three times of data integrity verification.

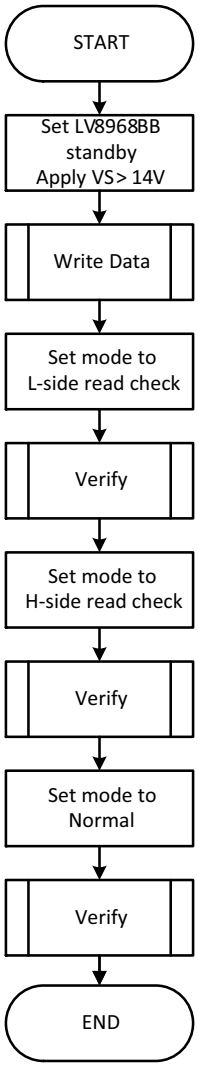


Figure 13. OTP Memory Write and Verify Flow

OTP Programming

The OTP registers can be programmed in Standby mode only while the write lock bit OSAENB is set 0. And, the supply voltage at pin VS must be more than 14 V. The actual write operation to the OTP memory will be done, when the state change from 0 to 1 is commanded. Once the bit state is changed to 1, it cannot be change back to 0. The number of writing is limited to one per bit.

The OBSY flag will be reset at the end of the write cycle. OBSY is in GSDAT register. To get GSDAT, SPI accesses to the register MRACK is recommended. MRACK doesn't interfere with the programming operation.

MRCONF0 ~ 3, ORCONF0 ~ 3, MRORB, MRODL registers cannot be accessed during an OTP write cycle.

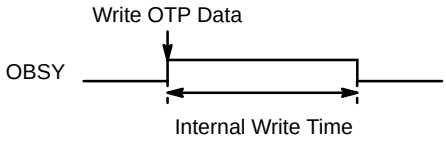


Figure 14. OTP Programming Timing

The programming takes 4 ms maximum. To simplify operation, a waiting for 4 ms plus margin can be applicable instead of a polling of the flag OBSY. (Figure 15)

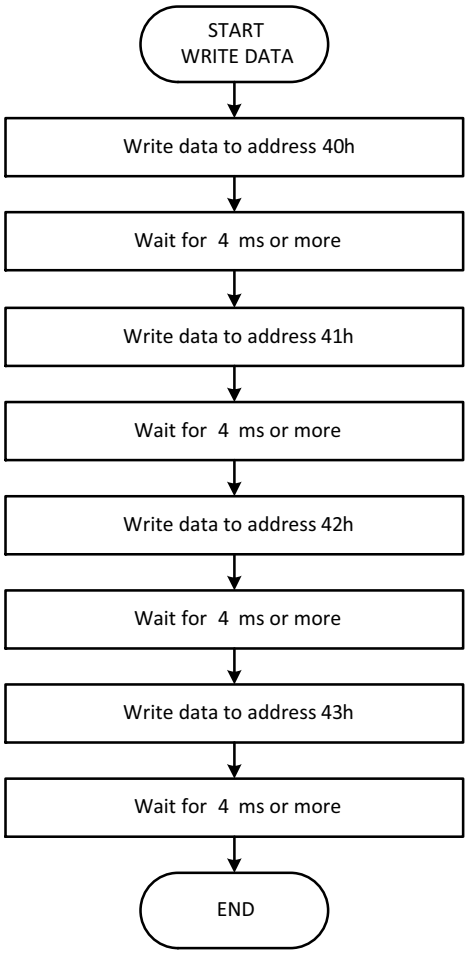


Figure 15. OTP Memory Write and Verify Flow

OTP Data Integrity Verification

In order to verify that the OTP programming operation was successful. It is strongly recommended to do an OTP margin check: To do this, the OTP registers are downloaded into the main register bank with minimum and maximum readout thresholds. This OTP download is forced by writing 00h to register MRODL. The readout threshold is set in register MRORB.

OTP Margin read check sequence after programmed:

1. Set OTP readout threshold “low” by setting ORBEN = 1 and ORBLV = 0 in register MRORB
2. Execute OTP download command by writing 00h to MRODL
3. Verify that the main register contents are consistent with the programmed OTP data
4. Set OTP readout threshold “high” by setting ORBEN = 1 and ORBLV = 1 in register MRORB
5. Execute OTP download command by writing 00h to MRODL
6. Verify that the main register contents are consistent with the programmed OTP data
7. Return OTP threshold to normal by setting ORBEN = 0 and ORBLV = 0
8. Execute OTP download command
9. Verify that the main register contents are consistent with the programmed OTP data

Locking OTP Register Contents

MSAENB bit and OSAENB bit are used in order to prevent write−access of main− and OTP registers respectively.

CAUTION: Inadvertent writing of these bits will permanently lock the corresponding register blocks from any further write access. Should only be set at end of development cycles.

Table 13. REGISTER MAP

WENB by WEN (1bit)	Write Time Condition	ADDR [6:0]	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Don't care	Don't care	−	GSDAT	0	ORBEN	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]	
OSAENB (Note 9)	EN=L	00h	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
		01h	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	
		02h	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
Read Only	Read Only	03h	MRCONF3	0	0	0	0	0	0	0	OSAENB
MSAENB (Note 9)	EN=L	04h	MRCONF4	0	WDTWT[2:0]			0	CSOFEN	AWODLEN	D3MDEN
		05h	MRCONF5	0	0	OCDL[1:0]		OCMASK[3:0]			
		06h	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	
		07h	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			
EN=L or H		08h	MRCONF8	0	0	0	0	0	0	0	MSAENB
EN=L or H	EN=L or H	10h	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0] (Default=7h)		
		11h	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	
		12h	MRFSDL	0	0	0	0	FSDL[3:0]			
		13h	MRFDTI	0	0	0	0	FDTI[3:0]			
		14h	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY
		15h	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							
	EN=L	16h	MRORB	0	0	0	0	0	0	ORBEN	ORBLV
		17h	MRODL	Write 00h: Execute OTP data download							
Read Only	Read Only	20h	MRDIAG0	0	0	0	WDTPO	THSPO	THWPO	FSPO	OCPO
		21h	MRDIAG1	0	0	0	VCUVPO	VGUVPO	VDOVPO	VSOVPO	VSUVPO
		22h	MRACK	0	1	0	1	0	1	0	1
OSAENB (Note 9)	EN=L	40h	ORCONF0	ORCONF0[7:6]		THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
		41h	ORCONF1	ORCONF1[7:5]			WDTPS	THSPS	THWPS	VGUVPS[1:0]	
		42h	ORCONF2	ORCONF2[7:6]		VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
		43h	ORCONF3	ORCONF3[7:1]							OSAENB

NOTE: SPI access to addresses not listed here will result in an SPI access failure error (SACF).

9. At Test mode, ENB = 1 setting is ignored.

MRCONF0 (Default: 00h)
(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL

THTSEL: THermal Thresholds SELection
Temperature warning threshold and error selection.
- THTSEL = 0: Thermal warning = 125°C, Thermal shutdown = 150°C
- THTSEL = 1: Thermal warning = 150°C, Thermal shutdown = 175°C

DFCSEL: Diag Flag Clearing SELection
Defines the condition under which the error registers are reset, by error condition removed only, or by error condition removed and subsequent SPI read access of the register in question.
- DFCSEL = 0: If error was cleared, DIAGS flag of GSDAT and MRDIAG0 and MRDIAG1 flags are reset by MRDIAG0 read, MRDIAG1 read
- DFCSEL = 1: DIAGS flag of GSDAT and MRDIAG0 and MRDIAG1 flag are reset by recovery condition

DIAGLTO: DIAG pin Latched errors Transition Only
If this bit is set, only latched errors result in a transition on DIAG. Otherwise all errors (and warnings) will be flagged.
- DIAGLTO = 0: At the time of detecting auto recover or latch off error, DIAG output is on
- DIAGLTO = 1: At the time of detecting latch off error, DIAG output is on

DIAGPOL: DIAG pin POLarity
Decides the polarity of the DIAG output.
- DIAGPOL = 0: At the time of detecting diagnostic error, DIAG output is L
- DIAGPOL = 1: At the time of detecting diagnostic error, DIAG output is H

VGVSEL: VG pin Voltage SELection
Selects if the IC is in logic level mode or normal mode which modifies the gate voltage of the drive section.
- VGVSEL = 0: VG normal mode (VG = 11 V)
- VGVSEL = 1: VG logic level mode (VG = 6 V)

VCVSEL: VCc pin Voltage SELection
Selects the output voltage of VCC to be either 3.3 V or 5 V. The wrong bit selection has a possibility to damage the microcontroller. Please make sure the appropriate selection.
- VCVSEL = 0: VCC = 3.3 V
- VCVSEL = 1: VCC = 5.0 V

MRCONF1 (Default: 00h)
(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
01h	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	

WDTPS: WatchDog Timeout Protection Setting
Watchdog error results in error response or is ignored.
- WDTPS = 0: Ignore WDT error
- WDTPS = 1: Emergency off and report a WDT error (Auto recover)

THSPS: THermal Shutdown Protection Setting
Thermal shutdown error results in error response or is ignored.
- THSPS = 0: Ignore thermal shutdown error
- THSPS = 1: Emergency off and report at thermal shutdown error (Auto recover)

THWPS: THermal Warning Protection Setting
- THWPS = 0: Ignore thermal warning error
- THWPS = 1: Report thermal warning error

VGUVPS[1:0]: VG pin UnderVoltage Protection Setting

- VGUVPS[1:0] = 0h: Ignore VG undervoltage error
- VGUVPS[1:0] = 1h: Report VG undervoltage error
- VGUVPS[1:0] = 2h, 3h: Emergency off and report at VG under voltage error (Auto recover)

MRCONF2 (Default: 00h)

(Write Access Only when EN = Low. OTP Backup Possible)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
02h	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	

VDOVPS[1:0]: VDh OverVoltage Protection Setting

- VDOVPS[1:0] = 0h: Ignore VDH overvoltage error
- VDOVPS[1:0] = 1h: Report VDH overvoltage error
- VDOVPS[1:0] = 2h, 3h: Emergency off and report at VDH over voltage error (Auto recover)

VSOVPS[1:0]: VS OverVoltage Protection Setting

- VSOVPS[1:0] = 0h: Ignore VS overvoltage error
- VSOVPS[1:0] = 1h: Report VS overvoltage error
- VSOVPS[1:0] = 2h, 3h: Emergency off and report at VS over voltage error (Auto recover)

VSUVPS[1:0]: VS UnderVoltage Protection Setting

- VSUVPS[1:0] = 0h: Ignore VS undervoltage error
- VSUVPS[1:0] = 1h: Report VS undervoltage error
- VSUVPS[1:0] = 2h, 3h: Emergency off and report at VS under voltage error (Auto recover)

MRCONF3 (Default: 00h)

(Read Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
03h	MRCONF3	0	0	0	0	0	0	0	OSAENB

OSAENB: Otp Spi write Access ENable Bar

Setting this bit disables all write access to the configuration registers MRCONF0, MRCONF1 and MRCONF2 and the OTP backup register. Set to prevent system parameters from being modified.

- OSAENB = 0: Enable write access of MRCONF0~2 and ORCONF0~3
- OSAENB = 1: Disable write access of MRCONF0~2 and ORCONF0~3

MRCONF4 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
04h	MRCONF4	0	WDTWT[2:0]			0	CSOFEN	AWODLEN	D3MDEN

WDTWT[2:0]: Watchdog Timeout Window Time
Defines the watchdog timer window sizes.
- WDTWT[2:0] = 0h: T_{FOW} = 409.6 ms, T_{CW} = 102.4 ms, T_{WT} = 204.8 ms
- WDTWT[2:0]=1h: T_{FOW} = 204.8 ms, T_{CW} = 51.2 ms, T_{WT} = 102.4 ms
  :
  : (1/2 step)
  :
- WDTWT[2:0] = 7h: T_{FOW} = 3.2 ms, T_{CW} = 0.8 ms, T_{WT} = 1.6 ms

CSOFEN: Current Sensor OFfset Enable
Selects the offset of the current sense amplifier.
- CSOFEN = 0: Current sense amp offset = 1.5 V
- CSOFEN = 1: Current sense amp offset = 0.2 V

AWODLEN: Automatic Window for Otp DownLoad Enable
Periodical (200 ms) OTP download during EN = H.
- AWODLEN = 0: Not download OTP data in normal mode
- AWODLEN = 1: Download OTP data periodically in normal mode

D3MDEN: Drive 3 Mode Drivers Enable
Chooses how the output drivers are addressed, with six PWM channels, or with three PWM channels and three enables.
- D3MDEN = 0: Drive 6 mode
- D3MDEN = 1: Drive 3 mode

MRCONF5 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
05h	MRCONF5	0	0	OCDL[1:0]		OCMASK[3:0]			

OCDL[1:0]: OverCurrent Detection Level
Defines the overcurrent detection threshold voltage between ISN and ISP.
- OCDL[1:0] = 0h: Overcurrent detect level = 200 mV
- OCDL[1:0] = 1h: Overcurrent detect level = 150 mV
- OCDL[1:0] = 2h, 3h: Overcurrent detect level = 100 mV

OCMASK[3:0]: OverCurrent MASKing time
Masking time for the overcurrent detection after every output transition.
- OCMASK[3:0] = 0h: Overcurrent mask time = 0.2 μs
- OCMASK[3:0] = 1h: Overcurrent mask time = 0.4 μs
  :
  : (0.2 μs step)
  :
- OCMASK[3:0] = Eh: Overcurrent mask time = 3.0 μs
- OCMASK[3:0] = Fh: Overcurrent mask time = 3.2 μs

MRCONF6 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
06h	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	

FSFT[1:0]: Fet Short detection debounce Filter Time
External FET short detection debounce time. A short condition has to remain valid during this time.
- FSFT[1:0] = 0h: FET short detect time = 0.8 μs
- FSFT[1:0] = 1h: FET short detect time = 1.6 μs
- FSFT[1:0] = 2h: FET short detect time = 2.4 μs
- FSFT[1:0] = 3h: FET short detect time = 3.2 μs

FSDT[1:0]: Fet Short Detection masking Time
External FET short−circuit detection masking time, starts after turn−on of the FET.
- FSDT[1:0] = 0h: FET short masking time = 3.2 μs
- FSDT[1:0] = 1h: FET short masking time = 6.4 μs
- FSDT[1:0] = 2h: FET short masking time = 9.6 μs
- FSDT[1:0] = 3h: FET short masking time = 12.8 μs

MRCONF7 (Default: 00h)
(Write Access Only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
07h	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			

FSPS[1:0]: Fet Short−circuit error Protection Setting
Short−circuit error decision mask.
- FSPS[1:0] = 0h: Ignore FET short error
- FSPS[1:0] = 1h: Report FET short error
- FSPS[1:0] = 2h: Emergency off and report at FET short error (Auto recover)
- FSPS[1:0] = 3h: Emergency off and report at FET short error (Latched off)

OCPS[1:0]: OverCurrent error Protection Setting
Overcurrent error decision mask.
- OCPS[1:0] = 0h: Ignore overcurrent error
- OCPS[1:0] = 1h: Report overcurrent error
- OCPS[1:0] = 2h: Emergency off and report at overcurrent error (Auto recover)
- OCPS[1:0] = 3h: Emergency off and report at overcurrent error (Latched off)

FDTILIM[3:0]: Fet Dead TIme LIMit
Minimum Dead time programming register.
- FDTILIM[3:0] = 0h: FET dead time = 3.2 μs
- FDTILIM[3:0] = 1h: FET dead time = 3.0 μs
  :
  : (−0.2 μs step)
  :
- FDTILIM[3:0] = Eh: FET dead time = 0.4 μs
- FDTILIM[3:0] = Fh: FET dead time = 0.2 μs

MRCONF8 (Default: 00h)
(Write access only when EN = Low)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
08h	MRCONF8	0	0	0	0	0	0	0	MSAENB

MSAENB: Mrconf Spi write Access ENable Bar
Setting this bit disables all write access to the configuration registers MRCONF4 to MRCONF7.
- MSAENB = 0: Enable write access of MRCONF4 ~ 7
- MSAENB = 1: Disable write access of MRCONF4 ~ 7

MRAOSEL (Default: 07h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
10h	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0]		

AOUTSEL[2:0]: AOUT pin output SELect
Select the internal nodes brought out on AOUT.
- AOUTSEL[2:0] = 0h: AOUT = Output VDH voltage level
- AOUTSEL[2:0] = 1h: AOUT = Output SH1 voltage level
- AOUTSEL[2:0] = 2h: AOUT = Output SH2 voltage level
- AOUTSEL[2:0] = 3h: AOUT = Output SH3 voltage level
- AOUTSEL[2:0] = 4h, 5h: AOUT = Output thermal monitor voltage level
- AOUTSEL[2:0] = 6h, 7h: AOUT = Hi−Z

MRCSG (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
11h	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	

CSGAIN[1:0]: Current Sense GAIN
Programs the gain of the current sense amplifier.
- CSGAIN[1:0] = 0h: Current sense amp gain = 7.5
- CSGAIN[1:0] = 1h: Current sense amp gain = 15
- CSGAIN[1:0] = 2h: Current sense amp gain = 22.5
- CSGAIN[1:0] = 3h: Current sense amp gain = 30

MRFSDL (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
12h	MRFSDL	0	0	0	0	FSDL[3:0]			

FSDL[3:0]: Fet Short Detection Level
Defines the maximum allowable drain source voltage across a power FET.
- FSDL[3:0] = 0h: FET short detect level = 100 mV
- FSDL[3:0] = 1h: FET short detect level = 200 mV
  :
  : (100 mV step)
  :
- FSDL[3:0] = Eh: FET short detect level = 1500 mV
- FSDL[3:0] = Fh: FET short detect level = 1600 mV

MRFDTI (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
13h	MRFDTI	0	0	0	0	FDTI[3:0]			

FDTI[3:0]: Fet Dead TIme

Dead time programming register. This dead time will be applied unless it is smaller than FDTILIM[3:0] in MRCONF7.

- FDTI[3:0] = 0h: FET dead time = 3.2 μs
- FDTI[3:0] = 1h: FET dead time = 3.0 μs

  :

  : (−0.2 μs step)

  :
- FDTI[3:0] = Eh: FET dead time = 0.4 μs
- FDTI[3:0] = Fh: FET dead time = 0.2 μs

MRFDTIF (Default: 00h)
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
14h	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY

FDTIBSY: Fet Dead TIme BuSY uploading

FDTIBSY goes high after the dead time register was written to via SPI but not uploaded into the dead time counter. Upload happens at the beginning of every dead time measuring period (falling edge of a gate signal) and clears the FDTIBSY flag.

A write access MRFDTIF = 01h also clears the FDTIBSY flag.

MRRST
(Full Dynamic Access)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
15h	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							

MRRST[7:0]: Master Register ReSeT

Write access to this register resets the Watchdog or the Error latch.

- Write MRRST[7:0] = 00h: Reset WDT
- Write MRRST[7:0] = FFh: Reset latch off

MRORB (Default: 00h)
(Register for OTP Programming Integrity Check. Write During EN = Low Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
16h	MRORB	0	0	0	0	0	0	ORBEN	ORBLV

ORBEN: Otp Read Bias mode Enable

Setting this bit puts the device into OTP integrity check mode.

- ORBEN = 0: Normal
- ORBEN = 1: OTP bias read mode

ORBLV: Otp Read Bias mode LeVel

Changes the OTP readout thresholds to high and low, to verify data integrity.

- ORBLV = 0: OTP low bias read mode at ORBEN = 1
- ORBLV = 1: OTP high bias read mode at ORBEN = 1

MRODL
(Write Access During EN = Low Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
17h	MRODL	Write 00h: Execute OTP data download							

MRODL[7:0]: Master Register Otp DownLoad
A write initiates an OTP data download into the main registers in standby mode. In Normal mode, OTP download can be initiated only when AWODLEN is set regardless of MRODL.

- Write MRODL[7:0] = 00h: Execute OTP data download

MRDIAG0
(Read Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
20h	MRDIAG0	0	0	0	WDTPO	THSPO	THWPO	FSPO	OCPO

WDTPO: WatchDog Timeout Protection Output
Watchdog error flag.

- WDTPO = 0: Normal
- WDTPO = 1: Detect WDT error

THSPO: THermal Shutdown Protection Output
Over temperature shutoff flag.

- THSPO = 0: Normal
- THSPO = 1: Detect thermal shutdown error

THWPO: THermal Warning Protection Output
Thermal warning flag.

- THWPO = 0: Normal
- THWPO = 1: Detect thermal warning error

FSPO: FET Short−circuit Protection Output
FET short−circuit detection flag.

- FSPO = 0: Normal
- FSPO = 1: Detect FET short error

OCPO: OverCurrent Protection Output
Overcurrent error flag.

- OCPO = 0: Normal
- OCPO = 1: Detect overcurrent error

MRDIAG1
(Read Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
21h	MRDIAG1	0	0	0	VCUVPO	VGUVPO	VDOVPO	VSOVPO	VSUVPO

VCUVPO: VCc UnderVoltage Protection Output
VCC undervoltage flag.

- VCUVPO = 0: Normal
- VCUVPO = 1: Detect VCC undervoltage error

VGUVPO: VG UnderVoltage Protection Output
VG undervoltage flag.

- VGUVPO = 0: Normal
- VGUVPO = 1: Detect VG undervoltage error

VDOVPO: VDh OverVoltage Protection Output
VDH overvoltage flag.
- VDOVPO = 0: Normal
- VDOVPO = 1: Detect VDH overvoltage error

VSOVPO: VS OverVoltage Protection Output
VS overvoltage flag.
- VSOVPO = 0: Normal
- VSOVPO = 1: Detect VS overvoltage error

VSUVPO: VS UnderVoltage Protection Output
VS undervoltage flag.
- VSUVPO = 0: Normal
- VSUVPO = 1: Detect VS undervoltage error

MRACK
(Read Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
22h	MRACK	0	1	0	1	0	1	0	1

MRACK[7:0]: Master Register ACKnowledge
For SPI data verification. A read must result in 55h.
- MRACK[7:0] read data is fixed 55h

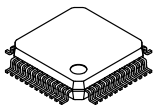
ORCONF0 ~ 3 (Default: 00h)
(OTP Backup for Critical System Registers. Programmable During EN = L Only)

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
40h	ORCONF0	ORCONF0[7:6]		THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
41h	ORCONF1	ORCONF1[7:5]			WDTPS	THSPS	THWPS	VGUVPS[1:0]	
42h	ORCONF2	ORCONF2[7:6]		VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
43h	ORCONF3	ORCONF3[7:1]							OSAENB

ORCONF0 ~ 3
- ORCONF0 ~ 3 data is transferred to MRCONF0 ~ 3 at OTP data download
- ORCONF0[7:6], ORCONF1[7:5], ORCONF2[7:6], ORCONF3[7:1] data is not transferred to MRCONF

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



SPQFP48 7x7 / SQFP48K
CASE 131AN
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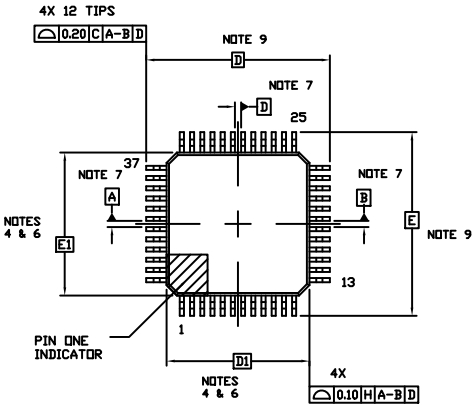
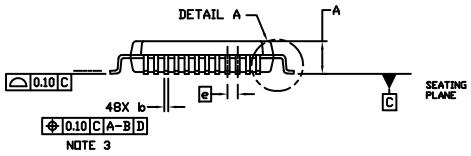
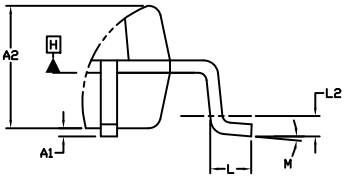
DATE 08 NOV 2013



TOP VIEW



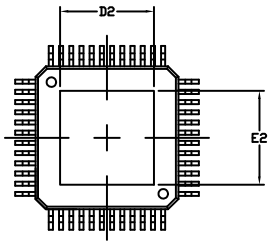
SIDE VIEW



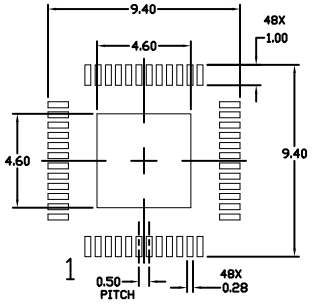
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.70
A1	0.00	0.15
A2	1.50 REF	
b	0.15	0.26
D	9.00 BSC	
D1	7.00 BSC	
D2	4.60 REF	
E	9.00 BSC	
E1	7.00 BSC	
E2	4.60 REF	
e	0.50 BSC	
L	0.30	0.70
L2	0.25 BSC	
M	0°	10°



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

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