4-Bit Bidirectional Level Shifter with Automatic Sensing & Ultra Tiny Package

Features

- High–Speed with 24 Mb/s Data Rate for push-pull applications
- High–Speed with 2 Mb/s Data Rate for open-drain applications
- 1.65V to 3.6V on A Port and 2.3V to 5.5V on B Port
- V_{CCA} must be less than or equal to V_{CCB}
- No Direction-Control Signal Needed
- Low Bit-to-Bit Skew
- Non-preferential Power-up Sequencing
- ESD protection exceeds JESD22-A114
  - A Port: 2500V HBM
  - B Port: 2500V HBM
- Integrated 10 kΩ Pull-Up Resistors
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 14-Pin, TSSOP (L)
  - 14-Pin, 3.5mm x 3.5mm, TQFN (ZB)
  - 12-Pin, 1.7mm x 2.0mm, XQFN (ZMA)
  - 12-Pin, 1.87mm x 1.37mm, WLCSP (GAB)

Application(s)

- I2C, SMBus, MDIO
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

Description

The DIODES™ LXS0104 is a 4-bit configurable, dual-supply, bidirectional, auto-sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. This allows bidirectional translation between lower and higher logic signal levels.

When the OE pin is low, all I/Os are configured to be in a high-impedance state.

Power-off protection is implemented to prevent current passing through the device when it is powered-down.

Block Diagram

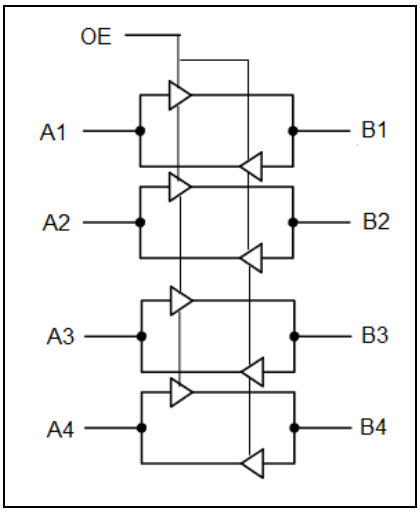
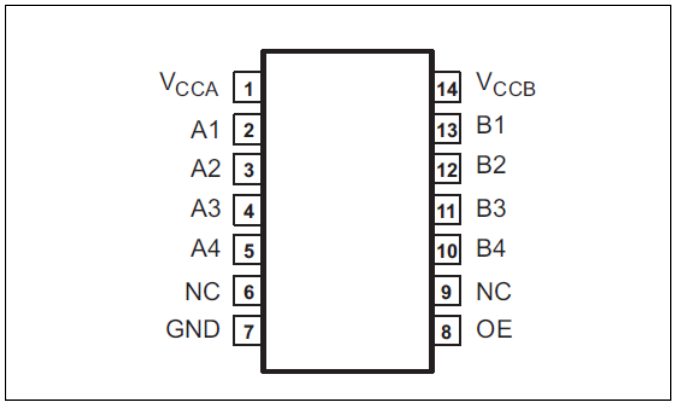


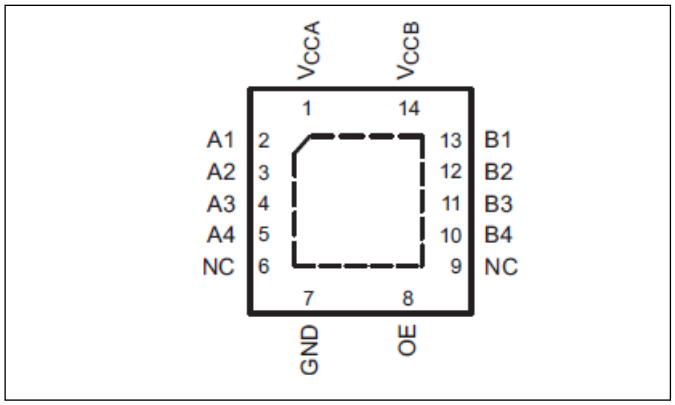
Figure 1: Block Diagram

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

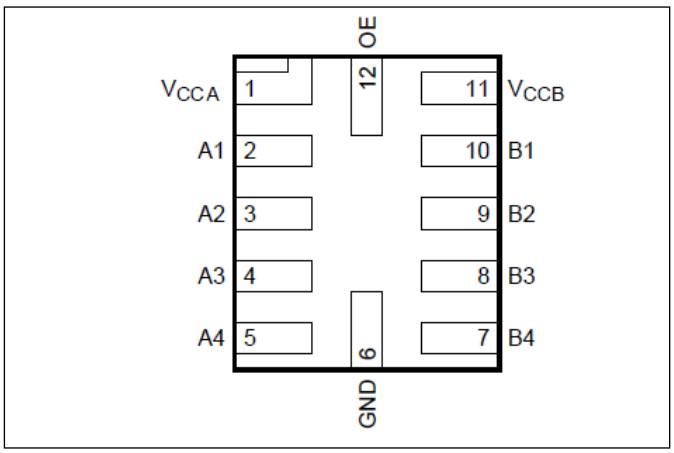
Pin Configuration



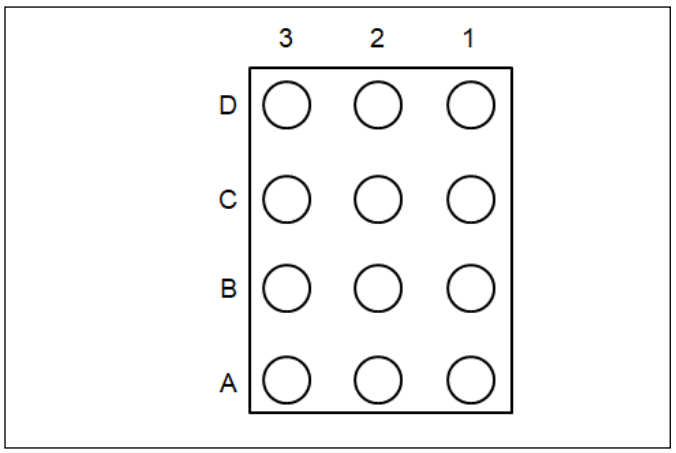
TSSOP-14 (TOP VIEW)



TQFN-14 (TOP VIEW)



XQFN-12 (TOP VIEW)



WLCSP (TOP VIEW)

Pin Description

Pin Name	TSSOP Pin#	TQFN Pin#	XQFN Pin#	WLCSP Pin#	Type	Description
V_{CCA}	1	1	1	B2	Power	A-port supply voltage.1.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	14	14	11	A2	Power	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5V
A1	2	2	2	A3	I/O	Input/output A. Referenced to V_{CCA}.
A2	3	3	3	B3	I/O	Input/output A. Referenced to V_{CCA}
A3	4	4	4	C3	I/O	Input/output A. Referenced to V_{CCA}
A4	5	5	5	D3	I/O	Input/output A. Referenced to V_{CCA}
B1	13	13	10	A1	I/O	Input/output B. Referenced to V_{CCB}
B2	12	12	9	B1	I/O	Input/output B. Referenced to V_{CCB}
B3	11	11	8	C1	I/O	Input/output B. Referenced to V_{CCB}
B4	10	10	7	D1	I/O	Input/output B. Referenced to V_{CCB}
OE	8	8	12	C2	Input	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	7	7	6	D2	GND	Ground.
NC	6,9	6,9	-	-	-	No Connection

Maximum Ratings

Storage Temperature	-65 °C to +150 °C
DC Supply Voltage port B	-0.5 V to +6.5 V
DC Supply Voltage port A	-0.5 V to +4.6 V
Vi (A) referenced DC Input Voltage	-0.5 V to +4.6 V
Vi (B) referenced DC Input Voltage	-0.5 V to +6.5 V
Enable Control Pin DC Input Voltage	-0.5 V to +4.6 V
Continuous output current, I/O	45 mA

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CCA}	V_{CCA} Positive DC Supply Voltage	1.65	-	3.6	V
V_{CCB}	V_{CCB} Positive DC Supply Voltage	2.3	-	5.5	V
V_{OE}	Enable Control Pin Voltage	GND	-	3.6	V
V_{IO}	I/O Pin Voltage (A1, A2, A3, A4)	GND	-	V_{CCA}	V
	I/O Pin Voltage (B1, B2, B3, B4)	GND	-	V_{CCB}	V
$\Delta t / \Delta v$	Input transition rise or fall time	-	-	-	-
	A or B port Push-Pull Driving, (V_{CCA} = 1.65 V to 3.6 V, V_{CCB} = 2.3 V to 5.5 V)	-	-	10	ns/V
	OE (V_{CCA} = 1.65 V to 3.6 V, V_{CCB} = 2.3 V to 5.5 V)	-	-	10	ns/V
T_A	Operating Temperature Range	−40	-	+85	°C

DC Electrical Characteristics

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

Symbol	Parameter	Test Conditions	V_{CCA}	V_{CCB}	Temp.	Min	Typ	Max	Unit
V_{IHB}	B port Input HIGH Voltage	I_{OHA} = -20 uA V_{IA} = V_{CCA} x 0.67	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	V_{CCI} – 0.4	-	-	V
V_{ILB}	B port Input LOW Voltage	I_{OLA} = 1 mA V_{IA} = 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	0.15	V
V_{IHA}	A port Input HIGH Voltage	I_{OHB}= -20 uA V_{IB} = V_{CCB} x 0.67	1.65 V to 1.95 V	2.3 V to 5.5 V	-40 to 85 ℃	V_{CCI} – 0.2	-	-	V
			1.65 V to 3.6 V	2.3 V to 5.5 V		V_{CCI} – 0.4			
V_{ILA}	A port Input LOW Voltage	I_{OLB} = 1 mA V_{IB} = 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	0.15	V
V_{IH}	Control Pin Input HIGH Voltage	-	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	V_{CCA} x 0.65	-	-	V
V_{IL}	Control Pin Input LOW Voltage	-	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	V_{CCA} x 0.35	V
V_{OHB}	B port Output HIGH Voltage	I_{OHB} = -20 uA $V_{IA} \geq V_{CCA}$ – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	0.8 x V_{CCB}	-	-	V
V_{OLB}	B port Output LOW Voltage	I_{OLB} = 1 mA $V_{IA} \leq$ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	0.4	V
V_{OHA}	A port Output HIGH Voltage	I_{OHA} = -20 uA $V_{IB} \geq V_{CCB}$ – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	0.8 * V_{CCA}	-	-	V
V_{OLA}	A port Output LOW Voltage	I_{OLA} = 1 mA $V_{IB} \leq$ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	0.4	V
I_I	Input leakage current	OE, V_I = V_{CCI} or GND	1.65 V to 3.6 V	2.3 V to 5.5 V	25 ℃	-	-	±1	µA
					-40 to 85 ℃	-	-	±2	
I_{OFF}	Partial power down current	A port	0 V	0 V to 5.5 V	25 ℃	-	-	±1	µA
					-40 to 85 ℃	-	-	±2	
		B port	0 V to 3.6 V	0 V	25 ℃	-	-	±1	
					-40 to 85 ℃	-	-	±2	
I_{OZ}	Off-state Leakage current	A or B port, OE = V_{IL}	1.65 V to 3.6 V	2.3 V to 5.5 V	25 ℃	-	-	±1	µA
					-40 to 85 ℃	-	-	±2	
I_{QVCCA}	V_{CCA} Supply Current	V_I = V_O = open, I_O = 0	1.65 V to 3.6	2.3 V to 5.5 V	-40 to 85 ℃	-	-	2.8	µA
			3.6 V	0 V	-40 to 85 ℃	-	-	2.2	
			0 V	5.5 V	-40 to 85 ℃	-	-	-1	

DC Electrical Characteristics Cont.

Symbol	Parameter	Test Conditions	V_{CCA}	V_{CCB}	Temp.	Min	Typ	Max	Unit
I_{QVCCB}	V_{CCB} Supply Current	V_I = V_O = open, I_O = 0	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	12	-
			3.6 V	0 V	-40 to 85 ℃	-	-	-1	μA
			0 V	5.5 V	-40 to 85 ℃	-	-	1	-
I_{QVCCA} + I_{QVCCB}	Total Supply current	V_I = V_O = open, I_O = 0	1.65 V to 3.6 V	2.3 V to 5.5 V	-40 to 85 ℃	-	-	14.4	μA
C_I	Input Capacitance	OE	3.3 V	3.3 V	25 ℃	-	2.5	-	pF
					-40 to 85 ℃	-	-	4.8	
C_{IO}	Input-to-output Capacitance	A or B port	3.3 V	3.3 V	25 ℃	-	12	-	pF
					-40 to 85 ℃	-	-	15	
		A port	0 V	0 V	25 ℃	-	5	6.5	
					-40 to 85 ℃	-	-	7.5	
		B port	0 V	0 V	25 ℃	-	6	7.5	
					-40 to 85 ℃	-	-	8.5	

AC Electrical Characteristics

(Unless otherwise specified, -40 ℃ ≤ T_A ≤ 85 ℃)

I/O test circuits of Figures 2, 3, 4 & 5, C_{LOAD} = 15 pF, R_{LOAD} = 1 MΩ, input pulse generator having the following characteristics: Z_O = 50 Ω, PRR ≤ 10 MHz, dv/dt ≥ 1 V / ns

V_{CCA}= 1.8 V ± 0.15 V

Symbol	Parameter	Test Conditions	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5.0 V ± 0.5 V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving	-	5.3	-	5.4	-	6.8	ns
		Open-Drain driving	-	8.8	-	9.6	-	10	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving	-	6.8	-	7.1	-	7.5	ns
		Open-Drain driving	-	260	-	208	-	198	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving	-	4.4	-	4.5	-	4.7	ns
		Open-Drain driving	-	5.3	-	4.4	-	4	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving	-	5.3	-	4.5	-	0.5	ns
		Open-Drain driving	-	175	-	140	-	102	
ten	Enable Time	OE to A or B	-	200	-	200	-	200	ns
tdis	Disable Time	OE to A or B	-	230	-	230	-	230	ns
t_{RA}	A port Rise Time	Push-pull driving	3.2	9.5	2.3	9.3	2.7	7.6	ns
		Open-Drain driving	32.8	165	27.9	132	20.5	95	
t_{RB}	B port Rise Time	Push-pull driving	2.8	10.8	2.7	9.1	2.1	7.6	ns
		Open-Drain driving	30	145	23	106	10	58	
t_{FA}	A port Fall Time	Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
		Open-Drain driving	3	6.9	3	6.4	3.1	6.1	
t_{FB}	B port Fall Time	Push-pull driving	2.9	13.8	2.8	16.2	2.8	16.2	ns
		Open-Drain driving	3.1	13.8	3.2	16.2	3.9	16.2	
t_{PPSKEW}	Channel-to-Channel Skew	-	-	0.7	-	0.7	-	0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	21	-	22	-	24	-	Mbps
		Open-Drain driving	2	-	2	-	2	-	

V_{CCA}= 2.5 V± 0.2 V

Symbol	Parameter	Test Conditions	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3V ± 0.3 V		V_{CCB} = 5.0 V ± 0.5 V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving	-	3.2	-	3.7	-	3.8	ns
		Open-Drain driving	-	6.3	-	6	-	5.8	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving	-	3.5	-	4.1	-	4.4	ns
		Open-Drain driving	-	250	-	206	-	190	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving	-	3	-	3.6	-	4.3	ns
		Open-Drain driving	-	4.7	-	4.2	-	4	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving	-	3.4	-	1.6	-	1	ns
		Open-Drain driving	-	170	-	140	-	103	
ten	Enable Time	OE to A or B	-	200	-	200	-	200	ns
tdis	Disable Time	OE to A or B	-	50	-	40	-	35	ns
t_{RA}	A port Rise Time	Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
		Open-Drain driving	24.9	149	22.8	121	18.4	89	
t_{RB}	B port Rise Time	Push-pull driving	2.7	8.3	2.4	7.2	2	6.1	ns
		Open-Drain driving	25.5	151	20.5	112	12	64	
t_{FA}	A port Fall Time	Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
		Open-Drain driving	2.9	6.9	2.9	6.2	2.9	5.8	
t_{FB}	B port Fall Time	Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
		Open-Drain driving	3	8.8	2.9	9.4	3.1	10.4	
t_{PPSKEW}	Channel-to-Channel Skew	-	-	0.7	-	0.7	-	0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	20	-	22	-	24	-	Mbps
		Open-Drain driving	2	-	2	-	2	-	

V_{CCA}= 3.3 V ± 0.3 V

Symbol	Parameter	Test Conditions	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5.0 V ± 0.5 V		Unit
			Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving	-	2.4	-	3.1	ns
		Open-Drain driving	-	4.2	-	4.6	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving	-	4.2	-	4.4	ns
		Open-Drain driving	-	204	-	165	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving	-	2.5	-	3.3	ns
		Open-Drain driving	-	124	-	97	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving	-	2.5	-	2.6	ns
		Open-Drain driving	-	139	-	105	
ten	Enable Time	OE to A or B	-	200	-	200	ns
tdis	Disable Time	OE to A or B	-	230	-	230	ns
t_{RA}	A port Rise Time	Push-pull driving	2.3	5.6	1.9	4.8	ns
		Open-Drain driving	17.4	116	15.4	85	
t_{RB}	B port Rise Time	Push-pull driving	2.5	6.4	2.1	7.4	ns
		Open-Drain driving	17.7	116	11.8	72	
t_{FA}	A port Fall Time	Push-pull driving	2	5.4	1.9	5	ns
		Open-Drain driving	2.8	6.1	2.8	5.7	
t_{FB}	B port Fall Time	Push-pull driving	2.3	7.4	2.4	7.6	ns
		Open-Drain driving	2.8	7.6	2.9	8.3	
t_{PPSKEW}	Channel-to-Channel Skew	-	-	0.7	-	0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	23	-	24	-	Mbps
		Open-Drain driving	2	-	2	-	

Test Circuits

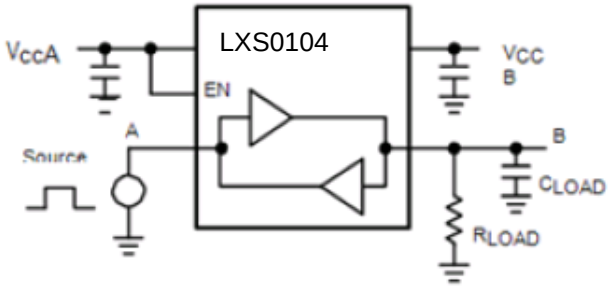


Figure 2: Rail-to-Rail Driving A

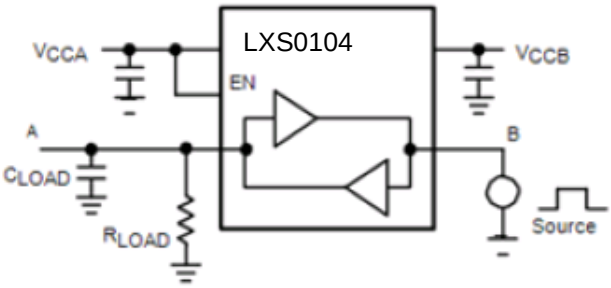


Figure 3: Rail-to-Rail Driving B

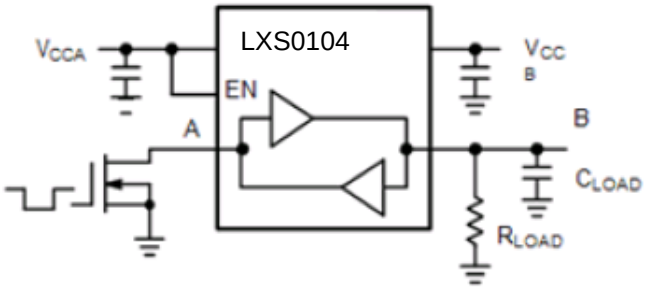


Figure 4: Open-Drain Driving A

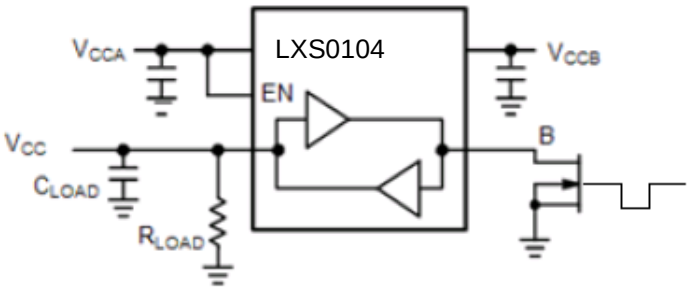
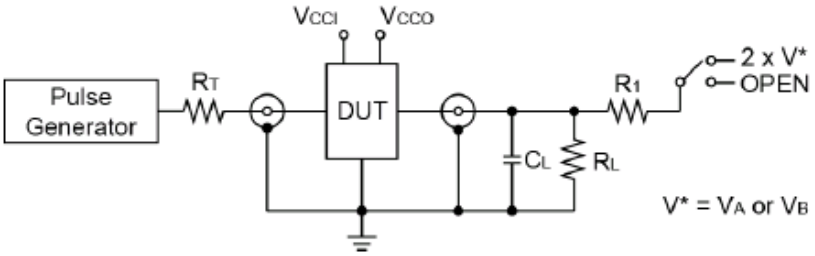


Figure 5: Open-Drain Driving B



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V*

C_L = 15pF
$R_L = R_1$ = 50kΩ
$R_T = Z_{OUT}$ of pulse generator (Typically 50Ω)
V* = V_A or V_B for A or B measurements, respectively.

Figure 6: Test Circuit for Enable/Disable Time Measurement

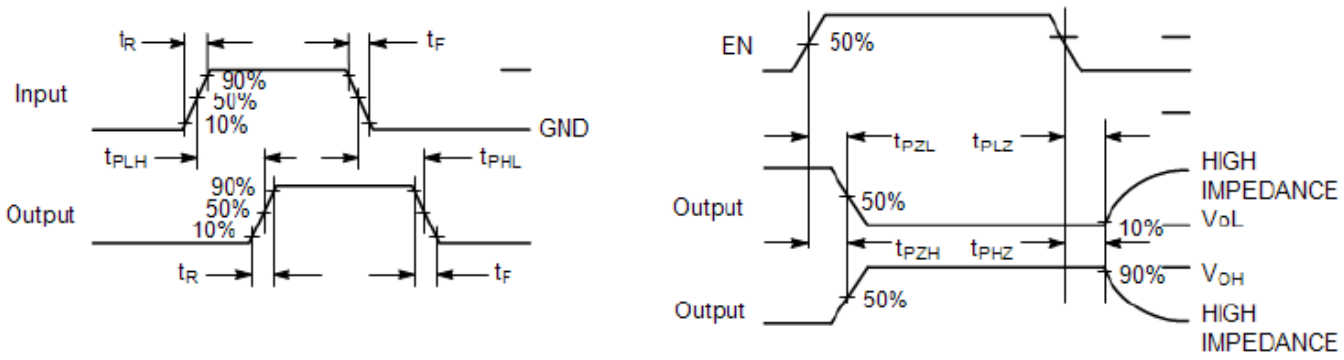


Figure 7: Timing Definitions for Propagation Delays and Enable/Disable Measurement

Functional Description

Level Translator Architecture

The LXS0104 is a 4-bit configurable, dual-supply, bidirectional, auto-sensing translator that does not require a directional control pin. The A port operating voltage range is from 1.65 V to 3.6 V, and the B port operating voltage range is from 2.3 V to 5.5 V.

The translator has integrated a 10 kΩ pull–up resistor on each I/O line. The integrated pull-up resistors are used to pull the I/O lines to either V_{CCA} or V_{CCB}. When OE goes low, the pull-up resistors are disabled. There is an nmos transistor that connects the A-port and B-port. In addition, each output has integrated an one-shot rising edge detector to turn on the pmos transistor within a short duration to improve the low-to-high transition.

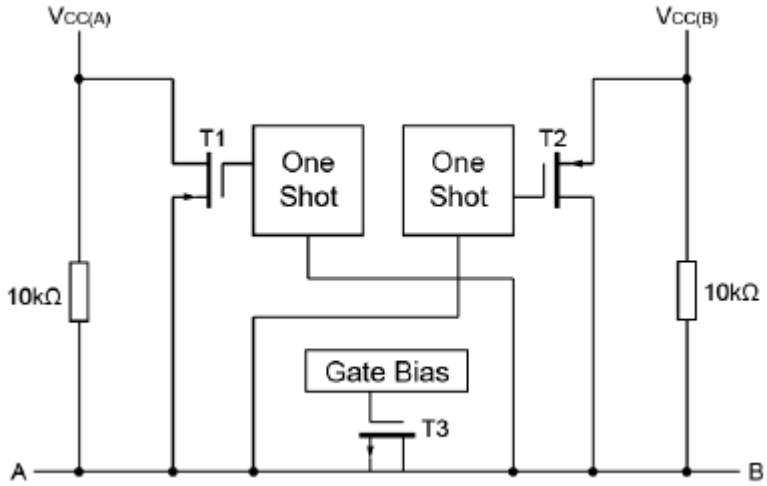


Figure 8: Architecture of LXS0104 I/O cell (one channel)

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull–up resistors. In addition, the propagation times (t_{PD}), and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 Ω.

Output Enable and Disable (OE)

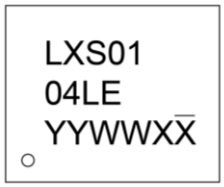
The LXS0104 has an Output Enable pin (OE) that enables the device by setting HIGH. Driving the Output Enable pin to a low logic level minimizes the power consumption of the device and set all I/Os in high-impedance OFF state. Normal translation operation occurs when the OE pin is equal to a logic high signal. The OE pin is referenced to the V_{CCA} supply.

Power Supply Guidelines

During normal operation, supply voltage V_{CCA} must be less than or equal to V_{CCB}. The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01µF to 0.1µF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

Part Marking

L Package



YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd "X" means Cu wire

ZB Package

YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above 2nd "X" means Cu wire

ZMA Package

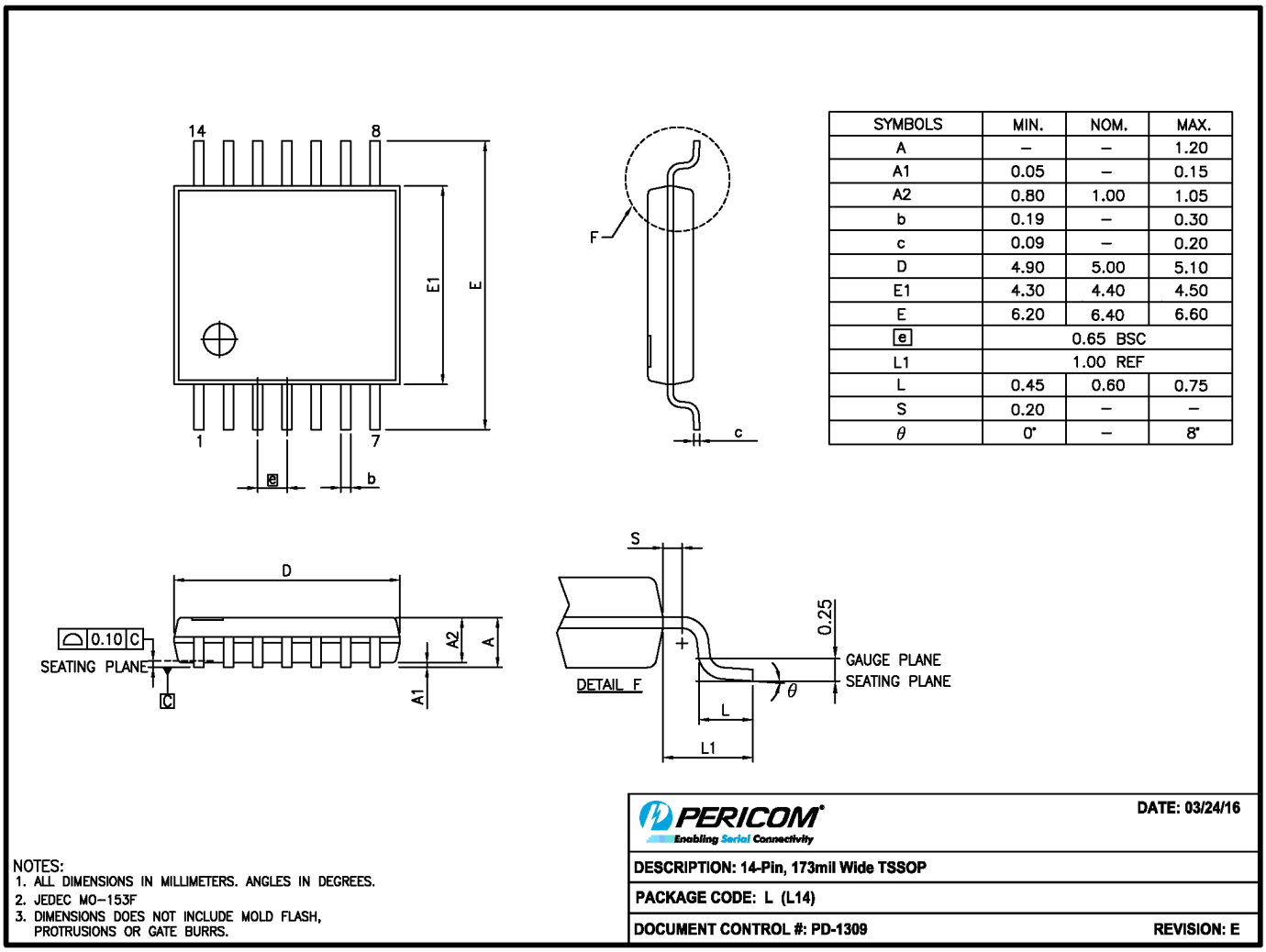
xW: LXS0104ZMAE
Y: Date Code (Year)
W: Date Code (Workweek)

GAB Package

YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code

Packaging Mechanical

TSSOP-14 (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/24/16

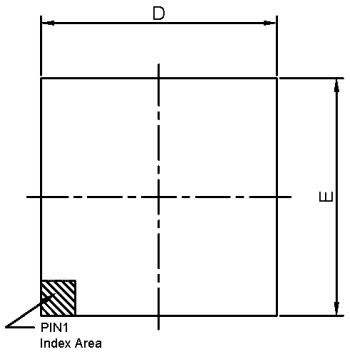
DESCRIPTION: 14-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L14)

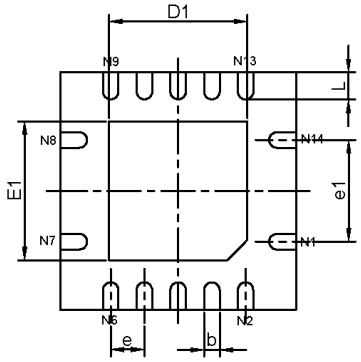
DOCUMENT CONTROL #: PD-1309 REVISION: E

16-0060

TQFN-14 (ZB)

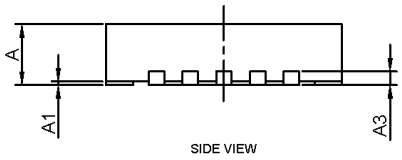


TOP VIEW

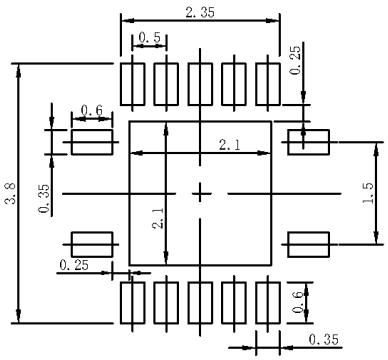


BOTTOM VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
D	3.42	3.58
E	3.42	3.58
D1	1.95	2.15
E1	1.95	2.15
b	0.20	0.30
e	0.50 TYP	
e1	1.50 TYP	
L	0.32	0.48



SIDE VIEW



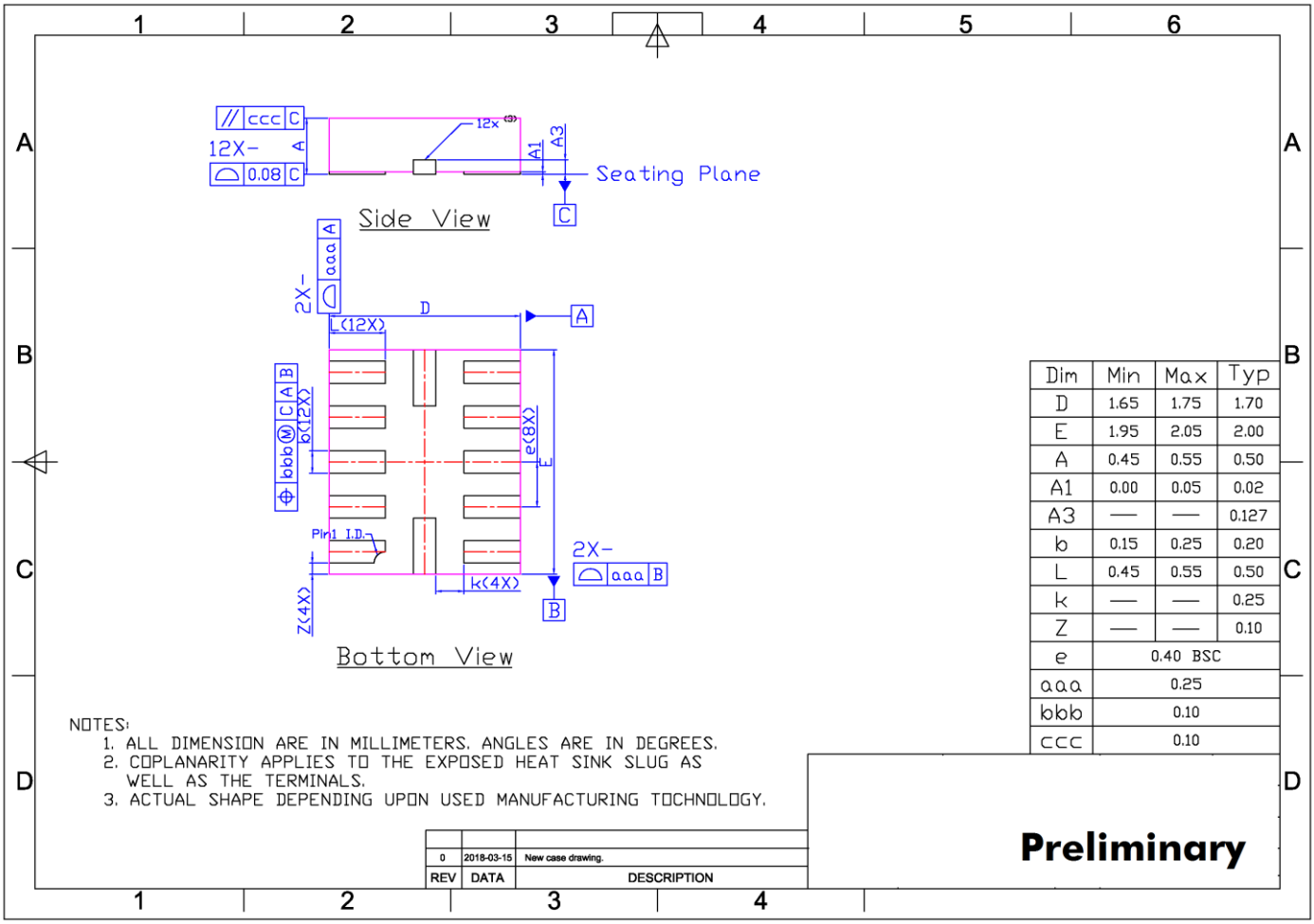
RECOMMENDED LAND PATTERN(unit:mm)

Notes:
1. Controlling dimensions in millimeters.
2. Ref: JEDEC MO-220
3.LAND PATTERN REFERENCE DIODES V-DFN3535-14 PACKAGE INFORMATION

	DATE: 03/11/21
DESCRIPTION: 14-Pin, TQFN, 3.5*3.5	
PACKAGE CODE: ZB (ZB14)	
DOCUMENT CONTROL#: PD-2154	REVISION: A

21-1377

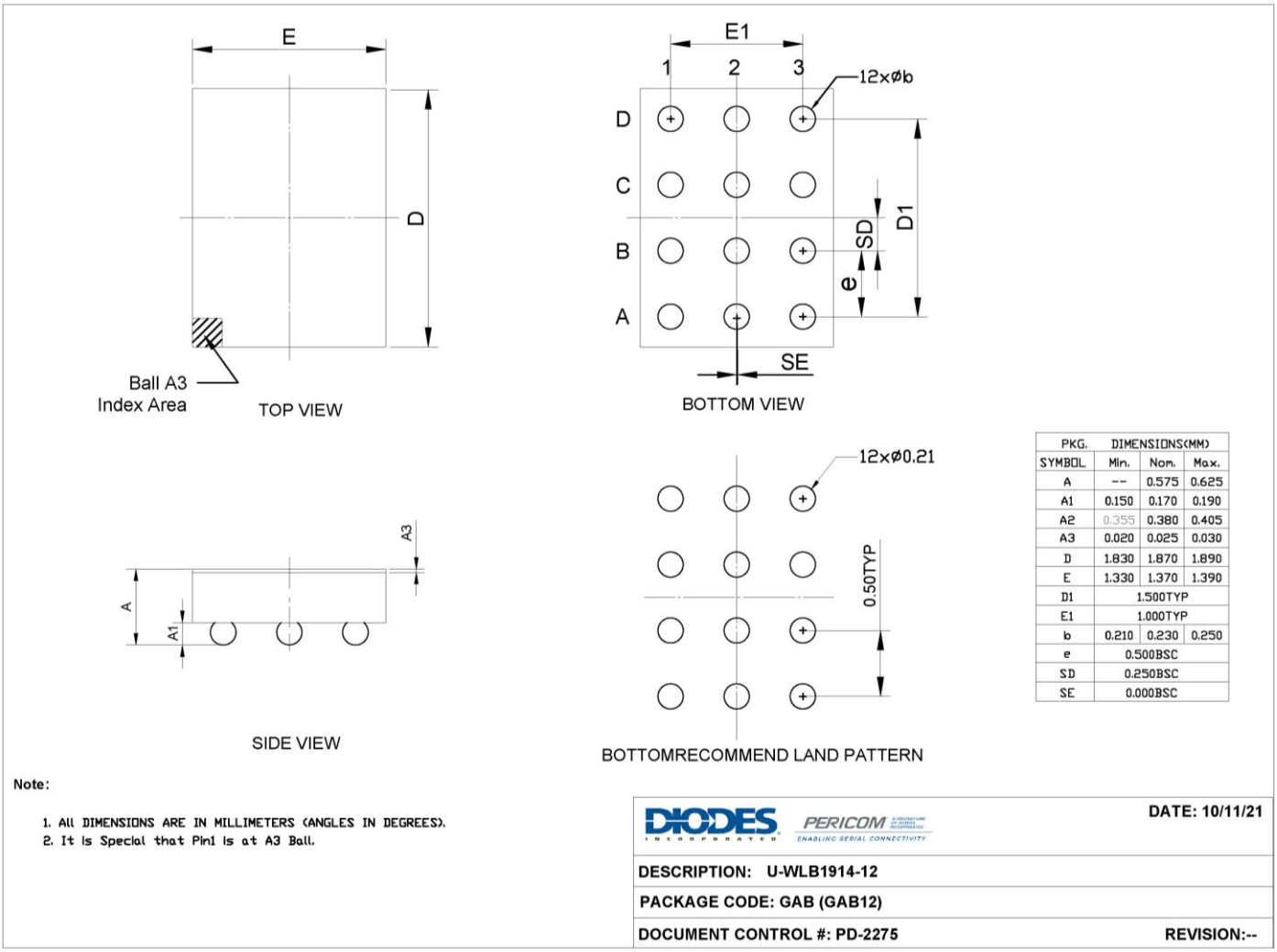
XQFN-12



Dim	Min	Max	Typ
D	1.65	1.75	1.70
E	1.95	2.05	2.00
A	0.45	0.55	0.50
A1	0.00	0.05	0.02
A3	—	—	0.127
b	0.15	0.25	0.20
L	0.45	0.55	0.50
k	—	—	0.25
Z	—	—	0.10
e	0.40 BSC		
aaa	0.25		
bbb	0.10		
ccc	0.10		

REV	DATA	DESCRIPTION
0	2018-03-15	New case drawing.

WLCSP-12



PKG.	DIMENSIONS(MM)		
SYMBOL	Min.	Nom.	Max.
A	--	0.575	0.625
A1	0.150	0.170	0.190
A2	0.355	0.380	0.405
A3	0.020	0.025	0.030
D	1.830	1.870	1.890
E	1.330	1.370	1.390
D1	1.500TYP		
E1	1.000TYP		
b	0.210	0.230	0.250
e	0.500BSC		
SD	0.250BSC		
SE	0.000BSC		

For latest package info.

Please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package Description
LXS0104LEX	L	14-pin, TSSOP
LXS0104ZBEX	ZB	14-pin,TQFN 3.5mm x 3.5mm
LXS0104ZMAEX	ZMA	12-pin, XQFN 1.7mm x 2.0mm
LXS0104GABEX	GAB	12-ball, WLCSP

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel