

Description

Mxxxx204 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 16Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually infinite endurance and retention, and scalable non-volatile memory technology.

Mxxxx204 is available in small footprint 8-pad DFN (WSON) and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

Mxxxx204 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Typical Applications

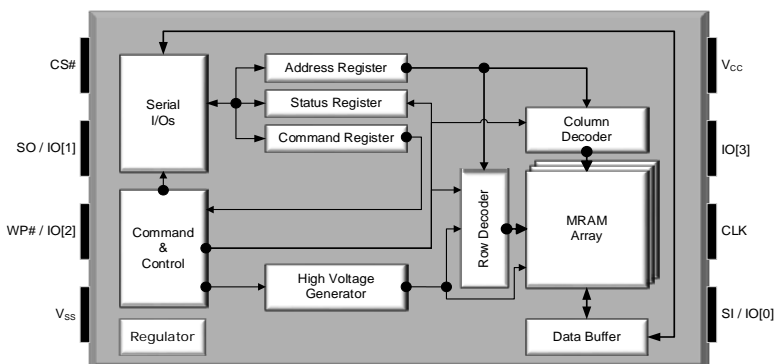
- Ideal for applications that must store and retrieve data without incurring large latency penalties.
- Factory Automation
- Multifunction Printers
- Industrial Control And Monitoring
- Medical Diagnostics
- Data Switches And Routers

Features

- Interface
 - Serial Peripheral Interface QSPI (4-4-4)
 - Single Data Rate Mode: 108MHz
 - Double Data Rate Mode: 54MHz
- Technology
 - 40nm pMTJ STT-MRAM

Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention specification in Table 31)
- Density
 - 4Mb, 8Mb, 16Mb
- Operating Voltage Range
 - VCC: 1.71V – 2.00V
 - VCC: 2.70V – 3.60V
- Operating Temperature Range
 - Industrial: -40°C to 85°C
 - Industrial Plus: -40°C to 105°C
- Packages
 - 8-pad DFN (WSON) (5.0mm x 6.0mm)
 - 8-pin SOIC (5.2mm x 5.2mm)
- Data Protection
 - Hardware Based: Write Protect Pin (WP#)
 - Software Based: Address Range Selectable through Configuration bits (Top/Bottom, Block Protect[2:0])
- Identification
 - 64-bit Unique ID
 - 64-bit User Programmable Serial Number
- Augmented Storage Array
 - 256-byte User Programmable with Write Protection
- Supports JEDEC Reset
- RoHS & REACH Compliant

Block Diagram



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1. General Description

Mxxxx204 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 16Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

Figure 1: Technology Comparison

| | SRAM | Flash | EEPROM | MRAM |
|--------------------------|------|-------|--------|------|
| Non-Volatility | - | √ | √ | √ |
| Write Performance | √ | - | - | √ |
| Read Performance | √ | - | - | √ |
| Endurance | √ | - | - | √ |
| Power | - | - | - | √ |

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually infinite endurance and retention, and scalable non-volatile memory technology.

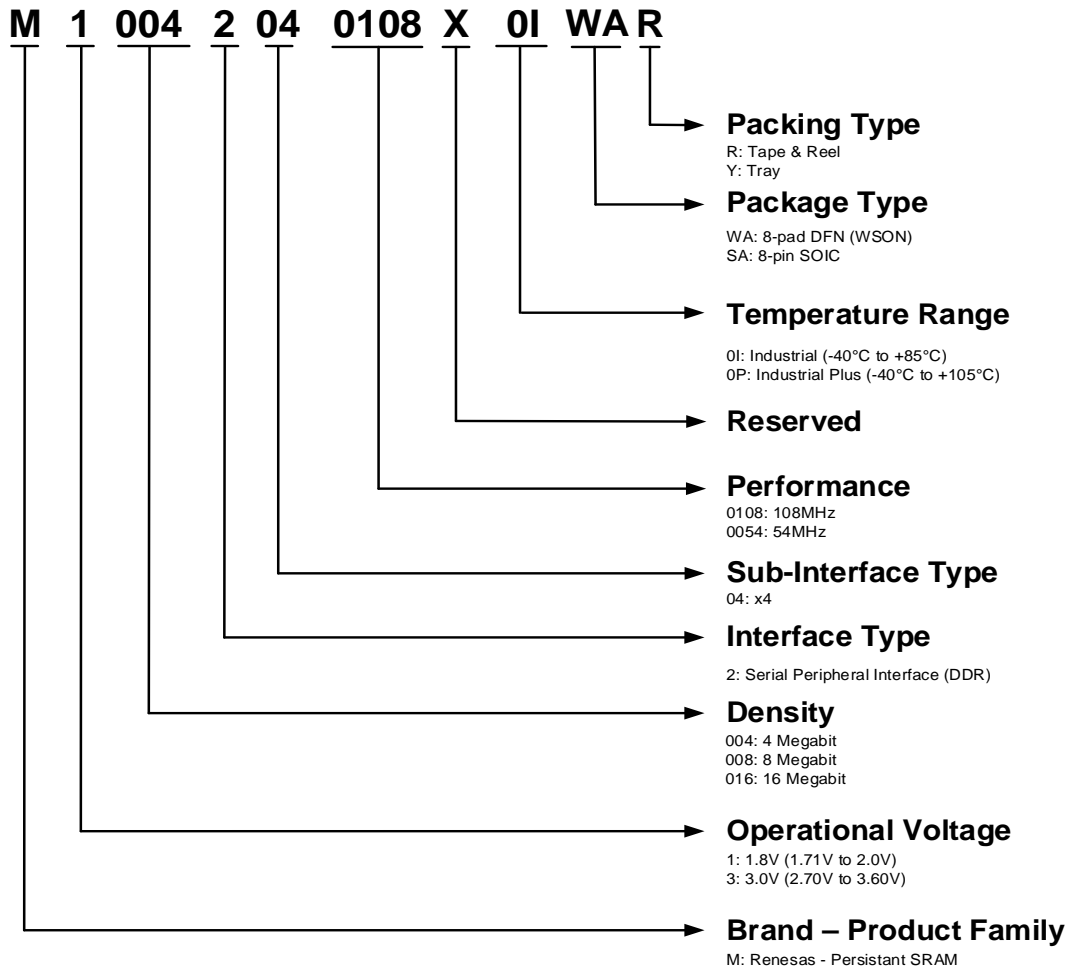
Mxxxx204 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

Mxxxx204 is available in small footprint 8-pad DFN (WSON) and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

Mxxxx204 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

2. Ordering Options

The ordering part numbers are formed by a valid combination of the following options:



2.1 Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1: Valid Combinations List

| Valid Combinations – 108MHz | | | | |
|-----------------------------|-------------------|--------------|--------------|--------------------|
| Base Part Number | Temperature Range | Package Type | Packing Type | Part Number |
| M10042040108X | 0I, 0P | WA, SA | R, Y | M10042040108X0IWAR |
| | | | | M10042040108X0IWAY |
| | | | | M10042040108X0ISAR |
| | | | | M10042040108X0ISAY |
| | | | | M10042040108X0PWAR |
| | | | | M10042040108X0PWAY |
| | | | | M10042040108X0PSAR |
| M10042040108X0PSAY | | | | |
| M30042040108X | 0I, 0P | WA, SA | R, Y | M30042040108X0IWAR |
| | | | | M30042040108X0IWAY |
| | | | | M30042040108X0ISAR |
| | | | | M30042040108X0ISAY |
| | | | | M30042040108X0PWAR |
| | | | | M30042040108X0PWAY |
| | | | | M30042040108X0PSAR |
| M30042040108X0PSAY | | | | |
| M10082040108X | 0I, 0P | WA, SA | R, Y | M10082040108X0IWAR |
| | | | | M10082040108X0IWAY |
| | | | | M10082040108X0ISAR |
| | | | | M10082040108X0ISAY |
| | | | | M10082040108X0PWAR |
| | | | | M10082040108X0PWAY |
| | | | | M10082040108X0PSAR |
| M10082040108X0PSAY | | | | |
| M30082040108X | 0I, 0P | WA, SA | R, Y | M30082040108X0IWAR |
| | | | | M30082040108X0IWAY |
| | | | | M30082040108X0ISAR |
| | | | | M30082040108X0ISAY |
| | | | | M30082040108X0PWAR |
| | | | | M30082040108X0PWAY |
| | | | | M30082040108X0PSAR |
| M30082040108X0PSAY | | | | |
| M10162040108X | 0I, 0P | WA, SA | R, Y | M10162040108X0IWAR |
| | | | | M10162040108X0IWAY |
| | | | | M10162040108X0ISAR |
| | | | | M10162040108X0ISAY |
| | | | | M10162040108X0PWAR |
| | | | | M10162040108X0PWAY |
| | | | | M10162040108X0PSAR |
| M10162040108X0PSAY | | | | |
| M30162040108X | 0I, 0P | WA, SA | R, Y | M30162040108X0IWAR |
| | | | | M30162040108X0IWAY |
| | | | | M30162040108X0ISAR |
| | | | | M30162040108X0ISAY |
| | | | | M30162040108X0PWAR |
| | | | | M30162040108X0PWAY |
| | | | | M30162040108X0PSAR |
| M30162040108X0PSAY | | | | |

| Valid Combinations – 54MHz | | | | |
|----------------------------|-------------------|--------------|--------------|--------------------|
| Base Part Number | Temperature Range | Package Type | Packing Type | Part Number |
| M10042040054X | 0I, 0P | WA, SA | R, Y | M10042040054X0IWAR |
| | | | | M10042040054X0IWAY |
| | | | | M10042040054X0ISAR |
| | | | | M10042040054X0ISAY |
| | | | | M10042040054X0PWAR |
| | | | | M10042040054X0PWAY |
| | | | | M10042040054X0PSAR |
| | | | | M10042040054X0PSAY |
| M30042040054X | 0I, 0P | WA, SA | R, Y | M30042040054X0IWAR |
| | | | | M30042040054X0IWAY |
| | | | | M30042040054X0ISAR |
| | | | | M30042040054X0ISAY |
| | | | | M30042040054X0PWAR |
| | | | | M30042040054X0PWAY |
| | | | | M30042040054X0PSAR |
| | | | | M30042040054X0PSAY |
| M10082040054X | 0I, 0P | WA, SA | R, Y | M10082040054X0IWAR |
| | | | | M10082040054X0IWAY |
| | | | | M10082040054X0ISAR |
| | | | | M10082040054X0ISAY |
| | | | | M10082040054X0PWAR |
| | | | | M10082040054X0PWAY |
| | | | | M10082040054X0PSAR |
| | | | | M10082040054X0PSAY |
| M30082040054X | 0I, 0P | WA, SA | R, Y | M30082040054X0IWAR |
| | | | | M30082040054X0IWAY |
| | | | | M30082040054X0ISAR |
| | | | | M30082040054X0ISAY |
| | | | | M30082040054X0PWAR |
| | | | | M30082040054X0PWAY |
| | | | | M30082040054X0PSAR |
| | | | | M30082040054X0PSAY |
| M10162040054X | 0I, 0P | WA, SA | R, Y | M10162040054X0IWAR |
| | | | | M10162040054X0IWAY |
| | | | | M10162040054X0ISAR |
| | | | | M10162040054X0ISAY |
| | | | | M10162040054X0PWAR |
| | | | | M10162040054X0PWAY |
| | | | | M10162040054X0PSAR |
| | | | | M10162040054X0PSAY |
| M30162040054X | 0I, 0P | WA, SA | R, Y | M30162040054X0IWAR |
| | | | | M30162040054X0IWAY |
| | | | | M30162040054X0ISAR |
| | | | | M30162040054X0ISAY |
| | | | | M30162040054X0PWAR |
| | | | | M30162040054X0PWAY |
| | | | | M30162040054X0PSAR |
| | | | | M30162040054X0PSAY |

3. Signal Description and Assignment

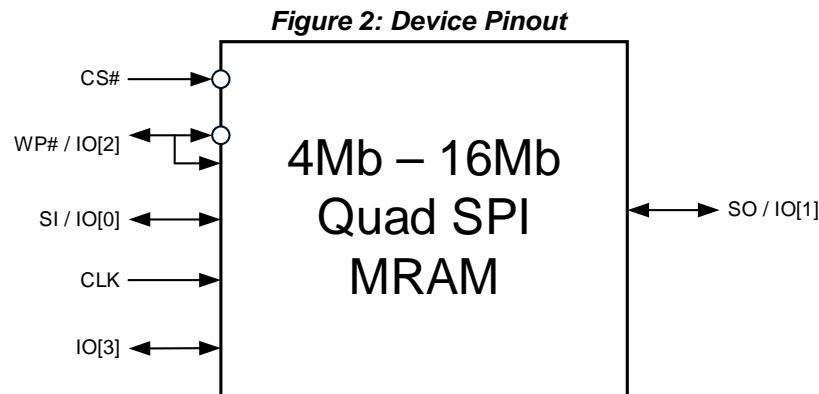


Table 2: Signal Description

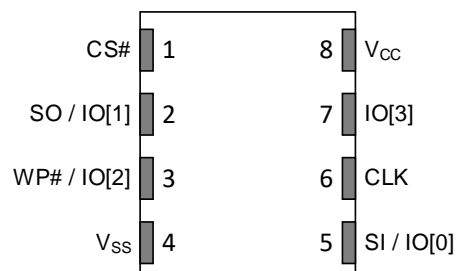
| Signal | Type | Description |
|-------------|-----------------------|---|
| CS# | Input | Chip Select: When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions. |
| WP# / IO[2] | Input / Bidirectional | Write Protect (SPI): Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used. Bidirectional Data 2 (DPI/QPI): The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes. |
| CLK | Input | Clock: Provides the timing for the serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. <ul style="list-style-type: none"> • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only |
| IO[3] | Bidirectional | Bidirectional Data 3 (DPI/QPI): The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes. This pin can be tied to Vcc if not used. |
| SI / IO[0] | Input / Bidirectional | Serial Data Input (SPI): The unidirectional I/O transfers data into the device on the rising edge of the clock in Single SPI mode. Bidirectional Data 0 (DPI/QPI): The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes. |

| Signal | Type | Description |
|-----------------|------------------------------|--|
| SO / IO[1] | Output / Bidirectional | Serial Data Output (SPI): The unidirectional I/O transfers data out of the device on the falling edge of the clock in Single SPI mode. Bidirectional Data 1 (DPI/QPI): The bidirectional I/O that transfers data into and out of the device in Dual and Quad SPI modes. |
| V _{CC} | Supply | V _{CC} : Core and I/O power supply. |
| V _{SS} | Supply | V _{SS} : Core and I/O ground supply. |

4. Package Options

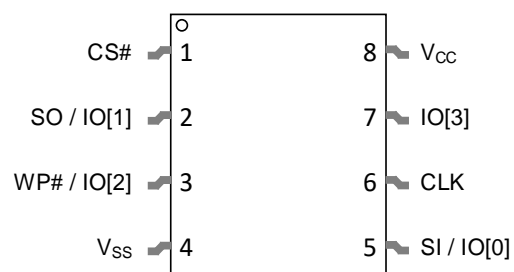
4.1 8-Pad DFN (WSON) (Top View)

Figure 3: 8-Pad DFN (WSON)



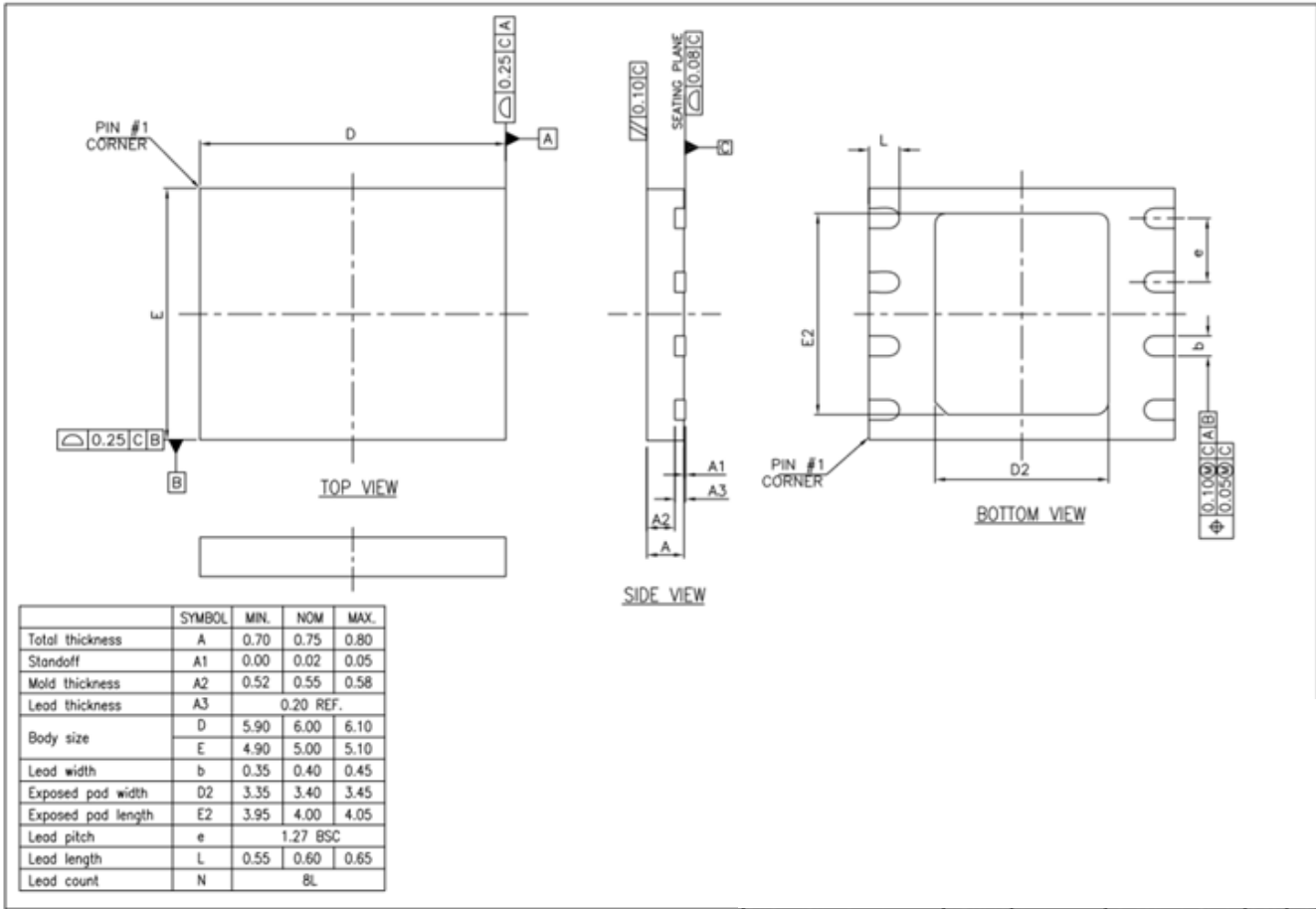
4.2 8-Pin SOIC (Top View)

Figure 4: 8-Pin SOIC

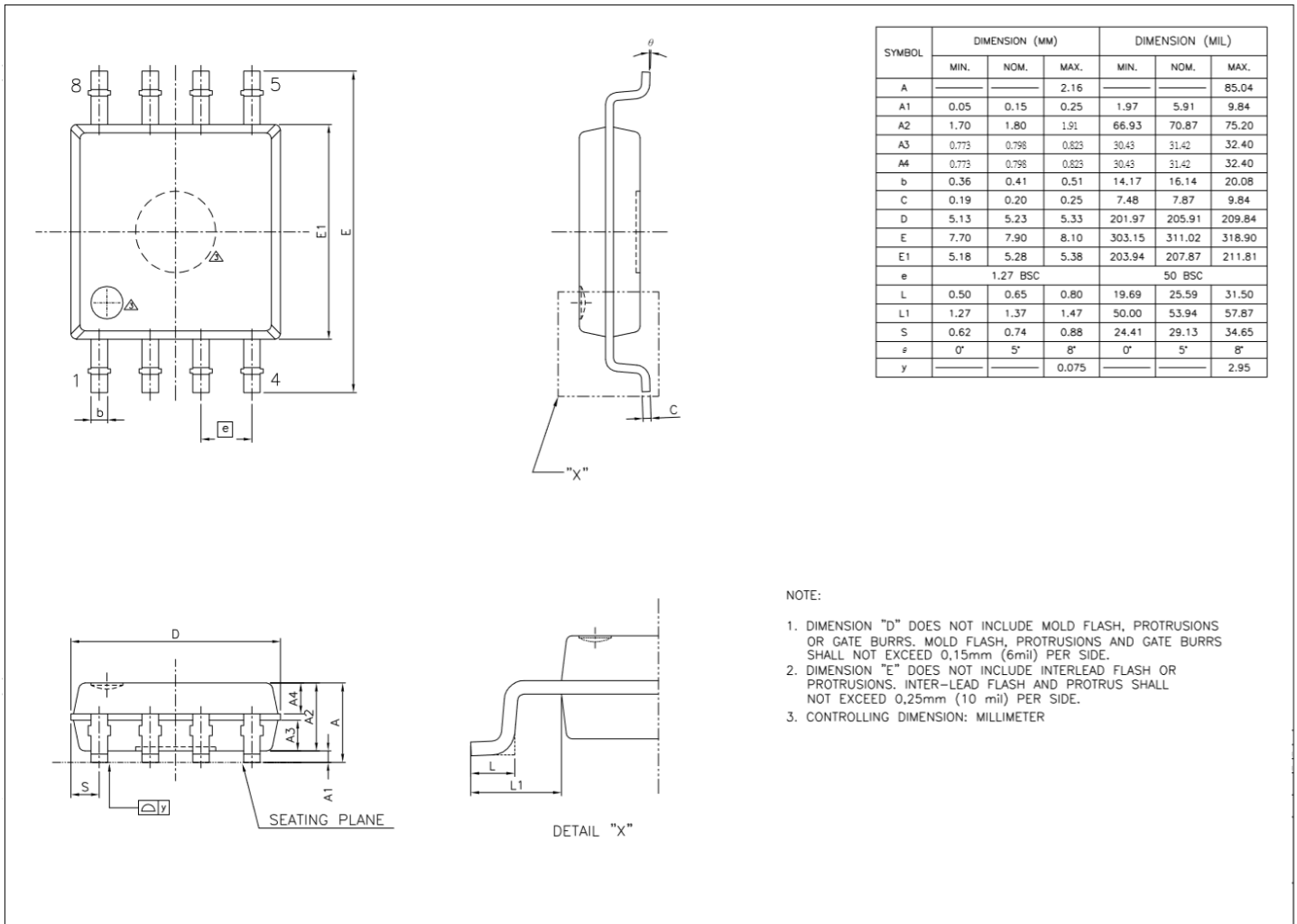


5. Package Drawings

5.1 8-Pad DFN (WSON)



5.2 8-Pin SOIC



6. Architecture

Mxxxx204 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running at 108MHz, eExecute-In-Place (XIP) functionality, and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

Mxxxx204 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin. In Dual and Quad SPI modes, IO[0:1] and IO[0:3] are used to access the device respectively. Furthermore, Single Data Rate (SDR) and Double Data Rate (DDR) instructions utilize CLK edges differently to transfer information; SDR uses a single CLK edge whereas DDR uses both edges of CLK. **Table 3** summarizes all the different interface modes supported and their respective I/O usage. **Table 4** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

Table 3: Interface Modes of Operations

| Instruction Component | Single SPI (1-1-1) | Dual Input Output SPI (1-1-2) | Dual I/O SPI (1-2-2) | DPI (2-2-2) | Quad Input Output SPI (1-1-4) | Quad I/O SPI (1-4-4) | QPI (4-4-4) |
|-----------------------|-----------------------|----------------------------------|-------------------------|----------------|----------------------------------|-------------------------|----------------|
| Command | SI / IO[0] | SI / IO[0] | SI / IO[0] | IO[1:0] | SI / IO[0] | SI / IO[0] | IO[3:0] |
| Address | SI / IO[0] | SI / IO[0] | IO[1:0] | IO[1:0] | SI / IO[0] | IO[3:0] | IO[3:0] |
| Data Input | SI / IO[0] | IO[1:0] | IO[1:0] | IO[1:0] | IO[3:0] | IO[3:0] | IO[3:0] |
| Data Output | SO / IO[1] | IO[1:0] | IO[1:0] | IO[1:0] | IO[3:0] | IO[3:0] | IO[3:0] |

Table 4: Clock Edge Used for instructions in SDR and DDR modes

| Instruction Type | Command | Address | Data Input | Data Output |
|------------------|--------------|---------------------------|---------------------------|-----------------------------|
| (1-1-1) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (1-1-1) DDR | \uparrow_R | $\uparrow_R \downarrow_F$ | $\uparrow_R \downarrow_F$ | $\downarrow_F \uparrow_R$ 1 |
| (1-1-2) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (1-2-2) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (2-2-2) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (2-2-2) DDR | \uparrow_R | $\uparrow_R \downarrow_F$ | $\uparrow_R \downarrow_F$ | $\downarrow_F \uparrow_R$ 1 |
| (1-1-4) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (1-4-4) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (1-4-4) DDR | \uparrow_R | $\uparrow_R \downarrow_F$ | $\uparrow_R \downarrow_F$ | $\downarrow_F \uparrow_R$ 1 |
| (4-4-4) SDR | \uparrow_R | \uparrow_R | \uparrow_R | \downarrow_F 1 |
| (4-4-4) DDR | \uparrow_R | $\uparrow_R \downarrow_F$ | $\uparrow_R \downarrow_F$ | $\downarrow_F \uparrow_R$ 1 |

Notes:

R: Rising Clock Edge

F: Falling Clock Edge

1: Data output from Mxxxx204 always begins on the falling edge of the clock – SDR & DDR

Mxxxx204 supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

Mxxxx204 offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

Mxxxx204 has a 256-byte Augmented Storage Array which is independent from the main memory array. It is user programmable and can be write protected against inadvertent writes.

Two lower power states are available in Mxxxx204, namely Deep Power Down and Hibernate. Data is not lost while the device is in either of these two low power states. Moreover, the device maintains all its configurations.

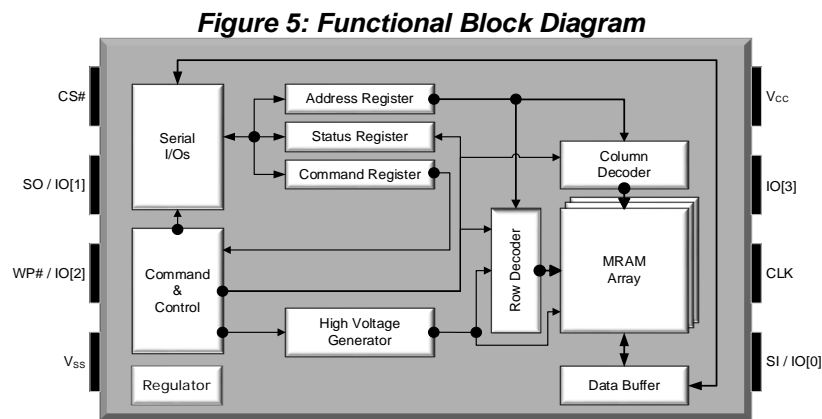


Table 5: Modes of Operation

| Mode | Current | CS# | CLK | SI / IO[3:0] | SO / IO[3:0] |
|------------------------|--------------------|-----|--------|------------------------------|--------------|
| Standby | I _{SB} | H | Gated | Gated / Hi-Z | Hi-Z / Hi-Z |
| Active - Read | I _{READ} | L | Toggle | Command, Address | Data Output |
| Active - Write | I _{WRITE} | L | Toggle | Command, Address, Data Input | Hi-Z |
| Deep Power Down | I _{DPD} | H | Gated | Gated / Hi-Z | Hi-Z / Hi-Z |
| Hibernate | I _{HBN} | H | Gated | Gated / Hi-Z | Hi-Z / Hi-Z |

Notes:

H: High (Logic '1')

L: Low (Logic '0')

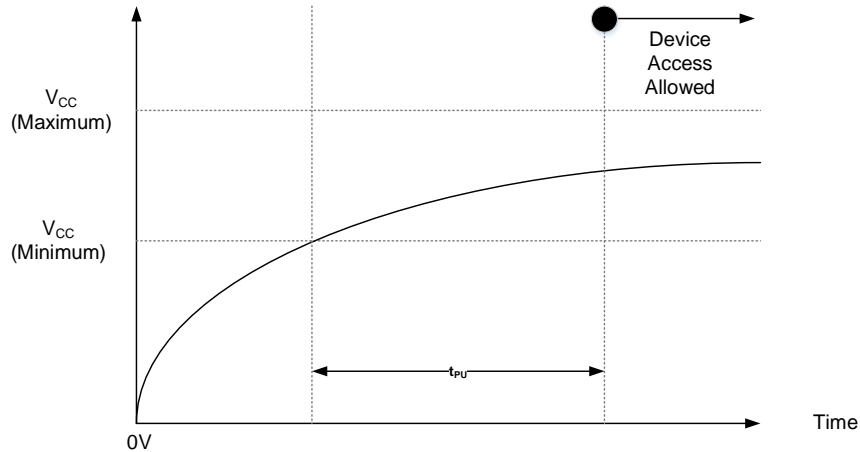
Hi-Z: High Impedance

7. Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (t_{RVR})
- CS# must follow V_{CC} during power-up (a 10K Ω pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- During initial Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences
- Upon Power-up, the device is in Standby mode

Figure 6: Power-Up Behavior



When powering down or in case of brown-out, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} below V_{CC_RST} level
- CS# must follow V_{CC} during power-down (a 10K Ω pull-up Resistor to V_{CC} is recommended)
- The device must not be selected and that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- The Power-up timing and device initialization needs to be observed after V_{CC} ramps up above V_{CC} (minimum)
- To stabilize the V_{CC} level, suitable decoupling capacitors close to package V_{CC} pin is recommended
- Chip functionality not guaranteed if V_{CC} ramps down between V_{CC_CUTOFF} and V_{CC_RST} and then ramps up to V_{CC}

Figure 7: Power-Down and Brown-out Behavior

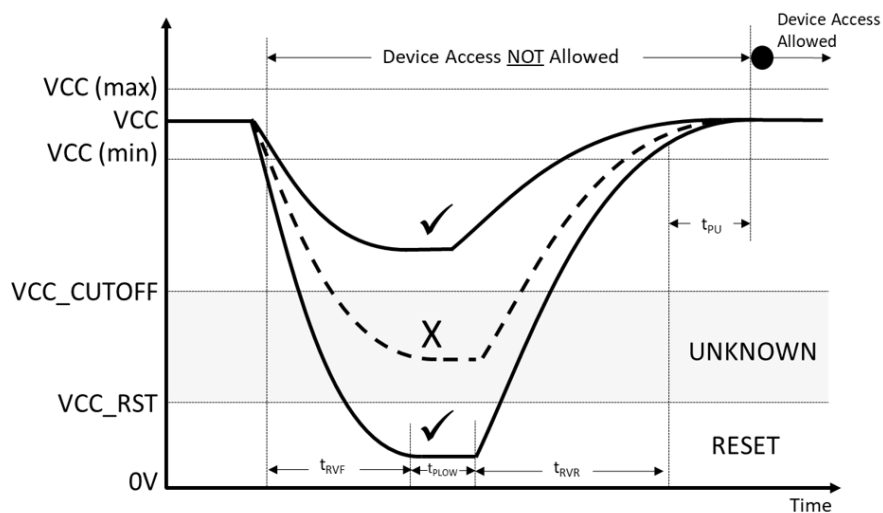


Table 6: Power Up/Down Timing – 3.0V

| Parameter | Symbol | Test Conditions | 3.0V | | | Units |
|---|------------------------|---|---------|---------|---------|-------|
| | | | Minimum | Typical | Maximum | |
| V _{CC} Range | V _{CC} | All operating voltages and temperatures | 2.7 | - | 3.6 | V |
| V _{CC} Ramp Up Time to V _{CC} (min) | t _{RVR} | | 30 | - | 1500 | μs |
| V _{CC} Ramp Down Time to V _{CC_RST} | t _{RVF} | | 20 | - | - | μs |
| V _{CC} Power Up to First Instruction | t _{PU} | | 250 | - | - | μs |
| V _{CC} Cutoff – Must Initialize Device | V _{CC_CUTOFF} | | 1.6 | - | - | V |
| V _{CC} Reset | V _{CC_RST} | | 0 | - | 0.3 | V |
| V _{CC} Power Down Low Time | t _{PLOW} | | 1000 | - | - | μs |
| Time to Enter Deep Power Down | t _{EDPD} | | - | - | 3 | μs |
| Time to Exit Deep Power Down | t _{EXDPD} | | - | - | 400 | μs |
| Time to Enter Hibernate | t _{ENTHIB} | | - | - | 3 | μs |
| Time to Exit Hibernate | t _{EXHIB} | | - | - | 450 | μs |
| CS# Pulse Width | t _{CSDPD} | | 50 | - | - | ns |

Table 7: Power Up/Down Timing – 1.8V

| Parameter | Symbol | Test Conditions | 1.8V | | | Units |
|---|------------------------|---|---------|---------|---------|-------|
| | | | Minimum | Typical | Maximum | |
| V _{CC} Range | V _{CC} | All operating voltages and temperatures | 1.71 | - | 2.0 | V |
| V _{CC} Ramp Up Time to V _{CC} (min) | t _{RVR} | | 30 | - | 1000 | μs |
| V _{CC} Ramp Down Time to V _{CC_RST} | t _{RVF} | | 20 | - | - | μs |
| V _{CC} Power Up to First Instruction | t _{PU} | | 250 | - | - | μs |
| V _{CC} Cutoff – Must Initialize Device | V _{CC_CUTOFF} | | 1.6 | - | - | V |
| V _{CC} Reset | V _{CC_RST} | | 0 | - | 0.2 | V |
| V _{CC} Power Down Low Time | t _{PLOW} | | 1000 | - | - | μs |
| Time to Enter Deep Power Down | t _{EDPD} | | - | - | 3 | μs |
| Time to Exit Deep Power Down | t _{EXDPD} | | - | - | 400 | μs |
| Time to Enter Hibernate | t _{ENTHIB} | | - | - | 3 | μs |
| Time to Exit Hibernate | t _{EXHIB} | | - | - | 450 | μs |
| CS# Pulse Width | t _{CSDPD} | | 50 | - | - | ns |

8. Memory Map

Table 8: Memory Map

| Density | Address Range | 24-bit Address [23:0] | |
|---------|--------------------|-----------------------|----------------------|
| 4Mb | 000000h – 07FFFFh | [23:19] – Logic '0' | [18:0] - Addressable |
| 8Mb | 000000h – 0FFFFFFh | [23:20] – Logic '0' | [19:0] - Addressable |
| 16Mb | 000000h – 1FFFFFFh | [23:21] – Logic '0' | [20:0] - Addressable |

9. Augmented Storage Array Map

Table 9: Augmented Storage Array Map

| Density | Address Range | 24-bit Address [23:0] | |
|---------|--------------------------------|-----------------------|---------------------|
| 4Mb | 000000h – 0000FFh ¹ | [23:8] – Logic '0' | [7:0] - Addressable |
| 8Mb | 000000h – 0000FFh ¹ | [23:8] – Logic '0' | [7:0] - Addressable |
| 16Mb | 000000h – 0000FFh ¹ | [23:8] – Logic '0' | [7:0] - Addressable |

Notes:

1: The 256-byte augmented storage array is divided into 8 individually readable and writeable sections (32 bytes per section). After an individual section is programmed, it can be write protected to prevent further programming.

Table 10: Individual Section Address Range

| Section | Address Range | 24-bit Address [23:0] | |
|---------|-------------------|-----------------------|---------------------|
| 0 | 000000h – 00001Fh | [23:8] – Logic '0' | [7:0] - Addressable |
| 1 | 000020h – 00003Fh | [23:8] – Logic '0' | [7:0] - Addressable |
| 2 | 000040h – 00005Fh | [23:8] – Logic '0' | [7:0] - Addressable |
| 3 | 000060h – 00007Fh | [23:8] – Logic '0' | [7:0] - Addressable |
| 4 | 000080h – 00009Fh | [23:8] – Logic '0' | [7:0] - Addressable |
| 5 | 0000A0h – 0000BFh | [23:8] – Logic '0' | [7:0] - Addressable |
| 6 | 0000C0h – 0000DFh | [23:8] – Logic '0' | [7:0] - Addressable |
| 7 | 0000E0h – 0000FFh | [23:8] – Logic '0' | [7:0] - Addressable |

10. Register Addresses

Table 11: Register Addresses

| Register Name | Address |
|--------------------------------|-----------|
| Status Register | 0x000000h |
| Configuration Register 1 | 0x000002h |
| Configuration Register 2 | 0x000003h |
| Configuration Register 3 | 0x000004h |
| Configuration Register 4 | 0x000005h |
| Device Identification Register | 0x000030h |
| Unique Identification Register | 0x000040h |

Note:

1: Register address space is different from the memory array and augmented storage array.

MRAM INITIALIZATION REQUIREMENT

After reflow temp cycle, MRAM Registers must be reconfigured to default settings. Please see the apps note; "Programming Non-Volatile Registers to Factory Default State Post-Reflow Application Note" for details.

11. Register Map

11.1 Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

Table 12: Status Register – Read and Write

| Bits | Name | Description | Read / Write | Default State | Selection Options |
|-------|----------|---|--------------|---------------|--|
| SR[7] | WP#EN | Hardware Based WP# Protection Enable/Disable | R/W | 0 | 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low |
| SR[6] | SNPEN | Serial Number Protection Enable/Disable | R/W | 0 | 1: S/N Write protected - protection enabled 0: S/N Writable - protection disabled |
| SR[5] | TBSEL | Software Top/Bottom Memory Array Protection Selection | R/W | 0 | 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range) |
| SR[4] | BPSEL[2] | Block Protect Selection Bit 2 | R/W | 0 | Block Protection Bits (Table 13, Table 14) |
| SR[3] | BPSEL[1] | Block Protect Selection Bit 1 | R/W | 0 | |
| SR[2] | BPSEL[0] | Block Protect Selection Bit 0 | R/W | 0 | |
| SR[1] | WREN | Write Operation Protection Enable/Disable | R | 0 | 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled |
| SR[0] | RSVD | Reserved | R | 0 | Reserved for future use |

Table 13: Top Block Protection Address Range Selection (TBPSEL=0)

| BPSEL [2] | BPSEL [1] | BPSEL [0] | Protected Portion | 4Mb | 8Mb | 16Mb |
|-----------|-----------|-----------|-------------------|-------------------|--------------------|--------------------|
| 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 1 | Upper 1/64 | 07E000h – 07FFFFh | 0FC000h – 0FFFFFFh | 1F8000h – 1FFFFFFh |
| 0 | 1 | 0 | Upper 1/32 | 07C000h – 07FFFFh | 0F8000h – 0FFFFFFh | 1F0000h – 1FFFFFFh |
| 0 | 1 | 1 | Upper 1/16 | 078000h – 07FFFFh | 0F0000h – 0FFFFFFh | 1E0000h – 1FFFFFFh |
| 1 | 0 | 0 | Upper 1/8 | 070000h – 07FFFFh | 0E0000h – 0FFFFFFh | 1C0000h – 1FFFFFFh |
| 1 | 0 | 1 | Upper 1/4 | 060000h – 07FFFFh | 0C0000h – 0FFFFFFh | 180000h – 1FFFFFFh |
| 1 | 1 | 0 | Upper 1/2 | 040000h – 07FFFFh | 080000h – 0FFFFFFh | 1F0000h – 1FFFFFFh |
| 1 | 1 | 1 | All | 000000h – 07FFFFh | 000000h – 0FFFFFFh | 000000h – 1FFFFFFh |

Table 14: Bottom Block Protection Address Range Selection (TBPSEL=1)

| BPSEL [2] | BPSEL [1] | BPSEL [0] | Protected Portion | 4Mb | 8Mb | 16Mb |
|-----------|-----------|-----------|-------------------|-------------------|-------------------|-------------------|
| 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 1 | Lower 1/64 | 000000h – 001FFFh | 000000h – 003FFFh | 000000h – 007FFFh |
| 0 | 1 | 0 | Lower 1/32 | 000000h – 003FFFh | 000000h – 007FFFh | 000000h – 00FFFFh |
| 0 | 1 | 1 | Lower 1/16 | 000000h – 007FFFh | 000000h – 00FFFFh | 000000h – 01FFFFh |
| 1 | 0 | 0 | Lower 1/8 | 000000h – 00FFFFh | 000000h – 01FFFFh | 000000h – 03FFFFh |
| 1 | 0 | 1 | Lower 1/4 | 000000h – 01FFFFh | 000000h – 03FFFFh | 000000h – 07FFFFh |
| 1 | 1 | 0 | Lower 1/2 | 000000h – 03FFFFh | 000000h – 07FFFFh | 000000h – 0FFFFFh |
| 1 | 1 | 1 | All | 000000h – 07FFFFh | 000000h – 0FFFFFh | 000000h – 1FFFFFh |

Table 15: Write Protection Modes

| WREN (Status Register) | WP#EN (Status Register) | WP# (Pin) | Status & Configuration Registers | Memory ¹ Array Protected Area | Memory ¹ Array Unprotected Area |
|------------------------|-------------------------|-----------|----------------------------------|--|--|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Unprotected | Protected | Unprotected |
| 1 | 1 | Low | Protected | Protected | Unprotected |
| 1 | 1 | High | Unprotected | Protected | Unprotected |

Notes:

High: Logic '1'

Low: Logic '0'

X: Don't Care – Can be Logic '0' or '1'

Protected: Write protected

Unprotected: Writable

1: Memory address range protection based on Block Protection Bits

11.2 Augmented Storage Array Protection Register (Read/Write)

Augmented Storage Array Protection register contains options for enabling/disabling data protection for eight 32-byte sections.

Table 16: Augmented Storage Array Protection Register – Read and Write

| Bits | Name | Description | Read / Write | Default State | Selection Options |
|--------|---------|---|--------------|---------------|---|
| ASP[7] | ASPS[7] | ASA Section 7 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[6] | ASPS[6] | ASA Section 6 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[5] | ASPS[5] | ASA Section 5 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[4] | ASPS[4] | ASA Section 4 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[3] | ASPS[3] | ASA Section 3 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[2] | ASPS[2] | ASA Section 2 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[1] | ASPS[1] | ASA Section 1 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |
| ASP[0] | ASPS[0] | ASA Section 0 Write Protection Enable/Disable | R/W | 0 | 1: Protection Enabled 0: Protection Disabled |

11.3 Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 17: Device Identification Register – Read Only

| Bits | Avalanche Manufacturer's ID | Device Configuration | | | | |
|----------|-----------------------------|----------------------|-----------|-----------|----------|---------|
| | | Interface | Voltage | Temp | Density | Freq |
| ID[31:0] | ID[31:24] | ID[23:20] | ID[19:16] | ID[15:12] | ID[11:8] | ID[7:0] |

| Manufacturer ID | Interface | Voltage | Temperature | Density | Frequency |
|-----------------|--------------|-------------|--------------------|-------------|---------------------|
| 31-24 | 23-20 | 19-16 | 15-12 | 11-8 | 7-0 |
| 1110 0110 | 0000-HP QSPI | 0001 - 3V | 0000 - -40°C- 85°C | 0010 - 4Mb | 00000001 - 108MHz |
| | | 0010 - 1.8V | 0001 - -40°C-105°C | 0011 - 8Mb | 00000010 - 54MHz |
| | | | | 0100 - 16Mb | 00000011 - Reserved |
| | | | | | 00000100 - Reserved |
| | | | | | 00000101 - Reserved |

11.4 Serial Number Register (Read/Write)

Serial Number register is user writable.

Table 18: Serial Number Register – Read and Write

| Bits | Name | Description | Read / Write | Default State ¹ | Selection Options |
|-----------------|------|---------------------|--------------|----------------------------|---------------------------------------|
| SN[63:0] | SN | Serial Number Value | R/W | 000000000000 0000h | Value stored is based on the customer |

Notes:

1: The default value is how the device is shipped from the factory.

11.5 Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 19: Unique ID Register – Read Only

| Bits | Name | Description | Read / Write | Selection Options |
|------------------|------|------------------------------------|--------------|---|
| UID[63:0] | UID | Unique Identification Number Value | R | Value stored is written in the factory and is device specific |

11.6 Configuration Register 1 (Read/Write)

Configuration Register 1 controls locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register.

Table 20: Configuration Register 1 – Read and Write

| Bits | Name | Description | Read / Write | Default State | Selection Options |
|--------|-------|---|--------------|---------------|--|
| CR1[7] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[6] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[5] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[4] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[3] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[2] | MAPLK | Status Register Lock Enable/Disable (TBSEL, BPSEL[2:0]) | R/W | 0 | 1: Lock TBSEL and BPSEL[2:0] 0: Unlock TBSEL and BPSEL[2:0] |
| CR1[1] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR1[0] | ASPLK | Augmented Storage Array Data Protection | R/W | 0 | 1: Write Protect Augmented Storage Array 0: Not Write Protect Augmented Storage Array |

11.7 Configuration Register 2 (Read/Write)

Configuration Register 2 controls the interface type along with memory array access latency.

Table 21: Configuration Register 2 – Read and Write

| Bits | Name | Description | Read / Write | Default State | Selection Options |
|--------|----------|--|----------------|---------------|---|
| CR2[7] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR2[6] | QPISL | Quad SPI (QPI 4-4-4) Interface Mode Enable/Disable | R ² | 0 | 1: Quad SPI (QPI 4-4-4) Enabled 0: Single SPI (SPI 1-1-1) Enabled |
| CR2[5] | RSVD | Reserved | R | 0 | Reserved for future use |
| CR2[4] | DPISL | Dual SPI (DPI 2-2-2) Interface Mode Enable/Disable | R ² | 0 | 1: Dual SPI (DPI 2-2-2) Enabled 0: Single SPI (SPI 1-1-1) Enabled |
| CR2[3] | MLATS[3] | Memory Array Read Latency Selection ¹ | R/W | 0 | 0000: 0 Cycles - Default |
| CR2[2] | MLATS[2] | | | 0 | 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles |
| CR2[1] | MLATS[1] | | | 0 | 0100: 4 Cycles 0101: 5 Cycles |
| CR2[0] | MLATS[0] | | | 0 | 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycle 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles |

Notes:

1: Latency is frequency dependent. Please consult Table 22 and Table 23.

2: These interface options can only be set through instructions.

Table 22: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

| Read Type | Latency | Max Frequency | |
|--------------------|---------|---------------|--------------|
| | | Mxxxx2x108xx | Mxxxx2x054xx |
| (1-1-1) SDR | 8-15 | 108MHz | 54MHz |
| (1-1-1) DDR | | 54MHz | 27MHz |
| (1-1-2) SDR | | 108MHz | 54MHz |
| (1-2-2) SDR | | 108MHz | 54MHz |
| (2-2-2) SDR | | 108MHz | 54MHz |
| (2-2-2) DDR | | 54MHz | 27MHz |
| (1-1-4) SDR | 12-15 | 108MHz | 54MHz |
| (1-4-4) SDR | | 108MHz | 54MHz |
| (1-4-4) DDR | | 54MHz | 27MHz |
| (4-4-4) SDR | | 108MHz | |
| (4-4-4) DDR | | 54MHz | 27MHz |

Table 23: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

| Read Type | Latency | Max Frequency | |
|--------------------|---------|---------------|--------------|
| | | Mxxxx2x108xx | Mxxxx2x054xx |
| (1-1-1) SDR | 0 | 50MHz | 40MHz |

Table 24: Augmented Storage Array Read Latency Cycles vs. Maximum Clock Frequency

| Read Type | Latency | Max Frequency | |
|--------------------|---------|---------------|--------------|
| | | Mxxxx2x108xx | Mxxxx2x054xx |
| (1-1-1) SDR | 8-15 | 50MHz | 40MHz |

Table 25: Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

| Read Type | Max Frequency | Latency Cycles |
|--------------------|---------------|----------------|
| (1-1-1) SDR | 108MHz | 8 |
| (2-2-2) SDR | 108MHz | 4 |
| (4-4-4) SDR | 108MHz | 2 |

11.8 Configuration Register 3 (Read/Write)

Configuration Register 3 controls the output driver strength along with read data wrap selection.

Table 26: Configuration Register 3 – Read and Write

| Bits | Name | Description | Read / Write | Default | | Selection Options | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|------------------|--|--------------|-------------|------|---|--|-------------|-------------|------|------------------|-----|------|------|-----|------|-----|-----|------|-----|------------------|------|-----|-----|------|-----|-----|------|-----|-----|------|-----|-----|
| | | | | 1.8V | 3.0V | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[7] | ODSEL[2] | Output Driver Strength Selector | R/W | 0 | 0 | <table border="0"> <tr> <td></td> <td><u>1.8V</u></td> <td><u>3.0V</u></td> </tr> <tr> <td>000:</td> <td>45Ω¹</td> <td>35Ω</td> </tr> <tr> <td>001:</td> <td>120Ω</td> <td>75Ω</td> </tr> <tr> <td>010:</td> <td>90Ω</td> <td>60Ω</td> </tr> <tr> <td>011:</td> <td>70Ω</td> <td>45Ω¹</td> </tr> <tr> <td>100:</td> <td>45Ω</td> <td>35Ω</td> </tr> <tr> <td>101:</td> <td>60Ω</td> <td>40Ω</td> </tr> <tr> <td>110:</td> <td>30Ω</td> <td>20Ω</td> </tr> <tr> <td>111:</td> <td>20Ω</td> <td>15Ω</td> </tr> </table> | | <u>1.8V</u> | <u>3.0V</u> | 000: | 45Ω ¹ | 35Ω | 001: | 120Ω | 75Ω | 010: | 90Ω | 60Ω | 011: | 70Ω | 45Ω ¹ | 100: | 45Ω | 35Ω | 101: | 60Ω | 40Ω | 110: | 30Ω | 20Ω | 111: | 20Ω | 15Ω |
| | <u>1.8V</u> | | | <u>3.0V</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000: | 45Ω ¹ | | | 35Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001: | 120Ω | | | 75Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010: | 90Ω | 60Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011: | 70Ω | 45Ω ¹ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100: | 45Ω | 35Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101: | 60Ω | 40Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 110: | 30Ω | 20Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111: | 20Ω | 15Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[6] | ODSEL[1] | | | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[5] | ODSEL[0] | | | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[4] | WRAPS | Read WRAP Enable / Disable (16/32/64/128/256 Byte) | R/W | 0 | | 1: Read Data Wrap Enabled 0: Read Data Wrap Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[3] | RSVD | Reserved | R | 0 | | Reserved for future use | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[2] | WRPLS[2] | Wrap Length Selector ² | R/W | 0 | | 000: 16-byte Boundary 001: 32-byte Boundary 010: 64-byte Boundary 011: 128-byte Boundary 100: 256-byte Boundary 101: Reserved 110: Reserved 111: Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[1] | WRPLS[1] | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR3[0] | WRPLS[0] | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Notes:

1: Default Setting (V_{CC} dependent).

2: If Wrap is enabled, the read data wraps within an aligned 16/32/64/128/256-byte boundary at any address. The starting address entered selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If read continues, the address wraps to the beginning of the group and continues to read sequentially.

11.9 Configuration Register 4 (Read/Write)

Configuration Register 4 controls Write Enable protection (WREN – Status Register) reset functionality during memory array writing¹. This functionality makes SPI MRAM compatible to other SPI devices.

Table 27: Configuration Register 4 – Read and Write

| Bits | Name | Description | Read / Write | Default State | Selection Options |
|--------|----------|--|--------------|---------------|--|
| CR4[7] | RSVD | Reserved | R/W | 0 | Reserved for future use |
| CR4[6] | RSVD | Reserved | | 0 | Reserved for future use |
| CR4[5] | RSVD | Reserved | | 0 | Reserved for future use |
| CR4[4] | RSVD | Reserved | | 0 | Reserved for future use |
| CR4[3] | RSVD | Reserved | | 0 | Reserved for future use |
| CR4[2] | RSVD | Reserved | | 1 | Reserved ² |
| CR4[1] | WRENS[1] | WREN Reset Selector | | 0 | 00: Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) 11: Illegal - Reserved for future use |
| CR4[0] | WRENS[0] | (Memory & Augmented Storage Array Write Functionality) | 1 | | |

Notes:

1: Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

2: Must be set to “1”. Writing a “0” to this bit may impact device functionality.

12. Instruction Set

Table 28: Instruction Set

| # | Instruction Name | Command (Opcode) | (1-0-0) | (1-0-1) | (1-1-1) | (1-1-2) | (1-2-2) | (2-0-0) | (2-0-2) | (2-2-2) | (1-1-4) | (1-4-4) | (4-0-0) | (4-0-4) | (4-4-4) | XIP | SDR | DDR | Latency Cycles | Data Bytes | Max. Frequency | Prerequisite |
|-----------------------------------|--|------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----|-----|-----|----------------|------------|----------------|--------------|
| Control Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 1 | No Operation | NOOP 00h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 2 | Write Enable | WREN 06h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 3 | Write Disable | WRDI 04h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 4 | Enable DPI | DPIE 37h | • | | | | | | | | | | • | | | | | | | | 108 MHz | |
| 5 | Enable QPI | QPIE 38h | • | | | | | • | | | | | | | | | | | | | 108 MHz | |
| 6 | Enable SPI | SPIE Fh | | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 7 | Enter Deep Power Down | DPDE B9h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 8 | Enter Hibernate | HBNE BAh | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 9 | Software Reset Enable | SRTE 66h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| 10 | Software Reset | SRST 99h | • | | | | | • | | | | | • | | | | | | | | 108 MHz | SRTE |
| 11 | Exit Deep Power Down | DPDX ABh | • | | | | | • | | | | | • | | | | | | | | 108 MHz | |
| Read Register Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 12 | Read Status Register | RDSR 05h | • | | | | | • | | | | | • | | | | | | | 1 | 54 MHz | |
| 13 | Read Configuration Register 1 | RDC1 35h | • | | | | | • | | | | | • | | | | | | | 1 | 54 MHz | |
| 14 | Read Configuration Register 2 | RDC2 3Fh | • | | | | | • | | | | | • | | | | | | | 1 | 54 MHz | |
| 15 | Read Configuration Register 3 | RDC3 44h | • | | | | | • | | | | | • | | | | | | | 1 | 54 MHz | |
| 16 | Read Configuration Register 4 | RDC4 45h | • | | | | | • | | | | | • | | | | | | | 1 | 54 MHz | |
| 17 | Read Configuration Register 1, 2, 3, 4 | RDCX 46h | • | | | | | • | | | | | • | | | | | | | 4 | 54 MHz | |
| 18 | Read Device ID | RDID 9Fh | • | | | | | • | | | | | • | | | | | | | 4 | 54 MHz | |
| 19 | Read Unique ID | RUID 4Ch | • | | | | | • | | | | | • | | | | | | | 8 | 54 MHz | |

| # | Instruction Name | Command (Opcode) | (1-0-0) | (1-0-1) | (1-1-1) | (1-1-2) | (1-2-2) | (2-0-0) | (2-0-2) | (2-2-2) | (1-1-4) | (1-4-4) | (4-0-0) | (4-0-4) | (4-4-4) | XIP | SDR | DDR | Latency Cycles | Data Bytes | Max. Frequency | Prerequisite |
|--|---|------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----|-----|-----|----------------|------------|----------------|--------------|
| 20 | Read Serial Number Register | RDSN C3h | | • | | | | | • | | | | | • | | | • | | | 8 | 54 MHz | |
| 21 | Read Augmented Array Protection Register | RDAP 14h | | • | | | | | • | | | | | • | | | • | | | 1 | 54 MHz | |
| 22 | Read Any Register - Address Based | RDAR 65h | | | • | | | | | • | | | | | • | | • | | • | 1 to 8 | 108 MHz | |
| Write Register Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 23 | Write Status Register | WRSR 01h | | • | | | | | • | | | | | • | | | • | | | 1 | 108 MHz | WREN |
| 24 | Write Configuration Registers 1, 2, 3, 4 | WRCX 87h | | • | | | | | • | | | | | • | | | • | | | 4 | 108 MHz | WREN |
| 25 | Write Serial Number Register | WRSN C2h | | • | | | | | • | | | | | • | | | • | | | 8 | 108 MHz | WREN |
| 26 | Write Augmented Array Protection Register | WRAP 1Ah | | • | | | | | • | | | | | • | | | • | | | 1 | 108 MHz | WREN |
| 27 | Write Any Register - Address Based | WRAR 71h | | | • | | | | | • | | | | | • | | • | | | 1 to 8 | 108 MHz | WREN |
| Read Memory Array Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 28 | Read Memory Array - SDR | READ 03h | | | • | | | | | | | | | | | | • | | | 1 to ∞ | 50 MHz | |
| 29 | Fast Read Memory Array - SDR | RDFT 0Bh | | | • | | | | | • | | | | • | • | • | • | | • | 1 to ∞ | 108 MHz | |
| 30 | Fast Read Memory Array - DDR | DRFR 0Dh | | | • | | | | | • | | | | • | • | | • | • | • | 1 to ∞ | 54 MHz | |
| 31 | Read Dual Output Memory Array - SDR | RDDO 3Bh | | | | • | | | | | | | | | • | • | | • | | 1 to ∞ | 108 MHz | |
| 32 | Read Quad Output Memory Array - SDR | RDQO 6Bh | | | | | | | | | • | | | | • | • | | • | | 1 to ∞ | 108 MHz | |
| 33 | Read Dual I/O Memory Read - SDR | RDDI BBh | | | | | • | | | | | | | | • | • | | • | | 1 to ∞ | 108 MHz | |
| 34 | Read Dual I/O Memory Read - DDR | DRDI BDh | | | | | • | | | | | | | | • | | • | • | | 1 to ∞ | 54 MHz | |
| 35 | Read Quad I/O Memory Read - SDR | RDQI EBh | | | | | | | | | | • | | | • | • | | • | | 1 to ∞ | 108 MHz | |
| 36 | Read Quad I/O Memory Read - DDR | DRQI EDh | | | | | | | | | | • | | | • | | • | • | | 1 to ∞ | 54 MHz | |
| Write Memory Array Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 37 | Write Memory Array - SDR | WRTE 02h | | | • | | | | | | | | | | | | • | | | 1 to ∞ | 108 MHz | WREN |
| 38 | Fast Write Memory Array - SDR | WRFT DAh | | | • | | | | | • | | | | • | • | • | • | | | 1 to ∞ | 108 MHz | WREN |
| 39 | Fast Write Memory Array - DDR | DRFW DEh | | | • | | | | | • | | | | • | • | | • | • | | 1 to ∞ | 54 MHz | WREN |

| # | Instruction Name | Command (Opcode) | (1-0-0) | (1-0-1) | (1-1-1) | (1-1-2) | (1-2-2) | (2-0-0) | (2-0-2) | (2-2-2) | (1-1-4) | (1-4-4) | (4-0-0) | (4-0-4) | (4-4-4) | XIP | SDR | DDR | Latency Cycles | Data Bytes | Max. Frequency | Prerequisite |
|---|-------------------------------------|------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----|-----|-----|----------------|------------|----------------|--------------|
| 40 | Write Dual Input Memory Array - SDR | WDUI A2h | | | | • | | | | | | | | | | • | • | | | 1 to ∞ | 108 MHz | WREN |
| 41 | Write Quad Input Memory Array - SDR | WQDI 32h | | | | | | | | | • | | | | | • | • | | | 1 to ∞ | 108 MHz | WREN |
| 42 | Write Quad Input Memory Array - DDR | DWQI 31h | | | | | | | | | • | | | | | • | | • | | 1 to ∞ | 54 MHz | WREN |
| 43 | Write Dual I/O Memory Array - SDR | WDIO A1h | | | | | • | | | | | | | | | • | • | | | 1 to ∞ | 108 MHz | WREN |
| 44 | Write Quad I/O Memory Array - SDR | WQIO D2h | | | | | | | | | | • | | | | • | • | | | 1 to ∞ | 108 MHz | WREN |
| 45 | Write Quad I/O Memory Array - DDR | DWQO D1h | | | | | | | | | | | • | | | • | | • | | 1 to ∞ | 54 MHz | WREN |
| Augmented Storage Array Instructions | | | | | | | | | | | | | | | | | | | | | | |
| 46 | Read Augmented Storage Array - SDR | RDAS 4Bh | | | • | | | | | | | | | | | | • | | • | 1 to 256 | 50 MHz | |
| 47 | Write Augmented Storage Array - SDR | WRAS 42h | | | • | | | | | | | | | | | | • | | | 1 to ∞ | 108 MHz | WREN |

Notes:

1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

2: XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.

3: Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.

4: The augmented storage array is 256-Bytes in size. The address bits ADDR[23:8] must be Logic '0' for this instruction.

5: Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

6: WREN prerequisite for array writing is configurable (Configuration Register 4 – CR4[1:0]).

7: For the Exit Deep Power Down command, the maximum frequency is 108MHz for 1-1-1 operation and 36MHz for 2-2-2 and 4-4-4 operations.

13. Instruction Description and Structures

All communication between a host and Mxxxx204 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from Mxxxx204. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- *Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic '1').*
- *CLK marks the transfer of each bit.*
- *Each instructions starts out with an 8-bit command. The command selects the type of operation Mxxxx204 must perform. The command is transferred on the rising edges of CLK.*
- *The command can be stand alone or followed by address to select a memory location or register. The address is always 24-bits wide.*
 - *SDR: The address is transferred on the rising edges of CLK.*
 - *DDR: The address is transferred on both edges of the CLK in DDR.*
- *The address bits are followed by data bits. For Write instructions:*
 - *SDR: Write data bits to Mxxxx204 are transferred on the rising edges of CLK.*
 - *DDR: Write data bits to Mxxxx204 are transferred on both edges of CLK.*
- *In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. Mxxxx204 offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array or the augmented storage array. These modes are set in Configuration Register 4.*
- *Similar to write instructions, the address bits are followed by data bits for read instructions:*
 - *SDR: Read data bits from Mxxxx204 are transferred on the falling edges of CLK.*
 - *DDR: Read data bits from Mxxxx204 are transferred on both edges of CLK. The start of read data transfer is always on the falling edge of the CLK.*
- *Mxxxx204 is a high performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of Mxxxx204.*
- *For Read and Write instructions, Mxxxx204 offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead. XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.*
- *For Read instructions, Mxxxx204 offers wrap mode. Wrap bursts are confined to address aligned 16/32/64/128/256 byte boundary. The read address can start anywhere within the wrap boundary. 16/32/64/128/256 wrap configuration is set in Configuration Register 3.*
- *The entire memory array can be read from or written to using a single read or write instruction. After the starting address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.*
- *All commands, address and data are shifted with the most significant bit first.*

Figure 8 to Figure 24 show the description of SDR instruction types supported.

Figure 8: Description of (1-0-0) Instruction Type

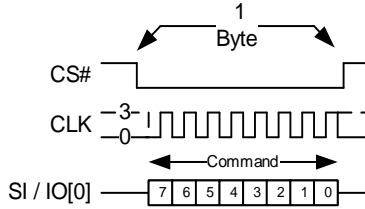


Figure 9: Description of (1-0-1) Instruction Type

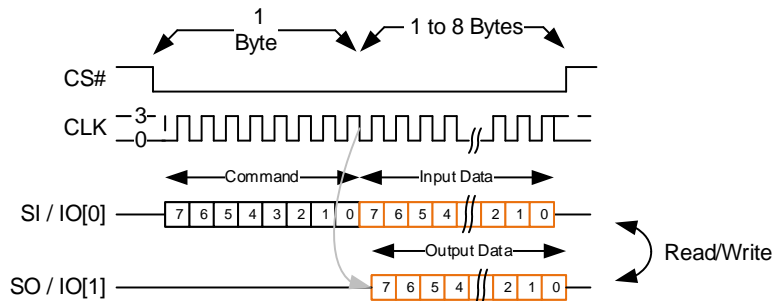


Figure 10: Description of (1-1-1) Instruction Type (Without XIP)

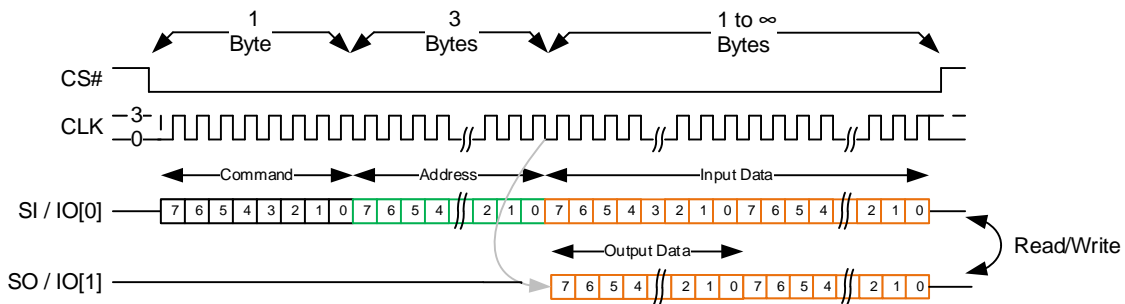


Figure 11: Description of (1-1-1) Augmented Storage Instruction Type

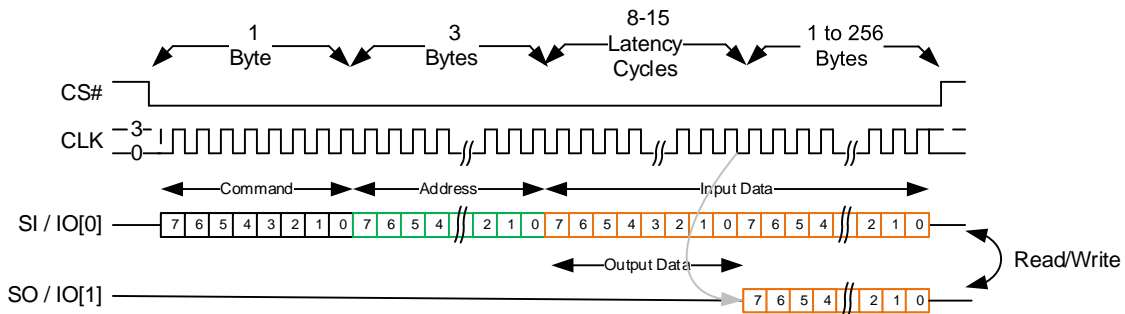


Figure 12: Description of (1-1-1) Instruction Type (With XIP)

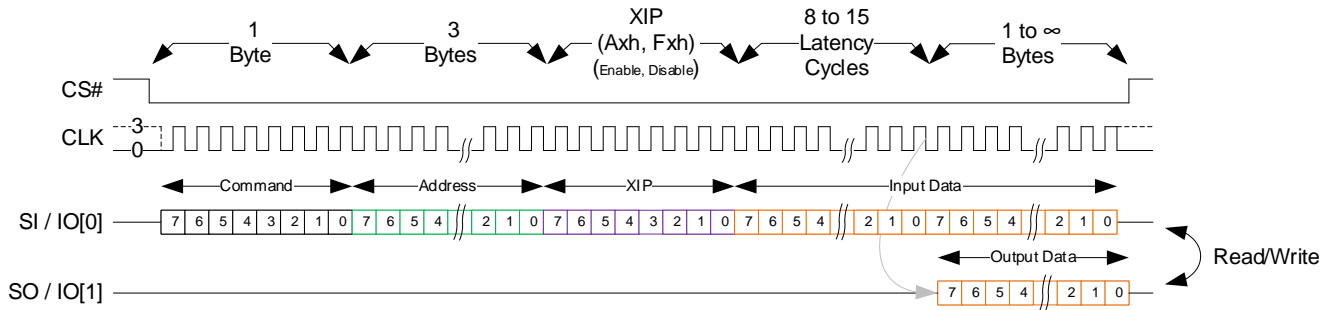


Figure 13: Description of (1-1-2) Instruction Type (With XIP)

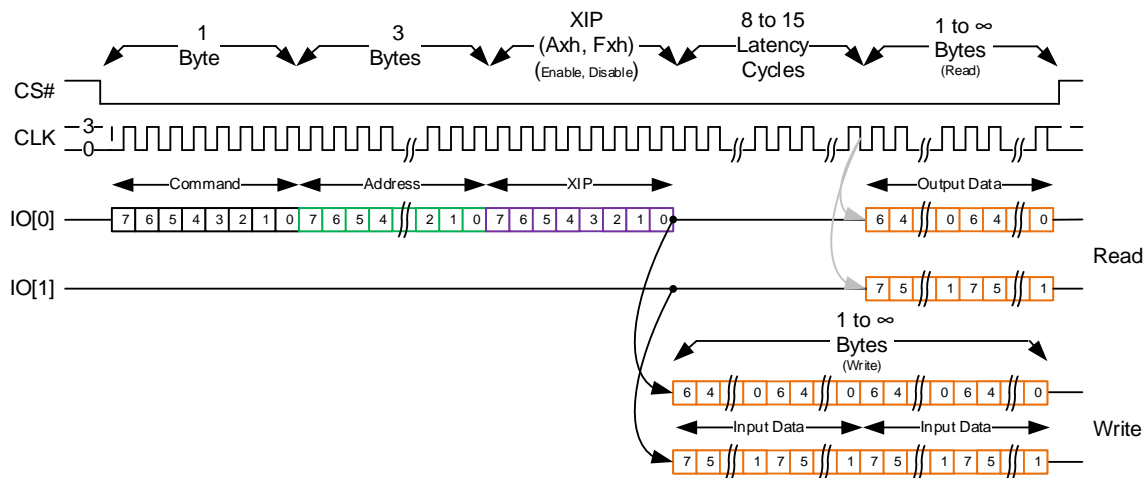


Figure 14: Description of (1-2-2) Instruction Type (With XIP)

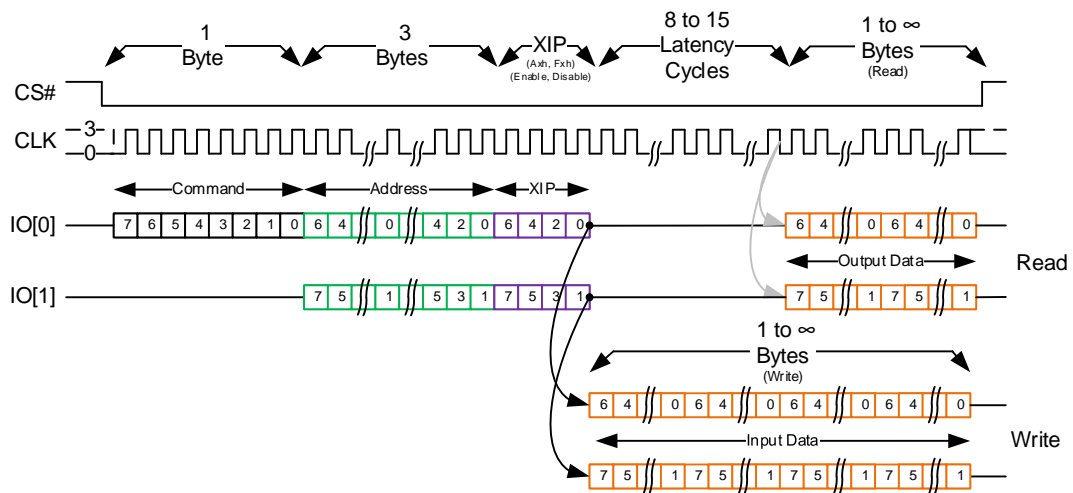


Figure 15: Description of (2-0-0) Instruction Type

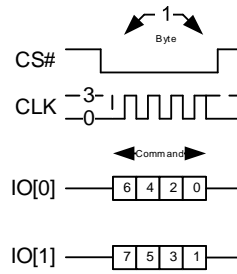


Figure 16: Description of (2-0-2) Instruction Type

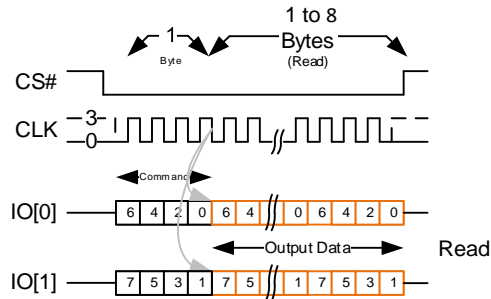


Figure 17: Description of (2-2-2) Any Register Instruction Type

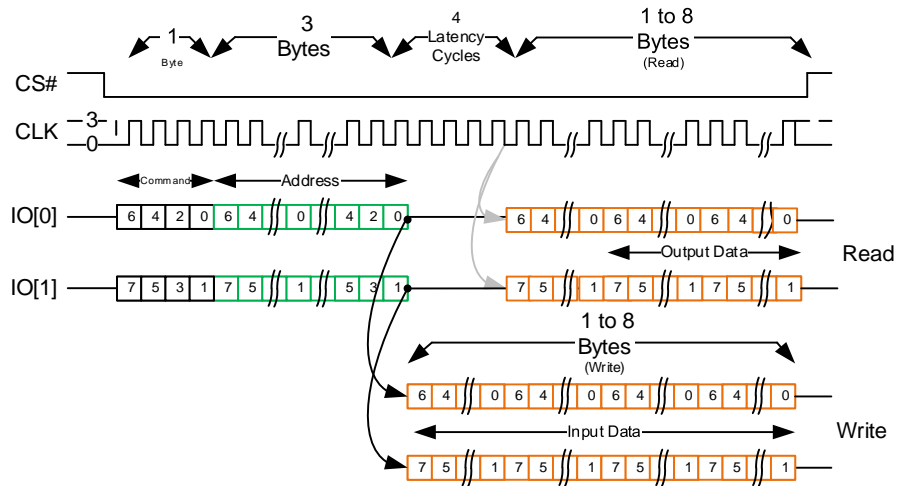


Figure 18: Description of (2-2-2) Instruction Type (With XIP)

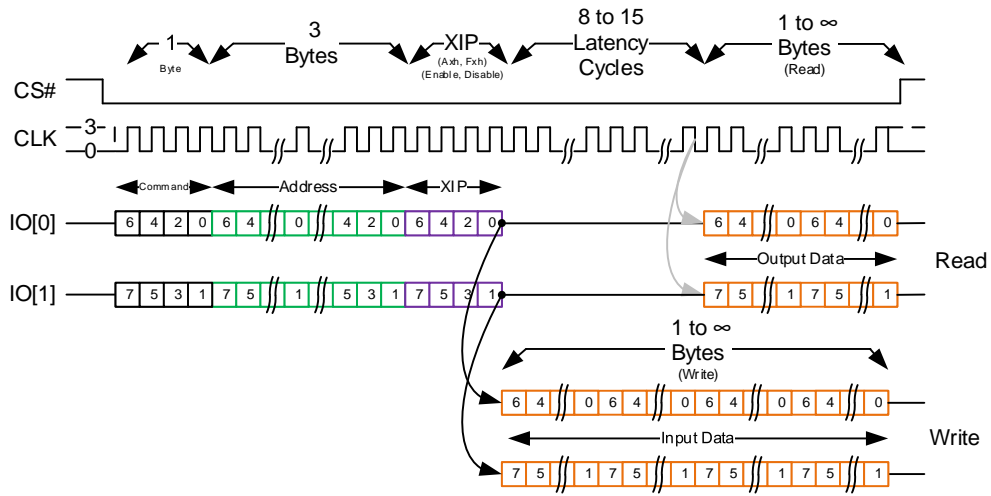


Figure 19: Description of (1-1-4) Instruction Type (With XIP)

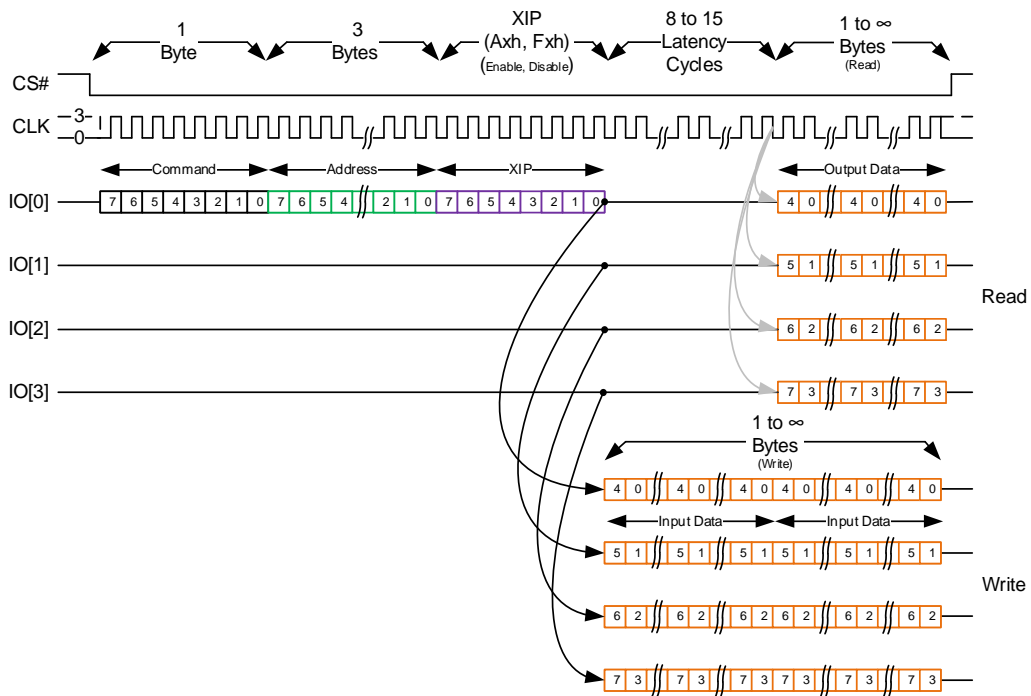


Figure 20: Description of (1-4-4) Instruction Type (With XIP)

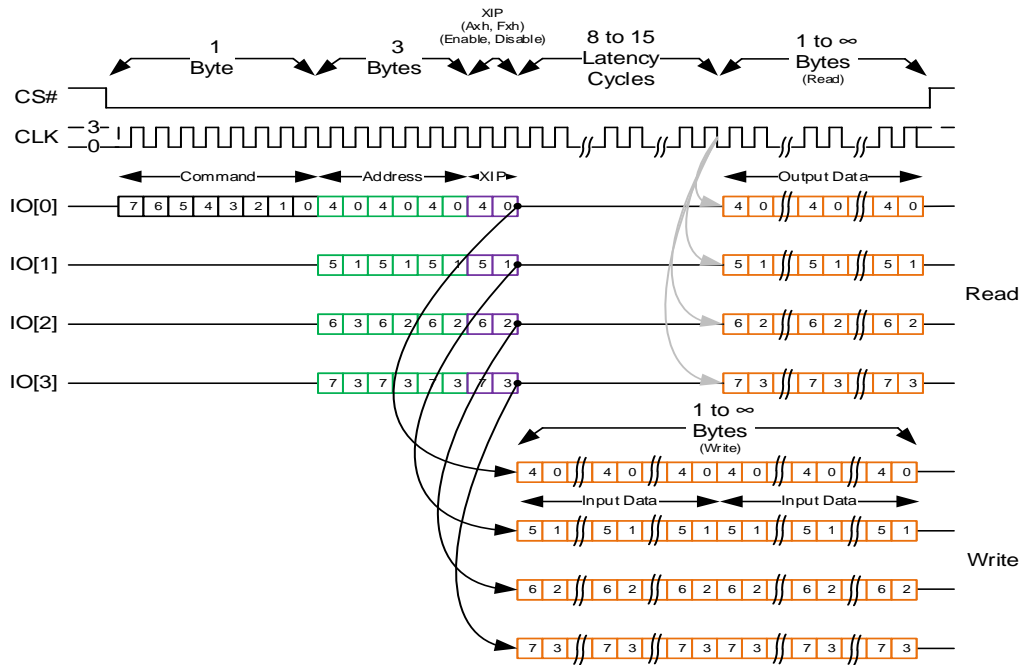


Figure 21: Description of (4-0-0) Instruction Type

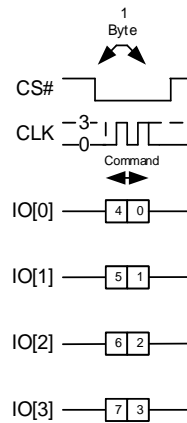


Figure 22: Description of (4-0-4) Instruction Type

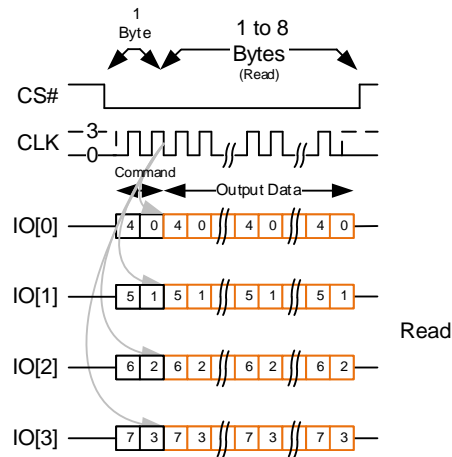


Figure 23: Description of (4-4-4) Any Register Instruction Type (Without XIP)

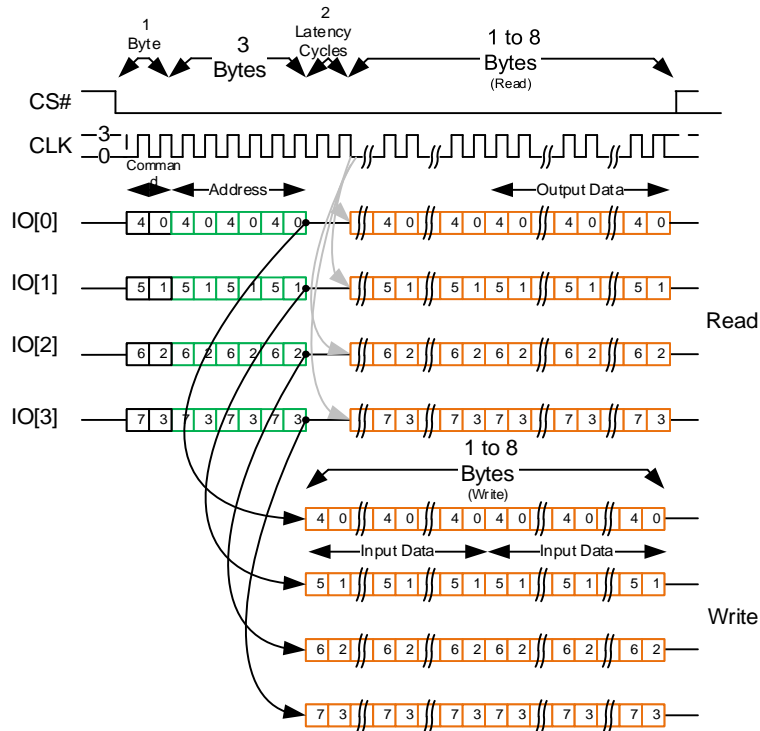


Figure 24: Description of (4-4-4) Instruction Type (With XIP)

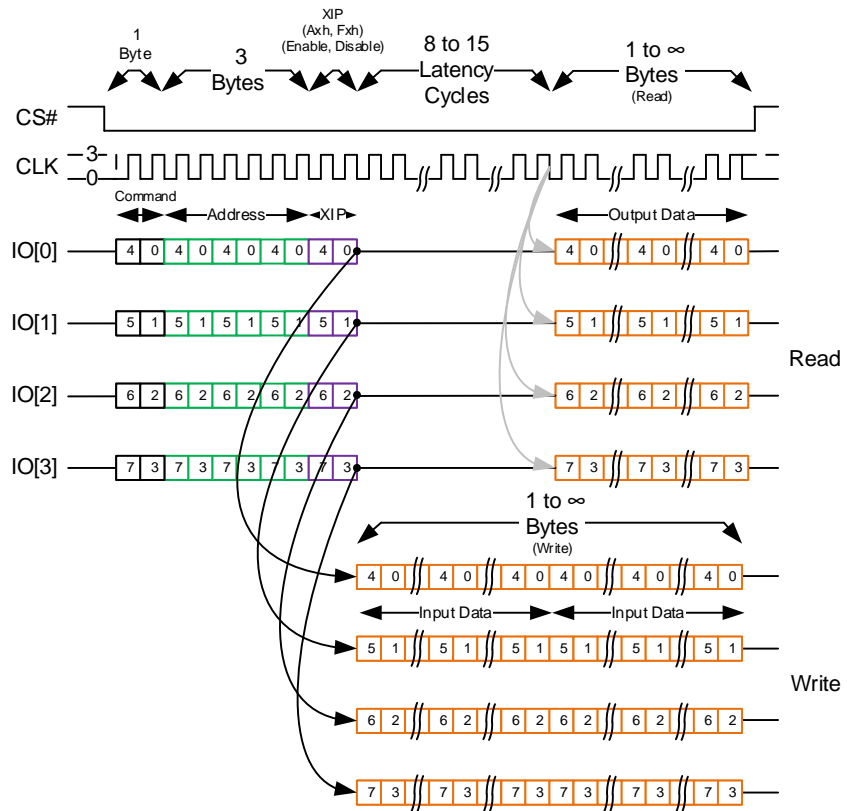


Figure 25 to Figure 29 show the description of DDR instruction types supported.

Figure 25: Description of (1-1-1) DDR Instruction Type (With XIP)

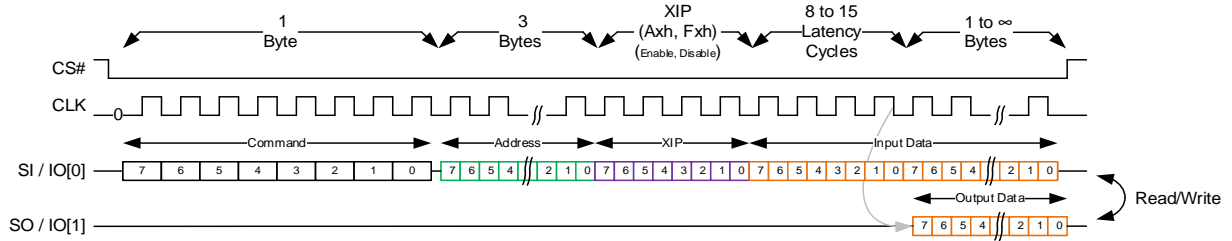


Figure 26: Description of (2-2-2) DDR Instruction Type (With XIP)

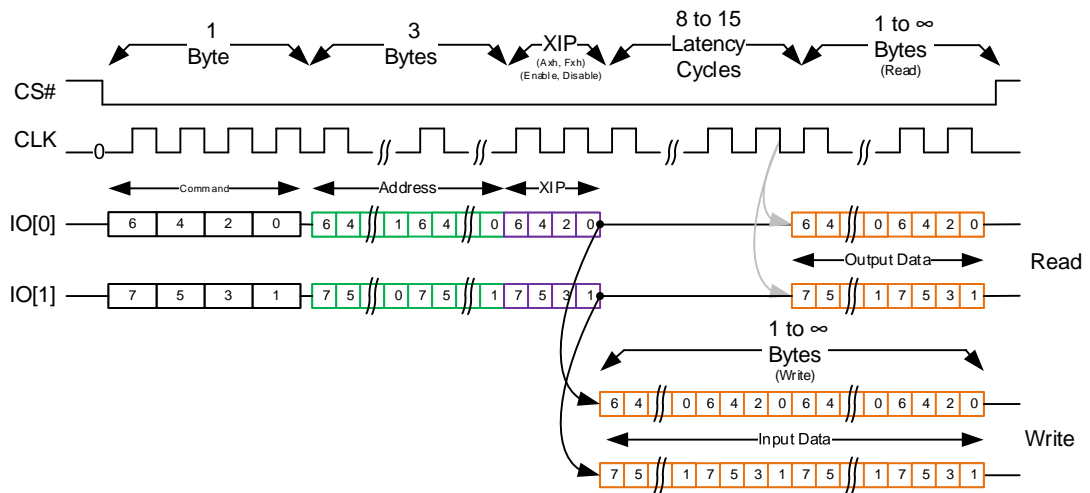


Figure 27: Description of (4-4-4) DDR Instruction Type (With XIP)

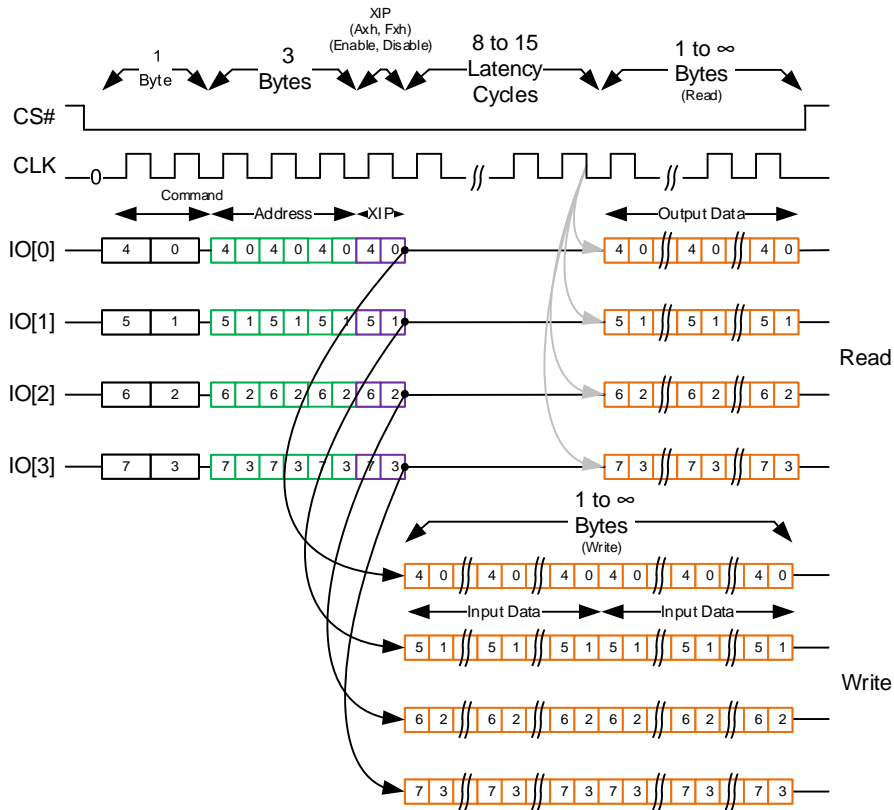


Figure 28: Description of (1-2-2) DDR Instruction Type (With XIP)

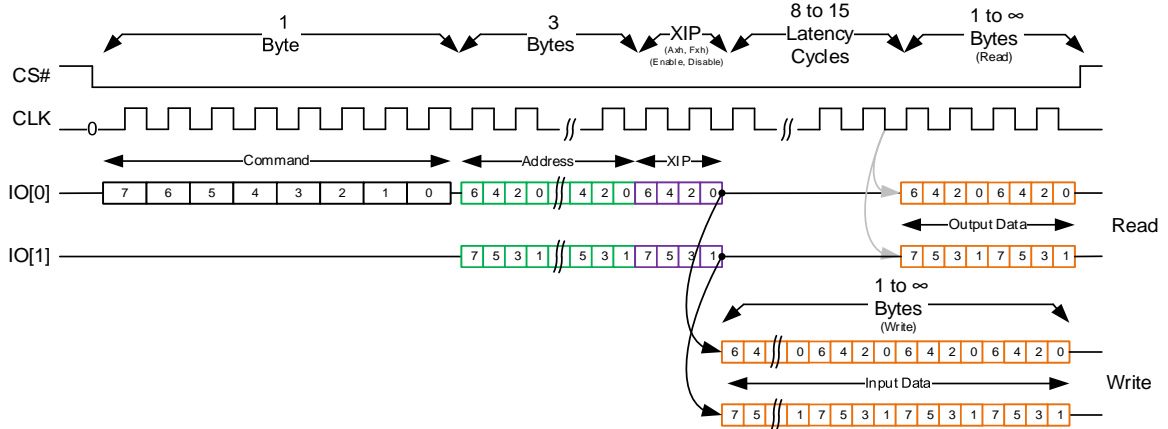
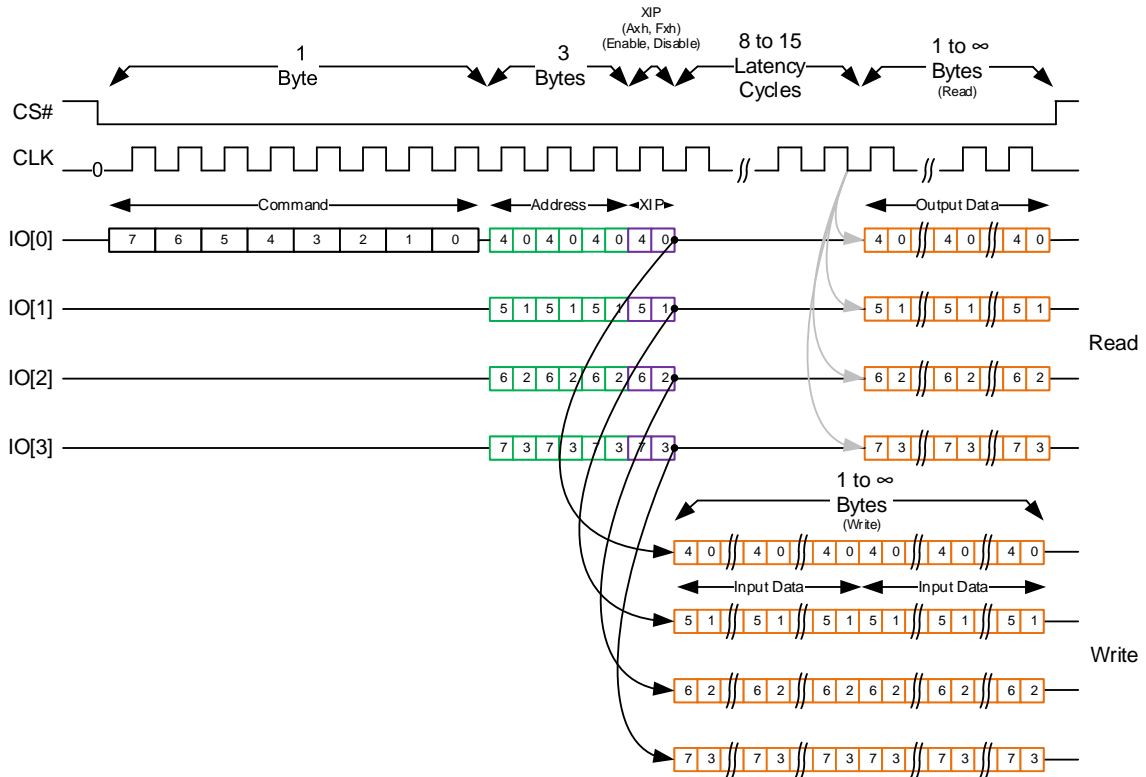


Figure 29: Description of (1-4-4) DDR Instruction Type (With XIP)



14. Electrical Specifications

Table 29: Recommended Operating Conditions

| Parameter / Condition | Minimum | Typical | Maximum | Units | |
|---------------------------------------|-----------------|---------|---------|-------|----|
| Operating Temperature | Industrial | -40.0 | - | 85.0 | °C |
| | Industrial Plus | -40.0 | - | 105.0 | °C |
| V _{CC} Supply Voltage (3.0V) | 3.0V | 2.7 | 3.0 | 3.6 | V |
| V _{CC} Supply Voltage (1.8V) | 1.8V | 1.71 | 1.8 | 2.0 | V |
| V _{SS} Supply Voltage | | 0.0 | 0.0 | 0.0 | V |

Table 30: Pin Capacitance

| Parameter | Test Conditions | Symbol | Maximum | Units |
|------------------------|--|--------------------|---------|-------|
| Input Pin Capacitance | TEMP = 25°C; f = 1 MHz; V _{IN} = 3.0V | C _{IN} | 5.0 | pF |
| Output Pin Capacitance | TEMP = 25°C; f = 1 MHz; V _{IN} = 3.0V | C _{INOUT} | 6.0 | pF |

Table 31: Endurance & Retention

| Parameter | Symbol | Test Conditions | Minimum | Units |
|-----------------|--------|-----------------|------------------|--------|
| Write Endurance | END | - | 10 ¹⁴ | cycles |
| Data Retention | RET | 105°C | 10 | years |
| | | 85°C | 1,000 | |
| | | 75°C | 10,000 | |
| | | 65°C | 1,000,000 | |

Table 32: 3.0V DC Characteristics

| Parameter | Symbol | Test Conditions | 3.0V Device (2.7V-3.6V) | | | Units | |
|---------------------------|---------------------|---|-------------------------|---------|----------------------|-------|----|
| | | | Minimum | Typical | Maximum | | |
| Read Current (1-1-1) SDR | I _{READ1} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 8 | 9 | mA | |
| Read Current (2-2-2) SDR | I _{READ2} | | - | 9 | 10 | mA | |
| Read Current (4-4-4) SDR | I _{READ3} | | - | 10 | 12 | mA | |
| Read Current (1-1-1) SDR | I _{READ4} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=108MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 13 | 15 | mA | |
| Read Current (2-2-2) SDR | I _{READ5} | | - | 15 | 17 | mA | |
| Read Current (4-4-4) SDR | I _{READ6} | | - | 19 | 21 | mA | |
| Read Current (1-1-1) DDR | I _{READ7} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 13 | 18 | mA | |
| Read Current (2-2-2) DDR | I _{READ8} | | - | 20 | 24 | mA | |
| Read Current (4-4-4) DDR | I _{READ9} | | - | 23 | 28 | mA | |
| Write Current (1-1-1) SDR | I _{WRITE1} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 14 | 16 | mA | |
| Write Current (2-2-2) SDR | I _{WRITE2} | | - | 17 | 20 | mA | |
| Write Current (4-4-4) SDR | I _{WRITE3} | | - | 22 | 25 | mA | |
| Write Current (1-1-1) SDR | I _{WRITE4} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=108MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 22 | 28 | mA | |
| Write Current (2-2-2) SDR | I _{WRITE5} | | - | 25 | 32 | mA | |
| Write Current (4-4-4) SDR | I _{WRITE6} | | - | 38 | 45 | mA | |
| Write Current (1-1-1) DDR | I _{WRITE7} | V _{CC} = 3.6V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 15 | 25 | mA | |
| Write Current (2-2-2) DDR | I _{WRITE8} | | - | 20 | 30 | mA | |
| Write Current (4-4-4) DDR | I _{WRITE9} | | - | 30 | 45 | mA | |
| Standby Current | I _{SB} | V _{CC} = 3.6V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | Ta = 25°C | - | 160 | - | μA |
| | | | Ta = 85°C | - | - | 400 | μA |
| | | | Ta = 105°C | - | - | 600 | μA |
| Deep Power Down Current | I _{DPD} | V _{CC} = 3.6V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | - | 5 | 25 | μA | |
| Hibernate Current | I _{HBN} | V _{CC} = 3.6V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | - | 0.1 | - | μA | |
| Input Leakage Current | I _{LI} | V _{IN} =0 to V _{CC} (max) | - | - | ±1.0 | μA | |
| Output Leakage Current | I _{LO} | V _{OUT} =0 to V _{CC} (max) | - | - | ±1.0 | μA | |
| Input High Voltage | V _{IH} | | 0.7xV _{CC} | - | V _{CC} +0.3 | V | |
| Input Low Voltage | V _{IL} | | -0.3 | - | 0.3xV _{CC} | V | |
| Output High Voltage Level | V _{OH} | I _{OH} = -100μA | V _{CC} -0.2 | - | - | V | |
| | | I _{OH} = -1mA | 2.4 | - | - | V | |
| Output Low Voltage Level | V _{OL} | I _{OL} = 150μA | - | - | 0.2 | V | |
| | | I _{OL} = 2mA | - | - | 0.4 | V | |

Table 33: 1.8V DC Characteristics

| Parameter | Symbol | Test Conditions | 1.8V Device (1.71V-2.0V) | | | Units | |
|---------------------------|---------------------|---|--------------------------|---------|----------------------|-------|----|
| | | | Minimum | Typical | Maximum | | |
| Read Current (1-1-1) SDR | I _{READ1} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 5 | 8 | mA | |
| Read Current (2-2-2) SDR | I _{READ2} | | - | 6 | 9 | mA | |
| Read Current (4-4-4) SDR | I _{READ3} | | - | 7 | 11 | mA | |
| Read Current (1-1-1) SDR | I _{READ4} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=108MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 8 | 12 | mA | |
| Read Current (2-2-2) SDR | I _{READ5} | | - | 9 | 13 | mA | |
| Read Current (4-4-4) SDR | I _{READ6} | | - | 12 | 17 | mA | |
| Read Current (1-1-1) DDR | I _{READ7} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 11 | 14 | mA | |
| Read Current (2-2-2) DDR | I _{READ8} | | - | 17 | 20 | mA | |
| Read Current (4-4-4) DDR | I _{READ9} | | - | 21 | 25 | mA | |
| Write Current (1-1-1) SDR | I _{WRITE1} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 13 | 15 | mA | |
| Write Current (2-2-2) SDR | I _{WRITE2} | | - | 16 | 19 | mA | |
| Write Current (4-4-4) SDR | I _{WRITE3} | | - | 20 | 23 | mA | |
| Write Current (1-1-1) SDR | I _{WRITE4} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=108MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 20 | 26 | mA | |
| Write Current (2-2-2) SDR | I _{WRITE5} | | - | 23 | 30 | mA | |
| Write Current (4-4-4) SDR | I _{WRITE6} | | - | 36 | 43 | mA | |
| Write Current (1-1-1) DDR | I _{WRITE7} | V _{CC} = 2.0V, I _{OUT} =0mA, CLK=54MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH} | - | 13 | 23 | mA | |
| Write Current (2-2-2) DDR | I _{WRITE8} | | - | 19 | 28 | mA | |
| Write Current (4-4-4) DDR | I _{WRITE9} | | - | 28 | 43 | mA | |
| Standby Current | I _{SB} | V _{CC} = 2.0V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | Ta = 25°C | - | 140 | - | μA |
| | | | Ta = 85°C | - | - | 350 | μA |
| | | | Ta=105°C | - | - | 500 | μA |
| Deep Power Down Current | I _{DPD} | V _{CC} = 2.0V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | - | 4 | 20 | μA | |
| Hibernate Current | I _{HBN} | V _{CC} = 2.0V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} | - | 0.1 | - | μA | |
| Input Leakage Current | I _{LI} | V _{IN} =0 to V _{CC} (max) | - | - | ±1.0 | μA | |
| WP# Leakage Current | I _{WP#LI} | V _{IN} =0 to V _{CC} (max) | -100.0 | - | +1.0 | μA | |
| Output Leakage Current | I _{LO} | V _{OUT} =0 to V _{CC} (max) | - | - | ±1.0 | μA | |
| Input High Voltage | V _{IH} | | 0.7xV _{CC} | - | V _{CC} +0.3 | V | |
| Input Low Voltage | V _{IL} | | -0.3 | - | 0.3xV _{CC} | V | |
| Output High Voltage Level | V _{OH} | I _{OH} = -100μA | V _{CC} -0.2 | - | - | V | |
| | | I _{OH} = -1mA | 1.5 | - | - | V | |
| Output Low Voltage Level | V _{OL} | I _{OL} = 150μA | - | - | 0.2 | V | |
| | | I _{OL} = 2mA | - | - | 0.4 | V | |

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 34: Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Units |
|---|------------|-----------|-------|
| Magnetic Field During Write | --- | 24000 | A/m |
| Magnetic Field During Read | --- | 24000 | A/m |
| Junction Temperature | --- | 125 | °C |
| Storage Temperature | -55 to 150 | | °C |
| Supply Voltage Vcc relative to Vss | -0.5 | 4.0 | V |
| Voltage on any pin | -0.5 | Vcc + 0.4 | V |
| DC output current Iout | ± 20 | | mA |
| ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017 | ≥ 2000 V | | V |
| ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018 | ≥ 500 V | | V |
| Latch-Up (I-test) JESD78 | ≥ 100 mA | | mA |
| Latch-Up (Vsupply over-voltage test) JESD78 | Passed | | --- |

Table 35: AC Test Conditions

| Parameter | Value |
|--|-------------|
| Input pulse levels | 0.0V to Vcc |
| Input rise and fall times | 3.0ns |
| Input and output measurement timing levels | Vcc/2 |
| Output Load | CL = 30.0pF |

14.1 CS# Operation & Timing

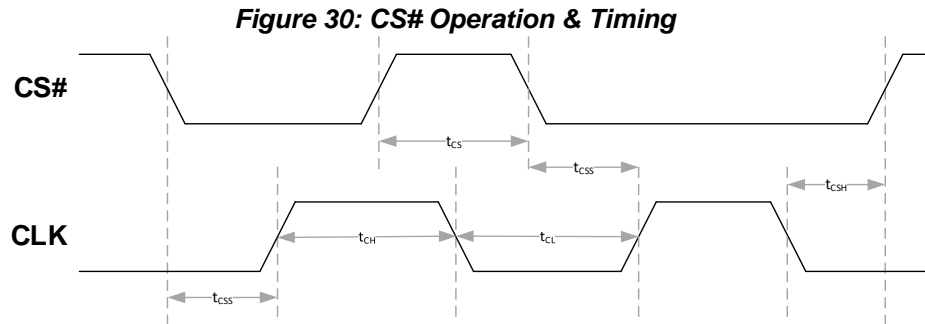


Table 36: CS# Operation

| Parameter | Symbol | Minimum | Maximum | Units |
|--|-----------|----------------------|-----------|---------|
| Clock Frequency | f_{CLK} | 1 | 108 (SDR) | MHz |
| Clock Low Time | t_{CL} | $0.45 * 1 / f_{CLK}$ | - | ns |
| Clock High Time | t_{CH} | $0.45 * 1 / f_{CLK}$ | - | ns |
| Chip Deselect Time after Read Cycle | t_{CS1} | 20 | - | ns |
| Chip Deselect Time after Register Write Cycle¹ | t_{CS2} | 5 | - | μ s |
| Chip Deselect Time after Write Cycle (SPI) | t_{CS3} | 280 | - | ns |
| Chip Deselect Time after Write Cycle (DPI) | t_{CS4} | 350 | - | ns |
| Chip Deselect Time after Write Cycle (QPI) | t_{CS5} | 490 ² | - | ns |
| CS# Setup Time (w.r.t CLK) | t_{CSS} | 5 | - | ns |
| CS# Hold Time (w.r.t CLK) | t_{CSH} | 4 | - | ns |

Notes:

Power supplies must be stable

1:SDR operation only

2:For single byte operations, t_{CS5} is 280ns

Command, Address, XIP and Data Input Operation & Timing

Figure 31: SDR Command, Address and Data Input Operation & Timing

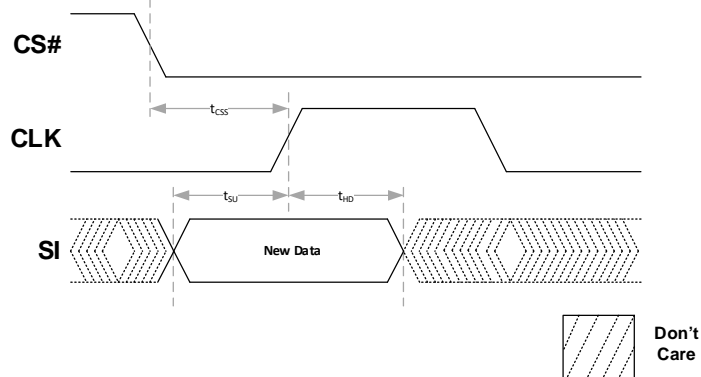


Table 37: SDR Command, Address, XIP, and Data Input Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|-----------------------------|----------|---------|---------|-------|
| Data Setup Time (w.r.t CLK) | t_{SU} | 2.0 | - | ns |
| Data Hold Time (w.r.t CLK) | t_{HD} | 3.0 | - | ns |

Notes:

Power supplies must be stable

Figure 32: DDR Command, Address and Data Input Operation & Timing

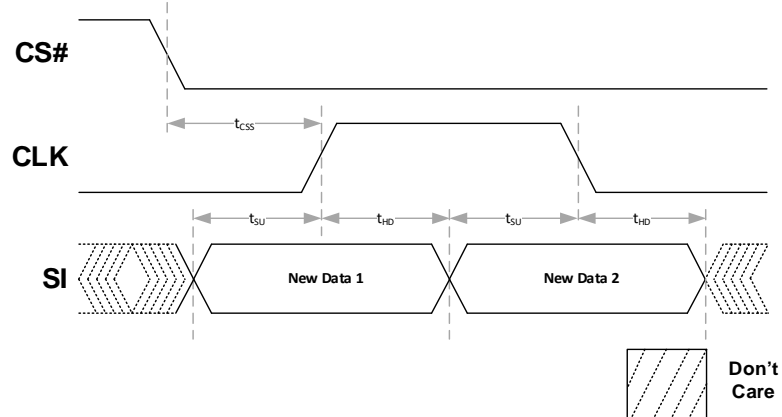


Table 38: DDR Command, Address, XIP, and Data Input Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|-----------------------------|----------|---------|---------|-------|
| Data Setup Time (w.r.t CLK) | t_{SU} | 4.0 | - | ns |
| Data Hold Time (w.r.t CLK) | t_{HD} | 4.0 | - | ns |

Notes:

Power supplies must be stable

14.2 Data Output Operation & Timing

Figure 33: SDR Data Output Operation & Timing

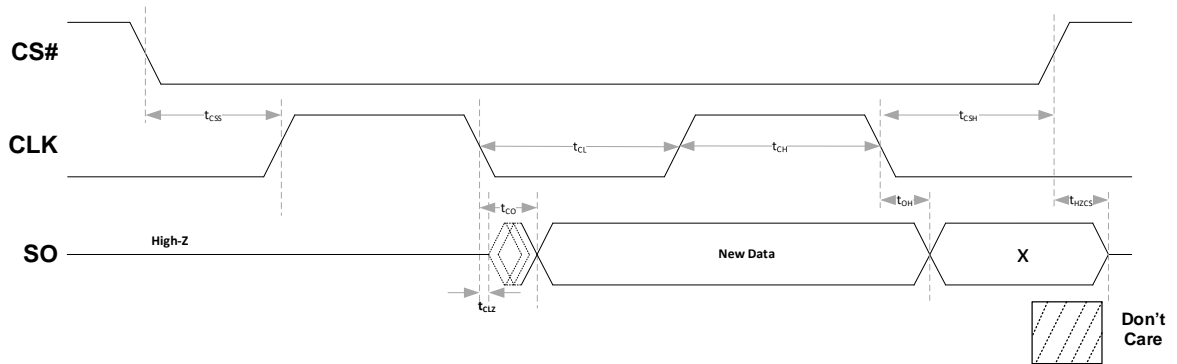


Table 39: SDR Data Output Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|----------------------------------|------------|---------|---------|-------|
| CLK Low to Output Low Z (Active) | t_{CLZ} | 0 | - | ns |
| Output Valid (w.r.t CLK) | t_{CO} | - | 7.0 | ns |
| Output Hold Time (w.r.t CLK) | t_{OH} | 1.0 | - | ns |
| Output Disable Time (w.r.t CS#) | t_{HZCS} | - | 7.0 | ns |

Notes:

Power supplies must be stable

Figure 34: DDR Data Output Operation & Timing

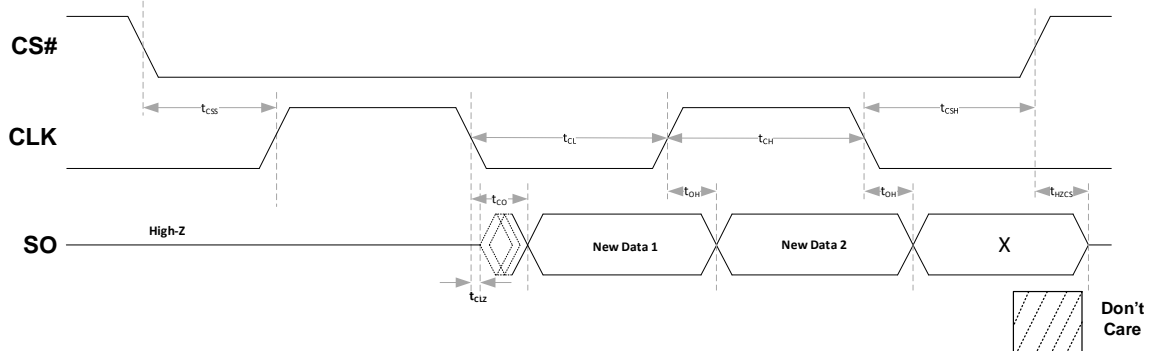


Table 40: DDR Data Output Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|----------------------------------|------------|---------|---------|-------|
| CLK Low to Output Low Z (Active) | t_{CLZ} | 0 | - | ns |
| Output Valid (w.r.t CLK) | t_{CO} | - | 7.0 | ns |
| Output Hold Time (w.r.t CLK) | t_{OH} | 1.0 | - | ns |
| Output Disable Time (w.r.t CS#) | t_{HZCS} | - | 6.0 | ns |

Notes:

Power supplies must be stable

14.3 WP# Operation & Timing

Figure 35: WP# Operation & Timing

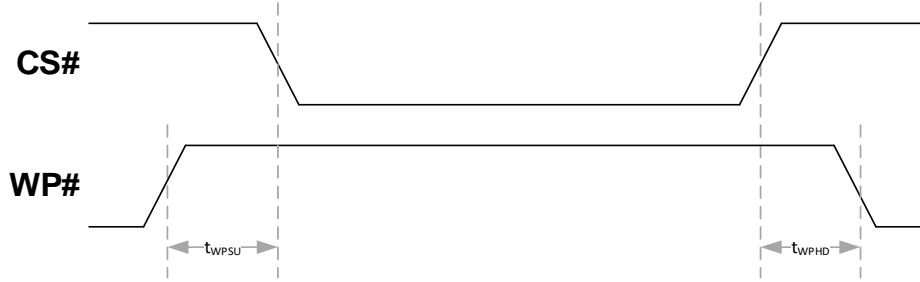


Table 41: WP# Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|----------------------------|------------|---------|---------|-------|
| WP# Setup Time (w.r.t CS#) | t_{WPSU} | 20 | - | ns |
| WP# Hold Time (w.r.t CS#) | t_{WPHD} | 20 | - | ns |

Notes:

Power supplies must be stable

JEDEC Reset Operation & Timing

Figure 36: JEDEC Reset Operation & Timing

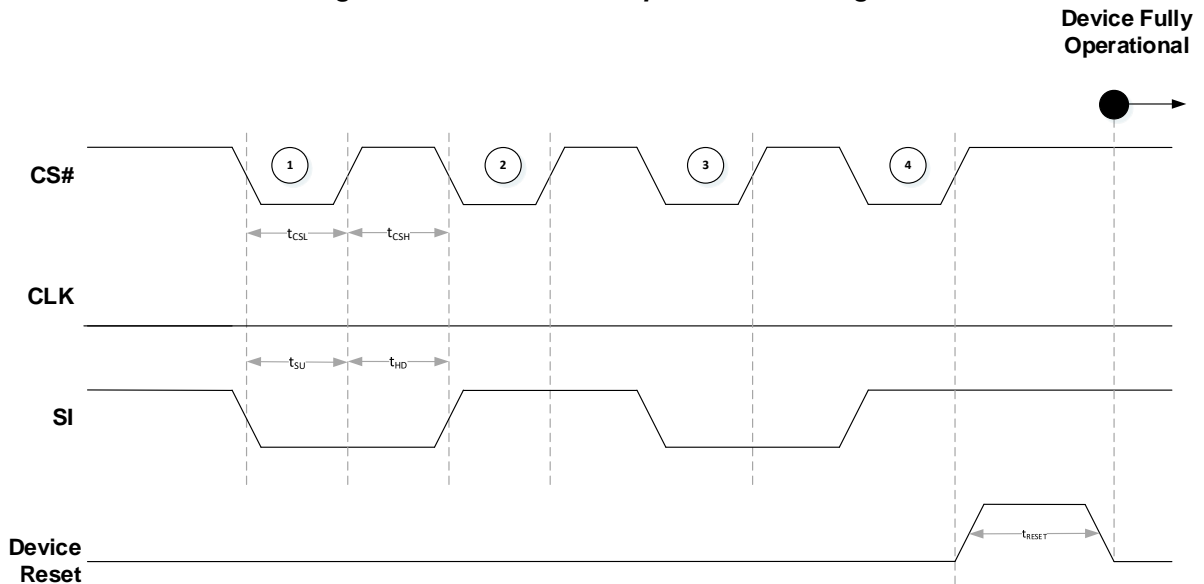


Table 42: JEDEC Reset Operation & Timing

| Parameter | Symbol | Minimum | Maximum | Units |
|-----------------------------|-------------|---------|---------|---------|
| CS# Low Time | t_{CL} | 1.0 | - | μ s |
| CS# High Time | t_{CH} | 1.0 | - | μ s |
| SI Setup Time (w.r.t CS#) | t_{SU} | 5.0 | - | ns |
| SI Hold Time (w.r.t CS#) | t_{HD} | 5.0 | - | ns |
| JEDEC Hardware Reset | t_{RESET} | - | 450.0 | μ s |
| Software Reset ¹ | t_{SRST} | - | 50.0 | μ s |

Notes:

Power supplies must be stable

1: Software Reset timing is for Instruction based Reset (SRST)

Enter Deep Power Down Command (EDP – B9h)

The command sequences are shown below. Executing the Enter Deep Power down (EDP) command is the only way to put the device in the deep power down mode. The device consumption drops to I_{DP} .

The deep power down mode subsequently reduces the standby current from I_{SB} to I_{DP} . No other command must be issued while the device is in deep power down mode.

To enter the deep power down mode, CS# is driven low, following the enter deep power down (EDPD) command, CS# must be driven high after the eighth bit of the command code has been latched in or the EDP command will not be executed. After CS# is driven high, it requires a delay of t_{EDPD} (Table 6 and 7) before the supply current is reduced to I_{DP} and the Deep Power Down mode is entered. The command can be issued in SPI, DPI or QPI modes.

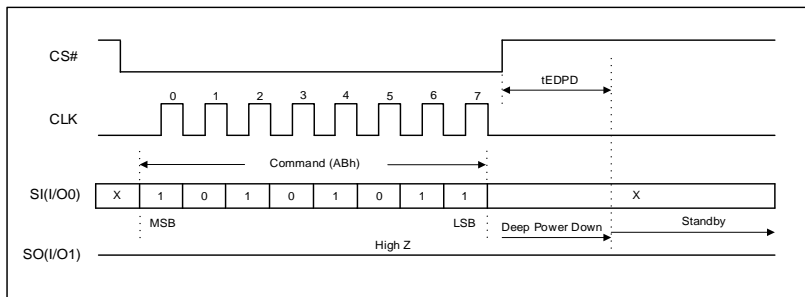


Figure 37: Enter Deep Power Down in SPI Command Sequence

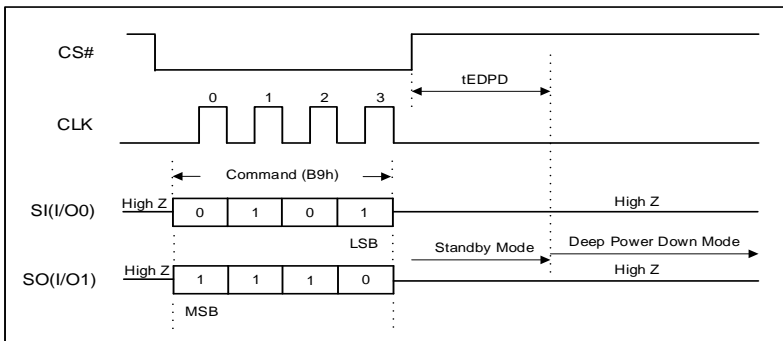


Figure 38: Enter Deep Power Down in DPI Command Sequence

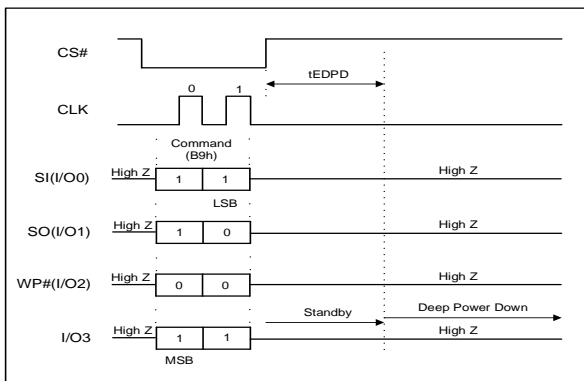


Figure 39: Enter Deep Power Down in QPI Command Sequence

Exit Deep Power Down Command (EXDPD - ABh)

The command sequences are shown below. There are two ways to exit deep power down mode:

1. Toggling CS# with a CS# pulse width of t_{CSDPD} while CLK and I/Os are Don't Care. During waking up from deep power down, I/Os remain to be in high Z.
2. Driving CS# low follows with the Exit Deep Power Down (EXDPD) command. CS# must be driven high after the eight bit of the command code has been latched in or the EXDPD command will not executed.

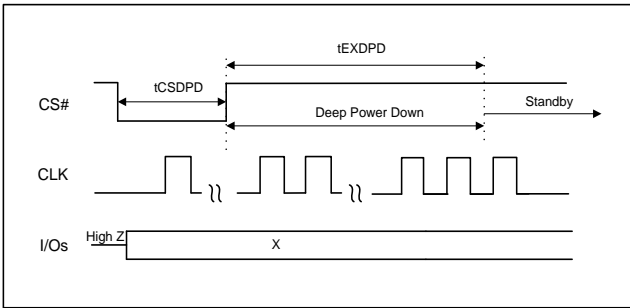


Figure 41: Exit Deep Power Down by Toggling CS#

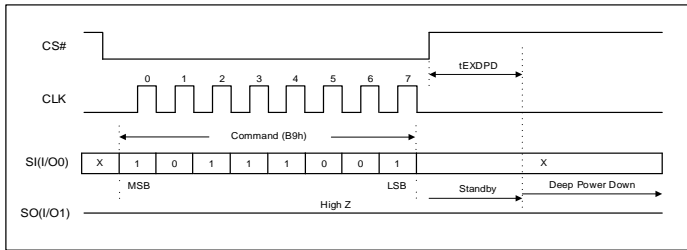


Figure 40: Exit Deep Power Down in SPI Command Sequence

It requires a delay of t_{EXDPD} (Table 6 and 7) before the device can fully exit the deep power down mode and enter standby mode. The command can be issued in SPI, DPI, and QPI mode. Status of all non-volatile bits in registers remains unchanged when the SPnVSRAM enters or exits the deep power down mode.

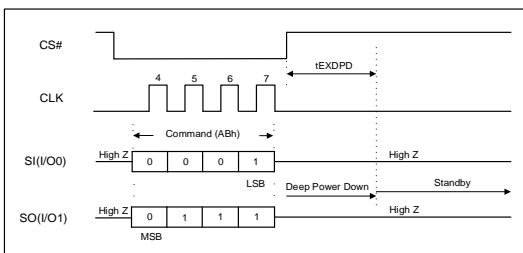


Figure 42: Exit Deep Power Down in DPI Command Sequence

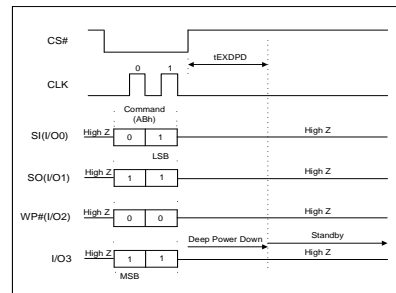


Figure 43: Exit Deep Power Down in QPI Command Sequence

Enter Hibernate Command (EHBN – BAh)

The command sequences are shown below. Executing the Enter Hibernate command is the only way to put the device in the hibernate mode. The device drops down to the lowest power consumption mode: I_{HBN}. When in hibernate mode, the CLK and SI pins are ignored and SO will be high-Z.

To enter the hibernate mode, CS# is driven low, following the Enter Hibernate (EHBN) command. After CS# is driven high, it requires a delay of t_{ENTHIB} time (Table 6 and 7) before the supply current is reduced to I_{HBN} and the hibernate mode is entered.

Toggleing CS# (low to high) will return the SPnvSRAM to standby mode. The command can be issued in SPI, DPI, and QPI modes.

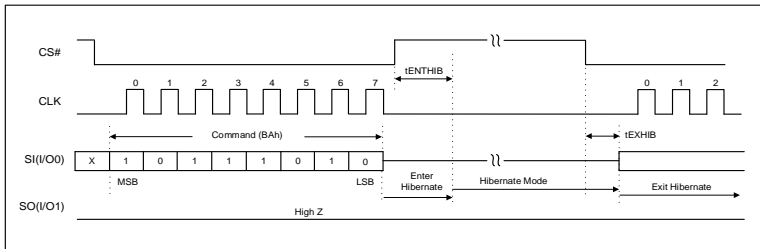


Figure 44: Enter Hibernate in SPI Command Sequence

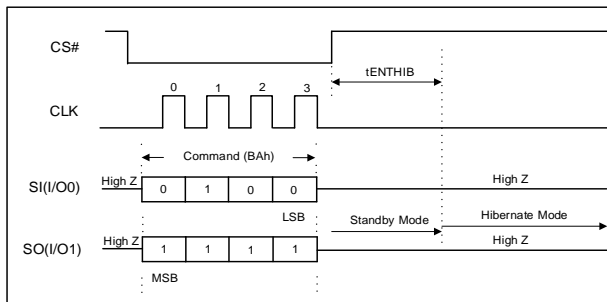


Figure 45: Enter Hibernate in DPI Command Sequence

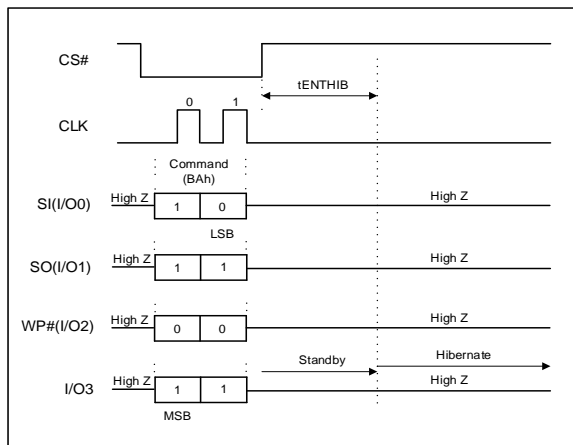


Figure 46: Enter Hibernate in QPI Command Sequence

15. Thermal Resistance

Table 43: Thermal Resistance

| Parameter | Description | Test Conditions | 8-pad DFN (WSON) | 8-pin SOIC | Unit |
|---------------|--|---|------------------|------------|------|
| θ_{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 43.67 | 53.59 | °C/W |
| θ_{JC} | Thermal resistance (junction to case) | | 18.54 | 4.29 | |

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

16. Revision History

| Revision Date | Description of Change |
|---------------|---|
| Apr.16.20 | Initial release. |
| Feb.25.21 | Update to the Endurance and Electrical parameters. Thermal Resistance table added to the datasheet. Revise various tables including Tables 22, 31, 32, 33, 34, 36 and 43. |
| Mar.18.22 | Added REACH compliant to features and updated Absolute Maximum Ratings table. |
| Feb.21.23 | Removed Performance table Updated Signal Description table Updated Power-Up Behavior diagram Updated Power-Down/Power-Up description Updated Power-Down and Brown-out Behavior diagram Added V _{CC} Ramp Up Time (max) Added VCC-RST parameters Updated SDR and DDR Data Output Operation & Timing diagrams |