



ProASIC[®] 3 Flash Family FPGAs with Optimal Soft ARM Support

INTRODUCTION

ProASIC[®] 3, the third-generation family of Microchip's flash FPGAs, offers performance, density, and features beyond those of the ProASIC^{PLUS}[®] family. Nonvolatile flash technology gives ProASIC 3 devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC 3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC 3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated Phase-Locked Loop (PLL). The A3P030 devices have no PLL or RAM support. ProASIC 3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

ProASIC 3 devices support the ARM Cortex-M1 processor. The ARM-enabled devices have Microchip ordering numbers that begin with M1A3P (Cortex-M1) and do not support AES decryption.

FEATURES AND BENEFITS

High Capacity

- 15K to 1M System Gates
- Up to 144 Kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance

- 350 MHz System Performance
- 3.3V, 66 MHz 64-Bit PCI

Note: A3P030 devices do not support this feature.

In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except ARM[®]-enabled ProASIC 3 devices) via JTAG (IEEE[®] 1532-compliant)
- FlashLock[®] to Secure FPGA Contents

Low Power

- Core Voltage for Low Power
- Support for 1.5V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (A3P250 and above)
- 1.5V, 1.8V, 2.5V, and 3.3V Mixed-Voltage Operation
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7V to 3.6V
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3V/2.5V/1.8V/1.5V, 3.3V PCI/3.3V PCI-X, and LVCMOS 2.5V/5.0V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (A3P250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os
- Supported only by A3P030 devices.
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC 3 Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

Embedded Memory

- 1 Kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)
- True Dual-Port SRAM (except ×18)

ARM Processor Support in ProASIC 3 FPGAs

- M1 ProASIC 3 Devices—ARM®Cortex®-M1 Soft Processor Available with or without Debug

TABLE 1 • ARM PROCESSOR SUPPORT IN PROASIC 3 FPGAS

| ProASIC 3 Devices | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--------------------------------|--------|--------|---------|----------|----------|----------|-----------|
| Cortex-M1 Devices ¹ | | | | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| System Gates | 30,000 | 60,000 | 125,000 | 250,000 | 400,000 | 600,000 | 1,000,000 |
| Typical Equivalent Macrocells | 256 | 512 | 1,024 | 2,048 | — | — | — |
| VersaTiles (D-flip-flops) | 768 | 1,536 | 3,072 | 6,144 | 9,216 | 13,824 | 24,576 |
| RAM Kbits (1,024 bits) | — | 18 | 36 | 36 | 54 | 108 | 144 |
| 4,608-Bit Blocks | — | 4 | 8 | 8 | 12 | 24 | 32 |

Note 1: Refer to the [Cortex-M1](#) product brief for more information.

2: AES is not available for Cortex-M1 ProASIC 3 devices.

3: Six chip (main) and three quadrant global networks are available for A3P060 and above.

4: The M1A3P250 device does not support FG256 package.

5: For higher densities and support of additional features, refer to the [ProASIC 3E Flash Family FPGAs](#) datasheet.

TABLE 1 • ARM PROCESSOR SUPPORT IN PROASIC 3 FPGAS

| ProASIC 3 Devices | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--------------------------------|----------------|--------|--------|----------------------------|----------------|-------------------|-------------------|
| Cortex-M1 Devices ¹ | | | | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| FlashROM Kbits | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Secure (AES) ISP ² | — | Yes | Yes | Yes | Yes | Yes | Yes |
| Integrated PLL in CCCs | — | 1 | 1 | 1 | 1 | 1 | 1 |
| VersaNet Globals ³ | 6 | 18 | 18 | 18 | 18 | 18 | 18 |
| I/O Banks | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| Maximum User I/Os | 77 | 96 | 133 | 157 | 178 | 235 | 300 |
| Package Pins | | | | | | | |
| QFN | QN48, QN68, | | | | | | |
| CS | | VQ100 | | | | | |
| VQFP | VQ100 | TQ144 | VQ100 | VQ100 | | | |
| TQFP | | | TQ144 | | | | |
| PQFP | | FG144 | PQ208 | PQ208 | PQ208 | PQ208 | PQ208 |
| FBGA | | | FG144 | FG144/ 256 ⁴ | FG144/ 256/ | FG144/256/ 484 | FG144/256/ 484 |

- Note 1:** Refer to the [Cortex-M1](#) product brief for more information.
- 2:** AES is not available for Cortex-M1 ProASIC 3 devices.
- 3:** Six chip (main) and three quadrant global networks are available for A3P060 and above.
- 4:** The M1A3P250 device does not support FG256 package.
- 5:** For higher densities and support of additional features, refer to the [ProASIC 3E Flash Family FPGAs](#) datasheet.

I/Os PER PACKAGE ¹

Table 2 • I/Os PER PACKAGE

| ProASIC 3 Devices | A3P030 | A3P060 | A3P125 | A3P250 ² | | A3P400 ² | | A3P600 | | A3P1000 | |
|----------------------|----------|------------------|------------------|-------------------------|-------------------------------|------------------------|-------------------------------|------------------------|-------------------------------|------------------------|-------------------------------|
| Cortex-M1 Devices | | | | M1A3P250 ^{2,4} | | M1A3P400 ² | | M1A3P600 | | M1A3P1000 | |
| Package | I/O Type | | | | | | | | | | |
| | | Single-Ended I/O | Single-Ended I/O | Single-Ended I/O | Single-Ended I/O ³ | Differential I/O Pairs | Single-Ended I/O ³ | Differential I/O Pairs | Single-Ended I/O ³ | Differential I/O Pairs | Single-Ended I/O ³ |
| QN48 | 34 | — | — | — | — | — | — | — | — | — | — |
| QN68 | 49 | — | — | — | — | — | — | — | — | — | — |
| QN132 ⁶ | 81 | 80 | 84 | 87 | 19 | — | — | — | — | — | — |
| VQ100 | 77 | 71 | 71 | 68 | 13 | — | — | — | — | — | — |
| TQ144 | — | 91 | 100 | — | — | — | — | — | — | — | — |
| PQ208 | — | — | 133 | 151 | 34 | 151 | 34 | 154 | 35 | 154 | 35 |
| FG144 | — | 96 | 97 | 97 | 24 | 97 | 25 | 97 | 25 | 97 | 25 |
| FG256 ^{4,5} | — | — | — | 157 | 38 | 178 | 38 | 177 | 43 | 177 | 44 |
| FG484 ⁵ | — | — | — | — | — | — | — | 235 | 60 | 300 | 74 |

- Note 1:** When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC 3 FPGA Fabric User Guide](#) to ensure complying with design and board migration requirements.
- 2:** For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the [ProASIC 3 FPGA Fabric User Guide](#) for position assignments of the 15 LVPECL pairs.
- 3:** Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- 4:** The M1A3P250 device does not support FG256 package.
- 5:** FG256 and FG484 are footprint-compatible packages.

TABLE 3 • PROASIC 3 FPGAS PACKAGE SIZES DIMENSIONS

| Package | QN48 | QN68 | QN132 | VQ100 | TQ144 | PQ208 | FG144 | FG256 | FG484 |
|---------------------------------|-------|-------|-------|---------|---------|---------|---------|---------|---------|
| Length × Width (mm × mm) | 6 × 6 | 8 × 8 | 8 × 8 | 14 × 14 | 20 × 20 | 28 × 28 | 13 × 13 | 17 × 17 | 23 × 23 |
| Nominal Area (mm ²) | 36 | 64 | 64 | 196 | 400 | 784 | 169 | 289 | 529 |
| Pitch (mm) | 0.4 | 0.4 | 0.5 | 0.5 | 0.5 | 0.5 | 1.0 | 1.0 | 1.0 |
| Height (mm) | 0.90 | 0.90 | 0.75 | 1.00 | 1.40 | 3.40 | 1.45 | 1.60 | 2.23 |

PROASIC 3 ORDERING INFORMATION

FIGURE 1: PROASIC 3 ORDERING INFORMATION



ProASIC3 Devices

- A3P030 = 30,000 System Gates
- A3P060 = 60,000 System Gates
- A3P125 = 125,000 System Gates
- A3P250 = 250,000 System Gates
- A3P400 = 400,000 System Gates
- A3P600 = 600,000 System Gates
- A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1

- M1A3P250 = 250,000 System Gates
- M1A3P400 = 400,000 System Gates
- M1A3P600 = 600,000 System Gates
- M1A3P1000 = 1,000,000 System Gates

PROASIC 3 DEVICE STATUS

TABLE 4 • PROASIC 3 DEVICE STATUS

| ProASIC 3 Devices | Status | Cortex-M1 Devices | Status |
|-------------------|------------|-------------------|------------|
| A3P030 | Production | | |
| A3P060 | Production | | |
| A3P125 | Production | | |
| A3P250 | Production | M1A3P250 | Production |
| A3P400 | Production | M1A3P400 | Production |
| A3P600 | Production | M1A3P600 | Production |
| A3P1000 | Production | M1A3P1000 | Production |

TEMPERATURE GRADE OFFERINGS

| Package | A3P015 ¹ | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--------------------------|---------------------|--------|--------|--------|---------------------------------|-----------------|-----------------|------------------|
| Cortex-M1 Devices | | | | | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| QN48 | — | C, I | — | — | — | — | — | — |
| QN68 | C, I | C, I | — | — | — | — | — | — |
| QN132 ² | — | C, I | C, I | C, I | C, I | — | — | — |
| CS121 | — | — | C, I | — | — | — | — | — |
| VQ100 | — | C, I | C, I | C, I | C, I | — | — | — |
| TQ144 | — | — | C, I | C, I | — | — | — | — |
| PQ208 | — | — | — | C, I | C, I | C, I | C, I | C, I |
| FG144 | — | — | C, I | C, I | C, I | C, I | C, I | C, I |
| FG256 | — | — | — | — | C ³ , I ³ | C, I | C, I | C, I |
| FG484 | — | — | — | — | — | C, I | C, I | C, I |

Note 1: A3P015 is not recommended for new designs.

2: Package not available

3: The M1A3P250 device does not support FG256 package.

C = Commercial temperature range: 0 °C to 85 °C junction temperature

I = Industrial temperature range: -40 °C to 100 °C junction temperature

SPEED GRADE AND TEMPERATURE GRADE MATRIX

| Temperature Grade | Std. | -1 | -2 |
|-------------------|------|----|----|
| C ¹ | P | P | P |
| I ² | P | P | P |

Note 1: C = Commercial temperature range: 0 °C to 85 °C junction temperature
2: I = Industrial temperature range: -40 °C to 100 °C junction temperature

References made to ProASIC 3 devices also apply to ARM-enabled ProASIC 3 devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

A3P015 and A3P030

The A3P015 and A3P030 are architecturally compatible; there are no RAM or PLL features.

DEVICES NOT RECOMMENDED FOR NEW DESIGNS

A3P015 is not recommended for new designs.

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1.0 FEATURES OF PROASIC 3 DEVICE FAMILY

The following sections describe important feature of the ProASIC 3 Device Family.

1.1 Flash Advantages

1.1.1 REDUCED COST OF OWNERSHIP

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC 3 devices allow all functionality to be Instant On, no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable Intellectual Property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC 3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC 3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

1.1.2 SECURITY

Nonvolatile, flash-based ProASIC 3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC 3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC 3 devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in ProASIC 3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC 3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC 3 devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

ARM-enabled ProASIC 3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC 3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC 3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks.

Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC 3 device provides the best available security for programmable logic designs.

1.1.3 SINGLE CHIP

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC 3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

1.1.4 INSTANT ON

Flash-based ProASIC 3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC 3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC 3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM,

expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC 3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

1.1.5 FIRM ERRORS

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC 3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC 3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

1.1.6 LOW POWER

Flash-based ProASIC 3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC 3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC 3 devices also have low dynamic power consumption to further maximize power savings.

1.2 Advanced Flash Technology

The ProASIC 3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

1.2.1 ADVANCED ARCHITECTURE

The proprietary ProASIC 3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC 3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory

Note: A3P030 does not support PLL or SRAM.

- Extensive CCCs and PLLs

Note: A3P030 does not support PLL or SRAM.

- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC 3 core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microchip ProASIC family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

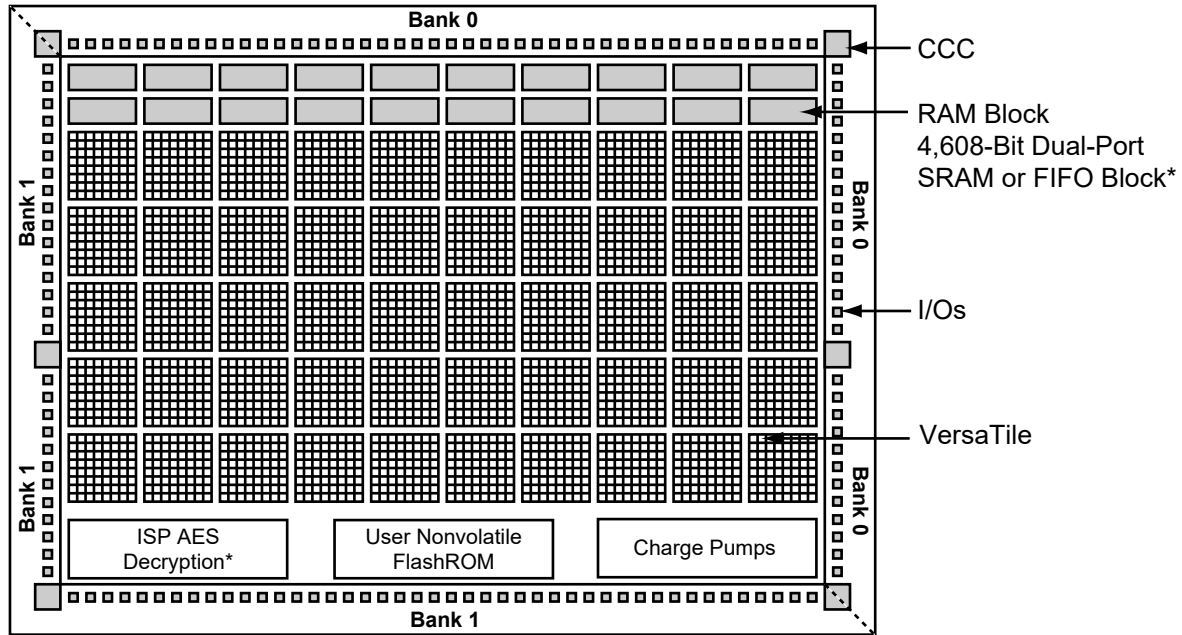
1.2.2 VERSATILES

The ProASIC 3 core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS} core tiles. The ProASIC 3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

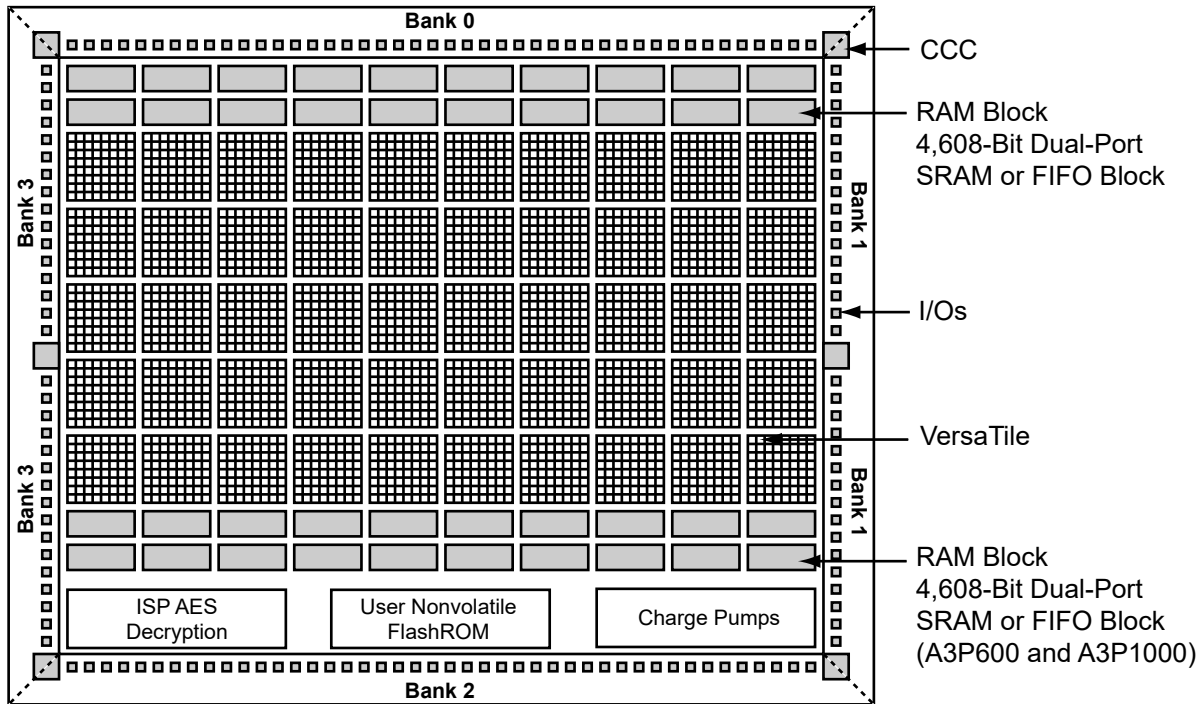
Refer to Figure 1-3 for VersaTile configurations.

FIGURE 1-1: PROASIC 3 DEVICE ARCHITECTURE OVERVIEW WITH TWO I/O BANKS (A3P030, A3P060, AND A3P125)



Note: Not supported by A3P030 devices

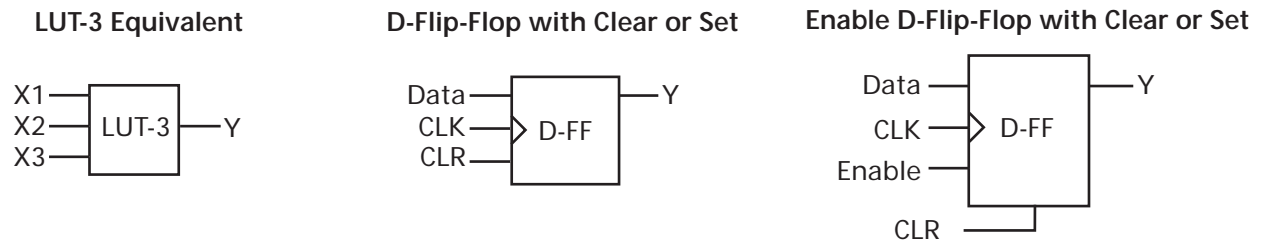
FIGURE 1-2: PROASIC 3 DEVICE ARCHITECTURE OVERVIEW WITH FOUR I/O BANKS (A3P250, A3P600, AND A3P1000)



1.2.3 USER NONVOLATILE FLASHROM

ProASIC 3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

FIGURE 1-3: VERSATILE CONFIGURATIONS



- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC 3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC 3 development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

1.2.4 SRAM AND FIFO

ProASIC 3 devices (except the A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

1.2.5 PLL AND CCC

ProASIC 3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC 3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from -7.56 ns to $+11.12$ ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0° , 90° , 180° , and 270° . Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = $50\% \pm 1.5\%$ or better (for PLL only)
- Low output jitter: worst case $< 2.5\% \times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = $300 \mu\text{s}$ (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of $40 \text{ ps} \times (350 \text{ MHz} / f_{OUT_CCC})$ (for PLL only)

1.2.6 GLOBAL CLOCKING

ProASIC 3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

1.2.7 I/O WITH ADVANCED I/O STANDARDS

The ProASIC 3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5V, 1.8V, 2.5V, and 3.3V). ProASIC 3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

TABLE 1-1: I/O STANDARDS SUPPORTED

| I/O Bank Type | Device and Bank Location | I/O Standards Supported | | |
|---------------|--|-------------------------|---------------|---------------------------------|
| | | LVTTTL/ LVCMOS | PCI/PCI-X | LVPECL, LVDS, B-LVDS, M-LVDS |
| Advanced | East and west Banks of A3P250 and larger devices | ✓ | ✓ | ✓ |
| Standard Plus | North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125 | ✓ | ✓ | Not supported |
| Standard | All banks of A3P030 | ✓ | Not supported | Not supported |

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications

- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC 3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

1.2.8 WIDE RANGE I/O SUPPORT

ProASIC 3 devices support JEDEC-defined wide range I/O operation. ProASIC 3 supports the JESD8-B specification, covering both 3V and 3.3V supplies, for an effective operating range of 2.7V to 3.6V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

1.3 Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-4](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tristate: I/O is tristated
6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

FIGURE 1-4: I/O STATES DURING PROGRAMMING WINDOW

| Port Name | Macro Cell | Pin Number | I/O State (Output Only) |
|------------|-----------------------|------------|-------------------------|
| BIST | ADLIB:INBUF | T2 | 1 |
| BYPASS_ID | ADLIB:INBUF | K1 | 1 |
| CLK | ADLIB:INBUF | B1 | 1 |
| ENOUT | ADLIB:INBUF | J16 | 1 |
| LED | ADLIB:OUTBUF | M3 | 0 |
| MONITOR[0] | ADLIB:OUTBUF | B5 | 0 |
| MONITOR[1] | ADLIB:OUTBUF | C7 | Z |
| MONITOR[2] | ADLIB:OUTBUF | D9 | Z |
| MONITOR[3] | ADLIB:OUTBUF | D7 | Z |
| MONITOR[4] | ADLIB:OUTBUF | A11 | Z |
| OEa | ADLIB:INBUF | E4 | Z |
| OEb | ADLIB:INBUF | F1 | Z |
| OSC_EN | ADLIB:INBUF | K3 | Z |
| PAD[10] | ADLIB:BIBUF_LVCMOS33U | M8 | Z |
| PAD[11] | ADLIB:BIBUF_LVCMOS33D | R7 | Z |
| PAD[12] | ADLIB:BIBUF_LVCMOS33U | D11 | Z |
| PAD[13] | ADLIB:BIBUF_LVCMOS33D | C12 | Z |
| PAD[14] | ADLIB:BIBUF_LVCMOS33U | R6 | Z |

2.0 PROASIC 3 DC AND SWITCHING CHARACTERISTICS

The following sections describe the DC and switching characteristics ProASIC 3 Device Family.

2.1 General Specifications

2.1.1 OPERATING CONDITIONS

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) is not implied.

TABLE 2-1: ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Limits | Units |
|-------------------------------|-------------------------------------|---|-------|
| VCC | DC core supply voltage | -0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | -0.3 to 3.75 | V |
| VPUMP | Programming voltage | -0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | -0.3 to 1.65 | V |
| VCCI | DC I/O output buffer supply voltage | -0.3 to 3.75 | V |
| VMV | DC I/O input buffer supply voltage | -0.3 to 3.75 | V |
| VI | I/O input voltage | -0.3V to 3.6V (when I/O hot insertion mode is enabled) -0.3V to (VCCI + 1 V) or 3.6V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| T _{STG} ² | Storage temperature | -65 to +150 | °C |
| T _J ² | Junction temperature | +125 | °C |

Note 1: The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#).

2: VMV pins must be connected to the corresponding VCCI pins. See the [Section 3.1.5 VMVx I/O Supply Voltage \(quiet\)](#) for further information.

3: For flash programming and retention maximum limits, refer to [Table 2-3](#), and for recommended operating limits, refer to [Table 2-2](#).

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS¹

| Symbol | Parameters ¹ | | Commercial | Industrial | Units |
|------------------|-----------------------------|------------------------|----------------------|-------------------------|-------|
| T _J | Junction temperature | | 0 to 85 ² | -40 to 100 ² | °C |
| VCC ³ | 1.5V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation ⁴ | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS ¹ (CONTINUED)

| Symbol | Parameters ¹ | Commercial | Industrial | Units |
|---------------------------|--|----------------|----------------|-------|
| VCCI and VMV ⁵ | 1.5V DC supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8V DC supply voltage | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5V DC supply voltage | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3V DC supply voltage | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3V wide range DC supply voltage ⁶ | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | LVDS/B-LVDS/M-LVDS differential I/O | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | 3.0 to 3.6 | 3.0 to 3.6 | V |

- Note 1:** All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 2:** Software Default Junction Temperature Range in the Libero[®] System-on-Chip (SoC) software is set to 0 °C to +70 °C for commercial, and -40 °C to +85 °C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the [Libero SoC Online Help](#).
- 3:** The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-18](#).
- 4:** VPUMP can be left floating during operation (not programming mode).
- 5:** VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the [Section 3.1.5 VMVx I/O Supply Voltage \(quiet\)](#) for further information.
- 6:** 3.3V wide range is compliant to the JESD8-B specification and supports 3.0V VCCI operation.

FIGURE 2-1: HIGH-TEMPERATURE DATA RETENTION (HTR)



Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

TABLE 2-3: FLASH PROGRAMMING LIMITS—RETENTION, STORAGE AND OPERATING TEMPERATURE

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature T _{STG} (°C) | Maximum Operating Junction Temperature T _J (°C) |
|---------------|--------------------|-------------------------------------|---|--|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

- Note 1:** This is a stress rating only; functional operation at any condition other than those indicated is not implied.
Note 2: These limits apply for program/data retention only. Refer to [Table 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS ¹

| VCCI and VMV | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ² | Maximum Overshoot/Undershoot ² |
|--------------|---|---|
| 2.7V or less | 10% | 1.4V |
| | 5% | 1.49V |
| 3V | 10% | 1.1V |
| | 5% | 1.19V |
| 3.3V | 10% | 0.79V |
| | 5% | 0.88V |
| 3.6V | 10% | 0.45V |
| | 5% | 0.54V |

- Note 1:** Based on reliability requirements at 85 °C.
Note 2: The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.
Note 3: This table does not provide PCI overshoot/undershoot limits.

2.1.2 I/O POWER-UP AND SUPPLY VOLTAGE THRESHOLDS FOR POWER-ON RESET (COMMERCIAL AND INDUSTRIAL)

Sophisticated power-up management circuitry is designed into every ProASIC 3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges.

In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-2](#).

There are five regions to consider during power-up.

ProASIC 3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-2](#)).
2. VCCI > VCC – 0.75V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6V < trip_point_up < 1.2V

Ramping down: 0.5V < trip_point_down < 1.1V

VCC Trip Point:

Ramping up: $0.6V < \text{trip_point_up} < 1.1V$

Ramping down: $0.5V < \text{trip_point_down} < 1V$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

2.1.2.1 PLL Behavior at Brownout Condition

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1V worst-case (see [Figure 2-2](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75V \pm 0.25V$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the [ProASIC 3 FPGA Fabric User's Guide](#) for information on clock and lock recovery.

2.1.2.2 Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

FIGURE 2-2: I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS



2.1.3 THERMAL CHARACTERISTICS

2.1.3.1 Introduction

The temperature variable in the Microchip Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in [Table 2-5](#).

P = Power dissipation

2.1.3.2 Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates.

The absolute maximum junction temperature is 100 °C. EQ 1 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.463\text{W}$$

EQ 1

TABLE 2-5: PACKAGE THERMAL RESISTIVITIES

| Package Type | Device | Pin Count | θ_{jc} | θ_{ja} | | | Units |
|-----------------------------------|-------------|-----------|---------------|---------------|------------|------------|-------|
| | | | | Still Air | 200 ft/min | 500 ft/min | |
| Quad Flat No Lead | A3P030 | 132 | 0.4 | 21.4 | 16.8 | 15.3 | °C/W |
| | A3P060 | 132 | 0.3 | 21.2 | 16.6 | 15.0 | °C/W |
| | A3P125 | 132 | 0.2 | 21.1 | 16.5 | 14.9 | °C/W |
| | A3P250 | 132 | 0.1 | 21.0 | 16.4 | 14.8 | °C/W |
| Very Thin Quad Flat Pack (VQFP) | All devices | 100 | 10.0 | 35.3 | 29.4 | 27.1 | °C/W |
| Thin Quad Flat Pack (TQFP) | All devices | 144 | 11.0 | 33.5 | 28.0 | 25.7 | °C/W |
| Plastic Quad Flat Pack (PQFP) | All devices | 208 | 8.0 | 26.1 | 22.5 | 20.8 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | See note* | 144 | 3.8 | 26.9 | 22.9 | 21.5 | °C/W |
| | See note* | 256 | 3.8 | 26.6 | 22.8 | 21.5 | °C/W |
| | See note* | 484 | 3.2 | 20.5 | 17.0 | 15.9 | °C/W |
| | A3P1000 | 144 | 6.3 | 31.6 | 26.2 | 24.2 | °C/W |
| | A3P1000 | 256 | 6.6 | 28.1 | 24.4 | 22.7 | °C/W |
| | A3P1000 | 484 | 8.0 | 23.3 | 19.0 | 16.7 | °C/W |

Note: *This information applies to all ProASIC 3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

2.1.3.3 Temperature and Voltage Derating Factors

TABLE 2-6: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$)

| Array Voltage V_{CC} (V) | Junction Temperature ($^\circ\text{C}$) | | | | | |
|----------------------------|---|---------------------------|----------------------------|----------------------------|----------------------------|-----------------------------|
| | $-40\text{ }^\circ\text{C}$ | $0\text{ }^\circ\text{C}$ | $25\text{ }^\circ\text{C}$ | $70\text{ }^\circ\text{C}$ | $85\text{ }^\circ\text{C}$ | $100\text{ }^\circ\text{C}$ |
| 1.425 | 0.88 | 0.93 | 0.95 | 1.00 | 1.02 | 1.04 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.96 | 0.98 |
| 1.575 | 0.80 | 0.84 | 0.87 | 0.91 | 0.93 | 0.94 |

2.2 Calculating Power Dissipation

2.2.1 QUIESCENT SUPPLY CURRENT

TABLE 2-7: QUIESCENT SUPPLY CURRENT CHARACTERISTICS

| | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|--|--------|--------|--------|--------|--------|--------|---------|
| Typical ($25\text{ }^\circ\text{C}$) | 2 mA | 2 mA | 2 mA | 3 mA | 3 mA | 5 mA | 8 mA |
| Max. (Commercial) | 10 mA | 10 mA | 10 mA | 20 mA | 20 mA | 30 mA | 50 mA |
| Max. (Industrial) | 15 mA | 15 mA | 15 mA | 30 mA | 30 mA | 45 mA | 75 mA |

Note: I_{DD} includes V_{CC} , V_{PUMP} , V_{CCI} , and V_{MV} currents. Values do not include I/O static contribution, which is shown in [Table 2-11](#) and [Table 2-12](#).

2.2.2 POWER PER I/O PIN

TABLE 2-8: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN)—DEFAULT I/O SOFTWARE SETTINGS APPLICABLE TO ADVANCED I/O BANKS

| | VMV (V) | Static Power P_{DC2} (mW) ¹ | Dynamic Power P_{AC9} ($\mu\text{W}/\text{MHz}$) ² |
|-------------------------------------|---------|--|---|
| Single-Ended | | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 3.3 | — | 16.22 |
| 3.3V LVCMOS Wide Range ³ | 3.3 | — | 16.22 |
| 2.5V LVCMOS | 2.5 | — | 5.12 |
| 1.8V LVCMOS | 1.8 | — | 2.13 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | — | 1.45 |
| 3.3V PCI | 3.3 | — | 18.11 |
| 3.3V PCI-X | 3.3 | — | 18.11 |
| Differential | | | |
| LVDS | 2.5 | 2.26 | 1.20 |
| LVPECL | 3.3 | 5.72 | 1.87 |

Note 1: P_{DC2} is the static power (where applicable) measured on VMV.

2: P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-9: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN)—DEFAULT I/O SOFTWARE SETTINGS APPLICABLE TO STANDARD PLUS I/O BANKS

| | VMV (V) | Static Power PDC2 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|-------------------------------------|---------|-------------------------------------|--|
| Single-Ended | | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 3.3 | — | 16.23 |
| 3.3V LVCMOS Wide Range ³ | 3.3 | — | 16.23 |
| 2.5V LVCMOS | 2.5 | — | 5.14 |
| 1.8V LVCMOS | 1.8 | — | 2.13 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | — | 1.48 |
| 3.3V PCI | 3.3 | — | 18.13 |
| 3.3V PCI-X | 3.3 | — | 18.13 |

- Note 1:** PDC2 is the static power (where applicable) measured on VMV.
2: PAC9 is the total dynamic power measured on VCC and VMV.
3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-10: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS APPLICABLE TO STANDARD I/O BANKS

| | VMV (V) | Static Power PDC2 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|-------------------------------------|---------|-------------------------------------|--|
| Single-Ended | | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 3.3 | — | 17.24 |
| 3.3V LVCMOS Wide Range ³ | 3.3 | — | 17.24 |
| 2.5V LVCMOS | 2.5 | — | 5.19 |
| 1.8V LVCMOS | 1.8 | — | 2.18 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | — | 1.52 |

- Note 1:** PDC2 is the static power (where applicable) measured on VMV.
2: PAC9 is the total dynamic power measured on VCC and VMV.
3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-11: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS¹ APPLICABLE TO ADVANCED I/O BANKS

| | C _{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|-------------------------------------|------------------------|----------|-------------------------------------|---|
| Single-Ended | | | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 35 | 3.3 | — | 468.67 |
| 3.3V LVCMOS Wide Range ⁴ | 35 | 3.3 | — | 468.67 |
| 2.5V LVCMOS | 35 | 2.5 | — | 267.48 |
| 1.8V LVCMOS | 35 | 1.8 | — | 149.46 |

TABLE 2-11: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS¹ APPLICABLE TO ADVANCED I/O BANKS

| | C _{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|------------------------|------------------------|----------|-------------------------------------|---|
| 1.5V LVCMOS (JESD8-11) | 35 | 1.5 | — | 103.12 |
| 3.3V PCI | 10 | 3.3 | — | 201.02 |
| 3.3V PCI-X | 10 | 3.3 | — | 201.02 |
| Differential | | | | |
| LVDS | — | 2.5 | 7.74 | 88.92 |
| LVPECL | — | 3.3 | 19.54 | 166.52 |

- Note 1:** Dynamic power consumption is given for standard load and software default drive strength and output slew.
- 2:** PDC3 is the static power (where applicable) measured on VCCI.
- 3:** PAC10 is the total dynamic power measured on VCC and VCCI.
- 4:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-12: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS¹ APPLICABLE TO STANDARD PLUS I/O BANKS

| | C _{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|-------------------------------------|------------------------|----------|-------------------------------------|---|
| Single-Ended | | | | |
| 3.3V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | — | 452.67 |
| 3.3V LVCMOS Wide Range ⁴ | 35 | 3.3 | — | 452.67 |
| 2.5V LVCMOS | 35 | 2.5 | — | 258.32 |
| 1.8V LVCMOS | 35 | 1.8 | — | 133.59 |
| 1.5V LVCMOS (JESD8-11) | 35 | 1.5 | — | 92.84 |
| 3.3V PCI | 10 | 3.3 | — | 184.92 |
| 3.3V PCI-X | 10 | 3.3 | — | 184.92 |

- Note 1:** Dynamic power consumption is given for standard load and software default drive strength and output slew.
- 2:** P_{DC3} is the static power (where applicable) measured on VMV.
- 3:** P_{AC10} is the total dynamic power measured on VCC and VMV.
- 4:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-13: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS ¹ APPLICABLE TO STANDARD I/O BANKS

| | C _{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|-------------------------------------|------------------------|----------|-------------------------------------|---|
| Single-Ended | | | | |
| 3.3V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | — | 431.08 |
| 3.3V LVCMOS Wide Range ⁴ | 35 | 3.3 | — | 431.08 |
| 2.5V LVCMOS | 35 | 2.5 | — | 247.36 |
| 1.8V LVCMOS | 35 | 1.8 | — | 128.46 |
| 1.5V LVCMOS (JESD8-11) | 35 | 1.5 | — | 89.46 |

- Note 1:** Dynamic power consumption is given for standard load and software default drive strength and output slew.
- 2:** P_{DC3} is the static power (where applicable) measured on VCCI.
- 3:** P_{AC10} is the total dynamic power measured on VCC and VCCI.
- 4:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

2.2.3 POWER CONSUMPTION OF VARIOUS INTERNAL RESOURCES

TABLE 2-14: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN PROASIC 3 DEVICES

| Parameter | Definition | Device Specific Dynamic Contributions (μW/MHz) | | | | | | |
|-----------|--|---|--------|--------|--------|--------|--------|--------|
| | | A3P1000 | A3P600 | A3P400 | A3P250 | A3P125 | A3P060 | A3P030 |
| PAC1 | Clock contribution of a Global Rib | 14.50 | 12.80 | 12.80 | 11.00 | 11.00 | 9.30 | 9.30 |
| PAC2 | Clock contribution of a Global Spine | 2.48 | 1.85 | 1.35 | 1.58 | 0.81 | 0.81 | 0.41 |
| PAC3 | Clock contribution of a VersaTile row | 0.81 | | | | | | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.12 | | | | | | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.07 | | | | | | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.29 | | | | | | |
| PAC7 | Contribution of a VersaTile used as a combinatorial Module | 0.29 | | | | | | |
| PAC8 | Average contribution of a routing net | 0.70 | | | | | | |
| PAC9 | Contribution of an I/O input pin (standard dependent) | See Table 2-8 through Table 2-10 . | | | | | | |
| PAC10 | Contribution of an I/O output pin (standard dependent) | See Table 2-11 through Table 2-13 . | | | | | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | | | | | |

TABLE 2-14: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN PROASIC 3 DEVICES

| | | |
|-------|--|-------|
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 |
| PAC13 | Dynamic contribution for PLL | 2.60 |

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip Power spreadsheet calculator or SmartPower tool in Libero SoC software.

TABLE 2-15: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN PROASIC 3 DEVICES

| Parameter | Definition | Device Specific Static Power (mW) | | | | | | |
|-----------|--|---|--------|--------|--------|--------|--------|--------|
| | | A3P1000 | A3P600 | A3P400 | A3P250 | A3P125 | A3P060 | A3P030 |
| PDC1 | Array static power in Active mode | See Table 2-7 . | | | | | | |
| PDC2 | I/O input pin static power (standard-dependent) | See Table 2-8 through Table 2-10 . | | | | | | |
| PDC3 | I/O output pin static power (standard-dependent) | See Table 2-11 through Table 2-13 . | | | | | | |
| PDC4 | Static PLL contribution | 2.55 mW | | | | | | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-7 . | | | | | | |

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip Power spreadsheet calculator or SmartPower tool in Libero SoC software.

2.2.4 POWER CALCULATION METHODOLOGY

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-16](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-17](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-17](#). The calculation should be repeated for each clock domain defined in the design.

2.2.4.1 Methodology

2.2.4.1.1 Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

2.2.4.1.2 Total Static Power Consumption— P_{STAT}

$$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

2.2.4.1.3 Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

2.2.4.1.4 Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [ProASIC 3 FPGA Fabric User's Guide](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [ProASIC 3 FPGA Fabric User's Guide](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

2.2.4.1.5 Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16](#).

F_{CLK} is the global clock signal frequency.

2.2.4.1.6 Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16](#).

F_{CLK} is the global clock signal frequency.

2.2.4.1.7 Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16](#).

F_{CLK} is the global clock signal frequency.

2.2.4.1.8 I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16](#).

F_{CLK} is the global clock signal frequency.

2.2.4.1.9 I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-16](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-17](#).

F_{CLK} is the global clock signal frequency.

2.2.4.1.10 RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{\text{WRITE-CLOCK}}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-17](#).

2.2.4.1.11 PLL Contribution— P_{PLL}

$$P_{\text{PLL}} = P_{\text{DC4}} + P_{\text{AC13}} * F_{\text{CLKOUT}}$$

F_{CLKOUT} is the output clock frequency.

Note: The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{\text{AC14}} * F_{\text{CLKOUT}}$ product) to the total PLL contribution.

2.2.4.2 Guidelines

2.2.4.2.1 Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

2.2.4.2.2 Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

TABLE 2-16: TOGGLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

| Component | Definition | Guideline |
|------------|----------------------------------|-----------|
| α_1 | Toggle rate of VersaTile outputs | 10% |
| α_2 | I/O buffer toggle rate | 10% |

TABLE 2-17: ENABLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

| Component | Definition | Guideline |
|-----------|--------------------------------------|-----------|
| β_1 | I/O output buffer enable rate | 100% |
| β_2 | RAM enable rate for read operations | 12.5% |
| β_3 | RAM enable rate for write operations | 12.5% |

2.3 User I/O Characteristics

2.3.1 TIMING MODEL

FIGURE 2-3: TIMING MODEL OPERATING CONDITIONS: -2 SPEED, COMMERCIAL TEMPERATURE RANGE ($T_J = 70\text{ }^\circ\text{C}$), WORST CASE $V_{CC} = 1.425\text{V}$



FIGURE 2-4: INPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



FIGURE 2-5: OUTPUT BUFFER MODEL AND DELAYS (EXAMPLE)



FIGURE 2-6: TRISTATE OUTPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



2.3.2 OVERVIEW OF I/O PERFORMANCE

2.3.2.1 Summary of I/O DC Input and Output Levels – Default I/O Software Settings

TABLE 2-18: APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS APPLICABLE TO ADVANCED I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ² | Slew Rate | VIL | | VIH | | VOL | VOH | IOL ₁ mA | IOH ₁ mA |
|-------------------------------------|--------------------------|--|-----------|-------|-------------|-------------|-------|-------------|-------------|---------------------|---------------------|
| | | | | Min V | Max V | Min V | Max V | Max V | Min V | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | – 0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3V LVCMOS Wide Range ³ | 100 µA | 12 mA | High | – 0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 0.1 | 0.1 |
| 2.5V LVCMOS | 12 mA | 12 mA | High | – 0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8V LVCMOS | 12 mA | 12 mA | High | – 0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5V LVCMOS | 12 mA | 12 mA | High | – 0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3V PCI | Per PCI specifications | | | | | | | | | | |
| 3.3V PCI-X | Per PCI-X specifications | | | | | | | | | | |

Note 1: Currents are measured at 85 °C junction temperature.

2: 3.3V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-19: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS APPLICABLE TO STANDARD PLUS I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ² | Slew Rate | VIL | | VIH | | VOL | VOH | IOL ¹ mA | IOH ¹ mA |
|-------------------------------------|--------------------------|--|-----------|-------|-------------|-------------|-------|-------------|-------------|---------------------|---------------------|
| | | | | Min V | Max V | Min V | Max V | Max V | Min V | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3V LVCMOS Wide Range ³ | 100 µA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 0.1 | 0.1 |
| 2.5V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8V LVCMOS | 8 mA | 8 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 8 | 8 |
| 1.5V LVCMOS | 4 mA | 4 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 |
| 3.3V PCI | Per PCI specifications | | | | | | | | | | |
| 3.3V PCI-X | Per PCI-X specifications | | | | | | | | | | |

Note 1: Currents are measured at 85 °C junction temperature.

2: 3.3V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-20: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS APPLICABLE TO STANDARD I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ² | Slew Rate | VIL | | VIH | | VOL | VOH | IO L ¹ mA | IO H ¹ mA |
|-------------------------------------|----------------|--|-----------|-------|-------------|-------------|-------|-------------|-------------|----------------------|----------------------|
| | | | | Min V | Max V | Min V | Max V | Max V | Min V | | |
| 3.3V LVTTTL / 3.3V LVCMOS | 8 mA | 8 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 3.3V LVCMOS Wide Range ³ | 100 µA | 8 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI - 0.2 | 0.1 | 0.1 |
| 2.5V LVCMOS | 8 mA | 8 mA | High | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 |
| 1.8V LVCMOS | 4 mA | 4 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 |
| 1.5V LVCMOS | 2 mA | 2 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |

Note 1: Currents are measured at 85 °C junction temperature.

2: 3.3V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-21: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|---------------------------|-------------------------|------------------|-------------------------|------------------|
| | III ³ | IIH ⁴ | III ³ | IIH ⁴ |
| | µA | µA | µA | µA |
| 3.3V LVTTTL / 3.3V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3V LVCMOS Wide Range | 10 | 10 | 15 | 15 |
| 2.5V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8V LVCMOS | 10 | 10 | 15 | 15 |

Note 1: Commercial range (0 °C < T_A < 70 °C)

2: Industrial range (-40 °C < T_A < 85 °C)

3: III is the input leakage current per I/O pin over recommended operation conditions where -0.3V < V_{IN} < V_{IL}.

4: IIH is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < VCCI. Input current is larger when operating outside recommended ranges.

TABLE 2-21: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|------------------|-------------------------|------------------|-------------------------|------------------|
| | IIL ³ | IIH ⁴ | IIL ³ | IIH ⁴ |
| | μA | μA | μA | μA |
| 1.5V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3V PCI | 10 | 10 | 15 | 15 |
| 3.3V PCI-X | 10 | 10 | 15 | 15 |

- Note 1:** Commercial range ($0\text{ }^{\circ}\text{C} < T_A < 70\text{ }^{\circ}\text{C}$)
Note 2: Industrial range ($-40\text{ }^{\circ}\text{C} < T_A < 85\text{ }^{\circ}\text{C}$)
Note 3: IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{V} < V_{IN} < V_{IL}$.
Note 4: IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.

2.3.2.2 Summary of I/O Timing Characteristics – Default I/O Software Settings

TABLE 2-22: SUMMARY OF AC MEASURING POINTS

| Standard | Measuring Trip Point (V_{trip}) |
|----------------------------|-------------------------------------|
| 3.3V LVTTTL / 3.3 V LVCMOS | 1.4V |
| 3.3V LVCMOS Wide Range | 1.4V |
| 2.5V LVCMOS | 1.2V |
| 1.8V LVCMOS | 0.90V |
| 1.5V LVCMOS | 0.75V |
| 3.3V PCI | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |
| 3.3V PCI-X | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |

TABLE 2-23: I/O AC PARAMETER DEFINITIONS

| Parameter | Parameter Definition |
|------------|--|
| t_{DP} | Data to Pad delay through the Output Buffer |
| t_{PY} | Pad to Data delay through the Input Buffer |
| t_{DOUT} | Data to Output Buffer delay through the I/O interface |
| t_{EOUT} | Enable to Output Buffer Tristate Control delay through the I/O interface |
| t_{DIN} | Input Buffer to Data delay through the I/O interface |
| t_{HZ} | Enable to Pad delay through the Output Buffer—High to Z |
| t_{ZH} | Enable to Pad delay through the Output Buffer—Z to High |
| t_{LZ} | Enable to Pad delay through the Output Buffer—Low to Z |

TABLE 2-23: I/O AC PARAMETER DEFINITIONS

| Parameter | Parameter Definition |
|------------------|---|
| t _{ZL} | Enable to Pad delay through the Output Buffer—Z to Low |
| t _{ZHS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| t _{ZLS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

TABLE 2-24: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS—2 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) ADVANCED I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t _{POUT} (ns) | t _{PP} (ns) | t _{DIN} (ns) | t _{PY} (ns) | t _{EOUT} (ns) | t _{ZL} (ns) | t _{ZH} (ns) | t _{LZ} (ns) | t _{HZ} (ns) | t _{ZLS} (ns) | t _{ZHS} (ns) | Units |
|-------------------------------------|----------------|--|-----------|----------------------|-----------------------|------------------------|----------------------|-----------------------|----------------------|------------------------|----------------------|----------------------|----------------------|----------------------|-----------------------|-----------------------|-------|
| 3.3V LVTTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | 35 | — | 0.4 5 | 2.6 4 | 0.0 3 | 0.7 6 | 0.3 2 | 2.6 9 | 2.1 1 | 2.4 0 | 2.6 8 | 4.3 6 | 3.7 8 | ns |
| 3.3V LVCMOS Wide Range ² | 100 μA | 12 mA | High | 35 | — | 0.4 5 | 4.0 8 | 0.0 3 | 0.7 6 | 0.3 2 | 4.0 8 | 3.2 0 | 3.7 1 | 4.1 4 | 6.6 1 | 5.7 4 | ns |
| 2.5V LVCMOS | 12 mA | 12 mA | High | 35 | — | 0.4 5 | 2.6 6 | 0.0 3 | 0.9 8 | 0.3 2 | 2.7 1 | 2.5 6 | 2.4 7 | 2.5 7 | 4.3 8 | 4.2 3 | ns |
| 1.8V LVCMOS | 12 mA | 12 mA | High | 35 | — | 0.4 5 | 2.6 4 | 0.0 3 | 0.9 1 | 0.3 2 | 2.6 9 | 2.2 7 | 2.7 6 | 3.0 5 | 4.3 6 | 3.9 4 | ns |
| 1.5V LVCMOS | 12 mA | 12 mA | High | 35 | — | 0.4 5 | 3.0 5 | 0.0 3 | 1.0 7 | 0.3 2 | 3.1 0 | 2.6 7 | 2.9 5 | 3.1 4 | 4.7 7 | 4.3 4 | ns |
| 3.3V PCI | Per PCI spec | — | High | 10 | 25 ⁴ | 0.4 5 | 2.0 0 | 0.0 3 | 0.6 5 | 0.3 2 | 2.0 4 | 1.4 6 | 2.4 0 | 2.6 8 | 3.7 1 | 3.1 3 | ns |
| 3.3V PCI-X | Per PCI-X spec | — | High | 10 | 25 ⁴ | 0.4 5 | 2.0 0 | 0.0 3 | 0.6 2 | 0.3 2 | 2.0 4 | 1.4 6 | 2.4 0 | 2.6 8 | 3.7 1 | 3.1 3 | ns |
| LVDS | 24 mA | — | High | — | — | 0.4 5 | 1.3 7 | 0.0 3 | 1.2 0 | — | — | — | — | — | — | — | ns |
| LVPECL | 24 mA | — | High | — | — | 0.4 5 | 1.3 4 | 0.0 3 | 1.0 5 | — | — | — | — | — | — | — | ns |

- Note 1:** The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.
- 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.
- 4:** Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11](#) for connectivity. This resistor is not required during normal operation.

TABLE 2-25: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS – 2 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST CASE $V_{CC} = 1.425\text{V}$, WORST-CASE V_{CCI} (PER STANDARD) STANDARD PLUS I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Slew Rate | Capacitive Load (pF) | External Resistor | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) | Units |
|-------------------------------------|-------------------|--|-----------|----------------------|-------------------|-----------------|---------------|----------------|---------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|-------|
| 3.3V LVTTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |
| 3.3V LVCMOS Wide Range ² | 100 μA | 12 mA | High | 35 | – | 0.45 | 3.65 | 0.03 | 1.14 | 0.32 | 3.65 | 2.93 | 3.22 | 3.72 | 6.18 | 5.46 | ns |
| 2.5V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 2.39 | 0.03 | 0.97 | 0.32 | 2.44 | 2.35 | 2.11 | 2.32 | 4.11 | 4.02 | ns |
| 1.8V LVCMOS | 8 mA | 8 mA | High | 35 | – | 0.45 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |
| 1.5V LVCMOS | 4 mA | 4 mA | High | 35 | – | 0.45 | 3.61 | 0.03 | 1.06 | 0.32 | 3.35 | 3.61 | 2.26 | 2.34 | 5.02 | 5.28 | ns |
| 3.3V PCI | Per PCI spec | – | High | 10 | 25 ⁴ | 0.45 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |
| 3.3V PCI-X | Per PCI-X spec | – | High | 10 | 25 ⁴ | 0.45 | 1.72 | 0.03 | 0.62 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

- Note 1:** The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- Note 2:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.
- Note 4:** Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11](#) for connectivity. This resistor is not required during normal operation.

TABLE 2-26: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS—2 SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) STANDARD I/O BANKS

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Slew Rate | Capacitive Load (pF) | External Resistor | t _{DOUT} (ns) | t _{DP} (ns) | t _{DIN} (ns) | t _{PY} (ns) | t _{EOUT} (ns) | t _{ZL} (ns) | t _{ZH} (ns) | t _{LZ} (ns) | t _{HZ} (ns) | Units |
|-------------------------------------|----------------|--|-----------|----------------------|-------------------|------------------------|----------------------|-----------------------|----------------------|------------------------|----------------------|----------------------|----------------------|----------------------|-------|
| 3.3V LVTTTL / 3.3V LVCMOS | 8 mA | 8 mA | High | 35 | – | 0.45 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 3.3V LVCMOS Wide Range ² | 100 μA | 8 mA | High | 35 | – | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |
| 2.5V LVCMOS | 8 mA | 8 mA | High | 35 | – | 0.45 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 1.8V LVCMOS | 4 mA | 4 mA | High | 35 | – | 0.45 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |
| 1.5V LVCMOS | 2 mA | 2 mA | High | 35 | – | 0.45 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

- Note 1:** The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.
- 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.3 I/O DC CHARACTERISTICS

TABLE 2-27: INPUT CAPACITANCE

| Symbol | Definition | Conditions | Min | Max | Units |
|--------------------|------------------------------------|----------------------------------|-----|-----|-------|
| C _{IN} | Input capacitance | V _{IN} = 0, f = 1.0 MHz | – | 8 | pF |
| C _{INCLK} | Input capacitance on the clock pin | V _{IN} = 0, f = 1.0 MHz | – | 8 | pF |

TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO ADVANCED I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-------------------------------------|----------------|---|---------------------------------------|
| 3.3V LVTTTL/3.3V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3V LVCMOS Wide Range ⁴ | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |
| 2.5V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$

3: $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO ADVANCED I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|----------------|-----------------------------|---|---------------------------------------|
| 1.5V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$

3: $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-29: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO STANDARD PLUS I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-------------------------------------|----------------|---|---------------------------------------|
| 3.3V LVTTTL /3.3V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 25 | 75 |
| 3.3V LVCMOS Wide Range ⁴ | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |
| 2.5V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$

3: $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-29: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO STANDARD PLUS I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|----------------|-----------------------------|---|---------------------------------------|
| 1.8V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| 1.5V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$

3: $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-30: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO STANDARD I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-------------------------------------|----------------|---|---------------------------------------|
| 3.3V LVTTTL/3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 3.3V LVCMOS Wide Range ⁴ | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |
| 2.5V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$

3: $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-30: I/O OUTPUT BUFFER MAXIMUM RESISTANCES¹ APPLICABLE TO STANDARD I/O BANKS

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-------------|----------------|---|---------------------------------------|
| 1.8V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5V LVCMOS | 2 mA | 200 | 224 |

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis>.

2: $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$

3: $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-31: I/O WEAK PULL-UP/PULL-DOWN RESISTANCES MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES

| VCCI | R _(WEAK PULL-UP) ¹ (Ω) | | R _(WEAK PULL-DOWN) ² (Ω) | |
|------------------------|--|-----|--|------|
| | Min | Max | Min | Max |
| 3.3V | 10k | 45k | 10k | 45k |
| 3.3V (wide range I/Os) | 10k | 45k | 10k | 45k |
| 2.5V | 11k | 55k | 12k | 74k |
| 1.8V | 18k | 70k | 17k | 110k |
| 1.5V | 19k | 90k | 19k | 140k |

Note 1: $R_{(WEAK PULL-UP-MAX)} = (VCCI_{MAX} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$

2: $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

TABLE 2-32: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO ADVANCED I/O BANKS

| | Drive Strength | IOSL (mA) ¹ | IOSH (mA) ¹ |
|-------------------------------------|----------------|-----------------------------|-----------------------------|
| 3.3V LVTTTL/3.3V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 3.3V LVCMOS Wide Range ² | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |

TABLE 2-32: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO ADVANCED I/O BANKS

| | Drive Strength | IOSL (mA) ¹ | IOSH (mA) ¹ |
|----------------|-----------------------------|------------------------|------------------------|
| 2.5V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| | 16 mA | 87 | 83 |
| | 24 mA | 124 | 169 |
| 1.8V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 51 | 45 |
| | 12 mA | 74 | 91 |
| | 16 mA | 74 | 91 |
| | 1.5V LVCMOS | 2 mA | 16 |
| 4 mA | | 33 | 25 |
| 6 mA | | 39 | 32 |
| 8 mA | | 55 | 66 |
| 12 mA | | 55 | 66 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

Note 1: $T_J = 100\text{ }^\circ\text{C}$

2: Applicable to 3.3V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-33: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO STANDARD PLUS I/O BANKS

| | Drive Strength | IOSL (mA) ¹ | IOSH (mA) ¹ |
|-------------------------------------|-------------------|-----------------------------|-----------------------------|
| 3.3V LVTTTL / 3.3V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 109 | 103 |
| 3.3V LVCMOS Wide Range ² | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |

TABLE 2-33: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO STANDARD PLUS I/O BANKS

| | Drive Strength | IOSL (mA) ¹ | IOSH (mA) ¹ |
|----------------|-----------------------------|------------------------|------------------------|
| 2.5V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| 1.8V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 44 | 35 |
| 1.5V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

Note 1: $T_J = 100\text{ }^\circ\text{C}$

- 2:** Applicable to 3.3V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

TABLE 2-34: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO STANDARD I/O BANKS

| | Drive Strength | IOSL (mA) ¹ | IOSH (mA) ¹ |
|-------------------------------------|-------------------|-----------------------------|-----------------------------|
| 3.3V LVTTTL / 3.3V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| 3.3V LVCMOS Wide Range ² | 100 μA | Same as regular 3.3V LVCMOS | Same as regular 3.3V LVCMOS |
| 2.5V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| 1.8V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| 1.5V LVCMOS | 2 mA | 16 | 13 |

Note 1: $T_J = 100\text{ }^\circ\text{C}$

- 2:** Applicable to 3.3V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100 °C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

TABLE 2-35: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE

| Temperature | Time before Failure |
|-------------|---------------------|
| -40 °C | > 20 years |
| 0 °C | > 20 years |
| 25 °C | > 20 years |
| 70 °C | 5 years |
| 85 °C | 2 years |
| 100 °C | 0.5 years |

TABLE 2-36: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY

| Input Buffer | Input Rise/Fall Time (min) | Input Rise/Fall Time (max) | Reliability |
|-------------------------------|----------------------------|----------------------------|-------------------|
| LVTTL/LVCMOS | No requirement | 10 ns * | 20 years (110 °C) |
| LVDS/B-LVDS/ M-LVDS/LVPECL | No requirement | 10 ns * | 10 years (100 °C) |

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.3.4 SINGLE-ENDED I/O CHARACTERISTICS

2.3.4.1 3.3V LVTTL/3.3V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

TABLE 2-37: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 3.3V LVTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------------------|----------|----------|----------|----------|----------|----------|-----|-----|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 10 | 10 |

TABLE 2-37: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 3.3V LVTTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------------------------|----------|----------|----------|----------|----------|----------|-----|-----|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at 100 °C junction temperature and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-38: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O BANKS

| 3.3V LVTTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------------------------|----------|----------|----------|----------|----------|----------|-----|-----|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 109 | 103 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at 100 °C junction temperature and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-39: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD I/O BANKS

| 3.3V LVTTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------------------------|----------|----------|----------|----------|----------|----------|-----|-----|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |

TABLE 2-39: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD I/O BANKS

| 3.3V LVTTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------------------------|----------|----------|----------|----------|----------|----------|-----|-----|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at 100 °C junction temperature and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-40: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 3.3 | 1.4 | 35 |

Note: *Measuring point = Vtrip. See [Table 2-22](#) for a complete table of trip points.

FIGURE 2-7: AC LOADING



2.3.4.1.1 Timing Characteristics

TABLE 2-41: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 7.66 | 0.04 | 1.02 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | -1 | 0.56 | 6.51 | 0.04 | 0.86 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | -2 | 0.49 | 5.72 | 0.03 | 0.76 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 4 mA | Std. | 0.66 | 7.66 | 0.04 | 1.02 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | -1 | 0.56 | 6.51 | 0.04 | 0.86 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | -2 | 0.49 | 5.72 | 0.03 | 0.76 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 6 mA | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | -1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | -2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 8 mA | Std. | 0.66 | 4.91 | 0.04 | 1.02 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | -1 | 0.56 | 4.17 | 0.04 | 0.86 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | -2 | 0.49 | 3.66 | 0.03 | 0.76 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.02 | 0.43 | 3.60 | 2.82 | 3.21 | 3.58 | 5.83 | 5.06 | ns |
| | -1 | 0.56 | 3.00 | 0.04 | 0.86 | 0.36 | 3.06 | 2.40 | 2.73 | 3.05 | 4.96 | 4.30 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.76 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 16 mA | Std. | 0.66 | 3.33 | 0.04 | 1.02 | 0.43 | 3.39 | 2.56 | 3.26 | 3.68 | 5.63 | 4.80 | ns |
| | -1 | 0.56 | 2.83 | 0.04 | 0.86 | 0.36 | 2.89 | 2.18 | 2.77 | 3.13 | 4.79 | 4.08 | ns |
| | -2 | 0.49 | 2.49 | 0.03 | 0.76 | 0.32 | 2.53 | 1.91 | 2.44 | 2.75 | 4.20 | 3.58 | ns |
| 24 mA | Std. | 0.66 | 3.08 | 0.04 | 1.02 | 0.43 | 3.13 | 2.12 | 3.32 | 4.06 | 5.37 | 4.35 | ns |
| | -1 | 0.56 | 2.62 | 0.04 | 0.86 | 0.36 | 2.66 | 1.80 | 2.83 | 3.45 | 4.57 | 3.70 | ns |
| | -2 | 0.49 | 2.30 | 0.03 | 0.76 | 0.32 | 2.34 | 1.58 | 2.48 | 3.03 | 4.01 | 3.25 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-42: 3.3V LVTTTL/3.3 V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | -1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | -2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-42: 3.3V LVTTTL/3.3 V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| | -1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | -2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | -1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | -2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | -1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | -2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | -1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | -2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | -1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | -2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-43: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 0.66 | 7.20 | 0.04 | 1.00 | 0.43 | 7.34 | 6.29 | 2.27 | 2.34 | 9.57 | 8.52 | ns |
| | -1 | 0.56 | 6.13 | 0.04 | 0.85 | 0.36 | 6.24 | 5.35 | 1.93 | 1.99 | 8.14 | 7.25 | ns |
| | -2 | 0.49 | 5.38 | 0.03 | 0.75 | 0.32 | 5.48 | 4.69 | 1.70 | 1.75 | 7.15 | 6.36 | ns |
| 4 mA | Std. | 0.66 | 7.20 | 0.04 | 1.00 | 0.43 | 7.34 | 6.29 | 2.27 | 2.34 | 9.57 | 8.52 | ns |
| | -1 | 0.56 | 6.13 | 0.04 | 0.85 | 0.36 | 6.24 | 5.35 | 1.93 | 1.99 | 8.14 | 7.25 | ns |
| | -2 | 0.49 | 5.38 | 0.03 | 0.75 | 0.32 | 5.48 | 4.69 | 1.70 | 1.75 | 7.15 | 6.36 | ns |
| 6 mA | Std. | 0.66 | 4.50 | 0.04 | 1.00 | 0.43 | 4.58 | 3.82 | 2.58 | 2.88 | 6.82 | 6.05 | ns |
| | -1 | 0.56 | 3.83 | 0.04 | 0.85 | 0.36 | 3.90 | 3.25 | 2.19 | 2.45 | 5.80 | 5.15 | ns |
| | -2 | 0.49 | 3.36 | 0.03 | 0.75 | 0.32 | 3.42 | 2.85 | 1.92 | 2.15 | 5.09 | 4.52 | ns |
| 8 mA | Std. | 0.66 | 4.50 | 0.04 | 1.00 | 0.43 | 4.58 | 3.82 | 2.58 | 2.88 | 6.82 | 6.05 | ns |
| | -1 | 0.56 | 3.83 | 0.04 | 0.85 | 0.36 | 3.90 | 3.25 | 2.19 | 2.45 | 5.80 | 5.15 | ns |
| | -2 | 0.49 | 3.36 | 0.03 | 0.75 | 0.32 | 3.42 | 2.85 | 1.92 | 2.15 | 5.09 | 4.52 | ns |

TABLE 2-43: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 12 mA | Std. | 0.66 | 3.16 | 0.04 | 1.00 | 0.43 | 3.22 | 2.58 | 2.79 | 3.22 | 5.45 | 4.82 | ns |
| | -1 | 0.56 | 2.69 | 0.04 | 0.85 | 0.36 | 2.74 | 2.20 | 2.37 | 2.74 | 4.64 | 4.10 | ns |
| | -2 | 0.49 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |
| 16 mA | Std. | 0.66 | 3.16 | 0.04 | 1.00 | 0.43 | 3.22 | 2.58 | 2.79 | 3.22 | 5.45 | 4.82 | ns |
| | -1 | 0.56 | 2.69 | 0.04 | 0.85 | 0.36 | 2.74 | 2.20 | 2.37 | 2.74 | 4.64 | 4.10 | ns |
| | -2 | 0.49 | 2.36 | 0.03 | 0.75 | 0.32 | 2.40 | 1.93 | 2.08 | 2.41 | 4.07 | 3.60 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-44: 3.3V LVTTTL/3.3V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 9.68 | 0.04 | 1.00 | 0.43 | 9.86 | 8.42 | 2.28 | 2.21 | 12.09 | 10.66 | ns |
| | -1 | 0.56 | 8.23 | 0.04 | 0.85 | 0.36 | 8.39 | 7.17 | 1.94 | 1.88 | 10.29 | 9.07 | ns |
| | -2 | 0.49 | 7.23 | 0.03 | 0.75 | 0.32 | 7.36 | 6.29 | 1.70 | 1.65 | 9.03 | 7.96 | ns |
| 4 mA | Std. | 0.66 | 9.68 | 0.04 | 1.00 | 0.43 | 9.86 | 8.42 | 2.28 | 2.21 | 12.09 | 10.66 | ns |
| | -1 | 0.56 | 8.23 | 0.04 | 0.85 | 0.36 | 8.39 | 7.17 | 1.94 | 1.88 | 10.29 | 9.07 | ns |
| | -2 | 0.49 | 7.23 | 0.03 | 0.75 | 0.32 | 7.36 | 6.29 | 1.70 | 1.65 | 9.03 | 7.96 | ns |
| 6 mA | Std. | 0.66 | 6.70 | 0.04 | 1.00 | 0.43 | 6.82 | 5.89 | 2.58 | 2.74 | 9.06 | 8.12 | ns |
| | -1 | 0.56 | 5.70 | 0.04 | 0.85 | 0.36 | 5.80 | 5.01 | 2.20 | 2.33 | 7.71 | 6.91 | ns |
| | -2 | 0.49 | 5.00 | 0.03 | 0.75 | 0.32 | 5.10 | 4.40 | 1.93 | 2.05 | 6.76 | 6.06 | ns |
| 8 mA | Std. | 0.66 | 6.70 | 0.04 | 1.00 | 0.43 | 6.82 | 5.89 | 2.58 | 2.74 | 9.06 | 8.12 | ns |
| | -1 | 0.56 | 5.70 | 0.04 | 0.85 | 0.36 | 5.80 | 5.01 | 2.20 | 2.33 | 7.71 | 6.91 | ns |
| | -2 | 0.49 | 5.00 | 0.03 | 0.75 | 0.32 | 5.10 | 4.40 | 1.93 | 2.05 | 6.76 | 6.06 | ns |
| 12 mA | Std. | 0.66 | 5.05 | 0.04 | 1.00 | 0.43 | 5.14 | 4.51 | 2.79 | 3.08 | 7.38 | 6.75 | ns |
| | -1 | 0.56 | 4.29 | 0.04 | 0.85 | 0.36 | 4.37 | 3.84 | 2.38 | 2.62 | 6.28 | 5.74 | ns |
| | -2 | 0.49 | 3.77 | 0.03 | 0.75 | 0.32 | 3.84 | 3.37 | 2.09 | 2.30 | 5.51 | 5.04 | ns |
| 16 mA | Std. | 0.66 | 5.05 | 0.04 | 1.00 | 0.43 | 5.14 | 4.51 | 2.79 | 3.08 | 7.38 | 6.75 | ns |
| | -1 | 0.56 | 4.29 | 0.04 | 0.85 | 0.36 | 4.37 | 3.84 | 2.38 | 2.62 | 6.28 | 5.74 | ns |
| | -2 | 0.49 | 3.77 | 0.03 | 0.75 | 0.32 | 3.84 | 3.37 | 2.09 | 2.30 | 5.51 | 5.04 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-45: 3.3 V LVTTTL / 3.3 V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 4 mA | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 6 mA | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 8 mA | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-46: 3.3 V LVTTTL / 3.3 V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | -1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | -2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 4 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | -1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | -2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 6 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | -1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | -2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |
| 8 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | -1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | -2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.4.2 3.3V LVCMOS Wide Range

TABLE 2-47: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 3.3 V LVCMOS Wide Range | Equiv. Software Default Drive Strength Option ¹ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ² | IIH ³ |
|-------------------------|--|-------|-------|-------|-------|-------|-----------|-----|-----|---------------------|---------------------|------------------|------------------|
| | | Min V | Max V | Min V | Max V | Max V | Min V | μA | μA | Max mA ⁴ | Max mA ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 μA | 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 132 | 127 | 10 | 10 |
| 100 μA | 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 268 | 181 | 10 | 10 |

- Note 1:** The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3V < VIN < VIL.
- 3:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.
- 6:** Software default selection highlighted in gray.

TABLE 2-48: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O BANKS

| 3.3 V LVCMOS Wide Range | Equiv. Software Default Drive Strength Option ¹ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ² | IIH ³ |
|-------------------------|--|-------|-------|-------|-------|-------|-----------|-----|-----|---------------------|---------------------|------------------|------------------|
| | | Min V | Max V | Min V | Max V | Max V | Min V | μA | μA | Max mA ⁴ | Max mA ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |

TABLE 2-48: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O BANKS

| 3.3 V LVC MOS Wide Range | Equiv. Software Default Drive Strength Option ¹ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ² | IIH ³ |
|--------------------------|--|-------|-------|-------|-------|-------|-----------|-----|-----|---------------------|---------------------|------------------|------------------|
| | | Min V | Max V | Min V | Max V | Max V | Min V | μA | μA | Max mA ⁴ | Max mA ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |

- Note 1:** The minimum drive strength for any LVC MOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3V < VIN < VIL.
- 3:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** All LVMCOS 3.3V software macros support LVC MOS 3.3V wide range as specified in the JESD8-B specification.
- 6:** Software default selection highlighted in gray.

TABLE 2-49: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD I/O BANKS

| 3.3 V LVC MOS Wide Range | Equiv. Software Default Drive Strength Option ¹ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ² | IIH ³ |
|--------------------------|--|-------|-------|-------|-------|-------|-----------|-----|-----|---------------------|---------------------|------------------|------------------|
| | | Min V | Max V | Min V | Max V | Max V | Min V | μA | μA | Max mA ⁴ | Max mA ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |

- Note 1:** The minimum drive strength for any LVC MOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3V < VIN < VIL.
- 3:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** All LVMCOS 3.3V software macros support LVC MOS 3.3V wide range as specified in the JESD8-B specification.
- 6:** Software default selection highlighted in gray.

2.3.4.2.1 Timing Characteristics

TABLE 2-50: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Unit s |
|----------------|--|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|--------|
| 100 μA | 4 mA | Std. | 0.60 | 11.84 | 0.04 | 1.02 | 0.43 | 11.84 | 10.00 | 4.10 | 4.04 | 15.23 | 13.40 | ns |
| | | -1 | 0.51 | 10.07 | 0.04 | 0.86 | 0.36 | 10.07 | 8.51 | 3.48 | 3.44 | 12.96 | 11.40 | ns |
| | | -2 | 0.45 | 8.84 | 0.03 | 0.76 | 0.32 | 8.84 | 7.47 | 3.06 | 3.02 | 11.38 | 10.00 | ns |
| 100 μA | 6 mA | Std. | 0.60 | 7.59 | 0.04 | 1.02 | 0.43 | 7.59 | 6.18 | 4.62 | 4.95 | 10.98 | 9.57 | ns |
| | | -1 | 0.51 | 6.45 | 0.04 | 0.86 | 0.36 | 6.45 | 5.25 | 3.93 | 4.21 | 9.34 | 8.14 | ns |
| | | -2 | 0.45 | 5.67 | 0.03 | 0.76 | 0.32 | 5.67 | 4.61 | 3.45 | 3.70 | 8.20 | 7.15 | ns |
| 100 μA | 8 mA | Std. | 0.60 | 7.59 | 0.04 | 1.02 | 0.43 | 7.59 | 6.18 | 4.62 | 4.95 | 10.98 | 9.57 | ns |
| | | -1 | 0.51 | 6.45 | 0.04 | 0.86 | 0.36 | 6.45 | 5.25 | 3.93 | 4.21 | 9.34 | 8.14 | ns |
| | | -2 | 0.45 | 5.67 | 0.03 | 0.76 | 0.32 | 5.67 | 4.61 | 3.45 | 3.70 | 8.20 | 7.15 | ns |
| 100 μA | 12 mA | Std. | 0.60 | 5.46 | 0.04 | 1.02 | 0.43 | 5.46 | 4.29 | 4.97 | 5.54 | 8.86 | 7.68 | ns |
| | | -1 | 0.51 | 4.65 | 0.04 | 0.86 | 0.36 | 4.65 | 3.65 | 4.22 | 4.71 | 7.53 | 6.54 | ns |
| | | -2 | 0.45 | 4.08 | 0.03 | 0.76 | 0.32 | 4.08 | 3.20 | 3.71 | 4.14 | 6.61 | 5.74 | ns |
| 100 μA | 16 mA | Std. | 0.60 | 5.15 | 0.04 | 1.02 | 0.43 | 5.15 | 3.89 | 5.04 | 5.69 | 8.55 | 7.29 | ns |
| | | -1 | 0.51 | 4.38 | 0.04 | 0.86 | 0.36 | 4.38 | 3.31 | 4.29 | 4.84 | 7.27 | 6.20 | ns |
| | | -2 | 0.45 | 3.85 | 0.03 | 0.76 | 0.32 | 3.85 | 2.91 | 3.77 | 4.25 | 6.38 | 5.44 | ns |
| 100 μA | 24 mA | Std. | 0.60 | 4.75 | 0.04 | 1.02 | 0.43 | 4.75 | 3.22 | 5.14 | 6.28 | 8.15 | 6.61 | ns |
| | | -1 | 0.51 | 4.04 | 0.04 | 0.86 | 0.36 | 4.04 | 2.74 | 4.37 | 5.34 | 6.93 | 5.62 | ns |
| | | -2 | 0.45 | 3.55 | 0.03 | 0.76 | 0.32 | 3.55 | 2.40 | 3.84 | 4.69 | 6.09 | 4.94 | ns |

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Software default selection highlighted in gray.

3: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-51: 3.3V LVTTTL/3.3V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|------|
| 100 μA | 2 mA | Std. | 0.60 | 15.86 | 0.04 | 1.54 | 0.43 | 15.86 | 13.51 | 4.09 | 3.80 | 19.25 | 16.90 | ns |
| | | -1 | 0.51 | 13.49 | 0.04 | 1.31 | 0.36 | 13.49 | 11.49 | 3.48 | 3.23 | 16.38 | 14.38 | ns |
| | | -2 | 0.45 | 11.84 | 0.03 | 1.15 | 0.32 | 11.84 | 10.09 | 3.05 | 2.84 | 14.38 | 12.62 | ns |
| 100 μA | 4 mA | Std. | 0.60 | 11.25 | 0.04 | 1.54 | 0.43 | 11.25 | 9.54 | 4.61 | 4.70 | 14.64 | 12.93 | ns |
| | | -1 | 0.51 | 9.57 | 0.04 | 1.31 | 0.36 | 9.57 | 8.11 | 3.92 | 4.00 | 12.46 | 11.00 | ns |
| | | -2 | 0.45 | 8.40 | 0.03 | 1.15 | 0.32 | 8.40 | 7.12 | 3.44 | 3.51 | 10.93 | 9.66 | ns |
| 100 μA | 6 mA | Std. | 0.60 | 11.25 | 0.04 | 1.54 | 0.43 | 11.25 | 9.54 | 4.61 | 4.70 | 14.64 | 12.93 | ns |
| | | -1 | 0.51 | 9.57 | 0.04 | 1.31 | 0.36 | 9.57 | 8.11 | 3.92 | 4.00 | 12.46 | 11.00 | ns |
| | | -2 | 0.45 | 8.40 | 0.03 | 1.15 | 0.32 | 8.40 | 7.12 | 3.44 | 3.51 | 10.93 | 9.66 | ns |
| 100 μA | 8 mA | Std. | 0.60 | 8.63 | 0.04 | 1.54 | 0.43 | 8.63 | 7.39 | 4.96 | 5.28 | 12.02 | 10.79 | ns |
| | | -1 | 0.51 | 7.34 | 0.04 | 1.31 | 0.36 | 7.34 | 6.29 | 4.22 | 4.49 | 10.23 | 9.18 | ns |
| | | -2 | 0.45 | 6.44 | 0.03 | 1.15 | 0.32 | 6.44 | 5.52 | 3.70 | 3.94 | 8.98 | 8.06 | ns |
| 100 μA | 16 mA | Std. | 0.60 | 8.05 | 0.04 | 1.54 | 0.43 | 8.05 | 6.93 | 5.03 | 5.43 | 11.44 | 10.32 | ns |
| | | -1 | 0.51 | 6.85 | 0.04 | 1.31 | 0.36 | 6.85 | 5.90 | 4.28 | 4.62 | 9.74 | 8.78 | ns |
| | | -2 | 0.45 | 6.01 | 0.03 | 1.15 | 0.32 | 6.01 | 5.18 | 3.76 | 4.06 | 8.55 | 7.71 | ns |
| 100 μA | 24 mA | Std. | 0.60 | 7.50 | 0.04 | 1.54 | 0.43 | 7.50 | 6.90 | 5.13 | 6.00 | 10.89 | 10.29 | ns |
| | | -1 | 0.51 | 6.38 | 0.04 | 1.31 | 0.36 | 6.38 | 5.87 | 4.36 | 5.11 | 9.27 | 8.76 | ns |
| | | -2 | 0.45 | 5.60 | 0.03 | 1.15 | 0.32 | 5.60 | 5.15 | 3.83 | 4.48 | 8.13 | 7.69 | ns |

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-52: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|------|
| 100 μA | 2 mA | Std. | 0.60 | 11.14 | 0.04 | 1.52 | 0.43 | 11.14 | 9.54 | 3.51 | 3.61 | 14.53 | 12.94 | ns |
| | | -1 | 0.51 | 9.48 | 0.04 | 1.29 | 0.36 | 9.48 | 8.12 | 2.99 | 3.07 | 12.36 | 11.00 | ns |
| | | -2 | 0.45 | 8.32 | 0.03 | 1.14 | 0.32 | 8.32 | 7.13 | 2.62 | 2.70 | 10.85 | 9.66 | ns |

TABLE 2-52: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit s |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|--------|
| 100 μA | 4 mA | Std. | 0.60 | 6.96 | 0.04 | 1.52 | 0.43 | 6.96 | 5.79 | 3.99 | 4.45 | 10.35 | 9.19 | ns |
| | | -1 | 0.51 | 5.92 | 0.04 | 1.29 | 0.36 | 5.92 | 4.93 | 3.39 | 3.78 | 8.81 | 7.82 | ns |
| | | -2 | 0.45 | 5.20 | 0.03 | 1.14 | 0.32 | 5.20 | 4.33 | 2.98 | 3.32 | 7.73 | 6.86 | ns |
| 100 μA | 6 mA | Std. | 0.60 | 6.96 | 0.04 | 1.52 | 0.43 | 6.96 | 5.79 | 3.99 | 4.45 | 10.35 | 9.19 | ns |
| | | -1 | 0.51 | 5.92 | 0.04 | 1.29 | 0.36 | 5.92 | 4.93 | 3.39 | 3.78 | 8.81 | 7.82 | ns |
| | | -2 | 0.45 | 5.20 | 0.03 | 1.14 | 0.32 | 5.20 | 4.33 | 2.98 | 3.32 | 7.73 | 6.86 | ns |
| 100 μA | 8 mA | Std. | 0.60 | 4.89 | 0.04 | 1.52 | 0.43 | 4.89 | 3.92 | 4.31 | 4.98 | 8.28 | 7.32 | ns |
| | | -1 | 0.51 | 4.16 | 0.04 | 1.29 | 0.36 | 4.16 | 3.34 | 3.67 | 4.24 | 7.04 | 6.22 | ns |
| | | -2 | 0.45 | 3.65 | 0.03 | 1.14 | 0.32 | 3.65 | 2.93 | 3.22 | 3.72 | 6.18 | 5.46 | ns |
| 100 μA | 16 mA | Std. | 0.60 | 4.89 | 0.04 | 1.52 | 0.43 | 4.89 | 3.92 | 4.31 | 4.98 | 8.28 | 7.32 | ns |
| | | -1 | 0.51 | 4.16 | 0.04 | 1.29 | 0.36 | 4.16 | 3.34 | 3.67 | 4.24 | 7.04 | 6.22 | ns |
| | | -2 | 0.45 | 3.65 | 0.03 | 1.14 | 0.32 | 3.65 | 2.93 | 3.22 | 3.72 | 6.18 | 5.46 | ns |

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: Software default selection highlighted in gray.

3: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

3.3V LVTTTL/3.3V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit s |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|--------|
| 100 μA | 2 mA | Std. | 0.60 | 14.97 | 0.04 | 1.52 | 0.43 | 14.97 | 12.79 | 3.52 | 3.41 | 18.36 | 16.18 | ns |
| | | -1 | 0.51 | 12.73 | 0.04 | 1.29 | 0.36 | 12.73 | 10.88 | 2.99 | 2.90 | 15.62 | 13.77 | ns |
| | | -2 | 0.45 | 11.18 | 0.03 | 1.14 | 0.32 | 11.18 | 9.55 | 2.63 | 2.55 | 13.71 | 12.08 | ns |
| 100 μA | 4 mA | Std. | 0.60 | 10.36 | 0.04 | 1.52 | 0.43 | 10.36 | 8.93 | 3.99 | 4.24 | 13.75 | 12.33 | ns |
| | | -1 | 0.51 | 8.81 | 0.04 | 1.29 | 0.36 | 8.81 | 7.60 | 3.39 | 3.60 | 11.70 | 10.49 | ns |
| | | -2 | 0.45 | 7.74 | 0.03 | 1.14 | 0.32 | 7.74 | 6.67 | 2.98 | 3.16 | 10.27 | 9.21 | ns |
| 100 μA | 6 mA | Std. | 0.60 | 10.36 | 0.04 | 1.52 | 0.43 | 10.36 | 8.93 | 3.99 | 4.24 | 13.75 | 12.33 | ns |
| | | -1 | 0.51 | 8.81 | 0.04 | 1.29 | 0.36 | 8.81 | 7.60 | 3.39 | 3.60 | 11.70 | 10.49 | ns |
| | | -2 | 0.45 | 7.74 | 0.03 | 1.14 | 0.32 | 7.74 | 6.67 | 2.98 | 3.16 | 10.27 | 9.21 | ns |

3.3V LVTTTL/3.3V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 μA | 8 mA | Std. | 0.60 | 7.81 | 0.04 | 1.52 | 0.43 | 7.81 | 6.85 | 4.32 | 4.76 | 11.20 | 10.24 | ns |
| | | -1 | 0.51 | 6.64 | 0.04 | 1.29 | 0.36 | 6.64 | 5.82 | 3.67 | 4.05 | 9.53 | 8.71 | ns |
| | | -2 | 0.45 | 5.83 | 0.03 | 1.14 | 0.32 | 5.83 | 5.11 | 3.22 | 3.56 | 8.36 | 7.65 | ns |
| 100 μA | 16 mA | Std. | 0.60 | 7.81 | 0.04 | 1.52 | 0.43 | 7.81 | 6.85 | 4.32 | 4.76 | 11.20 | 10.24 | ns |
| | | -1 | 0.51 | 6.64 | 0.04 | 1.29 | 0.36 | 6.64 | 5.82 | 3.67 | 4.05 | 9.53 | 8.71 | ns |
| | | -2 | 0.45 | 5.83 | 0.03 | 1.14 | 0.32 | 5.83 | 5.11 | 3.22 | 3.56 | 8.36 | 7.65 | ns |

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-53: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 100 μA | 2 mA | Std. | 0.60 | 10.93 | 0.04 | 1.52 | 0.43 | 10.93 | 9.46 | 3.20 | 3.32 | ns |
| | | -1 | 0.51 | 9.29 | 0.04 | 1.29 | 0.36 | 9.29 | 8.04 | 2.72 | 2.82 | ns |
| | | -2 | 0.45 | 8.16 | 0.03 | 1.13 | 0.32 | 8.16 | 7.06 | 2.39 | 2.48 | ns |
| 100 μA | 4 mA | Std. | 0.60 | 10.93 | 0.04 | 1.52 | 0.43 | 10.93 | 9.46 | 3.20 | 3.32 | ns |
| | | -1 | 0.51 | 9.29 | 0.04 | 1.29 | 0.36 | 9.29 | 8.04 | 2.72 | 2.82 | ns |
| | | -2 | 0.45 | 8.16 | 0.03 | 1.13 | 0.32 | 8.16 | 7.06 | 2.39 | 2.48 | ns |
| 100 μA | 6 mA | Std. | 0.60 | 6.82 | 0.04 | 1.52 | 0.43 | 6.82 | 5.70 | 3.70 | 4.16 | ns |
| | | -1 | 0.51 | 5.80 | 0.04 | 1.29 | 0.36 | 5.80 | 4.85 | 3.15 | 3.54 | ns |
| | | -2 | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |
| 100 μA | 8 mA | Std. | 0.60 | 6.82 | 0.04 | 1.52 | 0.43 | 6.82 | 5.70 | 3.70 | 4.16 | ns |

TABLE 2-53: 3.3V LVTTTL/3.3V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | Units |
|----------------|--|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | -1 | 0.51 | 5.80 | 0.04 | 1.29 | 0.36 | 5.80 | 4.85 | 3.15 | 3.54 | ns |
| | | -2 | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |

- Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** Software default selection highlighted in gray.
- 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-54: 3.3V LVTTTL/3.3V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Equiv. Software Default Drive Strength Option ¹ | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | Units |
|----------------|--|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|-------|
| 100 µA | 2 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | -1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | -2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | -1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | -2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | -1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | -2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | -1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | -2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |

- Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- 2:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.4.3 2.5V LVCMOS

Low-Voltage CMOS for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications.

TABLE 2-55: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL1 | IIH ² |
|--------------|--------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|-----------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-56: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O BANKS

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------|--------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-57: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD I/O BANKS

| 2.5 V LVCMOS Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------------------|--------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 16 | 18 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 32 | 37 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-58: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 2.5 | 1.2 | 35 |

Note: *Measuring point = Vtrip. See [Table 2-22](#) for a complete table of trip points.

FIGURE 2-8: AC LOADING



2.3.4.3.1 Timing Characteristics

TABLE 2-59: 2.5V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 2.3\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.60 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | -1 | 0.51 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | -2 | 0.45 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 6 mA | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | -1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | -2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 8 mA | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | -1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | -2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | Std. | 0.60 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | -1 | 0.51 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | -2 | 0.45 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | Std. | 0.60 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | -1 | 0.51 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | -2 | 0.45 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | Std. | 0.60 | 3.09 | 0.04 | 1.31 | 0.43 | 3.15 | 2.44 | 3.44 | 4.00 | 5.38 | 4.68 | ns |
| | -1 | 0.51 | 2.63 | 0.04 | 1.11 | 0.36 | 2.68 | 2.08 | 2.92 | 3.40 | 4.58 | 3.98 | ns |
| | -2 | 0.45 | 2.31 | 0.03 | 0.98 | 0.32 | 2.35 | 1.82 | 2.57 | 2.98 | 4.02 | 3.49 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-60: 2.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 2.3\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.60 | 11.40 | 0.04 | 1.31 | 0.43 | 11.22 | 11.40 | 2.68 | 2.20 | 13.45 | 13.63 | ns |
| | -1 | 0.51 | 9.69 | 0.04 | 1.11 | 0.36 | 9.54 | 9.69 | 2.28 | 1.88 | 11.44 | 11.60 | ns |
| | -2 | 0.45 | 8.51 | 0.03 | 0.98 | 0.32 | 8.38 | 8.51 | 2.00 | 1.65 | 10.05 | 10.18 | ns |
| 6 mA | Std. | 0.60 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | -1 | 0.51 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |
| | -2 | 0.45 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 8 mA | Std. | 0.60 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | -1 | 0.51 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |

TABLE 2-60: 2.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 2.3\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| | -2 | 0.45 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 12 mA | Std. | 0.60 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | -1 | 0.51 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | -2 | 0.45 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 16 mA | Std. | 0.60 | 5.76 | 0.04 | 1.31 | 0.43 | 5.87 | 5.53 | 3.36 | 3.44 | 8.11 | 7.76 | ns |
| | -1 | 0.51 | 4.90 | 0.04 | 1.11 | 0.36 | 4.99 | 4.70 | 2.86 | 2.92 | 6.90 | 6.60 | ns |
| | -2 | 0.45 | 4.30 | 0.03 | 0.98 | 0.32 | 4.38 | 4.13 | 2.51 | 2.57 | 6.05 | 5.80 | ns |
| 24 mA | Std. | 0.60 | 5.51 | 0.04 | 1.31 | 0.43 | 5.50 | 5.51 | 3.43 | 3.87 | 7.74 | 7.74 | ns |
| | -1 | 0.51 | 4.68 | 0.04 | 1.11 | 0.36 | 4.68 | 4.68 | 2.92 | 3.29 | 6.58 | 6.59 | ns |
| | -2 | 0.45 | 4.11 | 0.03 | 0.98 | 0.32 | 4.11 | 4.11 | 2.56 | 2.89 | 5.78 | 5.78 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-61: 2.5 V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$, WORST-CASE $V_{CCI} = 2.3\text{ V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 8.28 | 0.04 | 1.30 | 0.43 | 7.41 | 8.28 | 2.25 | 2.07 | 9.64 | 10.51 | ns |
| | -1 | 0.56 | 7.04 | 0.04 | 1.10 | 0.36 | 6.30 | 7.04 | 1.92 | 1.76 | 8.20 | 8.94 | ns |
| | -2 | 0.49 | 6.18 | 0.03 | 0.97 | 0.32 | 5.53 | 6.18 | 1.68 | 1.55 | 7.20 | 7.85 | ns |
| 6 mA | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 8 mA | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 12 mA | Std. | 0.66 | 3.21 | 0.04 | 1.30 | 0.43 | 3.27 | 3.14 | 2.82 | 3.11 | 5.50 | 5.38 | ns |
| | -1 | 0.56 | 2.73 | 0.04 | 1.10 | 0.36 | 2.78 | 2.67 | 2.40 | 2.65 | 4.68 | 4.57 | ns |
| | -2 | 0.49 | 2.39 | 0.03 | 0.97 | 0.32 | 2.44 | 2.35 | 2.11 | 2.32 | 4.11 | 4.02 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-62: 2.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 2.3\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 10.84 | 0.04 | 1.30 | 0.43 | 10.64 | 10.84 | 2.26 | 1.99 | 12.87 | 13.08 | ns |
| | -1 | 0.56 | 9.22 | 0.04 | 1.10 | 0.36 | 9.05 | 9.22 | 1.92 | 1.69 | 10.95 | 11.12 | ns |
| | -2 | 0.49 | 8.10 | 0.03 | 0.97 | 0.32 | 7.94 | 8.10 | 1.68 | 1.49 | 9.61 | 9.77 | ns |
| 6 mA | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | -1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | -2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 8 mA | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | -1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | -2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 12 mA | Std. | 0.66 | 5.63 | 0.04 | 1.30 | 0.43 | 5.73 | 5.51 | 2.83 | 3.01 | 7.97 | 7.74 | ns |
| | -1 | 0.56 | 4.79 | 0.04 | 1.10 | 0.36 | 4.88 | 4.68 | 2.41 | 2.56 | 6.78 | 6.59 | ns |
| | -2 | 0.49 | 4.20 | 0.03 | 0.97 | 0.32 | 4.28 | 4.11 | 2.11 | 2.25 | 5.95 | 5.78 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-63: 2.5V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 4 mA | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 6 mA | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 8 mA | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-64: 2.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|-------|
| 2 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | -1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | -2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 4 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | -1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | -2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 6 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | -1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | -2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |
| 8 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | -1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | -2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.4.4 1.8V LVCMOS

Low-voltage CMOS for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8V applications. It uses a 1.8V input buffer and a push-pull output buffer.

TABLE 2-65: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 1.8V LVCMOS | VIL | | VIH | | VOL | VOH | IO L | IO H | IOSL | IOSH | IIL ₁ | IIH ₂ |
|-------------|-------|-------------|-------------|-------|-------|-------------|------|------|---------------------|---------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | m A | m A | Max mA ³ | Max mA ³ | μA ₄ | μA ₄ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |

TABLE 2-65: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 1.8V LVCMOS | VIL | | VIH | | VOL | VOH | IO L | IO H | IOSL | IOSH | IIL ¹ | IIH ² |
|----------------|----------|-------------|-------------|----------|----------|-------------|---------|---------|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | m A | m A | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- Note 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- Note 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- Note 4:** Currents are measured at 85 °C junction temperature.
- Note 5:** Software default selection highlighted in gray.

TABLE 2-66: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O I/O BANKS

| 1.8V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|----------------|----------|-------------|-------------|----------|----------|-------------|--------|--------|------------------------|------------------------|------------------|------------------|
| | Min V | Max V | Min V | Max V | Max V | Min V | m A | m A | Max mA ³ | Max mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 8 | 8 | 44 | 35 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- Note 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- Note 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- Note 4:** Currents are measured at 85 °C junction temperature.
- Note 5:** Software default selection highlighted in gray.

**TABLE 2-67: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS
APPLICABLE TO STANDARD I/O BANKS**

| 1.8V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-------------------|-----------|-------------|-------------|-----------|-----------|-------------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-68: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 1.8 | 0.9 | 35 |

Note: *Measuring point = Vtrip. See [Table 2-22](#) for a complete table of trip points.

FIGURE 2-9: AC LOADING



2.3.4.4.1 Timing Characteristics

TABLE 2-69: 1.8 V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 11.86 | 0.04 | 1.22 | 0.43 | 9.14 | 11.86 | 2.77 | 1.66 | 11.37 | 14.10 | ns |
| | -1 | 0.56 | 10.09 | 0.04 | 1.04 | 0.36 | 7.77 | 10.09 | 2.36 | 1.41 | 9.67 | 11.99 | ns |
| | -2 | 0.49 | 8.86 | 0.03 | 0.91 | 0.32 | 6.82 | 8.86 | 2.07 | 1.24 | 8.49 | 10.53 | ns |
| 4 mA | Std. | 0.66 | 6.91 | 0.04 | 1.22 | 0.43 | 5.86 | 6.91 | 3.22 | 2.84 | 8.10 | 9.15 | ns |
| | -1 | 0.56 | 5.88 | 0.04 | 1.04 | 0.36 | 4.99 | 5.88 | 2.74 | 2.41 | 6.89 | 7.78 | ns |
| | -2 | 0.49 | 5.16 | 0.03 | 0.91 | 0.32 | 4.38 | 5.16 | 2.41 | 2.12 | 6.05 | 6.83 | ns |
| 6 mA | Std. | 0.66 | 4.45 | 0.04 | 1.22 | 0.43 | 4.18 | 4.45 | 3.53 | 3.38 | 6.42 | 6.68 | ns |
| | -1 | 0.56 | 3.78 | 0.04 | 1.04 | 0.36 | 3.56 | 3.78 | 3.00 | 2.88 | 5.46 | 5.69 | ns |
| | -2 | 0.49 | 3.32 | 0.03 | 0.91 | 0.32 | 3.12 | 3.32 | 2.64 | 2.53 | 4.79 | 4.99 | ns |
| 8 mA | Std. | 0.66 | 3.92 | 0.04 | 1.22 | 0.43 | 3.93 | 3.92 | 3.60 | 3.52 | 6.16 | 6.16 | ns |
| | -1 | 0.56 | 3.34 | 0.04 | 1.04 | 0.36 | 3.34 | 3.34 | 3.06 | 3.00 | 5.24 | 5.24 | ns |
| | -2 | 0.49 | 2.93 | 0.03 | 0.91 | 0.32 | 2.93 | 2.93 | 2.69 | 2.63 | 4.60 | 4.60 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | -1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | -1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-70: 1.8V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 15.53 | 0.04 | 1.22 | 0.43 | 14.11 | 15.53 | 2.78 | 1.60 | 16.35 | 17.77 | ns |
| | -1 | 0.56 | 13.21 | 0.04 | 1.04 | 0.36 | 12.01 | 13.21 | 2.36 | 1.36 | 13.91 | 15.11 | ns |
| | -2 | 0.49 | 11.60 | 0.03 | 0.91 | 0.32 | 10.54 | 11.60 | 2.07 | 1.19 | 12.21 | 13.27 | ns |
| 4 mA | Std. | 0.66 | 10.48 | 0.04 | 1.22 | 0.43 | 10.41 | 10.48 | 3.23 | 2.73 | 12.65 | 12.71 | ns |
| | -1 | 0.56 | 8.91 | 0.04 | 1.04 | 0.36 | 8.86 | 8.91 | 2.75 | 2.33 | 10.76 | 10.81 | ns |
| | -2 | 0.49 | 7.82 | 0.03 | 0.91 | 0.32 | 7.77 | 7.82 | 2.41 | 2.04 | 9.44 | 9.49 | ns |
| 6 mA | Std. | 0.66 | 8.05 | 0.04 | 1.22 | 0.43 | 8.20 | 7.84 | 3.54 | 3.27 | 10.43 | 10.08 | ns |
| | -1 | 0.56 | 6.85 | 0.04 | 1.04 | 0.36 | 6.97 | 6.67 | 3.01 | 2.78 | 8.88 | 8.57 | ns |

TABLE 2-70: 1.8V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 8 mA | –2 | 0.49 | 6.01 | 0.03 | 0.91 | 0.32 | 6.12 | 5.86 | 2.64 | 2.44 | 7.79 | 7.53 | ns |
| | Std. | 0.66 | 7.50 | 0.04 | 1.22 | 0.43 | 7.64 | 7.30 | 3.61 | 3.41 | 9.88 | 9.53 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.04 | 0.36 | 6.50 | 6.21 | 3.07 | 2.90 | 8.40 | 8.11 | ns |
| 12 mA | –2 | 0.49 | 5.60 | 0.03 | 0.91 | 0.32 | 5.71 | 5.45 | 2.69 | 2.55 | 7.38 | 7.12 | ns |
| | Std. | 0.66 | 7.29 | 0.04 | 1.22 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | –1 | 0.56 | 6.20 | 0.04 | 1.04 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| 16 mA | –2 | 0.49 | 5.45 | 0.03 | 0.91 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |
| | Std. | 0.66 | 7.29 | 0.04 | 1.22 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | –1 | 0.56 | 6.20 | 0.04 | 1.04 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| | –2 | 0.49 | 5.45 | 0.03 | 0.91 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-71: 1.8V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 11.33 | 0.04 | 1.20 | 0.43 | 8.72 | 11.33 | 2.24 | 1.52 | 10.96 | 13.57 | ns |
| | –1 | 0.56 | 9.64 | 0.04 | 1.02 | 0.36 | 7.42 | 9.64 | 1.91 | 1.29 | 9.32 | 11.54 | ns |
| | –2 | 0.49 | 8.46 | 0.03 | 0.90 | 0.32 | 6.51 | 8.46 | 1.68 | 1.14 | 8.18 | 10.13 | ns |
| 4 mA | Std. | 0.66 | 6.48 | 0.04 | 1.20 | 0.43 | 5.48 | 6.48 | 2.65 | 2.60 | 7.72 | 8.72 | ns |
| | –1 | 0.56 | 5.51 | 0.04 | 1.02 | 0.36 | 4.66 | 5.51 | 2.25 | 2.21 | 6.56 | 7.42 | ns |
| | –2 | 0.49 | 4.84 | 0.03 | 0.90 | 0.32 | 4.09 | 4.84 | 1.98 | 1.94 | 5.76 | 6.51 | ns |
| 6 mA | Std. | 0.66 | 4.06 | 0.04 | 1.20 | 0.43 | 3.84 | 4.06 | 2.93 | 3.10 | 6.07 | 6.30 | ns |
| | –1 | 0.56 | 3.45 | 0.04 | 1.02 | 0.36 | 3.27 | 3.45 | 2.49 | 2.64 | 5.17 | 5.36 | ns |
| | –2 | 0.49 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |
| 8 mA | Std. | 0.66 | 4.06 | 0.04 | 1.20 | 0.43 | 3.84 | 4.06 | 2.93 | 3.10 | 6.07 | 6.30 | ns |
| | –1 | 0.56 | 3.45 | 0.04 | 1.02 | 0.36 | 3.27 | 3.45 | 2.49 | 2.64 | 5.17 | 5.36 | ns |
| | –2 | 0.49 | 3.03 | 0.03 | 0.90 | 0.32 | 2.87 | 3.03 | 2.19 | 2.32 | 4.54 | 4.70 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-72: 1.8V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 14.80 | 0.04 | 1.20 | 0.43 | 13.49 | 14.80 | 2.25 | 1.46 | 15.73 | 17.04 | ns |
| | -1 | 0.56 | 12.59 | 0.04 | 1.02 | 0.36 | 11.48 | 12.59 | 1.91 | 1.25 | 13.38 | 14.49 | ns |
| | -2 | 0.49 | 11.05 | 0.03 | 0.90 | 0.32 | 10.08 | 11.05 | 1.68 | 1.09 | 11.75 | 12.72 | ns |
| 4 mA | Std. | 0.66 | 9.90 | 0.04 | 1.20 | 0.43 | 9.73 | 9.90 | 2.65 | 2.50 | 11.97 | 12.13 | ns |
| | -1 | 0.56 | 8.42 | 0.04 | 1.02 | 0.36 | 8.28 | 8.42 | 2.26 | 2.12 | 10.18 | 10.32 | ns |
| | -2 | 0.49 | 7.39 | 0.03 | 0.90 | 0.32 | 7.27 | 7.39 | 1.98 | 1.86 | 8.94 | 9.06 | ns |
| 6 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | -1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | -2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |
| 8 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | -1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | -2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-73: 1.8V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.7\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 11.21 | 0.04 | 1.20 | 0.43 | 8.53 | 11.21 | 1.99 | 1.21 | ns |
| | -1 | 0.56 | 9.54 | 0.04 | 1.02 | 0.36 | 7.26 | 9.54 | 1.69 | 1.03 | ns |
| | -2 | 0.49 | 8.37 | 0.03 | 0.90 | 0.32 | 6.37 | 8.37 | 1.49 | 0.90 | ns |
| 4 mA | Std. | 0.66 | 6.34 | 0.04 | 1.20 | 0.43 | 5.38 | 6.34 | 2.41 | 2.48 | ns |
| | -1 | 0.56 | 5.40 | 0.04 | 1.02 | 0.36 | 4.58 | 5.40 | 2.05 | 2.11 | ns |
| | -2 | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-74: 1.8V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 15.01 | 0.04 | 1.20 | 0.43 | 13.15 | 15.01 | 1.99 | 1.99 | ns |
| | -1 | 0.56 | 12.77 | 0.04 | 1.02 | 0.36 | 11.19 | 12.77 | 1.70 | 1.70 | ns |
| | -2 | 0.49 | 11.21 | 0.03 | 0.90 | 0.32 | 9.82 | 11.21 | 1.49 | 1.49 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-74: 1.8V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 4 mA | Std. | 0.66 | 10.10 | 0.04 | 1.20 | 0.43 | 9.55 | 10.10 | 2.41 | 2.37 | ns |
| | -1 | 0.56 | 8.59 | 0.04 | 1.02 | 0.36 | 8.13 | 8.59 | 2.05 | 2.02 | ns |
| | -2 | 0.49 | 7.54 | 0.03 | 0.90 | 0.32 | 7.13 | 7.54 | 1.80 | 1.77 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.4.5 1.5V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5V applications. It uses a 1.5V input buffer and a push-pull output buffer.

TABLE 2-75: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IO L | IO H | IOSL | IOSH | IIL ₁ | IIH ₂ |
|--------------|--------|-------------|-------------|---------|-------------|-------------|------|------|----------------------|----------------------|----------------------------|----------------------------|
| | Min. V | Max. V | Min. V | Max., V | Max. V | Min. V | m A | m A | Max. mA ³ | Max. mA ³ | μA ₄ | μA ₄ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{V} < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-76: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD PLUS I/O BANKS

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IO L | IO H | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------|-----------|----------------|-------------|-----------|----------------|----------------|---------|---------|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | m A | m A | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-77: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO STANDARD I/O BANKS

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IO H | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------|-----------|-------------|----------------|-----------|-------------|----------------|--------|---------|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | m A | m A | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |

- Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3 V < V_{IN} < V_{IL}$.
- 2:** IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- 3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
- 4:** Currents are measured at 85 °C junction temperature.
- 5:** Software default selection highlighted in gray.

TABLE 2-78: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|------------------------|
| 0 | 1.5 | 0.75 | 35 |

Note: *Measuring point = V_{trip} . See [Table 2-22](#) for a complete table of trip points.

FIGURE 2-10: AC LOADING



2.3.4.5.1 Timing Characteristics

TABLE 2-79: 1.5 V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE VCC = 1.425 V, WORST-CASE VCCI = 1.4 V APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
| | -1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
| | -2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
| | -1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
| | -2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 6 mA | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
| | -1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
| | -2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 8 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | -1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | -2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 12 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | -1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | -2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-80: 1.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.4V APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 12.78 | 0.04 | 1.44 | 0.43 | 12.81 | 12.78 | 3.40 | 2.64 | 15.05 | 15.02 | ns |
| | -1 | 0.56 | 10.87 | 0.04 | 1.22 | 0.36 | 10.90 | 10.87 | 2.89 | 2.25 | 12.80 | 12.78 | ns |
| | -2 | 0.49 | 9.55 | 0.03 | 1.07 | 0.32 | 9.57 | 9.55 | 2.54 | 1.97 | 11.24 | 11.22 | ns |
| 4 mA | Std. | 0.66 | 10.01 | 0.04 | 1.44 | 0.43 | 10.19 | 9.55 | 3.75 | 3.27 | 12.43 | 11.78 | ns |

TABLE 2-80: 1.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.4\text{V}$ APPLICABLE TO ADVANCED I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| | -1 | 0.56 | 8.51 | 0.04 | 1.22 | 0.36 | 8.67 | 8.12 | 3.19 | 2.78 | 10.57 | 10.02 | ns |
| | -2 | 0.49 | 7.47 | 0.03 | 1.07 | 0.32 | 7.61 | 7.13 | 2.80 | 2.44 | 9.28 | 8.80 | ns |
| 6 mA | Std. | 0.66 | 9.33 | 0.04 | 1.44 | 0.43 | 9.51 | 8.89 | 3.83 | 3.43 | 11.74 | 11.13 | ns |
| | -1 | 0.56 | 7.94 | 0.04 | 1.22 | 0.36 | 8.09 | 7.56 | 3.26 | 2.92 | 9.99 | 9.47 | ns |
| | -2 | 0.49 | 6.97 | 0.03 | 1.07 | 0.32 | 7.10 | 6.64 | 2.86 | 2.56 | 8.77 | 8.31 | ns |
| 8 mA | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | -1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | -2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |
| 12 mA | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | -1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | -2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-81: 1.5V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.4\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 7.83 | 0.04 | 1.42 | 0.43 | 6.42 | 7.83 | 2.71 | 2.55 | 8.65 | 10.07 | ns |
| | -1 | 0.56 | 6.66 | 0.04 | 1.21 | 0.36 | 5.46 | 6.66 | 2.31 | 2.17 | 7.36 | 8.56 | ns |
| | -2 | 0.49 | 5.85 | 0.03 | 1.06 | 0.32 | 4.79 | 5.85 | 2.02 | 1.90 | 6.46 | 7.52 | ns |
| 4 mA | Std. | 0.66 | 4.84 | 0.04 | 1.42 | 0.43 | 4.49 | 4.84 | 3.03 | 3.13 | 6.72 | 7.08 | ns |
| | -1 | 0.56 | 4.12 | 0.04 | 1.21 | 0.36 | 3.82 | 4.12 | 2.58 | 2.66 | 5.72 | 6.02 | ns |
| | -2 | 0.49 | 3.61 | 0.03 | 1.06 | 0.32 | 3.35 | 3.61 | 2.26 | 2.34 | 5.02 | 5.28 | ns |

Note 1: Software default selection highlighted in gray.

Note 2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-82: 1.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.4\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 12.08 | 0.04 | 1.42 | 0.43 | 12.01 | 12.08 | 2.72 | 2.43 | 14.24 | 14.31 | ns |
| | -1 | 0.56 | 10.27 | 0.04 | 1.21 | 0.36 | 10.21 | 10.27 | 2.31 | 2.06 | 12.12 | 12.18 | ns |
| | -2 | 0.49 | 9.02 | 0.03 | 1.06 | 0.32 | 8.97 | 9.02 | 2.03 | 1.81 | 10.64 | 10.69 | ns |
| 4 mA | Std. | 0.66 | 9.28 | 0.04 | 1.42 | 0.43 | 9.45 | 8.91 | 3.04 | 3.00 | 11.69 | 11.15 | ns |

TABLE 2-82: 1.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 1.4\text{V}$ APPLICABLE TO STANDARD PLUS I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| | -1 | 0.56 | 7.89 | 0.04 | 1.21 | 0.36 | 8.04 | 7.58 | 2.58 | 2.55 | 9.94 | 9.49 | ns |
| | -2 | 0.49 | 6.93 | 0.03 | 1.06 | 0.32 | 7.06 | 6.66 | 2.27 | 2.24 | 8.73 | 8.33 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-83: 1.5V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 7.65 | 0.04 | 1.42 | 0.43 | 6.31 | 7.65 | 2.45 | 2.45 | ns |
| | -1 | 0.56 | 6.50 | 0.04 | 1.21 | 0.36 | 5.37 | 6.50 | 2.08 | 2.08 | ns |
| | -2 | 0.49 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-84: 1.5V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$, WORST-CASE $V_{CCI} = 3.0\text{V}$ APPLICABLE TO STANDARD I/O BANKS

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 12.33 | 0.04 | 1.42 | 0.43 | 11.79 | 12.33 | 2.45 | 2.32 | ns |
| | -1 | 0.56 | 10.49 | 0.04 | 1.21 | 0.36 | 10.03 | 10.49 | 2.08 | 1.98 | ns |
| | -2 | 0.49 | 9.21 | 0.03 | 1.06 | 0.32 | 8.81 | 9.21 | 1.83 | 1.73 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.4.6 3.3V PCI, 3.3V PCI-X

Peripheral Component Interface for 3.3V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

TABLE 2-85: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IO L | IO H | IOSL | IOSH | IIL | IIH |
|-----------------------|----------------|--------|--------|--------|--------|--------|------|------|----------------------|----------------------|----------------------------|----------------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | m A | m A | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Note 1: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

2: Currents are measured at 85 °C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microchip loadings for enable path characterization are described in [Figure 2-11](#).

FIGURE 2-11: AC LOADING



AC loadings are defined per PCI/PCI-X specifications for the datapath; Microchip loading for tristate is described in [Table 2-86](#).

TABLE 2-86: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) | C_{LOAD} (pF) |
|---------------|----------------|--|-----------------|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$ | 10 |

Note: *Measuring point = V_{trip} . See [Table 2-22](#) for a complete table of trip points.

2.3.4.6.1 Timing Characteristics

TABLE 2-87: 3.3V PCI/PCI-X COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO ADVANCED I/O BANKS

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | ns |
| -1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | ns |
| -2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-88: 3.3V PCI/PCI-X COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V APPLICABLE TO STANDARD PLUS I/O BANKS

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.66 | 2.31 | 0.04 | 0.85 | 0.43 | 2.35 | 1.70 | 2.79 | 3.22 | 4.59 | 3.94 | ns |
| -1 | 0.56 | 1.96 | 0.04 | 0.72 | 0.36 | 2.00 | 1.45 | 2.37 | 2.74 | 3.90 | 3.35 | ns |
| -2 | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.5 DIFFERENTIAL I/O CHARACTERISTICS

2.3.5.1 Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microchip Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

2.3.5.2 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-12](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC 3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

TABLE 2-89: LVDS MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|--------------------|-----------------------------|-------|-------|-------|-------|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL ¹ | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH ¹ | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH ^{2,3} | Input High Leakage Current | — | — | 10 | μA |
| IIL ^{2,4} | Input Low Leakage Current | — | — | 10 | μA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

Note 1: IOL/IOH defined by VODIFF/(Resistor Network)

2: Currents are measured at 85 °C junction temperature.

3: IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.

4: IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < V_{IN} < V_{IL}$.

TABLE 2-90: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---------------|----------------|----------------------|
| 1.075 | 1.325 | Cross point |

Note: *Measuring point = V_{trip} . See [Table 2-22](#) for a complete table of trip points.

FIGURE 2-12: LVDS CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION



2.3.5.2.1 Timing Characteristics

TABLE 2-91: LVDS COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$, WORST-CASE $V_{CCI} = 2.3\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 1.83 | 0.04 | 1.60 | ns |
| -1 | 0.56 | 1.56 | 0.04 | 1.36 | ns |
| -2 | 0.49 | 1.37 | 0.03 | 1.20 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.5.3 B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microchip LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microchip LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-13](#). The input and output buffer delays are available in the LVDS section in [Table 2-91](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

FIGURE 2-13: B-LVDS/M-LVDS MULTIPOINT APPLICATION USING LVDS I/O BUFFERS



2.3.5.4 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-14](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

FIGURE 2-14: LVPECL CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION



TABLE 2-92: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|--------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | — | 300 | — | 300 | — | mV |

TABLE 2-93: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---------------|----------------|----------------------|
| 1.64 | 1.94 | Cross point |

Note: *Measuring point = V_{trip} . See [Table 2-22](#) for a complete table of trip points.

2.3.5.4.1 Timing Characteristics

TABLE 2-94: LVPECL COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$, WORST-CASE $V_{CCI} = 3.0\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 1.80 | 0.04 | 1.40 | ns |
| -1 | 0.56 | 1.53 | 0.04 | 1.19 | ns |
| -2 | 0.49 | 1.34 | 0.03 | 1.05 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.6 I/O REGISTER SPECIFICATIONS

2.3.6.1 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

TABLE 2-95: PARAMETER DEFINITION AND MEASURING NODES

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|--|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | H, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | F, H |
| t_{OHD} | Data Hold Time for the Output Data Register | F, H |
| t_{OSUE} | Enable Setup Time for the Output Data Register | G, H |
| t_{OHE} | Enable Hold Time for the Output Data Register | G, H |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | H, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | J, H |
| t_{OEHD} | Data Hold Time for the Output Enable Register | J, H |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | K, H |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | K, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| t_{iCLKQ} | Clock-to-Q of the Input Data Register | A, E |
| t_{iSUD} | Data Setup Time for the Input Data Register | C, A |
| t_{iHD} | Data Hold Time for the Input Data Register | C, A |
| t_{iSUE} | Enable Setup Time for the Input Data Register | B, A |
| t_{iHE} | Enable Hold Time for the Input Data Register | B, A |
| t_{iPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{iREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{iRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

Note: *See [Figure 2-15](#) for more information.

FIGURE 2-15: TIMING MODEL OF REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS PRESET



2.3.6.2 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

TABLE 2-96: PARAMETER DEFINITION AND MEASURING NODES

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------------|---|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | HH, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | FF, HH |
| t_{OHD} | Data Hold Time for the Output Data Register | FF, HH |
| t_{OSUE} | Enable Setup Time for the Output Data Register | GG, HH |
| t_{OHE} | Enable Hold Time for the Output Data Register | GG, HH |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| t_{OREMCLR} | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| t_{ORECCLR} | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | HH, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | JJ, HH |
| t_{OEHD} | Data Hold Time for the Output Enable Register | JJ, HH |

TABLE 2-96: PARAMETER DEFINITION AND MEASURING NODES

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|---|-----------------------------|
| t_{OESUE} | Enable Setup Time for the Output Enable Register | KK, HH |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| t_{iCLKQ} | Clock-to-Q of the Input Data Register | AA, EE |
| t_{iSUD} | Data Setup Time for the Input Data Register | CC, AA |
| t_{iHD} | Data Hold Time for the Input Data Register | CC, AA |
| t_{iSUE} | Enable Setup Time for the Input Data Register | BB, AA |
| t_{iHE} | Enable Hold Time for the Input Data Register | BB, AA |
| t_{iCLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{iREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{iRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See [Figure 2-16](#) for more information.

FIGURE 2-16: TIMING MODEL OF THE REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS CLEAR



2.3.6.4 Output Register

FIGURE 2-18: OUTPUT REGISTER TIMING DIAGRAM



2.3.6.4.1 Timing Characteristics

TABLE 2-98: OUTPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE
CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 0.59 | 0.67 | 0.79 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 0.44 | 0.50 | 0.59 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OCLKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OCLKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.6.5 Output Enable Register

FIGURE 2-19: OUTPUT ENABLE REGISTER TIMING DIAGRAM



2.3.6.5.1 Timing Characteristics

**TABLE 2-99: OUTPUT ENABLE REGISTER PROPAGATION DELAYS COMMERCIAL-CASE
CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$**

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 0.59 | 0.67 | 0.79 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWCCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWPRES}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.37 | 0.43 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.3.7 DDR MODULE SPECIFICATIONS

2.3.7.1 Input DDR Module

TABLE 2-100: PARAMETER DEFINITIONS

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|------------------------------|----------------------------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| t_{DDRIHD} | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

FIGURE 2-20: INPUT DDR TIMING MODEL



FIGURE 2-21: INPUT DDR TIMING DIAGRAM



2.3.7.1.1 Timing Characteristics

TABLE 2-101: INPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST CASE $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------------|--|------|------|------|-------|
| t_{DDRICKQ1} | Clock-to-Out Out_QR for Input DDR | 0.27 | 0.31 | 0.37 | ns |
| t_{DDRICKQ2} | Clock-to-Out Out_QF for Input DDR | 0.39 | 0.44 | 0.52 | ns |
| t_{DDRISUD} | Data Setup for Input DDR (Fall) | 0.25 | 0.28 | 0.33 | ns |
| | Data Setup for Input DDR (Rise) | 0.25 | 0.28 | 0.33 | ns |
| t_{DDRIHD} | Data Hold for Input DDR (Fall) | 0.00 | 0.00 | 0.00 | ns |
| | Data Hold for Input DDR (Rise) | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRICLR2Q1}}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.46 | 0.53 | 0.62 | ns |
| $t_{\text{DDRICLR2Q2}}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.57 | 0.65 | 0.76 | ns |
| $t_{\text{DDRIREMCLR}}$ | Asynchronous Clear Removal time for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRIRECCLR}}$ | Asynchronous Clear Recovery time for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDR IWCLR}}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDRICKMPWH}}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDRIMAX} | Maximum Frequency for Input DDR | 350 | 309 | 263 | MHz |

Note: For specific junction temperature and voltage-supply levels, refer to [Table 2-6](#) for derating values.

2.3.7.2 Output DDR Module

TABLE 2-102: PARAMETER DEFINITIONS

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|-------------------------|---------------------------|----------------------------|
| t_{DDROCLKQ} | Clock-to-Out | B, E |
| $t_{\text{DDROCLR2Q}}$ | Asynchronous Clear-to-Out | C, E |
| $t_{\text{DDROREMCLR}}$ | Clear Removal | C, B |
| $t_{\text{DDRORECCLR}}$ | Clear Recovery | C, B |
| t_{DDROSUD1} | Data Setup Data_F | A, B |
| t_{DDROSUD2} | Data Setup Data_R | D, B |
| t_{DDROHD1} | Data Hold Data_F | A, B |
| t_{DDROHD2} | Data Hold Data_R | D, B |

FIGURE 2-22: OUTPUT DDR TIMING MODEL



FIGURE 2-23: OUTPUT DDR TIMING DIAGRAM



2.3.7.2.1 Timing Characteristics

TABLE 2-103: OUTPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------------|---|------|------|------|-------|
| t_{DDROCLKQ} | Clock-to-Out of DDR for Output DDR | 0.70 | 0.80 | 0.94 | ns |
| t_{DDROSUD1} | Data_F Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| t_{DDROSUD2} | Data_R Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| t_{DDROHD1} | Data_F Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| t_{DDROHD2} | Data_R Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDROCLR2Q}}$ | Asynchronous Clear-to-Out for Output DDR | 0.80 | 0.91 | 1.07 | ns |
| $t_{\text{DDROREMCLR}}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRORECCLR}}$ | Asynchronous Clear Recovery Time for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDROWCLR1}}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDROCKMPWH}}$ | Clock Minimum Pulse Width High for the Output DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{\text{DDROCKMPWL}}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | 350 | 309 | 263 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.4 VersaTile Characteristics

2.4.1 VERSATILE SPECIFICATIONS AS A COMBINATORIAL MODULE

The ProASIC 3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [Fusion, IGLOO®/e, and ProASIC 3/E Macro Library Guide](#).

FIGURE 2-24: SAMPLE OF COMBINATORIAL CELLS



FIGURE 2-25: TIMING MODEL AND WAVEFORMS



2.4.1.1 Timing Characteristics

TABLE 2-104: COMBINATORIAL CELL PROPAGATION DELAYS COMMERCIAL-CASE
CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$

| Combinatorial Cell | Equation | Parameter | -2 | -1 | Std. | Units |
|--------------------|-----------------------------------|-----------|------|------|------|-------|
| INV | $Y = !A$ | t_{PD} | 0.40 | 0.46 | 0.54 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | $Y = A \text{ IS } + B \text{ S}$ | t_{PD} | 0.51 | 0.58 | 0.68 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 0.56 | 0.64 | 0.75 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.4.2 VERSATILE SPECIFICATIONS AS A SEQUENTIAL MODULE

The ProASIC 3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion, IGLOO/e, and ProASIC 3/E Macro Library Guide](#).

FIGURE 2-26: SAMPLE OF SEQUENTIAL CELLS



2.4.2.1 Timing Characteristics

FIGURE 2-27: TIMING MODEL AND WAVEFORMS



TABLE 2-105: REGISTER DELAYS COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|--------------|---|------|------|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECCLR} | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

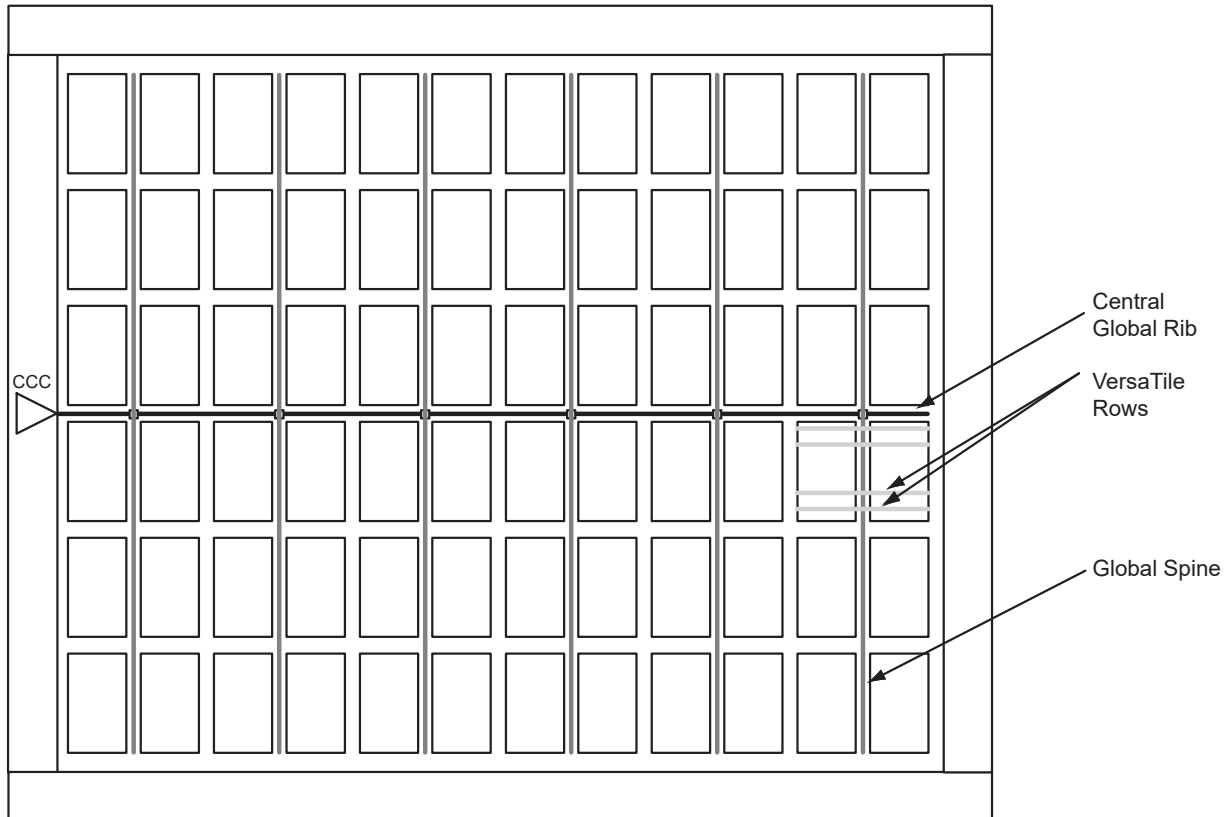
Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.5 Global Resource Characteristics

2.5.1 A3P250 CLOCK TREE TOPOLOGY

Clock delays are device-specific. [Figure 2-28](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-28](#) is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

FIGURE 2-28: EXAMPLE OF GLOBAL TREE USE IN AN A3P250 DEVICE FOR CLOCK ROUTING



2.5.2 GLOBAL TREE TIMING CHARACTERISTICS

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the [Section 2.6 Clock Conditioning Circuits](#). [Table 2-106](#) to [Table 2-112](#) present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

2.5.2.1 Timing Characteristics

TABLE 2-106: A3P030 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Unit s |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-----------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.67 | 0.81 | 0.76 | 0.92 | 0.89 | 1.09 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.68 | 0.85 | 0.77 | 0.97 | 0.91 | 1.14 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.18 | — | 0.21 | — | 0.24 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-107: A3P060 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Unit s |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-----------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.71 | 0.93 | 0.81 | 1.05 | 0.95 | 1.24 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.70 | 0.96 | 0.80 | 1.09 | 0.94 | 1.28 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.34 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-108: A3P125 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Unit s |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-----------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.77 | 0.99 | 0.87 | 1.12 | 1.03 | 1.32 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.76 | 1.02 | 0.87 | 1.16 | 1.02 | 1.37 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |

TABLE 2-108: A3P125 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|--|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.34 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-109: A3P250 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.80 | 1.01 | 0.91 | 1.15 | 1.07 | 1.36 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.78 | 1.04 | 0.89 | 1.18 | 1.04 | 1.39 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.34 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-110: A3P400 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.87 | 1.09 | 0.99 | 1.24 | 1.17 | 1.46 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.86 | 1.11 | 0.98 | 1.27 | 1.15 | 1.49 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.34 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-111: A3P600 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.87 | 1.09 | 0.99 | 1.24 | 1.17 | 1.46 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.86 | 1.11 | 0.98 | 1.27 | 1.15 | 1.49 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.34 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-112: A3P1000 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.94 | 1.16 | 1.07 | 1.32 | 1.26 | 1.55 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.93 | 1.19 | 1.06 | 1.35 | 1.24 | 1.59 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | — | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 0.96 | — | 1.13 | — | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | — | 0.26 | — | 0.29 | — | 0.35 | ns |

- Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Note 2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- Note 3:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.6 Clock Conditioning Circuits

2.6.1 CCC ELECTRICAL SPECIFICATIONS

2.6.1.1 Timing Characteristics

TABLE 2-113: PROASIC 3 CCC/PLL SPECIFICATION

| Parameter | Minimum | Typical | Maximum | Units |
|--|--------------------------------|------------------|------------------------|---------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | — | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | — | 350 | MHz |
| Serial Clock (SCLK) for Dynamic PLL ¹ | — | — | 125 | MHz |
| Delay Increments in Programmable Delay Blocks ^{2, 3} | — | 200 ⁴ | — | ps |
| Number of Programmable Values in Each Programmable Delay Block | — | — | 32 | — |
| Input Period Jitter | — | — | 1.5 | ns |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | — | 0.70% | — |
| 24 MHz to 100 MHz | 1.00% | — | 1.20% | — |
| 100 MHz to 250 MHz | 1.75% | — | 2.00% | — |
| 250 MHz to 350 MHz | 2.50% | — | 5.60% | — |
| Acquisition Time | — | — | — | — |
| (A3P250 and A3P1000 only)LockControl = 0 | — | — | 300 | μ s |
| LockControl = 1 | — | — | 300 | μ s |
| (all other dies)LockControl = 0 | — | — | 300 | μ s |
| LockControl = 1 | — | — | 6.0 | ms |
| Tracking Jitter ⁵ | — | — | — | — |
| (A3P250 and A3P1000 only)LockControl = 0 | — | — | 1.6 | ns |
| LockControl = 1 | — | — | 1.6 | ns |
| (all other dies)LockControl = 0 | — | — | 1.6 | ns |
| LockControl = 1 | — | — | 0.8 | ns |
| Output Duty Cycle | 48.5 | — | 51.5 | % |
| Delay Range in Block: Programmable Delay ^{1, 2, 3} | 0.6 | — | 5.56 | ns |

TABLE 2-113: PROASIC 3 CCC/PLL SPECIFICATION

| Parameter | Minimum | Typical | Maximum | Units |
|--|---------|---------|---------|-------|
| Delay Range in Block: Programmable Delay ^{2, 3} | 0.225 | — | 5.56 | ns |
| Delay Range in Block: Fixed Delay ^{2, 3} | — | 2.2 | — | ns |

- Note 1:** Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.
- 2:** This delay is a function of voltage and temperature. See [Table 2-6](#) for deratings.
- 3:** $T_J = 25\text{ }^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
- 4:** When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.
- 5:** Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
- 6:** The A3P030 device does not contain a PLL.

FIGURE 2-29: PEAK-TO-PEAK JITTER DEFINITION

Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

2.7 Embedded SRAM and FIFO Characteristics

2.7.1 SRAM

FIGURE 2-30: RAM MODELS



2.7.1.1 Timing Waveforms

FIGURE 2-31: RAM READ FOR PASS-THROUGH OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.



FIGURE 2-32: RAM READ FOR PIPELINED OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.



FIGURE 2-33: RAM WRITE, OUTPUT RETAINED. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.



FIGURE 2-34: RAM WRITE, OUTPUT AS WRITE DATA (WMODE = 1). APPLICABLE TO RAM4K9 ONLY.



FIGURE 2-35: RAM RESET. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.



2.7.1.2 Timing Characteristics

TABLE 2-114: RAM4K9 COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| t_{ENH} | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| t_{BKS} | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| t_{BKH} | BLK hold time | 0.02 | 0.02 | 0.02 | ns |
| t_{DS} | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.36 | 2.68 | 3.15 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 1.79 | 2.03 | 2.39 | ns |
| t_{CKQ2} | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t_{C2CWWL}^1 | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge | 0.33 | 0.28 | 0.25 | ns |
| t_{C2CWWH}^1 | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| t_{RSTBQ} | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |

TABLE 2-114: RAM4K9 COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$ (CONTINUED)

| Parameter | Description | -2 | -1 | Std. | Units |
|-----------|-------------------|------|------|------|-------|
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

- Note 1:** For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
- 2:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-115: RAM512X18 COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.13 | 0.15 | 0.17 | ns |
| t_{ENH} | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| t_{DS} | Input data (WD) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (WD) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on RD (output retained) | 2.16 | 2.46 | 2.89 | ns |
| t_{CKQ2} | Clock High to new data valid on RD (pipelined) | 0.90 | 1.02 | 1.20 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.50 | 0.43 | 0.38 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.59 | 0.50 | 0.44 | ns |
| t_{RSTBQ} | RESET Low to data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

- Note 1:** For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
- 2:** For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

2.7.2 FIFO

FIGURE 2-36: FIFO MODEL



2.7.2.1 Timing Waveforms

FIGURE 2-37: FIFO READ



FIGURE 2-38: FIFO WRITE



FIGURE 2-39: FIFO RESET



FIGURE 2-40: FIFO EMPTY FLAG AND AEMPTY FLAG ASSERTION



FIGURE 2-41: FIFO FULL FLAG AND AFULL FLAG ASSERTION



FIGURE 2-42: FIFO EMPTY FLAG AND AEMPTY FLAG DEASSERTION



FIGURE 2-43: FIFO FULL FLAG AND AFULL FLAG DEASSERTION



2.7.2.2 Timing Characteristics

**TABLE 2-116: FIFO (FOR ALL DIES EXCEPT A3P250) WORST COMMERCIAL-CASE CONDITIONS:
T_J = 70 °C, VCC = 1.425V**

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------|---|------|------|------|-------|
| t _{ENS} | REN, WEN Setup Time | 1.34 | 1.52 | 1.79 | ns |
| t _{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t _{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t _{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| t _{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| t _{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t _{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t _{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t _{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t _{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t _{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| t _{REMRSTB} | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| t _{RECRSTB} | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| t _{MPWRSTB} | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t _{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F _{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

TABLE 2-117: FIFO (FOR A3P250 ONLY, ASPECT-RATIO-DEPENDENT) WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

| Parameter | Description | -2 | -1 | Std. | Units |
|--------------------|---|------|------|------|-------|
| t _{ENS} | REN, WEN Setup Time | 3.26 | 3.71 | 4.36 | ns |
| t _{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t _{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t _{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| t _{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| t _{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t _{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |

TABLE 2-117: FIFO (FOR A3P250 ONLY, ASPECT-RATIO-DEPENDENT) WORST COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|--|------|------|------|-------|
| t_{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t_{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t_{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

TABLE 2-118: A3P250 FIFO 512 × 8 WORST COMMERCIAL-CASE CONDITIONS: $T_J = 70\text{ }^\circ\text{C}$, $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|---|------|------|------|-------|
| t_{ENS} | REN, WEN Setup Time | 3.75 | 4.27 | 5.02 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t_{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| t_{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| t_{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t_{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t_{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t_{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t_{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

TABLE 2-119: A3P250 FIFO 1K×4 WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------|---|------|------|------|-------|
| t _{ENS} | REN, WEN Setup Time | 4.05 | 4.61 | 5.42 | ns |
| t _{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t _{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t _{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| t _{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t _{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t _{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t _{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t _{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t _{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t _{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| t _{REMRSTB} | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| t _{RECRSTB} | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| t _{MPWRSTB} | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t _{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F _{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

TABLE 2-120: A3P250 FIFO 2K×2 WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

| Parameter | Description | -2 | -1 | Std. | Units |
|--------------------|---|------|------|------|-------|
| t _{ENS} | REN, WEN Setup Time | 4.39 | 5.00 | 5.88 | ns |
| t _{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t _{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t _{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| t _{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t _{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t _{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t _{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t _{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t _{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |

TABLE 2-120: A3P250 FIFO 2K×2 WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------|--|------|------|------|-------|
| t _{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| t _{REMRSTB} | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| t _{RECRSTB} | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| t _{MPWRSTB} | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t _{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F _{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

TABLE 2-121: A3P250 FIFO 4K×1 WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425 V

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------|---|------|------|------|-------|
| t _{ENS} | REN, WEN Setup Time | 4.86 | 5.53 | 6.50 | ns |
| t _{ENH} | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t _{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t _{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t _{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| t _{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t _{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t _{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t _{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t _{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t _{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t _{RSTBQ} | RESET Low to Data Out Low on DO (pass-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DO (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| t _{REMRSTB} | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| t _{RECRSTB} | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| t _{MPWRSTB} | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t _{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F _{MAX} | Maximum Frequency | 310 | 272 | 231 | MHz |

2.8 Embedded FlashROM Characteristics

FIGURE 2-44: TIMING DIAGRAM



2.8.1 TIMING CHARACTERISTICS

TABLE 2-122: EMBEDDED FLASHROM ACCESS TIME

| Parameter | Description | -2 | -1 | Std. | Units |
|------------|-------------------------|-------|-------|-------|-------|
| t_{SU} | Address Setup Time | 0.53 | 0.61 | 0.71 | ns |
| t_{HOLD} | Address Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{CK2Q} | Clock to Out | 21.42 | 24.40 | 28.68 | ns |
| F_{MAX} | Maximum Clock Frequency | 15 | 15 | 15 | MHz |

2.9 JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the [Section 2.3 User I/O Characteristics](#) for more details.

2.9.1 TIMING CHARACTERISTICS

TABLE 2-123: JTAG 1532 COMMERCIAL-CASE CONDITIONS: $T_J = 70^\circ\text{C}$, WORST-CASE $V_{CC} = 1.425\text{V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|-----------------------------|-------|-------|-------|-------|
| t_{DISU} | Test Data Input Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{DIHD} | Test Data Input Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TMSSU} | Test Mode Select Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{TMDHD} | Test Mode Select Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TCK2Q} | Clock to Q (data out) | 6.00 | 6.80 | 8.00 | ns |
| t_{RSTB2Q} | Reset to Q (data out) | 20.00 | 22.67 | 26.67 | ns |
| F_{TCKMAX} | TCK Maximum Frequency | 25.00 | 22.00 | 19.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.20 | 0.23 | 0.27 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | TBD | TBD | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) for derating values.

3.0 PIN DESCRIPTIONS

3.1 Supply Pins

3.1.1 GND GROUND

Ground supply voltage to the core, I/O outputs, and I/O logic.

3.1.2 GNDQ GROUND (QUIET)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

3.1.3 VCC CORE SUPPLY VOLTAGE

Supply voltage to the FPGA core, nominally 1.5V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

3.1.4 VCCIBX I/O SUPPLY VOLTAGE

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

3.1.5 VMVX I/O SUPPLY VOLTAGE (QUIET)

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

3.1.6 VCCPLA/B/C/D/E/F PLL SUPPLY VOLTAGE

Supply voltage to analog PLL, nominally 1.5V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC 3 Devices" chapter of the [ProASIC 3 FPGA Fabric User's Guide](#) for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on ProASIC 3 devices.

3.1.7 VCOMPLA/B/C/D/E/F PLL GROUND

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC 3 devices.

3.1.8 VJTAG JTAG SUPPLY VOLTAGE

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design.

If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.1.9 VPUMP PROGRAMMING SUPPLY VOLTAGE

ProASIC 3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in [Table 2-2](#).

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μF and 0.33 μF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.2 User Pins

3.2.1 I/O USER INPUT/OUTPUT

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI} . With V_{CCI} , VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

3.2.2 GL GLOBALS

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC 3 Devices" chapter of the [ProASIC 3 FPGA Fabric User's Guide](#). All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

3.2.3 FF FLASH*FREEZE MODE ACTIVATION PIN

Flash*Freeze is available on IGLOO, ProASIC 3L, and RT ProASIC 3 devices. It is not supported on ProASIC 3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. For IGLOOe, ProASIC 3EL, and RT ProASIC 3 only, the FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

3.3 JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

3.3.1 TCK TEST CLOCK

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements. Refer to [Table 3-1](#) for more information.

TABLE 3-1: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS

| VJTAG | Tie-Off Resistance |
|-------|--------------------|
| 3.3V | 200Ω –1 kΩ |
| 2.5V | 200Ω –1 kΩ |
| 1.8V | 500Ω –1 kΩ |
| 1.5V | 500Ω –1 kΩ |

- Note 1:** Equivalent parallel resistance if more than one device is on the JTAG chain
2: The TCK pin can be pulled up/down.
3: The TRST pin is pulled down.

3.3.2 TDI TEST DATA INPUT

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

3.3.3 TDO TEST DATA OUTPUT

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

3.3.4 TMS TEST MODE SELECT

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

3.3.5 TRST BOUNDARY SCAN RESET PIN

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from [Table 3-1](#) and must satisfy the parallel resistance value requirement. The values in [Table 3-1](#) correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements.

3.4 Special Function Pins

3.4.1 NC NO CONNECT

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

3.4.2 DC DO NOT CONNECT

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

3.5 Related Documents

3.5.1 USER'S GUIDES

ProASIC FPGA Fabric User's Guide

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/UserGuides/pa3_ug.pdf

3.5.2 PACKAGING

The following documents provide packaging information and device selection for low power flash devices.

3.5.2.1 *Product Catalog*

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/Brochures/igloo_lowpower_flash_fpgas_brochure.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

3.5.3 PACKAGE MECHANICAL DRAWINGS

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/PackagingSpecifications/PD3068-Package_Mechanical_Drawings_Datasheet_V62.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

4.0 PACKAGE PIN ASSIGNMENTS

4.1 QN48

FIGURE 4-1 • QN48—BOTTOM VIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| QN48 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| 1 | IO82RSB1 |
| 2 | GEC0/IO73RSB1 |
| 3 | GEA0/IO72RSB1 |
| 4 | GEB0/IO71RSB1 |
| 5 | GND |
| 6 | VCCIB1 |
| 7 | IO68RSB1 |
| 8 | IO67RSB1 |
| 9 | IO66RSB1 |
| 10 | IO65RSB1 |
| 11 | IO64RSB1 |
| 12 | IO62RSB1 |
| 13 | IO61RSB1 |
| 14 | IO60RSB1 |
| 15 | IO57RSB1 |
| 16 | IO55RSB1 |
| 17 | IO53RSB1 |
| 18 | VCC |
| 19 | VCCIB1 |
| 20 | IO46RSB1 |
| 21 | IO42RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | VPUMP |
| 26 | TDO |
| 27 | TRST |
| 28 | VJTAG |
| 29 | IO38RSB0 |
| 30 | GDB0/IO34RSB0 |
| 31 | GDA0/IO33RSB0 |
| 32 | GDC0/IO32RSB0 |
| 33 | VCCIB0 |
| 34 | GND |
| 35 | VCC |
| 36 | IO25RSB0 |

| QN48 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| 37 | IO24RSB0 |
| 38 | IO22RSB0 |
| 39 | IO20RSB0 |
| 40 | IO18RSB0 |
| 41 | IO16RSB0 |
| 42 | IO14RSB0 |
| 43 | IO10RSB0 |
| 44 | IO08RSB0 |
| 45 | IO06RSB0 |
| 46 | IO04RSB0 |
| 47 | IO02RSB0 |
| 48 | IO00RSB0 |

4.2 QN68

FIGURE 4-2 • QN68—BOTTOM VIEW

Note: .



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| QN68 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |
| 36 | TDO |

| QN68 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | VCCIB0 |
| 60 | GND |
| 61 | VCC |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

4.3 QN132

FIGURE 4-3 • QN132—BOTTOM VIEW



- Note 1:** The die attach paddle center of the package is tied to ground (GND).
- 2:** Option corner pads come with this device and package combination. It is optional to tie them to ground or leave them floating.
- 3:** The QN132 package is discontinued and is not available for ProASIC 3 devices.
- 4:** For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| QN132 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| A1 | IO01RSB1 |
| A2 | IO81RSB1 |
| A3 | NC |
| A4 | IO80RSB1 |
| A5 | GEC0/IO77RSB1 |
| A6 | NC |
| A7 | GEB0/IO75RSB1 |
| A8 | IO73RSB1 |
| A9 | NC |
| A10 | VCC |
| A11 | IO71RSB1 |
| A12 | IO68RSB1 |
| A13 | IO63RSB1 |
| A14 | IO60RSB1 |
| A15 | NC |
| A16 | IO59RSB1 |
| A17 | IO57RSB1 |
| A18 | VCC |
| A19 | IO54RSB1 |
| A20 | IO52RSB1 |
| A21 | IO49RSB1 |
| A22 | IO48RSB1 |
| A23 | IO47RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | IO44RSB0 |
| A27 | NC |
| A28 | IO43RSB0 |
| A29 | IO42RSB0 |
| A30 | IO40RSB0 |
| A31 | IO39RSB0 |
| A32 | GDC0/IO36RSB0 |
| A33 | NC |
| A34 | VCC |
| A35 | IO34RSB0 |
| A36 | IO31RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| A37 | IO26RSB0 |
| A38 | IO23RSB0 |
| A39 | NC |
| A40 | IO22RSB0 |
| A41 | IO20RSB0 |
| A42 | IO18RSB0 |
| A43 | VCC |
| A44 | IO15RSB0 |
| A45 | IO12RSB0 |
| A46 | IO10RSB0 |
| A47 | IO09RSB0 |
| A48 | IO06RSB0 |
| B1 | IO02RSB1 |
| B2 | IO82RSB1 |
| B3 | GND |
| B4 | IO79RSB1 |
| B5 | NC |
| B6 | GND |
| B7 | IO74RSB1 |
| B8 | NC |
| B9 | GND |
| B10 | IO70RSB1 |
| B11 | IO67RSB1 |
| B12 | IO64RSB1 |
| B13 | IO61RSB1 |
| B14 | GND |
| B15 | IO58RSB1 |
| B16 | IO56RSB1 |
| B17 | GND |
| B18 | IO53RSB1 |
| B19 | IO50RSB1 |
| B20 | GND |
| B21 | IO46RSB1 |
| B22 | TMS |
| B23 | TDO |
| B24 | IO45RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| B25 | GND |
| B26 | NC |
| B27 | IO41RSB0 |
| B28 | GND |
| B29 | GDA0/IO37RSB0 |
| B30 | NC |
| B31 | GND |
| B32 | IO33RSB0 |
| B33 | IO30RSB0 |
| B34 | IO27RSB0 |
| B35 | IO24RSB0 |
| B36 | GND |
| B37 | IO21RSB0 |
| B38 | IO19RSB0 |
| B39 | GND |
| B40 | IO16RSB0 |
| B41 | IO13RSB0 |
| B42 | GND |
| B43 | IO08RSB0 |
| B44 | IO05RSB0 |
| C1 | IO03RSB1 |
| C2 | IO00RSB1 |
| C3 | NC |
| C4 | IO78RSB1 |
| C5 | GEA0/IO76RSB1 |
| C6 | NC |
| C7 | NC |
| C8 | VCCIB1 |
| C9 | IO69RSB1 |
| C10 | IO66RSB1 |
| C11 | IO65RSB1 |
| C12 | IO62RSB1 |
| C13 | NC |
| C14 | NC |
| C15 | IO55RSB1 |
| C16 | VCCIB1 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P030 Function |
| C17 | IO51RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | NC |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | NC |
| C24 | NC |
| C25 | NC |
| C26 | GDB0/IO38RSB0 |
| C27 | NC |
| C28 | VCCIB0 |
| C29 | IO32RSB0 |
| C30 | IO29RSB0 |
| C31 | IO28RSB0 |
| C32 | IO25RSB0 |
| C33 | NC |
| C34 | NC |
| C35 | VCCIB0 |
| C36 | IO17RSB0 |
| C37 | IO14RSB0 |
| C38 | IO11RSB0 |
| C39 | IO07RSB0 |
| C40 | IO04RSB0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| A1 | GAB2/IO00RSB1 |
| A2 | IO93RSB1 |
| A3 | VCCIB1 |
| A4 | GFC1/IO89RSB1 |
| A5 | GFB0/IO86RSB1 |
| A6 | VCCPLF |
| A7 | GFA1/IO84RSB1 |
| A8 | GFC2/IO81RSB1 |
| A9 | IO78RSB1 |
| A10 | VCC |
| A11 | GEB1/IO75RSB1 |
| A12 | GEA0/IO72RSB1 |
| A13 | GEC2/IO69RSB1 |
| A14 | IO65RSB1 |
| A15 | VCC |
| A16 | IO64RSB1 |
| A17 | IO63RSB1 |
| A18 | IO62RSB1 |
| A19 | IO61RSB1 |
| A20 | IO58RSB1 |
| A21 | GDB2/IO55RSB1 |
| A22 | NC |
| A23 | GDA2/IO54RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO48RSB0 |
| A27 | VCC |
| A28 | IO47RSB0 |
| A29 | GCC2/IO46RSB0 |
| A30 | GCA2/IO44RSB0 |
| A31 | GCA0/IO43RSB0 |
| A32 | GCB1/IO40RSB0 |
| A33 | IO36RSB0 |
| A34 | VCC |
| A35 | IO31RSB0 |
| A36 | GBA2/IO28RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| A37 | GBB1/IO25RSB0 |
| A38 | GBC0/IO22RSB0 |
| A39 | VCCIB0 |
| A40 | IO21RSB0 |
| A41 | IO18RSB0 |
| A42 | IO15RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | GAB1/IO08RSB0 |
| A46 | NC |
| A47 | GAB0/IO07RSB0 |
| A48 | IO04RSB0 |
| B1 | IO01RSB1 |
| B2 | GAC2/IO94RSB1 |
| B3 | GND |
| B4 | GFC0/IO88RSB1 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO82RSB1 |
| B8 | IO79RSB1 |
| B9 | GND |
| B10 | GEB0/IO74RSB1 |
| B11 | VMV1 |
| B12 | GEB2/IO70RSB1 |
| B13 | IO67RSB1 |
| B14 | GND |
| B15 | NC |
| B16 | NC |
| B17 | GND |
| B18 | IO59RSB1 |
| B19 | GDC2/IO56RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO49RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO45RSB0 |
| B28 | GND |
| B29 | GCB0/IO41RSB0 |
| B30 | GCC1/IO38RSB0 |
| B31 | GND |
| B32 | GBB2/IO30RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO26RSB0 |
| B35 | GBC1/IO23RSB0 |
| B36 | GND |
| B37 | IO20RSB0 |
| B38 | IO17RSB0 |
| B39 | GND |
| B40 | IO12RSB0 |
| B41 | GAC0/IO09RSB0 |
| B42 | GND |
| B43 | GAA1/IO06RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO02RSB1 |
| C2 | IO95RSB1 |
| C3 | VCC |
| C4 | GFB1/IO87RSB1 |
| C5 | GFA0/IO85RSB1 |
| C6 | GFA2/IO83RSB1 |
| C7 | IO80RSB1 |
| C8 | VCCIB1 |
| C9 | GEA1/IO73RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO71RSB1 |
| C12 | IO68RSB1 |
| C13 | VCCIB1 |
| C14 | NC |
| C15 | NC |
| C16 | IO60RSB1 |

| QN132 | |
|-------------------|------------------------|
| Pin Number | A3P060 Function |
| C17 | IO57RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO42RSB0 |
| C27 | GCC0/IO39RSB0 |
| C28 | VCCIB0 |
| C29 | IO29RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO27RSB0 |
| C32 | GBB0/IO24RSB0 |
| C33 | VCC |
| C34 | IO19RSB0 |
| C35 | IO16RSB0 |
| C36 | IO13RSB0 |
| C37 | GAC1/IO10RSB0 |
| C38 | NC |
| C39 | GAA0/IO05RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| A1 | GAB2/IO69RSB1 |
| A2 | IO130RSB1 |
| A3 | VCCIB1 |
| A4 | GFC1/IO126RSB1 |
| A5 | GFB0/IO123RSB1 |
| A6 | VCCPLF |
| A7 | GFA1/IO121RSB1 |
| A8 | GFC2/IO118RSB1 |
| A9 | IO115RSB1 |
| A10 | VCC |
| A11 | GEB1/IO110RSB1 |
| A12 | GEA0/IO107RSB1 |
| A13 | GEC2/IO104RSB1 |
| A14 | IO100RSB1 |
| A15 | VCC |
| A16 | IO99RSB1 |
| A17 | IO96RSB1 |
| A18 | IO94RSB1 |
| A19 | IO91RSB1 |
| A20 | IO85RSB1 |
| A21 | IO79RSB1 |
| A22 | VCC |
| A23 | GDB2/IO71RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO61RSB0 |
| A27 | VCC |
| A28 | IO60RSB0 |
| A29 | GCC2/IO59RSB0 |
| A30 | GCA2/IO57RSB0 |
| A31 | GCA0/IO56RSB0 |
| A32 | GCB1/IO53RSB0 |
| A33 | IO49RSB0 |
| A34 | VCC |
| A35 | IO44RSB0 |
| A36 | GBA2/IO41RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| A37 | GBB1/IO38RSB0 |
| A38 | GBC0/IO35RSB0 |
| A39 | VCCIB0 |
| A40 | IO28RSB0 |
| A41 | IO22RSB0 |
| A42 | IO18RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | IO07RSB0 |
| A46 | VCC |
| A47 | GAC1/IO05RSB0 |
| A48 | GAB0/IO02RSB0 |
| B1 | IO68RSB1 |
| B2 | GAC2/IO131RSB1 |
| B3 | GND |
| B4 | GFC0/IO125RSB1 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO119RSB1 |
| B8 | IO116RSB1 |
| B9 | GND |
| B10 | GEB0/IO109RSB1 |
| B11 | VMV1 |
| B12 | GEB2/IO105RSB1 |
| B13 | IO101RSB1 |
| B14 | GND |
| B15 | IO98RSB1 |
| B16 | IO95RSB1 |
| B17 | GND |
| B18 | IO87RSB1 |
| B19 | IO81RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO62RSB0 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO58RSB0 |
| B28 | GND |
| B29 | GCB0/IO54RSB0 |
| B30 | GCC1/IO51RSB0 |
| B31 | GND |
| B32 | GBB2/IO43RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO39RSB0 |
| B35 | GBC1/IO36RSB0 |
| B36 | GND |
| B37 | IO26RSB0 |
| B38 | IO21RSB0 |
| B39 | GND |
| B40 | IO13RSB0 |
| B41 | IO08RSB0 |
| B42 | GND |
| B43 | GAC0/IO04RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO67RSB1 |
| C2 | IO132RSB1 |
| C3 | VCC |
| C4 | GFB1/IO124RSB1 |
| C5 | GFA0/IO122RSB1 |
| C6 | GFA2/IO120RSB1 |
| C7 | IO117RSB1 |
| C8 | VCCIB1 |
| C9 | GEA1/IO108RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO106RSB1 |
| C12 | IO103RSB1 |
| C13 | VCCIB1 |
| C14 | IO97RSB1 |
| C15 | IO93RSB1 |
| C16 | IO89RSB1 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| C17 | IO83RSB1 |
| C18 | VCCIB1 |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO55RSB0 |
| C27 | GCC0/IO52RSB0 |
| C28 | VCCIB0 |
| C29 | IO42RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| A1 | GAB2/IO117UPB3 |
| A2 | IO117VPB3 |
| A3 | VCCIB3 |
| A4 | GFC1/IO110PDB3 |
| A5 | GFB0/IO109NPB3 |
| A6 | VCCPLF |
| A7 | GFA1/IO108PPB3 |
| A8 | GFC2/IO105PPB3 |
| A9 | IO103NDB3 |
| A10 | VCC |
| A11 | GEA1/IO98PPB3 |
| A12 | GEA0/IO98NPB3 |
| A13 | GEC2/IO95RSB2 |
| A14 | IO91RSB2 |
| A15 | VCC |
| A16 | IO90RSB2 |
| A17 | IO87RSB2 |
| A18 | IO85RSB2 |
| A19 | IO82RSB2 |
| A20 | IO76RSB2 |
| A21 | IO70RSB2 |
| A22 | VCC |
| A23 | GDB2/IO62RSB2 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO58UDB1 |
| A27 | VCC |
| A28 | IO54NDB1 |
| A29 | IO52NDB1 |
| A30 | GCA2/IO51PPB1 |
| A31 | GCA0/IO50NPB1 |
| A32 | GCB1/IO49PDB1 |
| A33 | IO47NSB1 |
| A34 | VCC |
| A35 | IO41NPB1 |
| A36 | GBA2/IO41PPB1 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| A37 | GBB1/IO38RSB0 |
| A38 | GBC0/IO35RSB0 |
| A39 | VCCIB0 |
| A40 | IO28RSB0 |
| A41 | IO22RSB0 |
| A42 | IO18RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | IO07RSB0 |
| A46 | VCC |
| A47 | GAC1/IO05RSB0 |
| A48 | GAB0/IO02RSB0 |
| B1 | IO118VDB3 |
| B2 | GAC2/IO116UDB3 |
| B3 | GND |
| B4 | GFC0/IO110NDB3 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO106PSB3 |
| B8 | IO103PDB3 |
| B9 | GND |
| B10 | GEB0/IO99NDB3 |
| B11 | VMV3 |
| B12 | GEB2/IO96RSB2 |
| B13 | IO92RSB2 |
| B14 | GND |
| B15 | IO89RSB2 |
| B16 | IO86RSB2 |
| B17 | GND |
| B18 | IO78RSB2 |
| B19 | IO72RSB2 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO58VDB1 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| B25 | GND |
| B26 | IO54PDB1 |
| B27 | GCB2/IO52PDB1 |
| B28 | GND |
| B29 | GCB0/IO49NDB1 |
| B30 | GCC1/IO48PDB1 |
| B31 | GND |
| B32 | GBB2/IO42PDB1 |
| B33 | VMV1 |
| B34 | GBA0/IO39RSB0 |
| B35 | GBC1/IO36RSB0 |
| B36 | GND |
| B37 | IO26RSB0 |
| B38 | IO21RSB0 |
| B39 | GND |
| B40 | IO13RSB0 |
| B41 | IO08RSB0 |
| B42 | GND |
| B43 | GAC0/IO04RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO118UDB3 |
| C2 | IO116VDB3 |
| C3 | VCC |
| C4 | GFB1/IO109PPB3 |
| C5 | GFA0/IO108NPB3 |
| C6 | GFA2/IO107PSB3 |
| C7 | IO105NPB3 |
| C8 | VCCIB3 |
| C9 | GEB1/IO99PDB3 |
| C10 | GNDQ |
| C11 | GEA2/IO97RSB2 |
| C12 | IO94RSB2 |
| C13 | VCCIB2 |
| C14 | IO88RSB2 |
| C15 | IO84RSB2 |
| C16 | IO80RSB2 |

| QN132 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| C17 | IO74RSB2 |
| C18 | VCCIB2 |
| C19 | TCK |
| C20 | VMV2 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB1 |
| C24 | IO53NSB1 |
| C25 | IO51NPB1 |
| C26 | GCA1/IO50PPB1 |
| C27 | GCC0/IO48NDB1 |
| C28 | VCCIB1 |
| C29 | IO42NDB1 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

4.4 VQ100

Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

FIGURE 4-4 • VQ100—TOPVIEW



| VQ100 | | VQ100 | | VQ100 | |
|------------|-----------------|------------|-----------------|------------|-----------------|
| Pin Number | A3P030 Function | Pin Number | A3P030 Function | Pin Number | A3P030 Function |
| 1 | GND | 37 | VCC | 73 | IO27RSB0 |
| 2 | IO82RSB1 | 38 | GND | 74 | IO26RSB0 |
| 3 | IO81RSB1 | 39 | VCCIB1 | 75 | IO25RSB0 |
| 4 | IO80RSB1 | 40 | IO49RSB1 | 76 | IO24RSB0 |
| 5 | IO79RSB1 | 41 | IO47RSB1 | 77 | IO23RSB0 |
| 6 | IO78RSB1 | 42 | IO46RSB1 | 78 | IO22RSB0 |
| 7 | IO77RSB1 | 43 | IO45RSB1 | 79 | IO21RSB0 |
| 8 | IO76RSB1 | 44 | IO44RSB1 | 80 | IO20RSB0 |
| 9 | GND | 45 | IO43RSB1 | 81 | IO19RSB0 |
| 10 | IO75RSB1 | 46 | IO42RSB1 | 82 | IO18RSB0 |
| 11 | IO74RSB1 | 47 | TCK | 83 | IO17RSB0 |
| 12 | GEC0/IO73RSB1 | 48 | TDI | 84 | IO16RSB0 |
| 13 | GEA0/IO72RSB1 | 49 | TMS | 85 | IO15RSB0 |
| 14 | GEB0/IO71RSB1 | 50 | NC | 86 | IO14RSB0 |
| 15 | IO70RSB1 | 51 | GND | 87 | VCCIB0 |
| 16 | IO69RSB1 | 52 | VPUMP | 88 | GND |
| 17 | VCC | 53 | NC | 89 | VCC |
| 18 | VCCIB1 | 54 | TDO | 90 | IO12RSB0 |
| 19 | IO68RSB1 | 55 | TRST | 91 | IO10RSB0 |
| 20 | IO67RSB1 | 56 | VJTAG | 92 | IO08RSB0 |
| 21 | IO66RSB1 | 57 | IO41RSB0 | 93 | IO07RSB0 |
| 22 | IO65RSB1 | 58 | IO40RSB0 | 94 | IO06RSB0 |
| 23 | IO64RSB1 | 59 | IO39RSB0 | 95 | IO05RSB0 |
| 24 | IO63RSB1 | 60 | IO38RSB0 | 96 | IO04RSB0 |
| 25 | IO62RSB1 | 61 | IO37RSB0 | 97 | IO03RSB0 |
| 26 | IO61RSB1 | 62 | IO36RSB0 | 98 | IO02RSB0 |
| 27 | IO60RSB1 | 63 | GDB0/IO34RSB0 | 99 | IO01RSB0 |
| 28 | IO59RSB1 | 64 | GDA0/IO33RSB0 | 100 | IO00RSB0 |
| 29 | IO58RSB1 | 65 | GDC0/IO32RSB0 | | |
| 30 | IO57RSB1 | 66 | VCCIB0 | | |
| 31 | IO56RSB1 | 67 | GND | | |
| 32 | IO55RSB1 | 68 | VCC | | |
| 33 | IO54RSB1 | 69 | IO31RSB0 | | |
| 34 | IO53RSB1 | 70 | IO30RSB0 | | |
| 35 | IO52RSB1 | 71 | IO29RSB0 | | |
| 36 | IO51RSB1 | 72 | IO28RSB0 | | |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 1 | GND |
| 2 | GAA2/IO51RSB1 |
| 3 | IO52RSB1 |
| 4 | GAB2/IO53RSB1 |
| 5 | IO95RSB1 |
| 6 | GAC2/IO94RSB1 |
| 7 | IO93RSB1 |
| 8 | IO92RSB1 |
| 9 | GND |
| 10 | GFB1/IO87RSB1 |
| 11 | GFB0/IO86RSB1 |
| 12 | VCOMPLF |
| 13 | GFA0/IO85RSB1 |
| 14 | VCCPLF |
| 15 | GFA1/IO84RSB1 |
| 16 | GFA2/IO83RSB1 |
| 17 | VCC |
| 18 | VCCIB1 |
| 19 | GEC1/IO77RSB1 |
| 20 | GEB1/IO75RSB1 |
| 21 | GEB0/IO74RSB1 |
| 22 | GEA1/IO73RSB1 |
| 23 | GEA0/IO72RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO71RSB1 |
| 27 | GEB2/IO70RSB1 |
| 28 | GEC2/IO69RSB1 |
| 29 | IO68RSB1 |
| 30 | IO67RSB1 |
| 31 | IO66RSB1 |
| 32 | IO65RSB1 |
| 33 | IO64RSB1 |
| 34 | IO63RSB1 |
| 35 | IO62RSB1 |
| 36 | IO61RSB1 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB1 |
| 40 | IO60RSB1 |
| 41 | IO59RSB1 |
| 42 | IO58RSB1 |
| 43 | IO57RSB1 |
| 44 | GDC2/IO56RSB1 |
| 45 | GDB2/IO55RSB1 |
| 46 | GDA2/IO54RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO49RSB0 |
| 58 | GDC0/IO46RSB0 |
| 59 | GDC1/IO45RSB0 |
| 60 | GCC2/IO43RSB0 |
| 61 | GCB2/IO42RSB0 |
| 62 | GCA0/IO40RSB0 |
| 63 | GCA1/IO39RSB0 |
| 64 | GCC0/IO36RSB0 |
| 65 | GCC1/IO35RSB0 |
| 66 | VCCIB0 |
| 67 | GND |
| 68 | VCC |
| 69 | IO31RSB0 |
| 70 | GBC2/IO29RSB0 |
| 71 | GBB2/IO27RSB0 |
| 72 | IO26RSB0 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 73 | GBA2/IO25RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO24RSB0 |
| 77 | GBA0/IO23RSB0 |
| 78 | GBB1/IO22RSB0 |
| 79 | GBB0/IO21RSB0 |
| 80 | GBC1/IO20RSB0 |
| 81 | GBC0/IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO15RSB0 |
| 85 | IO13RSB0 |
| 86 | IO11RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO10RSB0 |
| 91 | IO09RSB0 |
| 92 | IO08RSB0 |
| 93 | GAC1/IO07RSB0 |
| 94 | GAC0/IO06RSB0 |
| 95 | GAB1/IO05RSB0 |
| 96 | GAB0/IO04RSB0 |
| 97 | GAA1/IO03RSB0 |
| 98 | GAA0/IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | IO130RSB1 |
| 8 | IO129RSB1 |
| 9 | GND |
| 10 | GFB1/IO124RSB1 |
| 11 | GFB0/IO123RSB1 |
| 12 | VCOMPLF |
| 13 | GFA0/IO122RSB1 |
| 14 | VCCPLF |
| 15 | GFA1/IO121RSB1 |
| 16 | GFA2/IO120RSB1 |
| 17 | VCC |
| 18 | VCCIB1 |
| 19 | GEC0/IO111RSB1 |
| 20 | GEB1/IO110RSB1 |
| 21 | GEB0/IO109RSB1 |
| 22 | GEA1/IO108RSB1 |
| 23 | GEA0/IO107RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO106RSB1 |
| 27 | GEB2/IO105RSB1 |
| 28 | GEC2/IO104RSB1 |
| 29 | IO102RSB1 |
| 30 | IO100RSB1 |
| 31 | IO99RSB1 |
| 32 | IO97RSB1 |
| 33 | IO96RSB1 |
| 34 | IO95RSB1 |
| 35 | IO94RSB1 |
| 36 | IO93RSB1 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB1 |
| 40 | IO87RSB1 |
| 41 | IO84RSB1 |
| 42 | IO81RSB1 |
| 43 | IO75RSB1 |
| 44 | GDC2/IO72RSB1 |
| 45 | GDB2/IO71RSB1 |
| 46 | GDA2/IO70RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO65RSB0 |
| 58 | GDC0/IO62RSB0 |
| 59 | GDC1/IO61RSB0 |
| 60 | GCC2/IO59RSB0 |
| 61 | GCB2/IO58RSB0 |
| 62 | GCA0/IO56RSB0 |
| 63 | GCA1/IO55RSB0 |
| 64 | GCC0/IO52RSB0 |
| 65 | GCC1/IO51RSB0 |
| 66 | VCCIB0 |
| 67 | GND |
| 68 | VCC |
| 69 | IO47RSB0 |
| 70 | GBC2/IO45RSB0 |
| 71 | GBB2/IO43RSB0 |
| 72 | IO42RSB0 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 73 | GBA2/IO41RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO32RSB0 |
| 83 | IO28RSB0 |
| 84 | IO25RSB0 |
| 85 | IO22RSB0 |
| 86 | IO19RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | IO09RSB0 |
| 94 | IO07RSB0 |
| 95 | GAC1/IO05RSB0 |
| 96 | GAC0/IO04RSB0 |
| 97 | GAB1/IO03RSB0 |
| 98 | GAB0/IO02RSB0 |
| 99 | GAA1/IO01RSB0 |
| 100 | GAA0/IO00RSB0 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 1 | GND |
| 2 | GAA2/IO118UDB3 |
| 3 | IO118VDB3 |
| 4 | GAB2/IO117UDB3 |
| 5 | IO117VDB3 |
| 6 | GAC2/IO116UDB3 |
| 7 | IO116VDB3 |
| 8 | IO112PSB3 |
| 9 | GND |
| 10 | GFB1/IO109PDB3 |
| 11 | GFB0/IO109NDB3 |
| 12 | VCOMPLF |
| 13 | GFA0/IO108NPB3 |
| 14 | VCCPLF |
| 15 | GFA1/IO108PPB3 |
| 16 | GFA2/IO107PSB3 |
| 17 | VCC |
| 18 | VCCIB3 |
| 19 | GFC2/IO105PSB3 |
| 20 | GEC1/IO100PDB3 |
| 21 | GEC0/IO100NDB3 |
| 22 | GEA1/IO98PDB3 |
| 23 | GEA0/IO98NDB3 |
| 24 | VMV3 |
| 25 | GNDQ |
| 26 | GEA2/IO97RSB2 |
| 27 | GEB2/IO96RSB2 |
| 28 | GEC2/IO95RSB2 |
| 29 | IO93RSB2 |
| 30 | IO92RSB2 |
| 31 | IO91RSB2 |
| 32 | IO90RSB2 |
| 33 | IO88RSB2 |
| 34 | IO86RSB2 |
| 35 | IO85RSB2 |
| 36 | IO84RSB2 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB2 |
| 40 | IO77RSB2 |
| 41 | IO74RSB2 |
| 42 | IO71RSB2 |
| 43 | GDC2/IO63RSB2 |
| 44 | GDB2/IO62RSB2 |
| 45 | GDA2/IO61RSB2 |
| 46 | GNDQ |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV2 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO60USB1 |
| 58 | GDC0/IO58VDB1 |
| 59 | GDC1/IO58UDB1 |
| 60 | IO52NDB1 |
| 61 | GCB2/IO52PDB1 |
| 62 | GCA1/IO50PDB1 |
| 63 | GCA0/IO50NDB1 |
| 64 | GCC0/IO48NDB1 |
| 65 | GCC1/IO48PDB1 |
| 66 | VCCIB1 |
| 67 | GND |
| 68 | VCC |
| 69 | IO43NDB1 |
| 70 | GBC2/IO43PDB1 |
| 71 | GBB2/IO42PSB1 |
| 72 | IO41NDB1 |

| VQ100 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 73 | GBA2/IO41PDB1 |
| 74 | VMV1 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO29RSB0 |
| 83 | IO27RSB0 |
| 84 | IO25RSB0 |
| 85 | IO23RSB0 |
| 86 | IO21RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | GAC1/IO05RSB0 |
| 94 | GAC0/IO04RSB0 |
| 95 | GAB1/IO03RSB0 |
| 96 | GAB0/IO02RSB0 |
| 97 | GAA1/IO01RSB0 |
| 98 | GAA0/IO00RSB0 |
| 99 | GNDQ |
| 100 | VMV0 |

4.5 TQ144

FIGURE 4-5 • TQ144—TOPVIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 1 | GAA2/IO51RSB1 |
| 2 | IO52RSB1 |
| 3 | GAB2/IO53RSB1 |
| 4 | IO95RSB1 |
| 5 | GAC2/IO94RSB1 |
| 6 | IO93RSB1 |
| 7 | IO92RSB1 |
| 8 | IO91RSB1 |
| 9 | VCC |
| 10 | GND |
| 11 | VCCIB1 |
| 12 | IO90RSB1 |
| 13 | GFC1/IO89RSB1 |
| 14 | GFC0/IO88RSB1 |
| 15 | GFB1/IO87RSB1 |
| 16 | GFB0/IO86RSB1 |
| 17 | VCOMPLF |
| 18 | GFA0/IO85RSB1 |
| 19 | VCCPLF |
| 20 | GFA1/IO84RSB1 |
| 21 | GFA2/IO83RSB1 |
| 22 | GFB2/IO82RSB1 |
| 23 | GFC2/IO81RSB1 |
| 24 | IO80RSB1 |
| 25 | IO79RSB1 |
| 26 | IO78RSB1 |
| 27 | GND |
| 28 | VCCIB1 |
| 29 | GEC1/IO77RSB1 |
| 30 | GEC0/IO76RSB1 |
| 31 | GEB1/IO75RSB1 |
| 32 | GEB0/IO74RSB1 |
| 33 | GEA1/IO73RSB1 |
| 34 | GEA0/IO72RSB1 |
| 35 | VMV1 |
| 36 | GNDQ |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 37 | NC |
| 38 | GEA2/IO71RSB1 |
| 39 | GEB2/IO70RSB1 |
| 40 | GEC2/IO69RSB1 |
| 41 | IO68RSB1 |
| 42 | IO67RSB1 |
| 43 | IO66RSB1 |
| 44 | IO65RSB1 |
| 45 | VCC |
| 46 | GND |
| 47 | VCCIB1 |
| 48 | NC |
| 49 | IO64RSB1 |
| 50 | NC |
| 51 | IO63RSB1 |
| 52 | NC |
| 53 | IO62RSB1 |
| 54 | NC |
| 55 | IO61RSB1 |
| 56 | NC |
| 57 | NC |
| 58 | IO60RSB1 |
| 59 | IO59RSB1 |
| 60 | IO58RSB1 |
| 61 | IO57RSB1 |
| 62 | NC |
| 63 | GND |
| 64 | NC |
| 65 | GDC2/IO56RSB1 |
| 66 | GDB2/IO55RSB1 |
| 67 | GDA2/IO54RSB1 |
| 68 | GNDQ |
| 69 | TCK |
| 70 | TDI |
| 71 | TMS |
| 72 | VMV1 |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 73 | VPUMP |
| 74 | NC |
| 75 | TDO |
| 76 | TRST |
| 77 | VJTAG |
| 78 | GDA0/IO50RSB0 |
| 79 | GDB0/IO48RSB0 |
| 80 | GDB1/IO47RSB0 |
| 81 | VCCIB0 |
| 82 | GND |
| 83 | IO44RSB0 |
| 84 | GCC2/IO43RSB0 |
| 85 | GCB2/IO42RSB0 |
| 86 | GCA2/IO41RSB0 |
| 87 | GCA0/IO40RSB0 |
| 88 | GCA1/IO39RSB0 |
| 89 | GCB0/IO38RSB0 |
| 90 | GCB1/IO37RSB0 |
| 91 | GCC0/IO36RSB0 |
| 92 | GCC1/IO35RSB0 |
| 93 | IO34RSB0 |
| 94 | IO33RSB0 |
| 95 | NC |
| 96 | NC |
| 97 | NC |
| 98 | VCCIB0 |
| 99 | GND |
| 100 | VCC |
| 101 | IO30RSB0 |
| 102 | GBC2/IO29RSB0 |
| 103 | IO28RSB0 |
| 104 | GBB2/IO27RSB0 |
| 105 | IO26RSB0 |
| 106 | GBA2/IO25RSB0 |
| 107 | VMV0 |
| 108 | GNDQ |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| 109 | NC |
| 110 | NC |
| 111 | GBA1/IO24RSB0 |
| 112 | GBA0/IO23RSB0 |
| 113 | GBB1/IO22RSB0 |
| 114 | GBB0/IO21RSB0 |
| 115 | GBC1/IO20RSB0 |
| 116 | GBC0/IO19RSB0 |
| 117 | VCCIB0 |
| 118 | GND |
| 119 | VCC |
| 120 | IO18RSB0 |
| 121 | IO17RSB0 |
| 122 | IO16RSB0 |
| 123 | IO15RSB0 |
| 124 | IO14RSB0 |
| 125 | IO13RSB0 |
| 126 | IO12RSB0 |
| 127 | IO11RSB0 |
| 128 | NC |
| 129 | IO10RSB0 |
| 130 | IO09RSB0 |
| 131 | IO08RSB0 |
| 132 | GAC1/IO07RSB0 |
| 133 | GAC0/IO06RSB0 |
| 134 | NC |
| 135 | GND |
| 136 | NC |
| 137 | GAB1/IO05RSB0 |
| 138 | GAB0/IO04RSB0 |
| 139 | GAA1/IO03RSB0 |
| 140 | GAA0/IO02RSB0 |
| 141 | IO01RSB0 |
| 142 | IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 1 | GAA2/IO67RSB1 |
| 2 | IO68RSB1 |
| 3 | GAB2/IO69RSB1 |
| 4 | IO132RSB1 |
| 5 | GAC2/IO131RSB1 |
| 6 | IO130RSB1 |
| 7 | IO129RSB1 |
| 8 | IO128RSB1 |
| 9 | VCC |
| 10 | GND |
| 11 | VCCIB1 |
| 12 | IO127RSB1 |
| 13 | GFC1/IO126RSB1 |
| 14 | GFC0/IO125RSB1 |
| 15 | GFB1/IO124RSB1 |
| 16 | GFB0/IO123RSB1 |
| 17 | VCOMPLF |
| 18 | GFA0/IO122RSB1 |
| 19 | VCCPLF |
| 20 | GFA1/IO121RSB1 |
| 21 | GFA2/IO120RSB1 |
| 22 | GFB2/IO119RSB1 |
| 23 | GFC2/IO118RSB1 |
| 24 | IO117RSB1 |
| 25 | IO116RSB1 |
| 26 | IO115RSB1 |
| 27 | GND |
| 28 | VCCIB1 |
| 29 | GEC1/IO112RSB1 |
| 30 | GEC0/IO111RSB1 |
| 31 | GEB1/IO110RSB1 |
| 32 | GEB0/IO109RSB1 |
| 33 | GEA1/IO108RSB1 |
| 34 | GEA0/IO107RSB1 |
| 35 | VMV1 |
| 36 | GNDQ |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 37 | NC |
| 38 | GEA2/IO106RSB1 |
| 39 | GEB2/IO105RSB1 |
| 40 | GEC2/IO104RSB1 |
| 41 | IO103RSB1 |
| 42 | IO102RSB1 |
| 43 | IO101RSB1 |
| 44 | IO100RSB1 |
| 45 | VCC |
| 46 | GND |
| 47 | VCCIB1 |
| 48 | IO99RSB1 |
| 49 | IO97RSB1 |
| 50 | IO95RSB1 |
| 51 | IO93RSB1 |
| 52 | IO92RSB1 |
| 53 | IO90RSB1 |
| 54 | IO88RSB1 |
| 55 | IO86RSB1 |
| 56 | IO84RSB1 |
| 57 | IO83RSB1 |
| 58 | IO82RSB1 |
| 59 | IO81RSB1 |
| 60 | IO80RSB1 |
| 61 | IO79RSB1 |
| 62 | VCC |
| 63 | GND |
| 64 | VCCIB1 |
| 65 | GDC2/IO72RSB1 |
| 66 | GDB2/IO71RSB1 |
| 67 | GDA2/IO70RSB1 |
| 68 | GNDQ |
| 69 | TCK |
| 70 | TDI |
| 71 | TMS |
| 72 | VMV1 |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 73 | VPUMP |
| 74 | NC |
| 75 | TDO |
| 76 | TRST |
| 77 | VJTAG |
| 78 | GDA0/IO66RSB0 |
| 79 | GDB0/IO64RSB0 |
| 80 | GDB1/IO63RSB0 |
| 81 | VCCIB0 |
| 82 | GND |
| 83 | IO60RSB0 |
| 84 | GCC2/IO59RSB0 |
| 85 | GCB2/IO58RSB0 |
| 86 | GCA2/IO57RSB0 |
| 87 | GCA0/IO56RSB0 |
| 88 | GCA1/IO55RSB0 |
| 89 | GCB0/IO54RSB0 |
| 90 | GCB1/IO53RSB0 |
| 91 | GCC0/IO52RSB0 |
| 92 | GCC1/IO51RSB0 |
| 93 | IO50RSB0 |
| 94 | IO49RSB0 |
| 95 | NC |
| 96 | NC |
| 97 | NC |
| 98 | VCCIB0 |
| 99 | GND |
| 100 | VCC |
| 101 | IO47RSB0 |
| 102 | GBC2/IO45RSB0 |
| 103 | IO44RSB0 |
| 104 | GBB2/IO43RSB0 |
| 105 | IO42RSB0 |
| 106 | GBA2/IO41RSB0 |
| 107 | VMV0 |
| 108 | GNDQ |

| TQ144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 109 | GBA1/IO40RSB0 |
| 110 | GBA0/IO39RSB0 |
| 111 | GBB1/IO38RSB0 |
| 112 | GBB0/IO37RSB0 |
| 113 | GBC1/IO36RSB0 |
| 114 | GBC0/IO35RSB0 |
| 115 | IO34RSB0 |
| 116 | IO33RSB0 |
| 117 | VCCIB0 |
| 118 | GND |
| 119 | VCC |
| 120 | IO29RSB0 |
| 121 | IO28RSB0 |
| 122 | IO27RSB0 |
| 123 | IO25RSB0 |
| 124 | IO23RSB0 |
| 125 | IO21RSB0 |
| 126 | IO19RSB0 |
| 127 | IO17RSB0 |
| 128 | IO16RSB0 |
| 129 | IO14RSB0 |
| 130 | IO12RSB0 |
| 131 | IO10RSB0 |
| 132 | IO08RSB0 |
| 133 | IO06RSB0 |
| 134 | VCCIB0 |
| 135 | GND |
| 136 | VCC |
| 137 | GAC1/IO05RSB0 |
| 138 | GAC0/IO04RSB0 |
| 139 | GAB1/IO03RSB0 |
| 140 | GAB0/IO02RSB0 |
| 141 | GAA1/IO01RSB0 |
| 142 | GAA0/IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

4.6 PQ208

FIGURE 4-6 • PQ208—TOPVIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | NC |
| 8 | NC |
| 9 | IO130RSB1 |
| 10 | IO129RSB1 |
| 11 | NC |
| 12 | IO128RSB1 |
| 13 | NC |
| 14 | NC |
| 15 | NC |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB1 |
| 19 | IO127RSB1 |
| 20 | NC |
| 21 | GFC1/IO126RSB1 |
| 22 | GFC0/IO125RSB1 |
| 23 | GFB1/IO124RSB1 |
| 24 | GFB0/IO123RSB1 |
| 25 | VCOMPLF |
| 26 | GFA0/IO122RSB1 |
| 27 | VCCPLF |
| 28 | GFA1/IO121RSB1 |
| 29 | GND |
| 30 | GFA2/IO120RSB1 |
| 31 | NC |
| 32 | GFB2/IO119RSB1 |
| 33 | NC |
| 34 | GFC2/IO118RSB1 |
| 35 | IO117RSB1 |
| 36 | NC |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 37 | IO116RSB1 |
| 38 | IO115RSB1 |
| 39 | NC |
| 40 | VCCIB1 |
| 41 | GND |
| 42 | IO114RSB1 |
| 43 | IO113RSB1 |
| 44 | GEC1/IO112RSB1 |
| 45 | GEC0/IO111RSB1 |
| 46 | GEB1/IO110RSB1 |
| 47 | GEB0/IO109RSB1 |
| 48 | GEA1/IO108RSB1 |
| 49 | GEA0/IO107RSB1 |
| 50 | VMV1 |
| 51 | GNDQ |
| 52 | GND |
| 53 | NC |
| 54 | NC |
| 55 | GEA2/IO106RSB1 |
| 56 | GEB2/IO105RSB1 |
| 57 | GEC2/IO104RSB1 |
| 58 | IO103RSB1 |
| 59 | IO102RSB1 |
| 60 | IO101RSB1 |
| 61 | IO100RSB1 |
| 62 | VCCIB1 |
| 63 | IO99RSB1 |
| 64 | IO98RSB1 |
| 65 | GND |
| 66 | IO97RSB1 |
| 67 | IO96RSB1 |
| 68 | IO95RSB1 |
| 69 | IO94RSB1 |
| 70 | IO93RSB1 |
| 71 | VCC |
| 72 | VCCIB1 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 73 | IO92RSB1 |
| 74 | IO91RSB1 |
| 75 | IO90RSB1 |
| 76 | IO89RSB1 |
| 77 | IO88RSB1 |
| 78 | IO87RSB1 |
| 79 | IO86RSB1 |
| 80 | IO85RSB1 |
| 81 | GND |
| 82 | IO84RSB1 |
| 83 | IO83RSB1 |
| 84 | IO82RSB1 |
| 85 | IO81RSB1 |
| 86 | IO80RSB1 |
| 87 | IO79RSB1 |
| 88 | VCC |
| 89 | VCCIB1 |
| 90 | IO78RSB1 |
| 91 | IO77RSB1 |
| 92 | IO76RSB1 |
| 93 | IO75RSB1 |
| 94 | IO74RSB1 |
| 95 | IO73RSB1 |
| 96 | GDC2/IO72RSB1 |
| 97 | GND |
| 98 | GDB2/IO71RSB1 |
| 99 | GDA2/IO70RSB1 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV1 |
| 105 | GND |
| 106 | VPUMP |
| 107 | NC |
| 108 | TDO |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO66RSB0 |
| 112 | GDA1/IO65RSB0 |
| 113 | GDB0/IO64RSB0 |
| 114 | GDB1/IO63RSB0 |
| 115 | GDC0/IO62RSB0 |
| 116 | GDC1/IO61RSB0 |
| 117 | NC |
| 118 | NC |
| 119 | NC |
| 120 | NC |
| 121 | NC |
| 122 | GND |
| 123 | VCCIB0 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO60RSB0 |
| 128 | GCC2/IO59RSB0 |
| 129 | GCB2/IO58RSB0 |
| 130 | GND |
| 131 | GCA2/IO57RSB0 |
| 132 | GCA0/IO56RSB0 |
| 133 | GCA1/IO55RSB0 |
| 134 | GCB0/IO54RSB0 |
| 135 | GCB1/IO53RSB0 |
| 136 | GCC0/IO52RSB0 |
| 137 | GCC1/IO51RSB0 |
| 138 | IO50RSB0 |
| 139 | IO49RSB0 |
| 140 | VCCIB0 |
| 141 | GND |
| 142 | VCC |
| 143 | IO48RSB0 |
| 144 | IO47RSB0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 145 | IO46RSB0 |
| 146 | NC |
| 147 | NC |
| 148 | NC |
| 149 | GBC2/IO45RSB0 |
| 150 | IO44RSB0 |
| 151 | GBB2/IO43RSB0 |
| 152 | IO42RSB0 |
| 153 | GBA2/IO41RSB0 |
| 154 | VMV0 |
| 155 | GNDQ |
| 156 | GND |
| 157 | NC |
| 158 | GBA1/IO40RSB0 |
| 159 | GBA0/IO39RSB0 |
| 160 | GBB1/IO38RSB0 |
| 161 | GBB0/IO37RSB0 |
| 162 | GND |
| 163 | GBC1/IO36RSB0 |
| 164 | GBC0/IO35RSB0 |
| 165 | IO34RSB0 |
| 166 | IO33RSB0 |
| 167 | IO32RSB0 |
| 168 | IO31RSB0 |
| 169 | IO30RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO29RSB0 |
| 173 | IO28RSB0 |
| 174 | IO27RSB0 |
| 175 | IO26RSB0 |
| 176 | IO25RSB0 |
| 177 | IO24RSB0 |
| 178 | GND |
| 179 | IO23RSB0 |
| 180 | IO22RSB0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| 181 | IO21RSB0 |
| 182 | IO20RSB0 |
| 183 | IO19RSB0 |
| 184 | IO18RSB0 |
| 185 | IO17RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO16RSB0 |
| 189 | IO15RSB0 |
| 190 | IO14RSB0 |
| 191 | IO13RSB0 |
| 192 | IO12RSB0 |
| 193 | IO11RSB0 |
| 194 | IO10RSB0 |
| 195 | GND |
| 196 | IO09RSB0 |
| 197 | IO08RSB0 |
| 198 | IO07RSB0 |
| 199 | IO06RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 1 | GND |
| 2 | GAA2/IO118UDB3 |
| 3 | IO118VDB3 |
| 4 | GAB2/IO117UDB3 |
| 5 | IO117VDB3 |
| 6 | GAC2/IO116UDB3 |
| 7 | IO116VDB3 |
| 8 | IO115UDB3 |
| 9 | IO115VDB3 |
| 10 | IO114UDB3 |
| 11 | IO114VDB3 |
| 12 | IO113PDB3 |
| 13 | IO113NDB3 |
| 14 | IO112PDB3 |
| 15 | IO112NDB3 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB3 |
| 19 | IO111PDB3 |
| 20 | IO111NDB3 |
| 21 | GFC1/IO110PDB3 |
| 22 | GFC0/IO110NDB3 |
| 23 | GFB1/IO109PDB3 |
| 24 | GFB0/IO109NDB3 |
| 25 | VCOMPLF |
| 26 | GFA0/IO108NPB3 |
| 27 | VCCPLF |
| 28 | GFA1/IO108PPB3 |
| 29 | GND |
| 30 | GFA2/IO107PDB3 |
| 31 | IO107NDB3 |
| 32 | GFB2/IO106PDB3 |
| 33 | IO106NDB3 |
| 34 | GFC2/IO105PDB3 |
| 35 | IO105NDB3 |
| 36 | NC |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 37 | IO104PDB3 |
| 38 | IO104NDB3 |
| 39 | IO103PSB3 |
| 40 | VCCIB3 |
| 41 | GND |
| 42 | IO101PDB3 |
| 43 | IO101NDB3 |
| 44 | GEC1/IO100PDB3 |
| 45 | GEC0/IO100NDB3 |
| 46 | GEB1/IO99PDB3 |
| 47 | GEB0/IO99NDB3 |
| 48 | GEA1/IO98PDB3 |
| 49 | GEA0/IO98NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | NC |
| 54 | NC |
| 55 | GEA2/IO97RSB2 |
| 56 | GEB2/IO96RSB2 |
| 57 | GEC2/IO95RSB2 |
| 58 | IO94RSB2 |
| 59 | IO93RSB2 |
| 60 | IO92RSB2 |
| 61 | IO91RSB2 |
| 62 | VCCIB2 |
| 63 | IO90RSB2 |
| 64 | IO89RSB2 |
| 65 | GND |
| 66 | IO88RSB2 |
| 67 | IO87RSB2 |
| 68 | IO86RSB2 |
| 69 | IO85RSB2 |
| 70 | IO84RSB2 |
| 71 | VCC |
| 72 | VCCIB2 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 73 | IO83RSB2 |
| 74 | IO82RSB2 |
| 75 | IO81RSB2 |
| 76 | IO80RSB2 |
| 77 | IO79RSB2 |
| 78 | IO78RSB2 |
| 79 | IO77RSB2 |
| 80 | IO76RSB2 |
| 81 | GND |
| 82 | IO75RSB2 |
| 83 | IO74RSB2 |
| 84 | IO73RSB2 |
| 85 | IO72RSB2 |
| 86 | IO71RSB2 |
| 87 | IO70RSB2 |
| 88 | VCC |
| 89 | VCCIB2 |
| 90 | IO69RSB2 |
| 91 | IO68RSB2 |
| 92 | IO67RSB2 |
| 93 | IO66RSB2 |
| 94 | IO65RSB2 |
| 95 | IO64RSB2 |
| 96 | GDC2/IO63RSB2 |
| 97 | GND |
| 98 | GDB2/IO62RSB2 |
| 99 | GDA2/IO61RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | VPUMP |
| 107 | NC |
| 108 | TDO |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO60VDB1 |
| 112 | GDA1/IO60UDB1 |
| 113 | GDB0/IO59VDB1 |
| 114 | GDB1/IO59UDB1 |
| 115 | GDC0/IO58VDB1 |
| 116 | GDC1/IO58UDB1 |
| 117 | IO57VDB1 |
| 118 | IO57UDB1 |
| 119 | IO56NDB1 |
| 120 | IO56PDB1 |
| 121 | IO55RSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO53NDB1 |
| 128 | GCC2/IO53PDB1 |
| 129 | GCB2/IO52PSB1 |
| 130 | GND |
| 131 | GCA2/IO51PSB1 |
| 132 | GCA1/IO50PDB1 |
| 133 | GCA0/IO50NDB1 |
| 134 | GCB0/IO49NDB1 |
| 135 | GCB1/IO49PDB1 |
| 136 | GCC0/IO48NDB1 |
| 137 | GCC1/IO48PDB1 |
| 138 | IO47NDB1 |
| 139 | IO47PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO46RSB1 |
| 144 | IO45NDB1 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 145 | IO45PDB1 |
| 146 | IO44NDB1 |
| 147 | IO44PDB1 |
| 148 | IO43NDB1 |
| 149 | GBC2/IO43PDB1 |
| 150 | IO42NDB1 |
| 151 | GBB2/IO42PDB1 |
| 152 | IO41NDB1 |
| 153 | GBA2/IO41PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | NC |
| 158 | GBA1/IO40RSB0 |
| 159 | GBA0/IO39RSB0 |
| 160 | GBB1/IO38RSB0 |
| 161 | GBB0/IO37RSB0 |
| 162 | GND |
| 163 | GBC1/IO36RSB0 |
| 164 | GBC0/IO35RSB0 |
| 165 | IO34RSB0 |
| 166 | IO33RSB0 |
| 167 | IO32RSB0 |
| 168 | IO31RSB0 |
| 169 | IO30RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO29RSB0 |
| 173 | IO28RSB0 |
| 174 | IO27RSB0 |
| 175 | IO26RSB0 |
| 176 | IO25RSB0 |
| 177 | IO24RSB0 |
| 178 | GND |
| 179 | IO23RSB0 |
| 180 | IO22RSB0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| 181 | IO21RSB0 |
| 182 | IO20RSB0 |
| 183 | IO19RSB0 |
| 184 | IO18RSB0 |
| 185 | IO17RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO16RSB0 |
| 189 | IO15RSB0 |
| 190 | IO14RSB0 |
| 191 | IO13RSB0 |
| 192 | IO12RSB0 |
| 193 | IO11RSB0 |
| 194 | IO10RSB0 |
| 195 | GND |
| 196 | IO09RSB0 |
| 197 | IO08RSB0 |
| 198 | IO07RSB0 |
| 199 | IO06RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 1 | GND |
| 2 | GAA2/IO155UDB3 |
| 3 | IO155VDB3 |
| 4 | GAB2/IO154UDB3 |
| 5 | IO154VDB3 |
| 6 | GAC2/IO153UDB3 |
| 7 | IO153VDB3 |
| 8 | IO152UDB3 |
| 9 | IO152VDB3 |
| 10 | IO151UDB3 |
| 11 | IO151VDB3 |
| 12 | IO150PDB3 |
| 13 | IO150NDB3 |
| 14 | IO149PDB3 |
| 15 | IO149NDB3 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB3 |
| 19 | IO148PDB3 |
| 20 | IO148NDB3 |
| 21 | GFC1/IO147PDB3 |
| 22 | GFC0/IO147NDB3 |
| 23 | GFB1/IO146PDB3 |
| 24 | GFB0/IO146NDB3 |
| 25 | VCOMPLF |
| 26 | GFA0/IO145NPB3 |
| 27 | VCCPLF |
| 28 | GFA1/IO145PPB3 |
| 29 | GND |
| 30 | GFA2/IO144PDB3 |
| 31 | IO144NDB3 |
| 32 | GFB2/IO143PDB3 |
| 33 | IO143NDB3 |
| 34 | GFC2/IO142PDB3 |
| 35 | IO142NDB3 |
| 36 | NC |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 37 | IO141PSB3 |
| 38 | IO140PDB3 |
| 39 | IO140NDB3 |
| 40 | VCCIB3 |
| 41 | GND |
| 42 | IO138PDB3 |
| 43 | IO138NDB3 |
| 44 | GEC1/IO137PDB3 |
| 45 | GEC0/IO137NDB3 |
| 46 | GEB1/IO136PDB3 |
| 47 | GEB0/IO136NDB3 |
| 48 | GEA1/IO135PDB3 |
| 49 | GEA0/IO135NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | NC |
| 55 | GEA2/IO134RSB2 |
| 56 | GEB2/IO133RSB2 |
| 57 | GEC2/IO132RSB2 |
| 58 | IO131RSB2 |
| 59 | IO130RSB2 |
| 60 | IO129RSB2 |
| 61 | IO128RSB2 |
| 62 | VCCIB2 |
| 63 | IO125RSB2 |
| 64 | IO123RSB2 |
| 65 | GND |
| 66 | IO121RSB2 |
| 67 | IO119RSB2 |
| 68 | IO117RSB2 |
| 69 | IO115RSB2 |
| 70 | IO113RSB2 |
| 71 | VCC |
| 72 | VCCIB2 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 73 | IO112RSB2 |
| 74 | IO111RSB2 |
| 75 | IO110RSB2 |
| 76 | IO109RSB2 |
| 77 | IO108RSB2 |
| 78 | IO107RSB2 |
| 79 | IO106RSB2 |
| 80 | IO104RSB2 |
| 81 | GND |
| 82 | IO102RSB2 |
| 83 | IO101RSB2 |
| 84 | IO100RSB2 |
| 85 | IO99RSB2 |
| 86 | IO98RSB2 |
| 87 | IO97RSB2 |
| 88 | VCC |
| 89 | VCCIB2 |
| 90 | IO94RSB2 |
| 91 | IO92RSB2 |
| 92 | IO90RSB2 |
| 93 | IO88RSB2 |
| 94 | IO86RSB2 |
| 95 | IO84RSB2 |
| 96 | GDC2/IO82RSB2 |
| 97 | GND |
| 98 | GDB2/IO81RSB2 |
| 99 | GDA2/IO80RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | VPUMP |
| 107 | NC |
| 108 | TDO |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO79VDB1 |
| 112 | GDA1/IO79UDB1 |
| 113 | GDB0/IO78VDB1 |
| 114 | GDB1/IO78UDB1 |
| 115 | GDC0/IO77VDB1 |
| 116 | GDC1/IO77UDB1 |
| 117 | IO76VDB1 |
| 118 | IO76UDB1 |
| 119 | IO75NDB1 |
| 120 | IO75PDB1 |
| 121 | IO74RSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO72NDB1 |
| 128 | GCC2/IO72PDB1 |
| 129 | GCB2/IO71PSB1 |
| 130 | GND |
| 131 | GCA2/IO70PSB1 |
| 132 | GCA1/IO69PDB1 |
| 133 | GCA0/IO69NDB1 |
| 134 | GCB0/IO68NDB1 |
| 135 | GCB1/IO68PDB1 |
| 136 | GCC0/IO67NDB1 |
| 137 | GCC1/IO67PDB1 |
| 138 | IO66NDB1 |
| 139 | IO66PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO65RSB1 |
| 144 | IO64NDB1 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 145 | IO64PDB1 |
| 146 | IO63NDB1 |
| 147 | IO63PDB1 |
| 148 | IO62NDB1 |
| 149 | GBC2/IO62PDB1 |
| 150 | IO61NDB1 |
| 151 | GBB2/IO61PDB1 |
| 152 | IO60NDB1 |
| 153 | GBA2/IO60PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO59RSB0 |
| 159 | GBA0/IO58RSB0 |
| 160 | GBB1/IO57RSB0 |
| 161 | GBB0/IO56RSB0 |
| 162 | GND |
| 163 | GBC1/IO55RSB0 |
| 164 | GBC0/IO54RSB0 |
| 165 | IO52RSB0 |
| 166 | IO49RSB0 |
| 167 | IO46RSB0 |
| 168 | IO43RSB0 |
| 169 | IO40RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO36RSB0 |
| 173 | IO35RSB0 |
| 174 | IO34RSB0 |
| 175 | IO33RSB0 |
| 176 | IO32RSB0 |
| 177 | IO31RSB0 |
| 178 | GND |
| 179 | IO29RSB0 |
| 180 | IO28RSB0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| 181 | IO27RSB0 |
| 182 | IO26RSB0 |
| 183 | IO25RSB0 |
| 184 | IO24RSB0 |
| 185 | IO23RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO21RSB0 |
| 189 | IO20RSB0 |
| 190 | IO19RSB0 |
| 191 | IO18RSB0 |
| 192 | IO17RSB0 |
| 193 | IO16RSB0 |
| 194 | IO15RSB0 |
| 195 | GND |
| 196 | IO13RSB0 |
| 197 | IO11RSB0 |
| 198 | IO09RSB0 |
| 199 | IO07RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 1 | GND |
| 2 | GAA2/IO174PDB3 |
| 3 | IO174NDB3 |
| 4 | GAB2/IO173PDB3 |
| 5 | IO173NDB3 |
| 6 | GAC2/IO172PDB3 |
| 7 | IO172NDB3 |
| 8 | IO171PDB3 |
| 9 | IO171NDB3 |
| 10 | IO170PDB3 |
| 11 | IO170NDB3 |
| 12 | IO169PDB3 |
| 13 | IO169NDB3 |
| 14 | IO168PDB3 |
| 15 | IO168NDB3 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB3 |
| 19 | IO166PDB3 |
| 20 | IO166NDB3 |
| 21 | GFC1/IO164PDB3 |
| 22 | GFC0/IO164NDB3 |
| 23 | GFB1/IO163PDB3 |
| 24 | GFB0/IO163NDB3 |
| 25 | VCOMPLF |
| 26 | GFA0/IO162NPB3 |
| 27 | VCCPLF |
| 28 | GFA1/IO162PPB3 |
| 29 | GND |
| 30 | GFA2/IO161PDB3 |
| 31 | IO161NDB3 |
| 32 | GFB2/IO160PDB3 |
| 33 | IO160NDB3 |
| 34 | GFC2/IO159PDB3 |
| 35 | IO159NDB3 |
| 36 | VCC |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 37 | IO152PDB3 |
| 38 | IO152NDB3 |
| 39 | IO150PSB3 |
| 40 | VCCIB3 |
| 41 | GND |
| 42 | IO147PDB3 |
| 43 | IO147NDB3 |
| 44 | GEC1/IO146PDB3 |
| 45 | GEC0/IO146NDB3 |
| 46 | GEB1/IO145PDB3 |
| 47 | GEB0/IO145NDB3 |
| 48 | GEA1/IO144PDB3 |
| 49 | GEA0/IO144NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | GEA2/IO143RSB2 |
| 55 | GEB2/IO142RSB2 |
| 56 | GEC2/IO141RSB2 |
| 57 | IO140RSB2 |
| 58 | IO139RSB2 |
| 59 | IO138RSB2 |
| 60 | IO137RSB2 |
| 61 | IO136RSB2 |
| 62 | VCCIB2 |
| 63 | IO135RSB2 |
| 64 | IO133RSB2 |
| 65 | GND |
| 66 | IO131RSB2 |
| 67 | IO129RSB2 |
| 68 | IO127RSB2 |
| 69 | IO125RSB2 |
| 70 | IO123RSB2 |
| 71 | VCC |
| 72 | VCCIB2 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 73 | IO120RSB2 |
| 74 | IO119RSB2 |
| 75 | IO118RSB2 |
| 76 | IO117RSB2 |
| 77 | IO116RSB2 |
| 78 | IO115RSB2 |
| 79 | IO114RSB2 |
| 80 | IO112RSB2 |
| 81 | GND |
| 82 | IO111RSB2 |
| 83 | IO110RSB2 |
| 84 | IO109RSB2 |
| 85 | IO108RSB2 |
| 86 | IO107RSB2 |
| 87 | IO106RSB2 |
| 88 | VCC |
| 89 | VCCIB2 |
| 90 | IO104RSB2 |
| 91 | IO102RSB2 |
| 92 | IO100RSB2 |
| 93 | IO98RSB2 |
| 94 | IO96RSB2 |
| 95 | IO92RSB2 |
| 96 | GDC2/IO91RSB2 |
| 97 | GND |
| 98 | GDB2/IO90RSB2 |
| 99 | GDA2/IO89RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |
| 108 | TDO |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO88NDB1 |
| 112 | GDA1/IO88PDB1 |
| 113 | GDB0/IO87NDB1 |
| 114 | GDB1/IO87PDB1 |
| 115 | GDC0/IO86NDB1 |
| 116 | GDC1/IO86PDB1 |
| 117 | IO84NDB1 |
| 118 | IO84PDB1 |
| 119 | IO82NDB1 |
| 120 | IO82PDB1 |
| 121 | IO81PSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | IO77NDB1 |
| 125 | IO77PDB1 |
| 126 | NC |
| 127 | IO74NDB1 |
| 128 | GCC2/IO74PDB1 |
| 129 | GCB2/IO73PSB1 |
| 130 | GND |
| 131 | GCA2/IO72PSB1 |
| 132 | GCA1/IO71PDB1 |
| 133 | GCA0/IO71NDB1 |
| 134 | GCB0/IO70NDB1 |
| 135 | GCB1/IO70PDB1 |
| 136 | GCC0/IO69NDB1 |
| 137 | GCC1/IO69PDB1 |
| 138 | IO67NDB1 |
| 139 | IO67PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO65PSB1 |
| 144 | IO64NDB1 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 145 | IO64PDB1 |
| 146 | IO63NDB1 |
| 147 | IO63PDB1 |
| 148 | IO62NDB1 |
| 149 | GBC2/IO62PDB1 |
| 150 | IO61NDB1 |
| 151 | GBB2/IO61PDB1 |
| 152 | IO60NDB1 |
| 153 | GBA2/IO60PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO59RSB0 |
| 159 | GBA0/IO58RSB0 |
| 160 | GBB1/IO57RSB0 |
| 161 | GBB0/IO56RSB0 |
| 162 | GND |
| 163 | GBC1/IO55RSB0 |
| 164 | GBC0/IO54RSB0 |
| 165 | IO52RSB0 |
| 166 | IO50RSB0 |
| 167 | IO48RSB0 |
| 168 | IO46RSB0 |
| 169 | IO44RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO36RSB0 |
| 173 | IO35RSB0 |
| 174 | IO34RSB0 |
| 175 | IO33RSB0 |
| 176 | IO32RSB0 |
| 177 | IO31RSB0 |
| 178 | GND |
| 179 | IO29RSB0 |
| 180 | IO28RSB0 |

| PQ208 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| 181 | IO27RSB0 |
| 182 | IO26RSB0 |
| 183 | IO25RSB0 |
| 184 | IO24RSB0 |
| 185 | IO23RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO20RSB0 |
| 189 | IO19RSB0 |
| 190 | IO18RSB0 |
| 191 | IO17RSB0 |
| 192 | IO16RSB0 |
| 193 | IO14RSB0 |
| 194 | IO12RSB0 |
| 195 | GND |
| 196 | IO10RSB0 |
| 197 | IO09RSB0 |
| 198 | IO08RSB0 |
| 199 | IO07RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 1 | GND |
| 2 | GAA2/IO225PDB3 |
| 3 | IO225NDB3 |
| 4 | GAB2/IO224PDB3 |
| 5 | IO224NDB3 |
| 6 | GAC2/IO223PDB3 |
| 7 | IO223NDB3 |
| 8 | IO222PDB3 |
| 9 | IO222NDB3 |
| 10 | IO220PDB3 |
| 11 | IO220NDB3 |
| 12 | IO218PDB3 |
| 13 | IO218NDB3 |
| 14 | IO216PDB3 |
| 15 | IO216NDB3 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB3 |
| 19 | IO212PDB3 |
| 20 | IO212NDB3 |
| 21 | GFC1/IO209PDB3 |
| 22 | GFC0/IO209NDB3 |
| 23 | GFB1/IO208PDB3 |
| 24 | GFB0/IO208NDB3 |
| 25 | VCOMPLF |
| 26 | GFA0/IO207NPB3 |
| 27 | VCCPLF |
| 28 | GFA1/IO207PPB3 |
| 29 | GND |
| 30 | GFA2/IO206PDB3 |
| 31 | IO206NDB3 |
| 32 | GFB2/IO205PDB3 |
| 33 | IO205NDB3 |
| 34 | GFC2/IO204PDB3 |
| 35 | IO204NDB3 |
| 36 | VCC |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 37 | IO199PDB3 |
| 38 | IO199NDB3 |
| 39 | IO197PSB3 |
| 40 | VCCIB3 |
| 41 | GND |
| 42 | IO191PDB3 |
| 43 | IO191NDB3 |
| 44 | GEC1/IO190PDB3 |
| 45 | GEC0/IO190NDB3 |
| 46 | GEB1/IO189PDB3 |
| 47 | GEB0/IO189NDB3 |
| 48 | GEA1/IO188PDB3 |
| 49 | GEA0/IO188NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | GEA2/IO187RSB2 |
| 55 | GEB2/IO186RSB2 |
| 56 | GEC2/IO185RSB2 |
| 57 | IO184RSB2 |
| 58 | IO183RSB2 |
| 59 | IO182RSB2 |
| 60 | IO181RSB2 |
| 61 | IO180RSB2 |
| 62 | VCCIB2 |
| 63 | IO178RSB2 |
| 64 | IO176RSB2 |
| 65 | GND |
| 66 | IO174RSB2 |
| 67 | IO172RSB2 |
| 68 | IO170RSB2 |
| 69 | IO168RSB2 |
| 70 | IO166RSB2 |
| 71 | VCC |
| 72 | VCCIB2 |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 73 | IO162RSB2 |
| 74 | IO160RSB2 |
| 75 | IO158RSB2 |
| 76 | IO156RSB2 |
| 77 | IO154RSB2 |
| 78 | IO152RSB2 |
| 79 | IO150RSB2 |
| 80 | IO148RSB2 |
| 81 | GND |
| 82 | IO143RSB2 |
| 83 | IO141RSB2 |
| 84 | IO139RSB2 |
| 85 | IO137RSB2 |
| 86 | IO135RSB2 |
| 87 | IO133RSB2 |
| 88 | VCC |
| 89 | VCCIB2 |
| 90 | IO128RSB2 |
| 91 | IO126RSB2 |
| 92 | IO124RSB2 |
| 93 | IO122RSB2 |
| 94 | IO120RSB2 |
| 95 | IO118RSB2 |
| 96 | GDC2/IO116RSB2 |
| 97 | GND |
| 98 | GDB2/IO115RSB2 |
| 99 | GDA2/IO114RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |
| 108 | TDO |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO113NDB1 |
| 112 | GDA1/IO113PDB1 |
| 113 | GDB0/IO112NDB1 |
| 114 | GDB1/IO112PDB1 |
| 115 | GDC0/IO111NDB1 |
| 116 | GDC1/IO111PDB1 |
| 117 | IO109NDB1 |
| 118 | IO109PDB1 |
| 119 | IO106NDB1 |
| 120 | IO106PDB1 |
| 121 | IO104PSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | IO99NDB1 |
| 125 | IO99PDB1 |
| 126 | NC |
| 127 | IO96NDB1 |
| 128 | GCC2/IO96PDB1 |
| 129 | GCB2/IO95PSB1 |
| 130 | GND |
| 131 | GCA2/IO94PSB1 |
| 132 | GCA1/IO93PDB1 |
| 133 | GCA0/IO93NDB1 |
| 134 | GCB0/IO92NDB1 |
| 135 | GCB1/IO92PDB1 |
| 136 | GCC0/IO91NDB1 |
| 137 | GCC1/IO91PDB1 |
| 138 | IO88NDB1 |
| 139 | IO88PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO86PSB1 |
| 144 | IO84NDB1 |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 145 | IO84PDB1 |
| 146 | IO82NDB1 |
| 147 | IO82PDB1 |
| 148 | IO80NDB1 |
| 149 | GBC2/IO80PDB1 |
| 150 | IO79NDB1 |
| 151 | GBB2/IO79PDB1 |
| 152 | IO78NDB1 |
| 153 | GBA2/IO78PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO77RSB0 |
| 159 | GBA0/IO76RSB0 |
| 160 | GBB1/IO75RSB0 |
| 161 | GBB0/IO74RSB0 |
| 162 | GND |
| 163 | GBC1/IO73RSB0 |
| 164 | GBC0/IO72RSB0 |
| 165 | IO70RSB0 |
| 166 | IO67RSB0 |
| 167 | IO63RSB0 |
| 168 | IO60RSB0 |
| 169 | IO57RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO54RSB0 |
| 173 | IO51RSB0 |
| 174 | IO48RSB0 |
| 175 | IO45RSB0 |
| 176 | IO42RSB0 |
| 177 | IO40RSB0 |
| 178 | GND |
| 179 | IO38RSB0 |
| 180 | IO35RSB0 |

| PQ208 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| 181 | IO33RSB0 |
| 182 | IO31RSB0 |
| 183 | IO29RSB0 |
| 184 | IO27RSB0 |
| 185 | IO25RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO22RSB0 |
| 189 | IO20RSB0 |
| 190 | IO18RSB0 |
| 191 | IO16RSB0 |
| 192 | IO15RSB0 |
| 193 | IO14RSB0 |
| 194 | IO13RSB0 |
| 195 | GND |
| 196 | IO12RSB0 |
| 197 | IO11RSB0 |
| 198 | IO10RSB0 |
| 199 | IO09RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

4.7 FG144

FIGURE 4-7 • FG144—BOTTOMVIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO04RSB0 |
| A4 | GAB1/IO05RSB0 |
| A5 | IO08RSB0 |
| A6 | GND |
| A7 | IO11RSB0 |
| A8 | VCC |
| A9 | IO16RSB0 |
| A10 | GBA0/IO23RSB0 |
| A11 | GBA1/IO24RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO53RSB1 |
| B2 | GND |
| B3 | GAA0/IO02RSB0 |
| B4 | GAA1/IO03RSB0 |
| B5 | IO00RSB0 |
| B6 | IO10RSB0 |
| B7 | IO12RSB0 |
| B8 | IO14RSB0 |
| B9 | GBB0/IO21RSB0 |
| B10 | GBB1/IO22RSB0 |
| B11 | GND |
| B12 | VMV0 |
| C1 | IO95RSB1 |
| C2 | GFA2/IO83RSB1 |
| C3 | GAC2/IO94RSB1 |
| C4 | VCC |
| C5 | IO01RSB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO17RSB0 |
| C10 | GBA2/IO25RSB0 |
| C11 | IO26RSB0 |
| C12 | GBC2/IO29RSB0 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| D1 | IO91RSB1 |
| D2 | IO92RSB1 |
| D3 | IO93RSB1 |
| D4 | GAA2/IO51RSB1 |
| D5 | GAC0/IO06RSB0 |
| D6 | GAC1/IO07RSB0 |
| D7 | GBC0/IO19RSB0 |
| D8 | GBC1/IO20RSB0 |
| D9 | GBB2/IO27RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | GCB1/IO37RSB0 |
| E1 | VCC |
| E2 | GFC0/IO88RSB1 |
| E3 | GFC1/IO89RSB1 |
| E4 | VCCIB1 |
| E5 | IO52RSB1 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO35RSB0 |
| E9 | VCCIB0 |
| E10 | VCC |
| E11 | GCA0/IO40RSB0 |
| E12 | IO30RSB0 |
| F1 | GFB0/IO86RSB1 |
| F2 | VCOMPLF |
| F3 | GFB1/IO87RSB1 |
| F4 | IO90RSB1 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO36RSB0 |
| F9 | GCB0/IO38RSB0 |
| F10 | GND |
| F11 | GCA1/IO39RSB0 |
| F12 | GCA2/IO41RSB0 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| G1 | GFA1/IO84RSB1 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO85RSB1 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO45RSB0 |
| G9 | IO32RSB0 |
| G10 | GCC2/IO43RSB0 |
| G11 | IO31RSB0 |
| G12 | GCB2/IO42RSB0 |
| H1 | VCC |
| H2 | GFB2/IO82RSB1 |
| H3 | GFC2/IO81RSB1 |
| H4 | GEC1/IO77RSB1 |
| H5 | VCC |
| H6 | IO34RSB0 |
| H7 | IO44RSB0 |
| H8 | GDB2/IO55RSB1 |
| H9 | GDC0/IO46RSB0 |
| H10 | VCCIB0 |
| H11 | IO33RSB0 |
| H12 | VCC |
| J1 | GEB1/IO75RSB1 |
| J2 | IO78RSB1 |
| J3 | VCCIB1 |
| J4 | GEC0/IO76RSB1 |
| J5 | IO79RSB1 |
| J6 | IO80RSB1 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO54RSB1 |
| J10 | TDO |
| J11 | GDA1/IO49RSB0 |
| J12 | GDB1/IO47RSB0 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P060 Function |
| K1 | GEB0/IO74RSB1 |
| K2 | GEA1/IO73RSB1 |
| K3 | GEA0/IO72RSB1 |
| K4 | GEA2/IO71RSB1 |
| K5 | IO65RSB1 |
| K6 | IO64RSB1 |
| K7 | GND |
| K8 | IO57RSB1 |
| K9 | GDC2/IO56RSB1 |
| K10 | GND |
| K11 | GDA0/IO50RSB0 |
| K12 | GDB0/IO48RSB0 |
| L1 | GND |
| L2 | VMV1 |
| L3 | GEB2/IO70RSB1 |
| L4 | IO67RSB1 |
| L5 | VCCIB1 |
| L6 | IO62RSB1 |
| L7 | IO59RSB1 |
| L8 | IO58RSB1 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV1 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO69RSB1 |
| M3 | IO68RSB1 |
| M4 | IO66RSB1 |
| M5 | IO63RSB1 |
| M6 | IO61RSB1 |
| M7 | IO60RSB1 |
| M8 | NC |
| M9 | TDI |
| M10 | VCCIB1 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO11RSB0 |
| A6 | GND |
| A7 | IO18RSB0 |
| A8 | VCC |
| A9 | IO25RSB0 |
| A10 | GBA0/IO39RSB0 |
| A11 | GBA1/IO40RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO69RSB1 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO08RSB0 |
| B6 | IO14RSB0 |
| B7 | IO19RSB0 |
| B8 | IO22RSB0 |
| B9 | GBB0/IO37RSB0 |
| B10 | GBB1/IO38RSB0 |
| B11 | GND |
| B12 | VMV0 |
| C1 | IO132RSB1 |
| C2 | GFA2/IO120RSB1 |
| C3 | GAC2/IO131RSB1 |
| C4 | VCC |
| C5 | IO10RSB0 |
| C6 | IO12RSB0 |
| C7 | IO21RSB0 |
| C8 | IO24RSB0 |
| C9 | IO27RSB0 |
| C10 | GBA2/IO41RSB0 |
| C11 | IO42RSB0 |
| C12 | GBC2/IO45RSB0 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| D1 | IO128RSB1 |
| D2 | IO129RSB1 |
| D3 | IO130RSB1 |
| D4 | GAA2/IO67RSB1 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO35RSB0 |
| D8 | GBC1/IO36RSB0 |
| D9 | GBB2/IO43RSB0 |
| D10 | IO28RSB0 |
| D11 | IO44RSB0 |
| D12 | GCB1/IO53RSB0 |
| E1 | VCC |
| E2 | GFC0/IO125RSB1 |
| E3 | GFC1/IO126RSB1 |
| E4 | VCCIB1 |
| E5 | IO68RSB1 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO51RSB0 |
| E9 | VCCIB0 |
| E10 | VCC |
| E11 | GCA0/IO56RSB0 |
| E12 | IO46RSB0 |
| F1 | GFB0/IO123RSB1 |
| F2 | VCOMPLF |
| F3 | GFB1/IO124RSB1 |
| F4 | IO127RSB1 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO52RSB0 |
| F9 | GCB0/IO54RSB0 |
| F10 | GND |
| F11 | GCA1/IO55RSB0 |
| F12 | GCA2/IO57RSB0 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P125 Function |
| G1 | GFA1/IO121RSB1 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO122RSB1 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO61RSB0 |
| G9 | IO48RSB0 |
| G10 | GCC2/IO59RSB0 |
| G11 | IO47RSB0 |
| G12 | GCB2/IO58RSB0 |
| H1 | VCC |
| H2 | GFB2/IO119RSB1 |
| H3 | GFC2/IO118RSB1 |
| H4 | GEC1/IO112RSB1 |
| H5 | VCC |
| H6 | IO50RSB0 |
| H7 | IO60RSB0 |
| H8 | GDB2/IO71RSB1 |
| H9 | GDC0/IO62RSB0 |
| H10 | VCCIB0 |
| H11 | IO49RSB0 |
| H12 | VCC |
| J1 | GEB1/IO110RSB1 |
| J2 | IO115RSB1 |
| J3 | VCCIB1 |
| J4 | GEC0/IO111RSB1 |
| J5 | IO116RSB1 |
| J6 | IO117RSB1 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO70RSB1 |
| J10 | TDO |
| J11 | GDA1/IO65RSB0 |
| J12 | GDB1/IO63RSB0 |

| FG144 | |
|-------------------|------------------------|
| Pin Number | A3P125 Function |
| K1 | GEB0/IO109RSB1 |
| K2 | GEA1/IO108RSB1 |
| K3 | GEA0/IO107RSB1 |
| K4 | GEA2/IO106RSB1 |
| K5 | IO100RSB1 |
| K6 | IO98RSB1 |
| K7 | GND |
| K8 | IO73RSB1 |
| K9 | GDC2/IO72RSB1 |
| K10 | GND |
| K11 | GDA0/IO66RSB0 |
| K12 | GDB0/IO64RSB0 |
| L1 | GND |
| L2 | VMV1 |
| L3 | GEB2/IO105RSB1 |
| L4 | IO102RSB1 |
| L5 | VCCIB1 |
| L6 | IO95RSB1 |
| L7 | IO85RSB1 |
| L8 | IO74RSB1 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV1 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO104RSB1 |
| M3 | IO103RSB1 |
| M4 | IO101RSB1 |
| M5 | IO97RSB1 |
| M6 | IO94RSB1 |
| M7 | IO86RSB1 |
| M8 | IO75RSB1 |
| M9 | TDI |
| M10 | VCCIB1 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO29RSB0 |
| A8 | VCC |
| A9 | IO33RSB0 |
| A10 | GBA0/IO39RSB0 |
| A11 | GBA1/IO40RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO117UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO22RSB0 |
| B8 | IO30RSB0 |
| B9 | GBB0/IO37RSB0 |
| B10 | GBB1/IO38RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO117VDB3 |
| C2 | GFA2/IO107PPB3 |
| C3 | GAC2/IO116UDB3 |
| C4 | VCC |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO24RSB0 |
| C8 | IO31RSB0 |
| C9 | IO34RSB0 |
| C10 | GBA2/IO41PDB1 |
| C11 | IO41NDB1 |
| C12 | GBC2/IO43PPB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| D1 | IO112NDB3 |
| D2 | IO112PDB3 |
| D3 | IO116VDB3 |
| D4 | GAA2/IO118UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO35RSB0 |
| D8 | GBC1/IO36RSB0 |
| D9 | GBB2/IO42PDB1 |
| D10 | IO42NDB1 |
| D11 | IO43NPB1 |
| D12 | GCB1/IO49PPB1 |
| E1 | VCC |
| E2 | GFC0/IO110NDB3 |
| E3 | GFC1/IO110PDB3 |
| E4 | VCCIB3 |
| E5 | IO118VPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO48PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO50NDB1 |
| E12 | IO51NDB1 |
| F1 | GFB0/IO109NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO109PPB3 |
| F4 | IO107NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO48NDB1 |
| F9 | GCB0/IO49NPB1 |
| F10 | GND |
| F11 | GCA1/IO50PDB1 |
| F12 | GCA2/IO51PDB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| G1 | GFA1/IO108PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO108NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO58UPB1 |
| G9 | IO53NDB1 |
| G10 | GCC2/IO53PDB1 |
| G11 | IO52NDB1 |
| G12 | GCB2/IO52PDB1 |
| H1 | VCC |
| H2 | GFB2/IO106PDB3 |
| H3 | GFC2/IO105PSB3 |
| H4 | GEC1/IO100PDB3 |
| H5 | VCC |
| H6 | IO79RSB2 |
| H7 | IO65RSB2 |
| H8 | GDB2/IO62RSB2 |
| H9 | GDC0/IO58VPB1 |
| H10 | VCCIB1 |
| H11 | IO54PSB1 |
| H12 | VCC |
| J1 | GEB1/IO99PDB3 |
| J2 | IO106NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO100NDB3 |
| J5 | IO88RSB2 |
| J6 | IO81RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO61RSB2 |
| J10 | TDO |
| J11 | GDA1/IO60UDB1 |
| J12 | GDB1/IO59UDB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| K1 | GEB0/IO99NDB3 |
| K2 | GEA1/IO98PDB3 |
| K3 | GEA0/IO98NDB3 |
| K4 | GEA2/IO97RSB2 |
| K5 | IO90RSB2 |
| K6 | IO84RSB2 |
| K7 | GND |
| K8 | IO66RSB2 |
| K9 | GDC2/IO63RSB2 |
| K10 | GND |
| K11 | GDA0/IO60VDB1 |
| K12 | GDB0/IO59VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO96RSB2 |
| L4 | IO91RSB2 |
| L5 | VCCIB2 |
| L6 | IO82RSB2 |
| L7 | IO80RSB2 |
| L8 | IO72RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO95RSB2 |
| M3 | IO92RSB2 |
| M4 | IO89RSB2 |
| M5 | IO87RSB2 |
| M6 | IO85RSB2 |
| M7 | IO78RSB2 |
| M8 | IO76RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO30RSB0 |
| A8 | VCC |
| A9 | IO34RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO154UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO23RSB0 |
| B8 | IO31RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO154VDB3 |
| C2 | GFA2/IO144PPB3 |
| C3 | GAC2/IO153UDB3 |
| C4 | VCC |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO25RSB0 |
| C8 | IO32RSB0 |
| C9 | IO53RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| D1 | IO149NDB3 |
| D2 | IO149PDB3 |
| D3 | IO153VDB3 |
| D4 | GAA2/IO155UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO68PPB1 |
| E1 | VCC |
| E2 | GFC0/IO147NDB3 |
| E3 | GFC1/IO147PDB3 |
| E4 | VCCIB3 |
| E5 | IO155VPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO67PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO69NDB1 |
| E12 | IO70NDB1 |
| F1 | GFB0/IO146NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO146PPB3 |
| F4 | IO144NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO67NDB1 |
| F9 | GCB0/IO68NPB1 |
| F10 | GND |
| F11 | GCA1/IO69PDB1 |
| F12 | GCA2/IO70PDB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| G1 | GFA1/IO145PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO145NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO77UPB1 |
| G9 | IO72NDB1 |
| G10 | GCC2/IO72PDB1 |
| G11 | IO71NDB1 |
| G12 | GCB2/IO71PDB1 |
| H1 | VCC |
| H2 | GFB2/IO143PDB3 |
| H3 | GFC2/IO142PSB3 |
| H4 | GEC1/IO137PDB3 |
| H5 | VCC |
| H6 | IO75PDB1 |
| H7 | IO75NDB1 |
| H8 | GDB2/IO81RSB2 |
| H9 | GDC0/IO77VPB1 |
| H10 | VCCIB1 |
| H11 | IO73PSB1 |
| H12 | VCC |
| J1 | GEB1/IO136PDB3 |
| J2 | IO143NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO137NDB3 |
| J5 | IO125RSB2 |
| J6 | IO116RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO80RSB2 |
| J10 | TDO |
| J11 | GDA1/IO79UDB1 |
| J12 | GDB1/IO78UDB1 |

| FG144 | |
|-------------------|------------------------|
| Pin Number | A3P400 Function |
| K1 | GEB0/IO136NDB3 |
| K2 | GEA1/IO135PDB3 |
| K3 | GEA0/IO135NDB3 |
| K4 | GEA2/IO134RSB2 |
| K5 | IO127RSB2 |
| K6 | IO121RSB2 |
| K7 | GND |
| K8 | IO104RSB2 |
| K9 | GDC2/IO82RSB2 |
| K10 | GND |
| K11 | GDA0/IO79VDB1 |
| K12 | GDB0/IO78VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO133RSB2 |
| L4 | IO128RSB2 |
| L5 | VCCIB2 |
| L6 | IO119RSB2 |
| L7 | IO114RSB2 |
| L8 | IO110RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO132RSB2 |
| M3 | IO129RSB2 |
| M4 | IO126RSB2 |
| M5 | IO124RSB2 |
| M6 | IO122RSB2 |
| M7 | IO117RSB2 |
| M8 | IO115RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO34RSB0 |
| A8 | VCC |
| A9 | IO50RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO173PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO19RSB0 |
| B7 | IO31RSB0 |
| B8 | IO39RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO173NDB3 |
| C2 | GFA2/IO161PPB3 |
| C3 | GAC2/IO172PDB3 |
| C4 | VCC |
| C5 | IO16RSB0 |
| C6 | IO25RSB0 |
| C7 | IO28RSB0 |
| C8 | IO42RSB0 |
| C9 | IO45RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| D1 | IO169PDB3 |
| D2 | IO169NDB3 |
| D3 | IO172NDB3 |
| D4 | GAA2/IO174PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO70PPB1 |
| E1 | VCC |
| E2 | GFC0/IO164NDB3 |
| E3 | GFC1/IO164PDB3 |
| E4 | VCCIB3 |
| E5 | IO174NPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO69PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO71NDB1 |
| E12 | IO72NDB1 |
| F1 | GFB0/IO163NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO163PPB3 |
| F4 | IO161NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO69NDB1 |
| F9 | GCB0/IO70NPB1 |
| F10 | GND |
| F11 | GCA1/IO71PDB1 |
| F12 | GCA2/IO72PDB1 |

| FG144 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| G1 | GFA1/IO162PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO162NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO86PPB1 |
| G9 | IO74NDB1 |
| G10 | GCC2/IO74PDB1 |
| G11 | IO73NDB1 |
| G12 | GCB2/IO73PDB1 |
| H1 | VCC |
| H2 | GFB2/IO160PDB3 |
| H3 | GFC2/IO159PSB3 |
| H4 | GEC1/IO146PDB3 |
| H5 | VCC |
| H6 | IO80PDB1 |
| H7 | IO80NDB1 |
| H8 | GDB2/IO90RSB2 |
| H9 | GDC0/IO86NPB1 |
| H10 | VCCIB1 |
| H11 | IO84PSB1 |
| H12 | VCC |
| J1 | GEB1/IO145PDB3 |
| J2 | IO160NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO146NDB3 |
| J5 | IO129RSB2 |
| J6 | IO131RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO89RSB2 |
| J10 | TDO |
| J11 | GDA1/IO88PDB1 |
| J12 | GDB1/IO87PDB1 |

| FG144 | |
|-------------------|------------------------|
| Pin Number | A3P600 Function |
| K1 | GEB0/IO145NDB3 |
| K2 | GEA1/IO144PDB3 |
| K3 | GEA0/IO144NDB3 |
| K4 | GEA2/IO143RSB2 |
| K5 | IO119RSB2 |
| K6 | IO111RSB2 |
| K7 | GND |
| K8 | IO94RSB2 |
| K9 | GDC2/IO91RSB2 |
| K10 | GND |
| K11 | GDA0/IO88NDB1 |
| K12 | GDB0/IO87NDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO142RSB2 |
| L4 | IO136RSB2 |
| L5 | VCCIB2 |
| L6 | IO115RSB2 |
| L7 | IO103RSB2 |
| L8 | IO97RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO141RSB2 |
| M3 | IO138RSB2 |
| M4 | IO123RSB2 |
| M5 | IO126RSB2 |
| M6 | IO134RSB2 |
| M7 | IO108RSB2 |
| M8 | IO99RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO44RSB0 |
| A8 | VCC |
| A9 | IO69RSB0 |
| A10 | GBA0/IO76RSB0 |
| A11 | GBA1/IO77RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO224PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO26RSB0 |
| B7 | IO35RSB0 |
| B8 | IO60RSB0 |
| B9 | GBB0/IO74RSB0 |
| B10 | GBB1/IO75RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO224NDB3 |
| C2 | GFA2/IO206PPB3 |
| C3 | GAC2/IO223PDB3 |
| C4 | VCC |
| C5 | IO16RSB0 |
| C6 | IO29RSB0 |
| C7 | IO32RSB0 |
| C8 | IO63RSB0 |
| C9 | IO66RSB0 |
| C10 | GBA2/IO78PDB1 |
| C11 | IO78NDB1 |
| C12 | GBC2/IO80PPB1 |

| FG144 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| D1 | IO213PDB3 |
| D2 | IO213NDB3 |
| D3 | IO223NDB3 |
| D4 | GAA2/IO225PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO72RSB0 |
| D8 | GBC1/IO73RSB0 |
| D9 | GBB2/IO79PDB1 |
| D10 | IO79NDB1 |
| D11 | IO80NPB1 |
| D12 | GCB1/IO92PPB1 |
| E1 | VCC |
| E2 | GFC0/IO209NDB3 |
| E3 | GFC1/IO209PDB3 |
| E4 | VCCIB3 |
| E5 | IO225NPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO91PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO93NDB1 |
| E12 | IO94NDB1 |
| F1 | GFB0/IO208NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO208PPB3 |
| F4 | IO206NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO91NDB1 |
| F9 | GCB0/IO92NPB1 |
| F10 | GND |
| F11 | GCA1/IO93PDB1 |
| F12 | GCA2/IO94PDB1 |

| FG144 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| G1 | GFA1/IO207PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO207NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO111PPB1 |
| G9 | IO96NDB1 |
| G10 | GCC2/IO96PDB1 |
| G11 | IO95NDB1 |
| G12 | GCB2/IO95PDB1 |
| H1 | VCC |
| H2 | GFB2/IO205PDB3 |
| H3 | GFC2/IO204PSB3 |
| H4 | GEC1/IO190PDB3 |
| H5 | VCC |
| H6 | IO105PDB1 |
| H7 | IO105NDB1 |
| H8 | GDB2/IO115RSB2 |
| H9 | GDC0/IO111NPB1 |
| H10 | VCCIB1 |
| H11 | IO101PSB1 |
| H12 | VCC |
| J1 | GEB1/IO189PDB3 |
| J2 | IO205NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO190NDB3 |
| J5 | IO160RSB2 |
| J6 | IO157RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO114RSB2 |
| J10 | TDO |
| J11 | GDA1/IO113PDB1 |
| J12 | GDB1/IO112PDB1 |

| FG144 | |
|-------------------|-------------------------|
| Pin Number | A3P1000 Function |
| K1 | GEB0/IO189NDB3 |
| K2 | GEA1/IO188PDB3 |
| K3 | GEA0/IO188NDB3 |
| K4 | GEA2/IO187RSB2 |
| K5 | IO169RSB2 |
| K6 | IO152RSB2 |
| K7 | GND |
| K8 | IO117RSB2 |
| K9 | GDC2/IO116RSB2 |
| K10 | GND |
| K11 | GDA0/IO113NDB1 |
| K12 | GDB0/IO112NDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO186RSB2 |
| L4 | IO172RSB2 |
| L5 | VCCIB2 |
| L6 | IO153RSB2 |
| L7 | IO144RSB2 |
| L8 | IO140RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO185RSB2 |
| M3 | IO173RSB2 |
| M4 | IO168RSB2 |
| M5 | IO161RSB2 |
| M6 | IO156RSB2 |
| M7 | IO145RSB2 |
| M8 | IO141RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

4.8 FG256

FIGURE 4-8 • FG256—BOTTOM VIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO07RSB0 |
| A6 | IO10RSB0 |
| A7 | IO11RSB0 |
| A8 | IO15RSB0 |
| A9 | IO20RSB0 |
| A10 | IO25RSB0 |
| A11 | IO29RSB0 |
| A12 | IO33RSB0 |
| A13 | GBB1/IO38RSB0 |
| A14 | GBA0/IO39RSB0 |
| A15 | GBA1/IO40RSB0 |
| A16 | GND |
| B1 | GAB2/IO117UDB3 |
| B2 | GAA2/IO118UDB3 |
| B3 | NC |
| B4 | GAB1/IO03RSB0 |
| B5 | IO06RSB0 |
| B6 | IO09RSB0 |
| B7 | IO12RSB0 |
| B8 | IO16RSB0 |
| B9 | IO21RSB0 |
| B10 | IO26RSB0 |
| B11 | IO30RSB0 |
| B12 | GBC1/IO36RSB0 |
| B13 | GBB0/IO37RSB0 |
| B14 | NC |
| B15 | GBA2/IO41PDB1 |
| B16 | IO41NDB1 |
| C1 | IO117VDB3 |
| C2 | IO118VDB3 |
| C3 | NC |
| C4 | NC |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO13RSB0 |
| C8 | IO17RSB0 |
| C9 | IO22RSB0 |
| C10 | IO27RSB0 |
| C11 | IO31RSB0 |
| C12 | GBC0/IO35RSB0 |
| C13 | IO34RSB0 |
| C14 | NC |
| C15 | IO42NPB1 |
| C16 | IO44PDB1 |
| D1 | IO114VDB3 |
| D2 | IO114UDB3 |
| D3 | GAC2/IO116UDB3 |
| D4 | NC |
| D5 | GNDQ |
| D6 | IO08RSB0 |
| D7 | IO14RSB0 |
| D8 | IO18RSB0 |
| D9 | IO23RSB0 |
| D10 | IO28RSB0 |
| D11 | IO32RSB0 |
| D12 | GNDQ |
| D13 | NC |
| D14 | GBB2/IO42PPB1 |
| D15 | NC |
| D16 | IO44NDB1 |
| E1 | IO113PDB3 |
| E2 | NC |
| E3 | IO116VDB3 |
| E4 | IO115UDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO19RSB0 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| E9 | IO24RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |
| E13 | GBC2/IO43PDB1 |
| E14 | IO46RSB1 |
| E15 | NC |
| E16 | IO45PDB1 |
| F1 | IO113NDB3 |
| F2 | IO112PPB3 |
| F3 | NC |
| F4 | IO115VDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO43NDB1 |
| F14 | NC |
| F15 | IO47PPB1 |
| F16 | IO45NDB1 |
| G1 | IO111NDB3 |
| G2 | IO111PDB3 |
| G3 | IO112NPB3 |
| G4 | GFC1/IO110PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| G13 | GCC1/IO48PPB1 |
| G14 | IO47NPB1 |
| G15 | IO54PDB1 |
| G16 | IO54NDB1 |
| H1 | GFB0/IO109NPB3 |
| H2 | GFA0/IO108NDB3 |
| H3 | GFB1/IO109PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO110NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO48NPB1 |
| H13 | GCB1/IO49PPB1 |
| H14 | GCA0/IO50NPB1 |
| H15 | NC |
| H16 | GCB0/IO49NPB1 |
| J1 | GFA2/IO107PPB3 |
| J2 | GFA1/IO108PDB3 |
| J3 | VCCPLF |
| J4 | IO106NDB3 |
| J5 | GFB2/IO106PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO52PPB1 |
| J13 | GCA1/IO50PPB1 |
| J14 | GCC2/IO53PPB1 |
| J15 | NC |
| J16 | GCA2/IO51PDB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| K1 | GFC2/IO105PDB3 |
| K2 | IO107NPB3 |
| K3 | IO104PPB3 |
| K4 | NC |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO52NPB1 |
| K14 | IO55RSB1 |
| K15 | IO53NPB1 |
| K16 | IO51NDB1 |
| L1 | IO105NDB3 |
| L2 | IO104NPB3 |
| L3 | NC |
| L4 | IO102RSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO59VPB1 |
| L14 | IO57VDB1 |
| L15 | IO57UDB1 |
| L16 | IO56PDB1 |
| M1 | IO103PDB3 |
| M2 | NC |
| M3 | IO101NPB3 |
| M4 | GEC0/IO100NPB3 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | NC |
| M9 | IO74RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | NC |
| M14 | GDB1/IO59UPB1 |
| M15 | GDC1/IO58UDB1 |
| M16 | IO56NDB1 |
| N1 | IO103NDB3 |
| N2 | IO101PPB3 |
| N3 | GEC1/IO100PPB3 |
| N4 | NC |
| N5 | GNDQ |
| N6 | GEA2/IO97RSB2 |
| N7 | IO86RSB2 |
| N8 | IO82RSB2 |
| N9 | IO75RSB2 |
| N10 | IO69RSB2 |
| N11 | IO64RSB2 |
| N12 | GNDQ |
| N13 | NC |
| N14 | VJTAG |
| N15 | GDC0/IO58VDB1 |
| N16 | GDA1/IO60UDB1 |
| P1 | GEB1/IO99PDB3 |
| P2 | GEB0/IO99NDB3 |
| P3 | NC |
| P4 | NC |
| P5 | IO92RSB2 |
| P6 | IO89RSB2 |
| P7 | IO85RSB2 |
| P8 | IO81RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| P9 | IO76RSB2 |
| P10 | IO71RSB2 |
| P11 | IO66RSB2 |
| P12 | NC |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO60VDB1 |
| R1 | GEA1/IO98PDB3 |
| R2 | GEA0/IO98NDB3 |
| R3 | NC |
| R4 | GEC2/IO95RSB2 |
| R5 | IO91RSB2 |
| R6 | IO88RSB2 |
| R7 | IO84RSB2 |
| R8 | IO80RSB2 |
| R9 | IO77RSB2 |
| R10 | IO72RSB2 |
| R11 | IO68RSB2 |
| R12 | IO65RSB2 |
| R13 | GDB2/IO62RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO94RSB2 |
| T3 | GEB2/IO96RSB2 |
| T4 | IO93RSB2 |
| T5 | IO90RSB2 |
| T6 | IO87RSB2 |
| T7 | IO83RSB2 |
| T8 | IO79RSB2 |
| T9 | IO78RSB2 |
| T10 | IO73RSB2 |
| T11 | IO70RSB2 |
| T12 | GDC2/IO63RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P250 Function |
| T13 | IO67RSB2 |
| T14 | GDA2/IO61RSB2 |
| T15 | TMS |
| T16 | GND |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO16RSB0 |
| A6 | IO17RSB0 |
| A7 | IO22RSB0 |
| A8 | IO28RSB0 |
| A9 | IO34RSB0 |
| A10 | IO37RSB0 |
| A11 | IO41RSB0 |
| A12 | IO43RSB0 |
| A13 | GBB1/IO57RSB0 |
| A14 | GBA0/IO58RSB0 |
| A15 | GBA1/IO59RSB0 |
| A16 | GND |
| B1 | GAB2/IO154UDB3 |
| B2 | GAA2/IO155UDB3 |
| B3 | IO12RSB0 |
| B4 | GAB1/IO03RSB0 |
| B5 | IO13RSB0 |
| B6 | IO14RSB0 |
| B7 | IO21RSB0 |
| B8 | IO27RSB0 |
| B9 | IO32RSB0 |
| B10 | IO38RSB0 |
| B11 | IO42RSB0 |
| B12 | GBC1/IO55RSB0 |
| B13 | GBB0/IO56RSB0 |
| B14 | IO44RSB0 |
| B15 | GBA2/IO60PDB1 |
| B16 | IO60NDB1 |
| C1 | IO154VDB3 |
| C2 | IO155VDB3 |
| C3 | IO11RSB0 |
| C4 | IO07RSB0 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO20RSB0 |
| C8 | IO24RSB0 |
| C9 | IO33RSB0 |
| C10 | IO39RSB0 |
| C11 | IO45RSB0 |
| C12 | GBC0/IO54RSB0 |
| C13 | IO48RSB0 |
| C14 | VMV0 |
| C15 | IO61NPB1 |
| C16 | IO63PDB1 |
| D1 | IO151VDB3 |
| D2 | IO151UDB3 |
| D3 | GAC2/IO153UDB3 |
| D4 | IO06RSB0 |
| D5 | GNDQ |
| D6 | IO10RSB0 |
| D7 | IO19RSB0 |
| D8 | IO26RSB0 |
| D9 | IO30RSB0 |
| D10 | IO40RSB0 |
| D11 | IO46RSB0 |
| D12 | GNDQ |
| D13 | IO47RSB0 |
| D14 | GBB2/IO61PPB1 |
| D15 | IO53RSB0 |
| D16 | IO63NDB1 |
| E1 | IO150PDB3 |
| E2 | IO08RSB0 |
| E3 | IO153VDB3 |
| E4 | IO152VDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO25RSB0 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| E9 | IO31RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |
| E13 | GBC2/IO62PDB1 |
| E14 | IO65RSB1 |
| E15 | IO52RSB0 |
| E16 | IO66PDB1 |
| F1 | IO150NDB3 |
| F2 | IO149NPB3 |
| F3 | IO09RSB0 |
| F4 | IO152UDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO62NDB1 |
| F14 | IO49RSB0 |
| F15 | IO64PPB1 |
| F16 | IO66NDB1 |
| G1 | IO148NDB3 |
| G2 | IO148PDB3 |
| G3 | IO149PPB3 |
| G4 | GFC1/IO147PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| G13 | GCC1/IO67PPB1 |
| G14 | IO64NPB1 |
| G15 | IO73PDB1 |
| G16 | IO73NDB1 |
| H1 | GFB0/IO146NPB3 |
| H2 | GFA0/IO145NDB3 |
| H3 | GFB1/IO146PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO147NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO67NPB1 |
| H13 | GCB1/IO68PPB1 |
| H14 | GCA0/IO69NPB1 |
| H15 | NC |
| H16 | GCB0/IO68NPB1 |
| J1 | GFA2/IO144PPB3 |
| J2 | GFA1/IO145PDB3 |
| J3 | VCCPLF |
| J4 | IO143NDB3 |
| J5 | GFB2/IO143PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO71PPB1 |
| J13 | GCA1/IO69PPB1 |
| J14 | GCC2/IO72PPB1 |
| J15 | NC |
| J16 | GCA2/IO70PDB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| K1 | GFC2/IO142PDB3 |
| K2 | IO144NPB3 |
| K3 | IO141PPB3 |
| K4 | IO120RSB2 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO71NPB1 |
| K14 | IO74RSB1 |
| K15 | IO72NPB1 |
| K16 | IO70NDB1 |
| L1 | IO142NDB3 |
| L2 | IO141NPB3 |
| L3 | IO125RSB2 |
| L4 | IO139RSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO78VPB1 |
| L14 | IO76VDB1 |
| L15 | IO76UDB1 |
| L16 | IO75PDB1 |
| M1 | IO140PDB3 |
| M2 | IO130RSB2 |
| M3 | IO138NPB3 |
| M4 | GEC0/IO137NPB3 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO108RSB2 |
| M9 | IO101RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO83RSB2 |
| M14 | GDB1/IO78UPB1 |
| M15 | GDC1/IO77UDB1 |
| M16 | IO75NDB1 |
| N1 | IO140NDB3 |
| N2 | IO138PPB3 |
| N3 | GEC1/IO137PPB3 |
| N4 | IO131RSB2 |
| N5 | GNDQ |
| N6 | GEA2/IO134RSB2 |
| N7 | IO117RSB2 |
| N8 | IO111RSB2 |
| N9 | IO99RSB2 |
| N10 | IO94RSB2 |
| N11 | IO87RSB2 |
| N12 | GNDQ |
| N13 | IO93RSB2 |
| N14 | VJTAG |
| N15 | GDC0/IO77VDB1 |
| N16 | GDA1/IO79UDB1 |
| P1 | GEB1/IO136PDB3 |
| P2 | GEB0/IO136NDB3 |
| P3 | VMV2 |
| P4 | IO129RSB2 |
| P5 | IO128RSB2 |
| P6 | IO122RSB2 |
| P7 | IO115RSB2 |
| P8 | IO110RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| P9 | IO98RSB2 |
| P10 | IO95RSB2 |
| P11 | IO88RSB2 |
| P12 | IO84RSB2 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO79VDB1 |
| R1 | GEA1/IO135PDB3 |
| R2 | GEA0/IO135NDB3 |
| R3 | IO127RSB2 |
| R4 | GEC2/IO132RSB2 |
| R5 | IO123RSB2 |
| R6 | IO118RSB2 |
| R7 | IO112RSB2 |
| R8 | IO106RSB2 |
| R9 | IO100RSB2 |
| R10 | IO96RSB2 |
| R11 | IO89RSB2 |
| R12 | IO85RSB2 |
| R13 | GDB2/IO81RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO126RSB2 |
| T3 | GEB2/IO133RSB2 |
| T4 | IO124RSB2 |
| T5 | IO116RSB2 |
| T6 | IO113RSB2 |
| T7 | IO107RSB2 |
| T8 | IO105RSB2 |
| T9 | IO102RSB2 |
| T10 | IO97RSB2 |
| T11 | IO92RSB2 |
| T12 | GDC2/IO82RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P400 Function |
| T13 | IO86RSB2 |
| T14 | GDA2/IO80RSB2 |
| T15 | TMS |
| T16 | GND |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO11RSB0 |
| A6 | IO16RSB0 |
| A7 | IO18RSB0 |
| A8 | IO28RSB0 |
| A9 | IO34RSB0 |
| A10 | IO37RSB0 |
| A11 | IO41RSB0 |
| A12 | IO43RSB0 |
| A13 | GBB1/IO57RSB0 |
| A14 | GBA0/IO58RSB0 |
| A15 | GBA1/IO59RSB0 |
| A16 | GND |
| B1 | GAB2/IO173PDB3 |
| B2 | GAA2/IO174PDB3 |
| B3 | GNDQ |
| B4 | GAB1/IO03RSB0 |
| B5 | IO13RSB0 |
| B6 | IO14RSB0 |
| B7 | IO21RSB0 |
| B8 | IO27RSB0 |
| B9 | IO32RSB0 |
| B10 | IO38RSB0 |
| B11 | IO42RSB0 |
| B12 | GBC1/IO55RSB0 |
| B13 | GBB0/IO56RSB0 |
| B14 | IO52RSB0 |
| B15 | GBA2/IO60PDB1 |
| B16 | IO60NDB1 |
| C1 | IO173NDB3 |
| C2 | IO174NDB3 |
| C3 | VMV3 |
| C4 | IO07RSB0 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO20RSB0 |
| C8 | IO24RSB0 |
| C9 | IO33RSB0 |
| C10 | IO39RSB0 |
| C11 | IO44RSB0 |
| C12 | GBC0/IO54RSB0 |
| C13 | IO51RSB0 |
| C14 | VMV0 |
| C15 | IO61NPB1 |
| C16 | IO63PDB1 |
| D1 | IO171NDB3 |
| D2 | IO171PDB3 |
| D3 | GAC2/IO172PDB3 |
| D4 | IO06RSB0 |
| D5 | GNDQ |
| D6 | IO10RSB0 |
| D7 | IO19RSB0 |
| D8 | IO26RSB0 |
| D9 | IO30RSB0 |
| D10 | IO40RSB0 |
| D11 | IO45RSB0 |
| D12 | GNDQ |
| D13 | IO50RSB0 |
| D14 | GBB2/IO61PPB1 |
| D15 | IO53RSB0 |
| D16 | IO63NDB1 |
| E1 | IO166PDB3 |
| E2 | IO167NPB3 |
| E3 | IO172NDB3 |
| E4 | IO169NDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO25RSB0 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| E9 | IO31RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |
| E13 | GBC2/IO62PDB1 |
| E14 | IO67PPB1 |
| E15 | IO64PPB1 |
| E16 | IO66PDB1 |
| F1 | IO166NDB3 |
| F2 | IO168NPB3 |
| F3 | IO167PPB3 |
| F4 | IO169PDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO62NDB1 |
| F14 | IO64NPB1 |
| F15 | IO65PPB1 |
| F16 | IO66NDB1 |
| G1 | IO165NDB3 |
| G2 | IO165PDB3 |
| G3 | IO168PPB3 |
| G4 | GFC1/IO164PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| G13 | GCC1/IO69PPB1 |
| G14 | IO65NPB1 |
| G15 | IO75PDB1 |
| G16 | IO75NDB1 |
| H1 | GFB0/IO163NPB3 |
| H2 | GFA0/IO162NDB3 |
| H3 | GFB1/IO163PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO164NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO69NPB1 |
| H13 | GCB1/IO70PPB1 |
| H14 | GCA0/IO71NPB1 |
| H15 | IO67NPB1 |
| H16 | GCB0/IO70NPB1 |
| J1 | GFA2/IO161PPB3 |
| J2 | GFA1/IO162PDB3 |
| J3 | VCCPLF |
| J4 | IO160NDB3 |
| J5 | GFB2/IO160PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO73PPB1 |
| J13 | GCA1/IO71PPB1 |
| J14 | GCC2/IO74PPB1 |
| J15 | IO80PPB1 |
| J16 | GCA2/IO72PDB1 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| K1 | GFC2/IO159PDB3 |
| K2 | IO161NPB3 |
| K3 | IO156PPB3 |
| K4 | IO129RSB2 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO73NPB1 |
| K14 | IO80NPB1 |
| K15 | IO74NPB1 |
| K16 | IO72NDB1 |
| L1 | IO159NDB3 |
| L2 | IO156NPB3 |
| L3 | IO151PPB3 |
| L4 | IO158PSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO87NPB1 |
| L14 | IO85NDB1 |
| L15 | IO85PDB1 |
| L16 | IO84PDB1 |
| M1 | IO150PDB3 |
| M2 | IO151NPB3 |
| M3 | IO147NPB3 |
| M4 | GEC0/IO146NPB3 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO117RSB2 |
| M9 | IO110RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO94RSB2 |
| M14 | GDB1/IO87PPB1 |
| M15 | GDC1/IO86PDB1 |
| M16 | IO84NDB1 |
| N1 | IO150NDB3 |
| N2 | IO147PPB3 |
| N3 | GEC1/IO146PPB3 |
| N4 | IO140RSB2 |
| N5 | GNDQ |
| N6 | GEA2/IO143RSB2 |
| N7 | IO126RSB2 |
| N8 | IO120RSB2 |
| N9 | IO108RSB2 |
| N10 | IO103RSB2 |
| N11 | IO99RSB2 |
| N12 | GNDQ |
| N13 | IO92RSB2 |
| N14 | VJTAG |
| N15 | GDC0/IO86NDB1 |
| N16 | GDA1/IO88PDB1 |
| P1 | GEB1/IO145PDB3 |
| P2 | GEB0/IO145NDB3 |
| P3 | VMV2 |
| P4 | IO138RSB2 |
| P5 | IO136RSB2 |
| P6 | IO131RSB2 |
| P7 | IO124RSB2 |
| P8 | IO119RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| P9 | IO107RSB2 |
| P10 | IO104RSB2 |
| P11 | IO97RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO88NDB1 |
| R1 | GEA1/IO144PDB3 |
| R2 | GEA0/IO144NDB3 |
| R3 | IO139RSB2 |
| R4 | GEC2/IO141RSB2 |
| R5 | IO132RSB2 |
| R6 | IO127RSB2 |
| R7 | IO121RSB2 |
| R8 | IO114RSB2 |
| R9 | IO109RSB2 |
| R10 | IO105RSB2 |
| R11 | IO98RSB2 |
| R12 | IO96RSB2 |
| R13 | GDB2/IO90RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO137RSB2 |
| T3 | GEB2/IO142RSB2 |
| T4 | IO134RSB2 |
| T5 | IO125RSB2 |
| T6 | IO123RSB2 |
| T7 | IO118RSB2 |
| T8 | IO115RSB2 |
| T9 | IO111RSB2 |
| T10 | IO106RSB2 |
| T11 | IO102RSB2 |
| T12 | GDC2/IO91RSB2 |

| FG256 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| T13 | IO93RSB2 |
| T14 | GDA2/IO89RSB2 |
| T15 | TMS |
| T16 | GND |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO16RSB0 |
| A6 | IO22RSB0 |
| A7 | IO28RSB0 |
| A8 | IO35RSB0 |
| A9 | IO45RSB0 |
| A10 | IO50RSB0 |
| A11 | IO55RSB0 |
| A12 | IO61RSB0 |
| A13 | GBB1/IO75RSB0 |
| A14 | GBA0/IO76RSB0 |
| A15 | GBA1/IO77RSB0 |
| A16 | GND |
| B1 | GAB2/IO224PDB3 |
| B2 | GAA2/IO225PDB3 |
| B3 | GNDQ |
| B4 | GAB1/IO03RSB0 |
| B5 | IO17RSB0 |
| B6 | IO21RSB0 |
| B7 | IO27RSB0 |
| B8 | IO34RSB0 |
| B9 | IO44RSB0 |
| B10 | IO51RSB0 |
| B11 | IO57RSB0 |
| B12 | GBC1/IO73RSB0 |
| B13 | GBB0/IO74RSB0 |
| B14 | IO71RSB0 |
| B15 | GBA2/IO78PDB1 |
| B16 | IO81PDB1 |
| C1 | IO224NDB3 |
| C2 | IO225NDB3 |
| C3 | VMV3 |
| C4 | IO11RSB0 |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| C7 | IO25RSB0 |
| C8 | IO36RSB0 |
| C9 | IO42RSB0 |
| C10 | IO49RSB0 |
| C11 | IO56RSB0 |
| C12 | GBC0/IO72RSB0 |
| C13 | IO62RSB0 |
| C14 | VMV0 |
| C15 | IO78NDB1 |
| C16 | IO81NDB1 |
| D1 | IO222NDB3 |
| D2 | IO222PDB3 |
| D3 | GAC2/IO223PDB3 |
| D4 | IO223NDB3 |
| D5 | GNDQ |
| D6 | IO23RSB0 |
| D7 | IO29RSB0 |
| D8 | IO33RSB0 |
| D9 | IO46RSB0 |
| D10 | IO52RSB0 |
| D11 | IO60RSB0 |
| D12 | GNDQ |
| D13 | IO80NDB1 |
| D14 | GBB2/IO79PDB1 |
| D15 | IO79NDB1 |
| D16 | IO82NSB1 |
| E1 | IO217PDB3 |
| E2 | IO218PDB3 |
| E3 | IO221NDB3 |
| E4 | IO221PDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO38RSB0 |
| E9 | IO47RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| E13 | GBC2/IO80PDB1 |
| E14 | IO83PPB1 |
| E15 | IO86PPB1 |
| E16 | IO87PDB1 |
| F1 | IO217NDB3 |
| F2 | IO218NDB3 |
| F3 | IO216PDB3 |
| F4 | IO216NDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO83NPB1 |
| F14 | IO86NPB1 |
| F15 | IO90PPB1 |
| F16 | IO87NDB1 |
| G1 | IO210PSB3 |
| G2 | IO213NDB3 |
| G3 | IO213PDB3 |
| G4 | GFC1/IO209PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |
| G13 | GCC1/IO91PPB1 |
| G14 | IO90NPB1 |
| G15 | IO88PDB1 |
| G16 | IO88NDB1 |
| H1 | GFB0/IO208NPB3 |
| H2 | GFA0/IO207NDB3 |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| H3 | GFB1/IO208PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO209NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO91NPB1 |
| H13 | GCB1/IO92PPB1 |
| H14 | GCA0/IO93NPB1 |
| H15 | IO96NPB1 |
| H16 | GCB0/IO92NPB1 |
| J1 | GFA2/IO206PSB3 |
| J2 | GFA1/IO207PDB3 |
| J3 | VCCPLF |
| J4 | IO205NDB3 |
| J5 | GFB2/IO205PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO95PPB1 |
| J13 | GCA1/IO93PPB1 |
| J14 | GCC2/IO96PPB1 |
| J15 | IO100PPB1 |
| J16 | GCA2/IO94PSB1 |
| K1 | GFC2/IO204PDB3 |
| K2 | IO204NDB3 |
| K3 | IO203NDB3 |
| K4 | IO203PDB3 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO95NPB1 |
| K14 | IO100NPB1 |
| K15 | IO102NDB1 |
| K16 | IO102PDB1 |
| L1 | IO202NDB3 |
| L2 | IO202PDB3 |
| L3 | IO196PPB3 |
| L4 | IO193PPB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO112NPB1 |
| L14 | IO106NDB1 |
| L15 | IO106PDB1 |
| L16 | IO107PDB1 |
| M1 | IO197NSB3 |
| M2 | IO196NPB3 |
| M3 | IO193NPB3 |
| M4 | GEC0/IO190NPB3 |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO147RSB2 |
| M9 | IO136RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO110NDB1 |
| M14 | GDB1/IO112PPB1 |

| FG256 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| M15 | GDC1/IO111PDB1 |
| M16 | IO107NDB1 |
| N1 | IO194PSB3 |
| N2 | IO192PPB3 |
| N3 | GEC1/IO190PPB3 |
| N4 | IO192NPB3 |
| N5 | GNDQ |
| N6 | GEA2/IO187RSB2 |
| N7 | IO161RSB2 |
| N8 | IO155RSB2 |
| N9 | IO141RSB2 |
| N10 | IO129RSB2 |
| N11 | IO124RSB2 |
| N12 | GNDQ |
| N13 | IO110PDB1 |
| N14 | VJTAG |
| N15 | GDC0/IO111NDB1 |
| N16 | GDA1/IO113PDB1 |
| P1 | GEB1/IO189PDB3 |
| P2 | GEB0/IO189NDB3 |
| P3 | VMV2 |
| P4 | IO179RSB2 |
| P5 | IO171RSB2 |
| P6 | IO165RSB2 |
| P7 | IO159RSB2 |
| P8 | IO151RSB2 |
| P9 | IO137RSB2 |
| P10 | IO134RSB2 |
| P11 | IO128RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO113NDB1 |
| R1 | GEA1/IO188PDB3 |
| R2 | GEA0/IO188NDB3 |
| R3 | IO184RSB2 |
| R4 | GEC2/IO185RSB2 |

| FG256 | |
|-------------------|-------------------------|
| Pin Number | A3P1000 Function |
| R5 | IO168RSB2 |
| R6 | IO163RSB2 |
| R7 | IO157RSB2 |
| R8 | IO149RSB2 |
| R9 | IO143RSB2 |
| R10 | IO138RSB2 |
| R11 | IO131RSB2 |
| R12 | IO125RSB2 |
| R13 | GDB2/IO115RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO183RSB2 |
| T3 | GEB2/IO186RSB2 |
| T4 | IO172RSB2 |
| T5 | IO170RSB2 |
| T6 | IO164RSB2 |
| T7 | IO158RSB2 |
| T8 | IO153RSB2 |
| T9 | IO142RSB2 |
| T10 | IO135RSB2 |
| T11 | IO130RSB2 |
| T12 | GDC2/IO116RSB2 |
| T13 | IO120RSB2 |
| T14 | GDA2/IO114RSB2 |
| T15 | TMS |
| T16 | GND |

4.9 FG484

FIGURE 4-9 • FG484—BOTTOM VIEW



Note: For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | NC |
| A5 | NC |
| A6 | IO09RSB0 |
| A7 | IO15RSB0 |
| A8 | NC |
| A9 | NC |
| A10 | IO22RSB0 |
| A11 | IO23RSB0 |
| A12 | IO29RSB0 |
| A13 | IO35RSB0 |
| A14 | NC |
| A15 | NC |
| A16 | IO46RSB0 |
| A17 | IO48RSB0 |
| A18 | NC |
| A19 | NC |
| A20 | VCCIB0 |
| A21 | GND |
| A22 | GND |
| B1 | GND |
| B2 | VCCIB3 |
| B3 | NC |
| B4 | NC |
| B5 | NC |
| B6 | IO08RSB0 |
| B7 | IO12RSB0 |
| B8 | NC |
| B9 | NC |
| B10 | IO17RSB0 |
| B11 | NC |
| B12 | NC |
| B13 | IO36RSB0 |
| B14 | NC |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| B15 | NC |
| B16 | IO47RSB0 |
| B17 | IO49RSB0 |
| B18 | NC |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB1 |
| B22 | GND |
| C1 | VCCIB3 |
| C2 | NC |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | NC |
| C7 | NC |
| C8 | VCC |
| C9 | VCC |
| C10 | NC |
| C11 | NC |
| C12 | NC |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| D7 | GAB0/IO02RSB0 |
| D8 | IO11RSB0 |
| D9 | IO16RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | IO34RSB0 |
| D13 | IO37RSB0 |
| D14 | IO41RSB0 |
| D15 | IO43RSB0 |
| D16 | GBB1/IO57RSB0 |
| D17 | GBA0/IO58RSB0 |
| D18 | GBA1/IO59RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | NC |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO173PDB3 |
| E5 | GAA2/IO174PDB3 |
| E6 | GNDQ |
| E7 | GAB1/IO03RSB0 |
| E8 | IO13RSB0 |
| E9 | IO14RSB0 |
| E10 | IO21RSB0 |
| E11 | IO27RSB0 |
| E12 | IO32RSB0 |
| E13 | IO38RSB0 |
| E14 | IO42RSB0 |
| E15 | GBC1/IO55RSB0 |
| E16 | GBB0/IO56RSB0 |
| E17 | IO52RSB0 |
| E18 | GBA2/IO60PDB1 |
| E19 | IO60NDB1 |
| E20 | GND |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO173NDB3 |
| F5 | IO174NDB3 |
| F6 | VMV3 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO44RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO51RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | IO170NDB3 |
| G2 | IO170PDB3 |
| G3 | NC |
| G4 | IO171NDB3 |
| G5 | IO171PDB3 |
| G6 | GAC2/IO172PDB3 |
| G7 | IO06RSB0 |
| G8 | GNDQ |
| G9 | IO10RSB0 |
| G10 | IO19RSB0 |
| G11 | IO26RSB0 |
| G12 | IO30RSB0 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| G13 | IO40RSB0 |
| G14 | IO45RSB0 |
| G15 | GNDQ |
| G16 | IO50RSB0 |
| G17 | GBB2/IO61PPB1 |
| G18 | IO53RSB0 |
| G19 | IO63NDB1 |
| G20 | NC |
| G21 | NC |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | VCC |
| H4 | IO166PDB3 |
| H5 | IO167NPB3 |
| H6 | IO172NDB3 |
| H7 | IO169NDB3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO25RSB0 |
| H12 | IO31RSB0 |
| H13 | VCCIB0 |
| H14 | VCCIB0 |
| H15 | VMV1 |
| H16 | GBC2/IO62PDB1 |
| H17 | IO67PPB1 |
| H18 | IO64PPB1 |
| H19 | IO66PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO166NDB3 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| J5 | IO168NPB3 |
| J6 | IO167PPB3 |
| J7 | IO169PDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO62NDB1 |
| J17 | IO64NPB1 |
| J18 | IO65PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | IO68PDB1 |
| J22 | IO68NDB1 |
| K1 | IO157PDB3 |
| K2 | IO157NDB3 |
| K3 | NC |
| K4 | IO165NDB3 |
| K5 | IO165PDB3 |
| K6 | IO168PPB3 |
| K7 | GFC1/IO164PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB1 |
| K16 | GCC1/IO69PPB1 |
| K17 | IO65NPB1 |
| K18 | IO75PDB1 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| K19 | IO75NDB1 |
| K20 | NC |
| K21 | IO76NDB1 |
| K22 | IO76PDB1 |
| L1 | NC |
| L2 | IO155PDB3 |
| L3 | NC |
| L4 | GFB0/IO163NPB3 |
| L5 | GFA0/IO162NDB3 |
| L6 | GFB1/IO163PPB3 |
| L7 | VCOMPLF |
| L8 | GFC0/IO164NPB3 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO69NPB1 |
| L16 | GCB1/IO70PPB1 |
| L17 | GCA0/IO71NPB1 |
| L18 | IO67NPB1 |
| L19 | GCB0/IO70NPB1 |
| L20 | IO77PDB1 |
| L21 | IO77NDB1 |
| L22 | IO78NPB1 |
| M1 | NC |
| M2 | IO155NDB3 |
| M3 | IO158NPB3 |
| M4 | GFA2/IO161PPB3 |
| M5 | GFA1/IO162PDB3 |
| M6 | VCCPLF |
| M7 | IO160NDB3 |
| M8 | GFB2/IO160PDB3 |
| M9 | VCC |
| M10 | GND |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO73PPB1 |
| M16 | GCA1/IO71PPB1 |
| M17 | GCC2/IO74PPB1 |
| M18 | IO80PPB1 |
| M19 | GCA2/IO72PDB1 |
| M20 | IO79PPB1 |
| M21 | IO78PPB1 |
| M22 | NC |
| N1 | IO154NDB3 |
| N2 | IO154PDB3 |
| N3 | NC |
| N4 | GFC2/IO159PDB3 |
| N5 | IO161NPB3 |
| N6 | IO156PPB3 |
| N7 | IO129RSB2 |
| N8 | VCCIB3 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB1 |
| N16 | IO73NPB1 |
| N17 | IO80NPB1 |
| N18 | IO74NPB1 |
| N19 | IO72NDB1 |
| N20 | NC |
| N21 | IO79NPB1 |
| N22 | NC |
| P1 | NC |
| P2 | IO153PDB3 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| P3 | IO153NDB3 |
| P4 | IO159NDB3 |
| P5 | IO156NPB3 |
| P6 | IO151PPB3 |
| P7 | IO158PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO87NPB1 |
| P17 | IO85NDB1 |
| P18 | IO85PDB1 |
| P19 | IO84PDB1 |
| P20 | NC |
| P21 | IO81PDB1 |
| P22 | NC |
| R1 | NC |
| R2 | NC |
| R3 | VCC |
| R4 | IO150PDB3 |
| R5 | IO151NPB3 |
| R6 | IO147NPB3 |
| R7 | GEC0/IO146NPB3 |
| R8 | VMV3 |
| R9 | VCCIB2 |
| R10 | VCCIB2 |
| R11 | IO117RSB2 |
| R12 | IO110RSB2 |
| R13 | VCCIB2 |
| R14 | VCCIB2 |
| R15 | VMV2 |
| R16 | IO94RSB2 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| R17 | GDB1/IO87PPB1 |
| R18 | GDC1/IO86PDB1 |
| R19 | IO84NDB1 |
| R20 | VCC |
| R21 | IO81NDB1 |
| R22 | IO82PDB1 |
| T1 | IO152PDB3 |
| T2 | IO152NDB3 |
| T3 | NC |
| T4 | IO150NDB3 |
| T5 | IO147PPB3 |
| T6 | GEC1/IO146PPB3 |
| T7 | IO140RSB2 |
| T8 | GNDQ |
| T9 | GEA2/IO143RSB2 |
| T10 | IO126RSB2 |
| T11 | IO120RSB2 |
| T12 | IO108RSB2 |
| T13 | IO103RSB2 |
| T14 | IO99RSB2 |
| T15 | GNDQ |
| T16 | IO92RSB2 |
| T17 | VJTAG |
| T18 | GDC0/IO86NDB1 |
| T19 | GDA1/IO88PDB1 |
| T20 | NC |
| T21 | IO83PDB1 |
| T22 | IO82NDB1 |
| U1 | IO149PDB3 |
| U2 | IO149NDB3 |
| U3 | NC |
| U4 | GEB1/IO145PDB3 |
| U5 | GEB0/IO145NDB3 |
| U6 | VMV2 |
| U7 | IO138RSB2 |
| U8 | IO136RSB2 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| U9 | IO131RSB2 |
| U10 | IO124RSB2 |
| U11 | IO119RSB2 |
| U12 | IO107RSB2 |
| U13 | IO104RSB2 |
| U14 | IO97RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO88NDB1 |
| U20 | NC |
| U21 | IO83NDB1 |
| U22 | NC |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO144PDB3 |
| V5 | GEA0/IO144NDB3 |
| V6 | IO139RSB2 |
| V7 | GEC2/IO141RSB2 |
| V8 | IO132RSB2 |
| V9 | IO127RSB2 |
| V10 | IO121RSB2 |
| V11 | IO114RSB2 |
| V12 | IO109RSB2 |
| V13 | IO105RSB2 |
| V14 | IO98RSB2 |
| V15 | IO96RSB2 |
| V16 | GDB2/IO90RSB2 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | NC |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| W1 | NC |
| W2 | IO148PDB3 |
| W3 | NC |
| W4 | GND |
| W5 | IO137RSB2 |
| W6 | GEB2/IO142RSB2 |
| W7 | IO134RSB2 |
| W8 | IO125RSB2 |
| W9 | IO123RSB2 |
| W10 | IO118RSB2 |
| W11 | IO115RSB2 |
| W12 | IO111RSB2 |
| W13 | IO106RSB2 |
| W14 | IO102RSB2 |
| W15 | GDC2/IO91RSB2 |
| W16 | IO93RSB2 |
| W17 | GDA2/IO89RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB3 |
| Y2 | IO148NDB3 |
| Y3 | NC |
| Y4 | NC |
| Y5 | GND |
| Y6 | NC |
| Y7 | NC |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | NC |
| Y11 | NC |
| Y12 | NC |
| Y13 | NC |
| Y14 | VCC |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB1 |
| AA1 | GND |
| AA2 | VCCIB3 |
| AA3 | NC |
| AA4 | NC |
| AA5 | NC |
| AA6 | IO135RSB2 |
| AA7 | IO133RSB2 |
| AA8 | NC |
| AA9 | NC |
| AA10 | NC |
| AA11 | NC |
| AA12 | NC |
| AA13 | NC |
| AA14 | NC |
| AA15 | NC |
| AA16 | IO101RSB2 |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB2 |
| AB4 | NC |
| AB5 | NC |
| AB6 | IO130RSB2 |

| FG484 | |
|------------|-----------------|
| Pin Number | A3P600 Function |
| AB7 | IO128RSB2 |
| AB8 | IO122RSB2 |
| AB9 | IO116RSB2 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO113RSB2 |
| AB13 | IO112RSB2 |
| AB14 | NC |
| AB15 | NC |
| AB16 | IO100RSB2 |
| AB17 | IO95RSB2 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB2 |
| AB21 | GND |
| AB22 | GND |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO07RSB0 |
| A5 | IO09RSB0 |
| A6 | IO13RSB0 |
| A7 | IO18RSB0 |
| A8 | IO20RSB0 |
| A9 | IO26RSB0 |
| A10 | IO32RSB0 |
| A11 | IO40RSB0 |
| A12 | IO41RSB0 |
| A13 | IO53RSB0 |
| A14 | IO59RSB0 |
| A15 | IO64RSB0 |
| A16 | IO65RSB0 |
| A17 | IO67RSB0 |
| A18 | IO69RSB0 |
| A19 | NC |
| A20 | VCCIB0 |
| A21 | GND |
| A22 | GND |
| B1 | GND |
| B2 | VCCIB3 |
| B3 | NC |
| B4 | IO06RSB0 |
| B5 | IO08RSB0 |
| B6 | IO12RSB0 |
| B7 | IO15RSB0 |
| B8 | IO19RSB0 |
| B9 | IO24RSB0 |
| B10 | IO31RSB0 |
| B11 | IO39RSB0 |
| B12 | IO48RSB0 |
| B13 | IO54RSB0 |
| B14 | IO58RSB0 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| B15 | IO63RSB0 |
| B16 | IO66RSB0 |
| B17 | IO68RSB0 |
| B18 | IO70RSB0 |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB1 |
| B22 | GND |
| C1 | VCCIB3 |
| C2 | IO220PDB3 |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | IO10RSB0 |
| C7 | IO14RSB0 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO30RSB0 |
| C11 | IO37RSB0 |
| C12 | IO43RSB0 |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | IO219PDB3 |
| D2 | IO220NDB3 |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| D7 | GAB0/IO02RSB0 |
| D8 | IO16RSB0 |
| D9 | IO22RSB0 |
| D10 | IO28RSB0 |
| D11 | IO35RSB0 |
| D12 | IO45RSB0 |
| D13 | IO50RSB0 |
| D14 | IO55RSB0 |
| D15 | IO61RSB0 |
| D16 | GBB1/IO75RSB0 |
| D17 | GBA0/IO76RSB0 |
| D18 | GBA1/IO77RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | IO219NDB3 |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO224PDB3 |
| E5 | GAA2/IO225PDB3 |
| E6 | GNDQ |
| E7 | GAB1/IO03RSB0 |
| E8 | IO17RSB0 |
| E9 | IO21RSB0 |
| E10 | IO27RSB0 |
| E11 | IO34RSB0 |
| E12 | IO44RSB0 |
| E13 | IO51RSB0 |
| E14 | IO57RSB0 |
| E15 | GBC1/IO73RSB0 |
| E16 | GBB0/IO74RSB0 |
| E17 | IO71RSB0 |
| E18 | GAA2/IO78PDB1 |
| E19 | IO81PDB1 |
| E20 | GND |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| E21 | NC |
| E22 | IO84PDB1 |
| F1 | NC |
| F2 | IO215PDB3 |
| F3 | IO215NDB3 |
| F4 | IO224NDB3 |
| F5 | IO225NDB3 |
| F6 | VMV3 |
| F7 | IO11RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO25RSB0 |
| F11 | IO36RSB0 |
| F12 | IO42RSB0 |
| F13 | IO49RSB0 |
| F14 | IO56RSB0 |
| F15 | GBC0/IO72RSB0 |
| F16 | IO62RSB0 |
| F17 | VMV0 |
| F18 | IO78NDB1 |
| F19 | IO81NDB1 |
| F20 | IO82PPB1 |
| F21 | NC |
| F22 | IO84NDB1 |
| G1 | IO214NDB3 |
| G2 | IO214PDB3 |
| G3 | NC |
| G4 | IO222NDB3 |
| G5 | IO222PDB3 |
| G6 | GAC2/IO223PDB3 |
| G7 | IO223NDB3 |
| G8 | GNDQ |
| G9 | IO23RSB0 |
| G10 | IO29RSB0 |
| G11 | IO33RSB0 |
| G12 | IO46RSB0 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| G13 | IO52RSB0 |
| G14 | IO60RSB0 |
| G15 | GNDQ |
| G16 | IO80NDB1 |
| G17 | GBB2/IO79PDB1 |
| G18 | IO79NDB1 |
| G19 | IO82NPB1 |
| G20 | IO85PDB1 |
| G21 | IO85NDB1 |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | VCC |
| H4 | IO217PDB3 |
| H5 | IO218PDB3 |
| H6 | IO221NDB3 |
| H7 | IO221PDB3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO38RSB0 |
| H12 | IO47RSB0 |
| H13 | VCCIB0 |
| H14 | VCCIB0 |
| H15 | VMV1 |
| H16 | GBC2/IO80PDB1 |
| H17 | IO83PPB1 |
| H18 | IO86PPB1 |
| H19 | IO87PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | IO212NDB3 |
| J2 | IO212PDB3 |
| J3 | NC |
| J4 | IO217NDB3 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| J5 | IO218NDB3 |
| J6 | IO216PDB3 |
| J7 | IO216NDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO83NPB1 |
| J17 | IO86NPB1 |
| J18 | IO90PPB1 |
| J19 | IO87NDB1 |
| J20 | NC |
| J21 | IO89PDB1 |
| J22 | IO89NDB1 |
| K1 | IO211PDB3 |
| K2 | IO211NDB3 |
| K3 | NC |
| K4 | IO210PPB3 |
| K5 | IO213NDB3 |
| K6 | IO213PDB3 |
| K7 | GFC1/IO209PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB1 |
| K16 | GCC1/IO91PPB1 |
| K17 | IO90NPB1 |
| K18 | IO88PDB1 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| K19 | IO88NDB1 |
| K20 | IO94NPB1 |
| K21 | IO98NDB1 |
| K22 | IO98PDB1 |
| L1 | NC |
| L2 | IO200PDB3 |
| L3 | IO210NPB3 |
| L4 | GFB0/IO208NPB3 |
| L5 | GFA0/IO207NDB3 |
| L6 | GFB1/IO208PPB3 |
| L7 | VCOMPLF |
| L8 | GFC0/IO209NPB3 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO91NPB1 |
| L16 | GCB1/IO92PPB1 |
| L17 | GCA0/IO93NPB1 |
| L18 | IO96NPB1 |
| L19 | GCB0/IO92NPB1 |
| L20 | IO97PDB1 |
| L21 | IO97NDB1 |
| L22 | IO99NPB1 |
| M1 | NC |
| M2 | IO200NDB3 |
| M3 | IO206NDB3 |
| M4 | GFA2/IO206PDB3 |
| M5 | GFA1/IO207PDB3 |
| M6 | VCCPLF |
| M7 | IO205NDB3 |
| M8 | GFB2/IO205PDB3 |
| M9 | VCC |
| M10 | GND |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO95PPB1 |
| M16 | GCA1/IO93PPB1 |
| M17 | GCC2/IO96PPB1 |
| M18 | IO100PPB1 |
| M19 | GCA2/IO94PPB1 |
| M20 | IO101PPB1 |
| M21 | IO99PPB1 |
| M22 | NC |
| N1 | IO201NDB3 |
| N2 | IO201PDB3 |
| N3 | NC |
| N4 | GFC2/IO204PDB3 |
| N5 | IO204NDB3 |
| N6 | IO203NDB3 |
| N7 | IO203PDB3 |
| N8 | VCCIB3 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB1 |
| N16 | IO95NPB1 |
| N17 | IO100NPB1 |
| N18 | IO102NDB1 |
| N19 | IO102PDB1 |
| N20 | NC |
| N21 | IO101NPB1 |
| N22 | IO103PDB1 |
| P1 | NC |
| P2 | IO199PDB3 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| P3 | IO199NDB3 |
| P4 | IO202NDB3 |
| P5 | IO202PDB3 |
| P6 | IO196PPB3 |
| P7 | IO193PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO112NPB1 |
| P17 | IO106NDB1 |
| P18 | IO106PDB1 |
| P19 | IO107PDB1 |
| P20 | NC |
| P21 | IO104PDB1 |
| P22 | IO103NDB1 |
| R1 | NC |
| R2 | IO197PPB3 |
| R3 | VCC |
| R4 | IO197NPB3 |
| R5 | IO196NPB3 |
| R6 | IO193NPB3 |
| R7 | GEC0/IO190NPB3 |
| R8 | VMV3 |
| R9 | VCCIB2 |
| R10 | VCCIB2 |
| R11 | IO147RSB2 |
| R12 | IO136RSB2 |
| R13 | VCCIB2 |
| R14 | VCCIB2 |
| R15 | VMV2 |
| R16 | IO110NDB1 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| R17 | GDB1/IO112PPB1 |
| R18 | GDC1/IO111PDB1 |
| R19 | IO107NDB1 |
| R20 | VCC |
| R21 | IO104NDB1 |
| R22 | IO105PDB1 |
| T1 | IO198PDB3 |
| T2 | IO198NDB3 |
| T3 | NC |
| T4 | IO194PPB3 |
| T5 | IO192PPB3 |
| T6 | GEC1/IO190PPB3 |
| T7 | IO192NPB3 |
| T8 | GNDQ |
| T9 | GEA2/IO187RSB2 |
| T10 | IO161RSB2 |
| T11 | IO155RSB2 |
| T12 | IO141RSB2 |
| T13 | IO129RSB2 |
| T14 | IO124RSB2 |
| T15 | GNDQ |
| T16 | IO110PDB1 |
| T17 | VJTAG |
| T18 | GDC0/IO111NDB1 |
| T19 | GDA1/IO113PDB1 |
| T20 | NC |
| T21 | IO108PDB1 |
| T22 | IO105NDB1 |
| U1 | IO195PDB3 |
| U2 | IO195NDB3 |
| U3 | IO194NPB3 |
| U4 | GEB1/IO189PDB3 |
| U5 | GEB0/IO189NDB3 |
| U6 | VMV2 |
| U7 | IO179RSB2 |
| U8 | IO171RSB2 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| U9 | IO165RSB2 |
| U10 | IO159RSB2 |
| U11 | IO151RSB2 |
| U12 | IO137RSB2 |
| U13 | IO134RSB2 |
| U14 | IO128RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO113NDB1 |
| U20 | NC |
| U21 | IO108NDB1 |
| U22 | IO109PDB1 |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO188PDB3 |
| V5 | GEA0/IO188NDB3 |
| V6 | IO184RSB2 |
| V7 | GEC2/IO185RSB2 |
| V8 | IO168RSB2 |
| V9 | IO163RSB2 |
| V10 | IO157RSB2 |
| V11 | IO149RSB2 |
| V12 | IO143RSB2 |
| V13 | IO138RSB2 |
| V14 | IO131RSB2 |
| V15 | IO125RSB2 |
| V16 | GDB2/IO115RSB2 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO109NDB1 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| W1 | NC |
| W2 | IO191PDB3 |
| W3 | NC |
| W4 | GND |
| W5 | IO183RSB2 |
| W6 | GEB2/IO186RSB2 |
| W7 | IO172RSB2 |
| W8 | IO170RSB2 |
| W9 | IO164RSB2 |
| W10 | IO158RSB2 |
| W11 | IO153RSB2 |
| W12 | IO142RSB2 |
| W13 | IO135RSB2 |
| W14 | IO130RSB2 |
| W15 | GDC2/IO116RSB2 |
| W16 | IO120RSB2 |
| W17 | GDA2/IO114RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB3 |
| Y2 | IO191NDB3 |
| Y3 | NC |
| Y4 | IO182RSB2 |
| Y5 | GND |
| Y6 | IO177RSB2 |
| Y7 | IO174RSB2 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO154RSB2 |
| Y11 | IO148RSB2 |
| Y12 | IO140RSB2 |
| Y13 | NC |
| Y14 | VCC |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB1 |
| AA1 | GND |
| AA2 | VCCIB3 |
| AA3 | NC |
| AA4 | IO181RSB2 |
| AA5 | IO178RSB2 |
| AA6 | IO175RSB2 |
| AA7 | IO169RSB2 |
| AA8 | IO166RSB2 |
| AA9 | IO160RSB2 |
| AA10 | IO152RSB2 |
| AA11 | IO146RSB2 |
| AA12 | IO139RSB2 |
| AA13 | IO133RSB2 |
| AA14 | NC |
| AA15 | NC |
| AA16 | IO122RSB2 |
| AA17 | IO119RSB2 |
| AA18 | IO117RSB2 |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB2 |
| AB4 | IO180RSB2 |
| AB5 | IO176RSB2 |
| AB6 | IO173RSB2 |

| FG484 | |
|------------|------------------|
| Pin Number | A3P1000 Function |
| AB7 | IO167RSB2 |
| AB8 | IO162RSB2 |
| AB9 | IO156RSB2 |
| AB10 | IO150RSB2 |
| AB11 | IO145RSB2 |
| AB12 | IO144RSB2 |
| AB13 | IO132RSB2 |
| AB14 | IO127RSB2 |
| AB15 | IO126RSB2 |
| AB16 | IO123RSB2 |
| AB17 | IO121RSB2 |
| AB18 | IO118RSB2 |
| AB19 | NC |
| AB20 | VCCIB2 |
| AB21 | GND |
| AB22 | GND |

APPENDIX A: REVISION HISTORY

The following table lists critical changes that were made in each version of the ProASIC 3 datasheet

A.1 Revision C - 01/2023

The following is the summary of changes in revision C of this document:

- Updated [Table 1](#) in ARM Processor Support in ProASIC 3 FPGAs section

A.2 Revision B - 03/2022

The following is the summary of changes in revision B of the document:

- Updated [ProASIC 3 Ordering Information](#): Interchanged the position of I and Y values.

A.3 Revision A - 02/2022

The following is the summary of changes in revision A of the document:

- The document number was changed from 51700097 to DS50003269.
- The document was migrated to the Microchip template

A.4 Revision 19 - 11/2019

The following is the summary of changes in revision B of the document:

- Removed the A3P015 device and its related details across the document.
- Migrated to Microchip-Microsemi template changes.

A.5 Revision 18 - 03/2016

The following is the summary of changes in revision B of the document:

- Updated 3.3V DC supply voltage's maximum Commercial and Industrial values from 3.3V to 3.6V in [Table 2-2](#) (SAR 72693).
- Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833).

A.6 Revision 17 - 06/2015

The following is the summary of changes in revision B of the document:

- Removed PQFP embedded heat spreader info. from [Table 2-5](#) (SAR 52320).
- Updated [Section 3.1.4 VCCIBx I/O Supply Voltage](#) (SAR 43323).

A.7 Revision 16 - 12/2014

The following is the summary of changes in revision B of the document:

- Updated [ProASIC 3 Ordering Information](#). Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079). Added Note "Only devices with package size greater than or equal to 5x5 are supported".
- Updated Table Note (2) in [Table 2-3](#) so that the Table Note is not applicable for Maximum Storage Temperature T_{STG} (SAR 54297).
- Added values for Drive strength 2 mA in [Table 2-41](#), [Table 2-42](#), [Table 2-43](#), and [Table 2-44](#) (SAR 57184).
- Added [Table 2-1](#) (SAR 45466).
- Updates made to maintain the style and consistency of the document.

A.8 Revision 15 - 07/2014

The following is the summary of changes in revision B of the document:

- Added corner pad table note (3) to [Section 4.3 QN132](#) (SAR 47442).
- Ambient temperature removed in [Table 2-2](#), table notes and [ProASIC 3 Ordering Information](#) figure were modified (SAR 48343).

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- Other updates were made to maintain the style and consistency of the datasheet.

A.9 Revision 14 - 04/2014

The following is the summary of changes in revision B of the document:

- Note added for the discontinuance of QN132 package to the following tables and section: [I/Os PER PACKAGE 1](#) and [Section 4.3 QN132](#) (SAR 55118).

A.10 Revision 13 - 01/2013

The following is the summary of changes in revision B of the document:

- The [ProASIC 3 Ordering Information](#) has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).
- Added a note to [Table 2-2](#) (SAR 43644): The programming temperature range supported is $T_{\text{ambient}} = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.
- The note in [Table 2-113](#) referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).
- Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284). Live at Power-Up (LAPU) has been replaced with 'Instant On'.

A.11 Revision 12 - 09/2012

The following is the summary of changes in revision B of the document:

- The Security section was modified to clarify that Microsemi does not support read-back of programmed data.
- Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the [Section 3.1.5 VMVx I/O Supply Voltage \(quiet\)](#) for further information" to [Table 2-1](#) and [Table 2-2](#) (SAR 38321)
- [Table 2-35](#) was revised to change the maximum temperature from $110\text{ }^{\circ}\text{C}$ to $100\text{ }^{\circ}\text{C}$, with an example of six months instead of three months (SAR 37933).
- In [Table 2-92](#), VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).
- [Figure 2-37](#) and [Figure 2-38](#) are new (SAR 28371).
- The following sentence was removed from the [Section 3.1.5 VMVx I/O Supply Voltage \(quiet\)](#) in the [Section 3.0 Pin Descriptions](#) chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.

A.12 Revision 11 - 03/2012

The following is the summary of changes in revision B of the document:

- Note indicating that A3P015 is not recommended for new designs has been added. The [Devices Not Recommended For New Designs](#) is new (SAR 36760).
- The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687).
- The reference to guidelines for global spines and VersaTile rows, given in the [Section 2.2.4.1.4 Global Clock Contribution—PCLOCK](#), was corrected to the "Spine Architecture" section of the Global Resources chapter in the [ProASIC 3 FPGA Fabric User's Guide](#) (SAR 34734).
- [Figure 2-4](#) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430).
- The AC Loading figures in the [Section 2.3.4 Single-Ended I/O Characteristics](#) were updated to match tables in the [Section 2.3.2.2 Summary of I/O Timing Characteristics – Default I/O Software Settings](#) (SAR 34883).
- Added values for minimum pulse width and removed the FRMAX row from [Table 2-106](#) through [Table 2-112](#) in the [Section 2.5.2 Global Tree Timing Characteristics](#). Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269).

A.13 Revision 10 - 09/2011

The following is the summary of changes in revision B of the document:

- Note indicating that A3P015 is not recommended for new designs has been added. The [Devices Not Recommended For New Designs](#) is new (SAR 36760).
- The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687).
- The reference to guidelines for global spines and VersaTile rows, given in the [Section 2.2.4.1.4 Global Clock Contribution—PCLOCK](#), was corrected to the "Spine Architecture" section of the Global Resources chapter in the [ProASIC 3 FPGA Fabric User's Guide](#) (SAR 34734).
- [Figure 2-4](#) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430).
- The AC Loading figures in the [Section 2.3.4 Single-Ended I/O Characteristics](#) were updated to match tables in the [Section 2.3.2.2 Summary of I/O Timing Characteristics – Default I/O Software Settings](#) (SAR 34883).
- Added values for minimum pulse width and removed the FRMAX row from [Table 2-106](#) through [Table 2-112](#) in the [Section 2.5.2 Global Tree Timing Characteristics](#). Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269).
- "TBD" for 3.3 V LVCMOS Wide Range in [Table 2-28](#) through [Table 2-30](#) was replaced by "Same as regular 3.3V" (SAR 33852).
- The equations in the notes for [Table 2-31](#) were corrected (SAR 32470).
- "TBD" for 3.3 V LVCMOS Wide Range in [Table 2-32](#) through [Table 2-34](#) was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33852).
- In the [Section 2.3.4.2 3.3V LVCMOS Wide Range](#), values were added to [Table 2-47](#) through [Table 2-49](#) for IOSL and IOSH, replacing "TBD" (SAR 33852).
- The following sentence was deleted from the [Section 2.3.4.3 2.5V LVCMOS](#) (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer."
- The table notes were revised for [Table 2-89](#) (SAR 33859).
- Values were added for $F_{DDRIMAX}$ and F_{DDOMAX} in [Table 2-101](#) and [Table 2-103](#) (SAR 23919).
- [Table 2-113](#) was updated. A note was added to indicate that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).
- The following figures were deleted (SAR 29991). Reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs, which covers these cases in detail (SAR 21770).
- [Figure 2-34](#) • Write Access after Write onto Same Address
- [Figure 2-35](#) • Read Access after Write onto Same Address
- [Figure 2-35](#) • Read Access after Write onto Same Address
- The port names in the SRAM [Section 2.7.1.1 Timing Waveforms](#), SRAM [Section 2.7.1.2 Timing Characteristics](#) tables, [Figure 2-39](#) • FIFO Reset, and the FIFO [Section 2.7.2.2 Timing Characteristics](#) tables were revised to ensure consistency with the software names (SARs 29991, 30510).
- The [Section 3.0 Pin Descriptions](#) chapter has been added (SAR 21642).
- Package names used in the [Section 4.0 Package Pin Assignments](#) were revised to match standards given in [Section 3.5.3 Package Mechanical Drawings](#) (SAR 27395).
- The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The [ProASIC 3 Device Status](#) indicates the status for each device in the device family.

A.14 Revision 9 - 10/2009

The following is the summary of changes in revision B of the document:

- The CS121 package was added to table under [Features and Benefits](#), the [I/Os PER PACKAGE 1](#) table, [Table 3, ProASIC 3 Ordering Information](#), and the [Temperature Grade Offerings](#) table.
- [ProASIC 3 Ordering Information](#) was revised to include the fact that some RoHS compliant packages are halogen-free.
- The figure and pin table for A3P060 are new.

A.15 Revision 8 - 08/2009

The following is the summary of changes in revision B of the document:

- All references to M7 devices (CoreMP7) and speed grade –F were removed from this document.
- Table 1-1 I/O Standards supported is new.
- The I/Os with Advanced I/O Standards section was revised to add definitions of hot-swap and cold-sparing.
- 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.
- I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.
- –F was removed from the datasheet. The speed grade is no longer supported.
- The notes in [Table 2-2](#) were updated.
- [Table 2-4](#) was updated.
- [Table 2-6](#) was updated.
- In [Table 2-114](#), the following specifications were removed:
 - t_{WRO}
 - t_{CCKH}
- In [Table 2-115](#), the following specifications were removed:
 - t_{WRO}
 - t_{CCKH}
- In the title of [Table 2-73](#), VCCI had a typo. It was changed from 3.0V to 1.7V.
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A.16 Revision 7 - 02/2019

The following is the summary of changes in revision B of the document:

- The [Advanced I/O](#) section was revised to add a bullet regarding wide range power supply voltage support.
- The table under [Features and Benefits](#), was updated to include a value for typical equivalent macrocells for A3P250.
- The QN48 package was added to the following tables: the table under [Features and Benefits](#), [I/Os PER PACKAGE 1](#), and [Temperature Grade Offerings](#).
- The number of singled-ended I/Os for QN68 was added to the [I/Os PER PACKAGE 1](#) table.
- The Wide Range I/O Support section is new

A.17 Revision 6 - 12/2008

The following is the summary of changes in revision B of the document:

- The [Section 4.1 QN48](#) section is new.
- The [QN68](#) pin table for A3P030 is new.

A.18 Revision 5 - 08/2008

The following is the summary of changes in revision B of the document:

- T_J , Maximum Junction Temperature, was changed to 100° from 110° in the [Section 2.1.3 Thermal Characteristics](#) and [EQ 1](#). The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.
- Values for the A3P015 device were added to [Table 2-7](#).
- Values for the A3P015 device were added to [Table 2-14](#). P_{AC14} was removed. [Table 2-15](#) is new.
- The [Section 2.2.4.1.11 PLL Contribution—PPLL](#) was updated to change the P_{PLL} formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$.
- Both fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in [Table 2-101](#).
- [Table 2-106](#) is new.
- The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in [Table 2-113](#).

A.19 Revision 4 - 06/2008

The following is the summary of changes in revision B of the document:

- Table note references were added to [Table 2-2](#), and the order of the table notes was changed.
- The title for [Table 2-4](#) was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."
- The [Section 2.2.2 Power per I/O Pin](#) was updated to include 3 additional tables pertaining to input buffer power and output buffer power.
- [Table 2-29](#) was revised to include values for 3.3V PCI/PCI-X.
- [Table 2-89](#) was updated.

A.20 Revision 3 - 06/2008

The following is the summary of changes in revision B of the document:

- Pin numbers were added to the [Section 4.2 QN68](#) package diagram. Note 2 was added below the diagram.
- The [Section 4.3 QN132](#) package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.

A.21 Revision 2 - 02/2008

The following is the summary of changes in revision B of the document:

- This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.
- This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated:
 - [Features and Benefits](#)
 - [ProASIC 3 Ordering Information](#)
 - [Temperature Grade Offerings](#)
 - [with Optional Soft ARM Support](#)
 - [A3P015 and A3P030](#) note
 - Introduction and Overview (NA)
- The [ProASIC3 FPGAs Package Sizes Dimensions](#) table is new.
- In the [ProASIC 3 Ordering Information](#), the QN package measurements were updated to include both 0.4 mm and 0.5 mm.
- In the General Description section the number of I/Os was updated from 288 to 300.
- The [Section 4.2 QN68](#) is new.
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A.22 Revision 1 - 02/2008

The following is the summary of changes in revision 1 of the document:

- In [Table 2-2](#), T_J was listed in the symbol column and was incorrect. It was corrected and changed to T_A .
- In [Table 2-3](#), Maximum Operating Junction Temperature was changed from 110 °C to 100 °C for both commercial and industrial grades.
- The [Section 2.1.2.1 PLL Behavior at Brownout Condition](#) is new.
- In the [Section 2.2.4.1.11 PLL Contribution—PPLL](#), the following was deleted:
 - FCLKIN is the input clock frequency.
- In [Table 2-21](#), the note was incorrect. It previously said T_J and it was corrected and changed to T_A .
- In [Table 2-113](#), the SCLK parameter and note 1 are new.
- [Table 2-123](#) was populated with the parameter data, which was not in the previous version of the document.
- In the [VQ100 A3P030](#) pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0.

A.23 Revision 0 - 01/2008

The following is the summary of changes in revision 0 of the document:

- This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers.

A.24 Revision 2.2 - 07/2007

The following is the summary of changes in revision 2.2 of the document:

- The M7 and M1 device part numbers have been updated in Table 1 • ProASIC 3 Product Family, "I/Os Per Package", "Automotive ProASIC 3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix".
- The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC 3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections.
- The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added.

A.25 Revision 2.1 - 05/2007

The following is the summary of changes in revision 2.1 of the document:

- In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz).
- The "Clock Conditioning Circuit (CCC) and PLL" section was updated.
- In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated.
- Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new.
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A.26 Revision 2.0 - 04/2007

The following is the summary of changes in revision 2.0 of the document:

- In the "Packaging Tables", Ambient was deleted.
- The timing characteristics tables were updated.
- The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.
- The "PLL Macro" section was updated to include power-up information.
- Table 2-11 • ProASIC 3 CCC/PLL Specification was updated.
- Figure 2-19 • Peak-to-Peak Jitter Definition is new.
- The "SRAM and FIFO" section was updated with operation and timing requirement information.
- The "RESET" section was updated with read and write information.
- The "RESET" section was updated with read and write information.
- The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.
- PCI-X 3.3 V was added to Table 2-11 • VCCI Voltages and Compatible Standards.
- In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC 3 compliance descriptions were updated for levels 3 and 4.
- Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC 3 Devices was updated.
- Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.
- The "VCCPLF PLL Supply Voltage" section was updated.
- The "VPUMP Programming Supply Voltage" section was updated.
- The "GL Globals" section was updated to include information about direct input into quadrant clocks.
- V_{JTAG} was deleted from the "TCK Test Clock" section.

- In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.
- Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".
- Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1.
- In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951.
- Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.
- Table 3-5 • Package Thermal Resistivities was updated.
- Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated.
- Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.
- Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC 3 Devices was updated.
- Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.
- Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.
- Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.
- The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.
- Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.
- Figure 3-43 • Timing Diagram was updated.
- Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".
- Notes were added to the package diagrams identifying if they were top or bottom view.
- The A3P030 "132-Pin QFN" table is new.
- The A3P060 "132-Pin QFN" table is new.
- The A3P125 "132-Pin QFN" table is new.
- The A3P250 "132-Pin QFN" table is new.
- The A3P030 "100-Pin VQFP" table is new.

A.27 Revision 0.7 - 01/2007

The following is the summary of changes in revision 0.7 of the document:

- In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77

A.28 Revision 0.6 - 04/2006

The following is the summary of changes in revision 0.6 of the document:

- The term flow-through was changed to pass-through.
- Table 1 was updated to include the QN132.
- The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.
- "Automotive ProASIC 3 Ordering Information" was updated with the QN132.
- "Temperature Grade Offerings" was updated with the QN132.
- B-LVDS and M-LDVS are new I/O standards added to the datasheet.
- The term flow-through was changed to pass-through.
- Figure 2-7 • Efficient Long-Line Resources was updated.
- The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.

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- The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC 3E CCC Options.
 - The "SRAM and FIFO" section was updated.
 - The "RESET" section was updated.
 - The "WCLK and RCLK" section was updated.
 - The "RESET" section was updated.
 - The "RESET" section was updated.
 - The "Introduction" of the "Advanced I/Os" section was updated.
 - The "I/O Banks" section is new. This section explains the following types of I/Os:
 - Advanced
 - Standard+
 - Standard
 - Table 2-12 • Automotive ProASIC 3 Bank Types Definition and Differences is new. This table describes the standards listed above.
 - PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards
 - Table 2-13 • ProASIC 3 I/O Features was updated.
 - The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.
 - The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.
 - Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC 3 Devices.
 - The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC 3 Devices were updated.
 - The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.
 - A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC 3 Devices (maximum drive strength and high slew selected).
 - Table 2-18 • Automotive ProASIC 3 I/O Attributes vs. I/O Standard Applications
 - Table 2-50 • ProASIC 3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device)
 - Table 2-51 • ProASIC 3 Output Drive for Standard+ I/O Bank Type was updated.
 - Table 2-54 • ProASIC 3 Output Drive for Advanced I/O Bank Type was updated.
 - The "x" was updated in the "User I/O Naming Convention" section.
 - The "VCC Core Supply Voltage" pin description was updated.
 - The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.
 - The "VJTAG JTAG Supply Voltage" pin description was updated.
 - The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.
 - The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.
 - The "JTAG Pins" section was updated to include information on what happens when the pin is unused.
 - The "Programming" section was updated to include information concerning serialization.
 - The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.
 - "DC and Switching Characteristics" chapter was updated with new information.
 - The A3P060 "100-Pin VQFP" pin table was updated.
 - The A3P125 "100-Pin VQFP" pin table was updated.
 - The A3P060 "144-Pin TQFP" pin table was updated.
 - The A3P125 "144-Pin TQFP" pin table was updated.
 - The A3P125 "208-Pin PQFP" pin table was updated.
 - The A3P400 "208-Pin PQFP" pin table was updated.
 - The A3P060 "144-Pin FBGA" pin table was updated.
 - The A3P125 "144-Pin FBGA" pin table is new.

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- The A3P400 "144-Pin FBGA" is new.
 - The A3P400 "256-Pin FBGA" was updated.
 - The A3P1000 "256-Pin FBGA" was updated.
 - The A3P400 "484-Pin FBGA" was updated.
 - The A3P1000 "484-Pin FBGA" was updated.
 - The A3P250 "100-Pin VQFP*" pin table was updated.
 - The A3P250 "208-Pin PQFP*" pin table was updated.
 - The A3P1000 "208-Pin PQFP*" pin table was updated.
 - The A3P250 "144-Pin FBGA*" pin table was updated.
 - The A3P1000 "144-Pin FBGA*" pin table was updated.
 - The A3P250 "256-Pin FBGA*" pin table was updated.
 - The A3P1000 "256-Pin FBGA*" pin table was updated.
 - The A3P1000 "484-Pin FBGA*" pin table was updated.

A.29 Revision 0.5 - 11/2005

The following is the summary of changes in revision 0.5 of the document:

- The "I/Os Per Package" table was updated for the following devices and packages:
 - Device Package
 - A3P250/M7ACP250VQ100
 - A3P250/M7ACP250FG144
 - A3P1000FG256

A.30 Revision 0.4

The following is the summary of changes in revision 0.4 of the document:

- M7 device information is new.
- The I/O counts in the "I/Os Per Package" table were updated.

A.31 Revision 0.3

The following is the summary of changes in revision 0.3 of the document:

- The "I/Os Per Package" table was updated.
- M7 device information is new.
- Table 2-4 • ProASIC 3 Globals/Spines/Rows by Device was updated to include the number of rows in each top or bottom spine.
- EXTFB was removed from Figure 2-24 • ProASIC 3E CCC Options.
- The "PLL Macro" section was updated. EXTFB information was removed from this section.
- The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-11 • ProASIC 3 CCC/PLL Specification
- EXTFB was removed from Figure 2-27 • CCC/PLL Macro.
- Table 2-13 • ProASIC 3 I/O Features was updated.
- The "Hot-Swap Support" section was updated.
- The "Cold-Sparing Support" section was updated.
- "Electrostatic Discharge (ESD) Protection" section was updated.
- The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC 3 Devices was updated.
- In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to VCC_IB1.
- The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.
- The "JTAG Pins" section was updated.
- "128-Bit AES Decryption" section was updated to include M7 device information.
- Table 3-6 was updated.
- Table 3-7 was updated.

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- In Table 3-11, PAC4 was updated.
 - Table 3-20 was updated.
 - The note in Table 3-32 was updated.
 - All Timing Characteristics tables were updated from LVTTTL to Register Delays
 - The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.
 - F_{TCKMAX} was updated in Table 3-110.

A.32 Revision 0.2

The following is the summary of changes in revision 0.2 of the document:

- Figure 2-11 was updated.
- The "Clock Resources (VersaNets)" section was updated.
- The "VersaNet Global Networks and Spine Access" section was updated.
- The "PLL Macro" section was updated.
- Figure 2-27 was updated.
- Figure 2-20 was updated.
- Table 2-5 was updated.
- Table 2-6 was updated.
- The "FIFO Flag Usage Considerations" section was updated.
- Table 2-13 was updated.
- Figure 2-24 was updated.
- The "Cold-Sparing Support" section is new.
- Table 2-43 was updated.
- Table 2-18 was updated.
- Pin descriptions in the "JTAG Pins" section were updated.
- The "User I/O Naming Convention" section was updated.
- Table 3-7 was updated.
- The "Methodology" section was updated.
- Table 3-40 and Table 3-39 were updated.
- The A3P250 "100-Pin VQFP*" pin table was updated.
- The A3P250 "208-Pin PQFP*" pin table was updated.
- The A3P1000 "208-Pin PQFP*" pin table was updated.
- The A3P250 "144-Pin FBGA*" pin table was updated.
- The A3P1000 "144-Pin FBGA*" pin table was updated.
- The A3P250 "256-Pin FBGA*" pin table was updated.
- The A3P1000 "256-Pin FBGA*" pin table was updated.
- The A3P1000 "484-Pin FBGA*" pin table was updated.

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