M21518-13

3G/HD/SD-SDI Multi-rate Video Cable Driver

Rev V5

The M21518 is a very low power cable driver for SMPTE compliant digital video applications. The M21518 can drive a pair of 75 Ω coaxial cables or 50 Ω equivalent loads at SDI data rates from 270 Mbps to 2.97 Gbps. The device is capable of outputting SDI signals with typical jitter values of 12 ps peak–to–peak, when operating at 2.97 Gbps.

The M21518 cable driver includes integrated input and output termination resistors, input equalization for up to 36" of FR4 trace, two connectors, and exceptional Output Return Loss (ORL) making it ideal for high speed, 3G-SDI, designs.

The device features integrated supply regulators, allowing it to be powered from 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.8 V, the cable driver consumes only 52 mW at 2.97 Gbps. Furthermore, the power rails for the input and output circuitry are electrically isolated on-chip and as such may be connected to different voltage rails on the board. This feature enables the device to be DC coupled to any upstream device in the 1.2 V to 3.3 V range.

The cable driver also provides cable detect and Loss of Signal (LOS) functionality. The device may be configured to automatically power down at cable disconnect or loss of input signal.

The M21518 is available in a green and RoHS-compliant 24-pin QFN package.

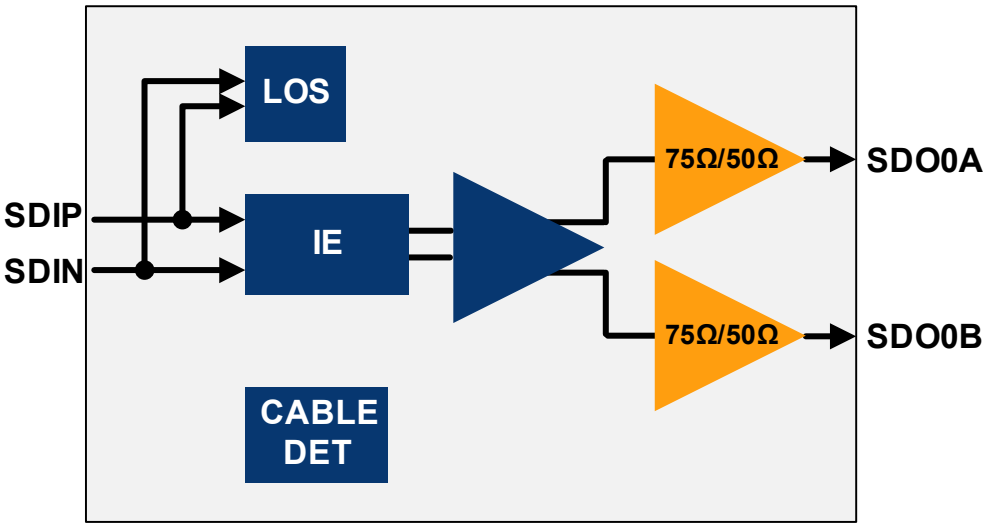
Applications

- 3G/HD/SD Video Switchers
- 3G/HD/SD Video Routers
- 3G/HD/SD Distribution Amplifiers
- DVB-ASI Equipment
- SMPTE 259C/D, 292, 424M, DVB ASI 270 Mbps

Features

- Two non-inverting outputs
- Typical output jitter of 12 ps peak–to–peak at 2.97 Gbps
- Exceptional Output Return Loss with no matching network
- Very low power design; 52 mW @1.8 V
- Selectable slew rate for SD and 3G/HD operation
- Input equalization for up to 36" of FR4 + 2 connectors
- Integrated, selectable 75 Ω or 50 Ω output termination
- Integrated 50 Ω input termination
- On-chip regulators for operation from 1.8 V to 3.3 V DC supply
- Universal DC coupling at the input from 1.2 V to 3.3 V
- Cable detect on both outputs with automatic power down and power up upon cable disconnect and re-connect
- Loss of input signal detection output
- Output mute and power down
- Industrial operating temperature range: -40 °C to 85 °C
- 4 kV HBM and 500 V CDM ESD rating
- 4 mm x 4 mm 24-pin QFN package
- Green and RoHS compliant

M21518 Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M21518G-13*	4 mm x 4 mm 24-pin QFN (RoHS compliant)	–40 °C to 85 °C

* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

Revision History

Revision	Level	Date	Description
V5	Release	December 2015	Updated marking diagram. Added footnotes to Figure 3-8 & Figure 3-9.
V4	Release	November 2015	Revised Z_CTRL resistor value for 75Ω output impedance in Table 3-1. Revised Section 4.3. Updated Figure 3-8 & Figure 3-9..
E (V3)	Release	July 2011	Changed SDI data rates on front page from 143 Mbps to 270 Mbps. Fixed Theta symbol in Table 1-3. In Table 3-1, added Pin 20 to AV_{DD}RegA and Pin 11 to AV_{DD}RegB.
D (V2)	Release	April 2010	Corrected package dimensions in Figure 3-8. Revised description of C_DET_CTRL in Table 4-5. Changed T_{AMB} to T_{CASE} in Table 1-2. Revised DR minimum in Table 1-5. Revised JAO_{PP} minimum in Table 1-5. Changed SMPTE 259 to SMPTE 259C/D. Changed SMPTE 292M to 292.
C (V1)	Release	December 2009	Added thermal resistance coefficient to Table 1-3. Revised maximum power and current figures in Table 1-3. Revised Table 1-5. Added Eye Diagams in Section 2.0.
B (V2A)	Advance	September 2009	Pinout and power down functionality revised.
A (V1A)	Advance	September 2008	Initial Release.

M21518 Marking Diagram

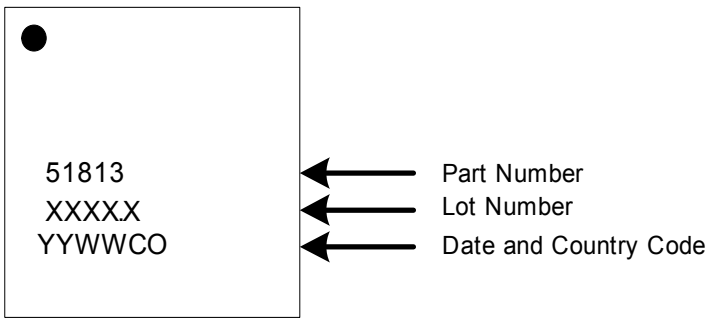


Table of Contents

1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with AV_{DDO} = 1.8 V, AV_{DDI} = 1.2 V, CML inputs at 800 mV differential (R_{LOAD} = 50 Ω), PRBS 2^{10} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	1	-0.5	—	3.6	V
$AV_{DD}OA/B$	Analog supply for output circuitry	1	-0.5	—	3.6	V
T_{STORE}	Storage Temperature	1	-65	—	150	°C
ESD	Human Body Model (HBM)	1	-4	—	4	KV
ESD	Charge Device Model (CDM)	1	-500	—	500	V
LU	Latch Up @ 85 °C	1	-200	—	200	mA
HSIC	Maximum High-speed input current	1	-100	—	100	mA
HSOC	Maximum High-speed output short circuit current	1	-100	—	100	mA
V_{INMAX}	Input voltage range	1	-0.5	—	AV_{DDI}+0.5	V

NOTES:

1. Exposure to these conditions over extended periods of time may affect device reliability.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	—	1.14	1.2, 1.8, 2.5, or 3.3	3.465	V
$AV_{DD}OA/B$	Analog supply for output circuitry	—	1.71	1.8, 2.5, or 3.3	3.465	V
T_{CASE}	Ambient Operating temperature	1	-40	25	+85	°C
ESD	Human Body Model (HBM)	—	-4	—	4	kV

NOTES:

1. Case temperature.

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
P_{TOTAL}	Total power consumption	AV_{DDI} = 1.2 V AV_{DDO} = 1.8 V Both outputs enabled	1,3	—	52	83	mW
P_{TOTAL}	Total power consumption	AV_{DDI} = 1.2 V AV_{DDO} = 1.8 V One output enabled	1,3	—	41	69	mW
$I\_ AV_{DDI}$	Total AV_{DDI} supply current	AV_{DDI} = 1.2 V	1,3	—	1	3	mA
$I\_ AV_{DDI}$	Total AV_{DDI} supply current	AV_{DDI} = 1.8 V	1,3	—	3	7	mA
$I\_ AV_{DDI}$	Total AV_{DDI} supply current	AV_{DDI} = 3.3 V	1,3	—	10	17	mA
$I\_ AV_{DDO}$	Total AV_{DDO} supply current	Both outputs on	1,2,3	—	28	44	mA
$I\_ AV_{DDO}$	Total AV_{DDO} supply current	One output on	1,2,3	—	22	36	mA
θ_{JA}	Junction to ambient Thermal Resistance		4	—	63	—	°C/W

NOTES:

1. Recommended operating condition—see Table 1-2
2. Current consumption does not change with AV_{DDO} = 1.8 V, 2.5 V or 3.3 V.
3. SD/xHD pin = 0.
4. Airflow = 0 m/s.

Table 1-4. Digital Input and Open Drain Output Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{IH}	Input Logic High	—	0.85 x AV_{DDI}	—	AV_{DDI} + 0.5	V
V_{IF}	Input Logic Floating State	—	0.25 x AV_{DDI}	—	0.75 x AV_{DDI}	V
V_{IL}	Input Logic Low	—	0	—	0.15 x AV_{DDI}	V
I_{IH}	Input Current—Logic High	—	-100	—	100	µA
I_{IL}	Input Current—Logic Low	—	-100	—	100	µA
V_{OL}	Output Logic Low, I_{OL} = 24 mA	—	—	0	0.2 x AV_{DDI}	V

Table 1-5. High Speed Input/Output Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_O	Output Voltage Range	1	730	800	850	mV
t_R/t_F	SD Rise/Fall Time (20–80%)	1,3,4	400	600	800	ps
t_R/t_F	3G/HD Rise/Fall Time (20–80%)	1	—	70	90	ps
t_R-t_F	SD Rise/Fall Time Mismatch	1,3,4	—	—	125	ps
t_R-t_F	3G/HD Rise/Fall Time Mismatch	1,3	—	—	30	ps
DCD	Duty Cycle Distortion, SD	1,4	—	—	100	ps
DCD	Duty Cycle Distortion, 3G, HD	1,3	—	—	30	ps
JAO_{PP}	Additive Output Jitter, SD	1,2,4	—	60	100	ps
JAO_{PP}	Additive Output Jitter, 3G, HD	1,2	—	12	29	ps
S_{22}	Output Return Loss (5 MHz to 1.5 GHz)	6,8	20	—	—	dB
S_{22}	Output Return Loss (5 MHz to 3.0 GHz)	5,8	11	—	—	dB
S_{22}	Output Return Loss (5 MHz to 3.0 GHz)	6,8	14	—	—	dB
DR	Input Data rate	—	270	—	2970	Mbps
V_{ID}	Differential Input Voltage (p–p)	7	400	—	1600	mV
V_{IC}	Input Common mode range	—	AV_{DDI} – 0.6	—	AV_{DDI} + 0.1	V
IE	Input Equalizer Gain Off (EN_EQ = 0)	—	—	0	—	dB
	Input Equalizer Gain Med (EN_EQ = F)	—	—	4	—	dB
	Input Equalizer Gain High (EN_EQ = H)	—	—	6	—	dB
R_{INT}	Input Termination to AV_{DDI}	—	40	50	60	Ω

NOTES:

1. Measured AC coupled into 1 m coaxial cable, terminated with appropriate 75 Ω or 50 Ω load.
2. Measured with PRBS 2^{15}-1 test pattern.
3. For data rates above 360 Mbps, the cable driver must be in HD mode (SD/xHD = 0).
4. SD/xHD = 1, measured at 270 Mbps.
5. Without external matching network.
6. With external matching network $R_{matching}$=75 Ω, $L_{matching}$=1nH, only applicable to 75 Ω mode.
7. EQ_EN = L (input equalization off), point blank.
8. As measured on MACOM EVM at BNC connector with output impedance set to 75 Ω.

2.0 Typical Performance Characteristics

Figure 2-1. Eye Diagram at 270 Mbps

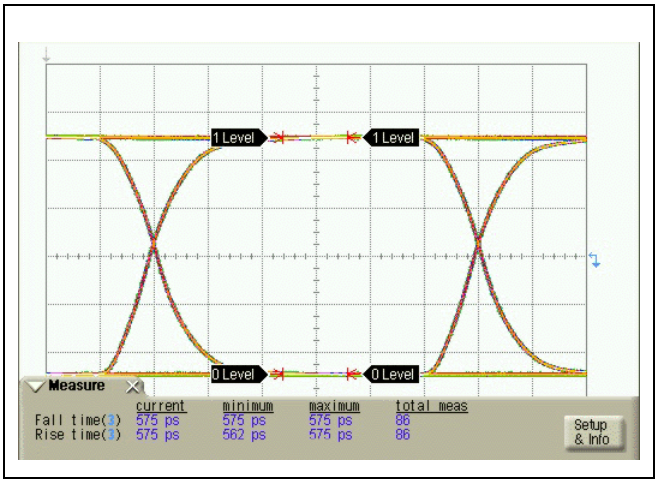


Figure 2-2. Eye Diagram at 1485 Mbps

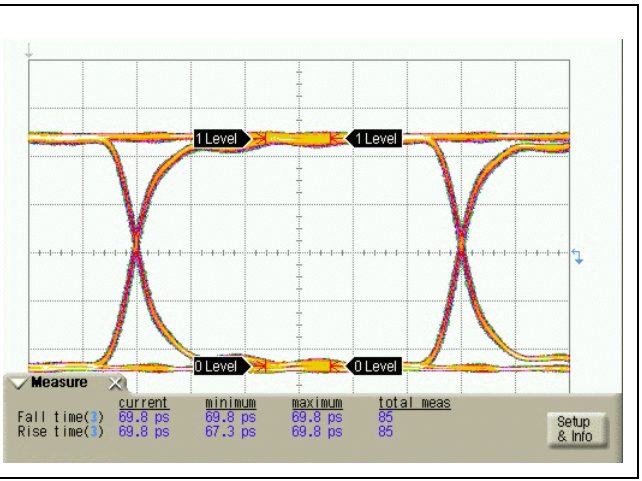
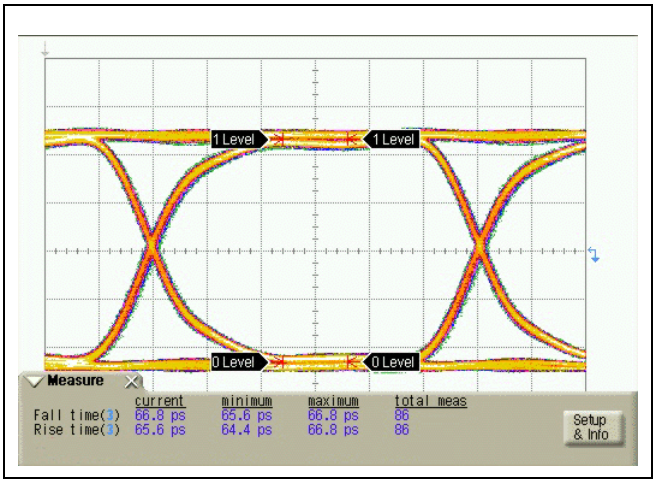


Figure 2-3. Eye Diagram at 2970 Mbps



3.0 Pinout Diagram, Pin Description, and Package Drawing

Figure 3-1. Pinout Diagram (Top View)

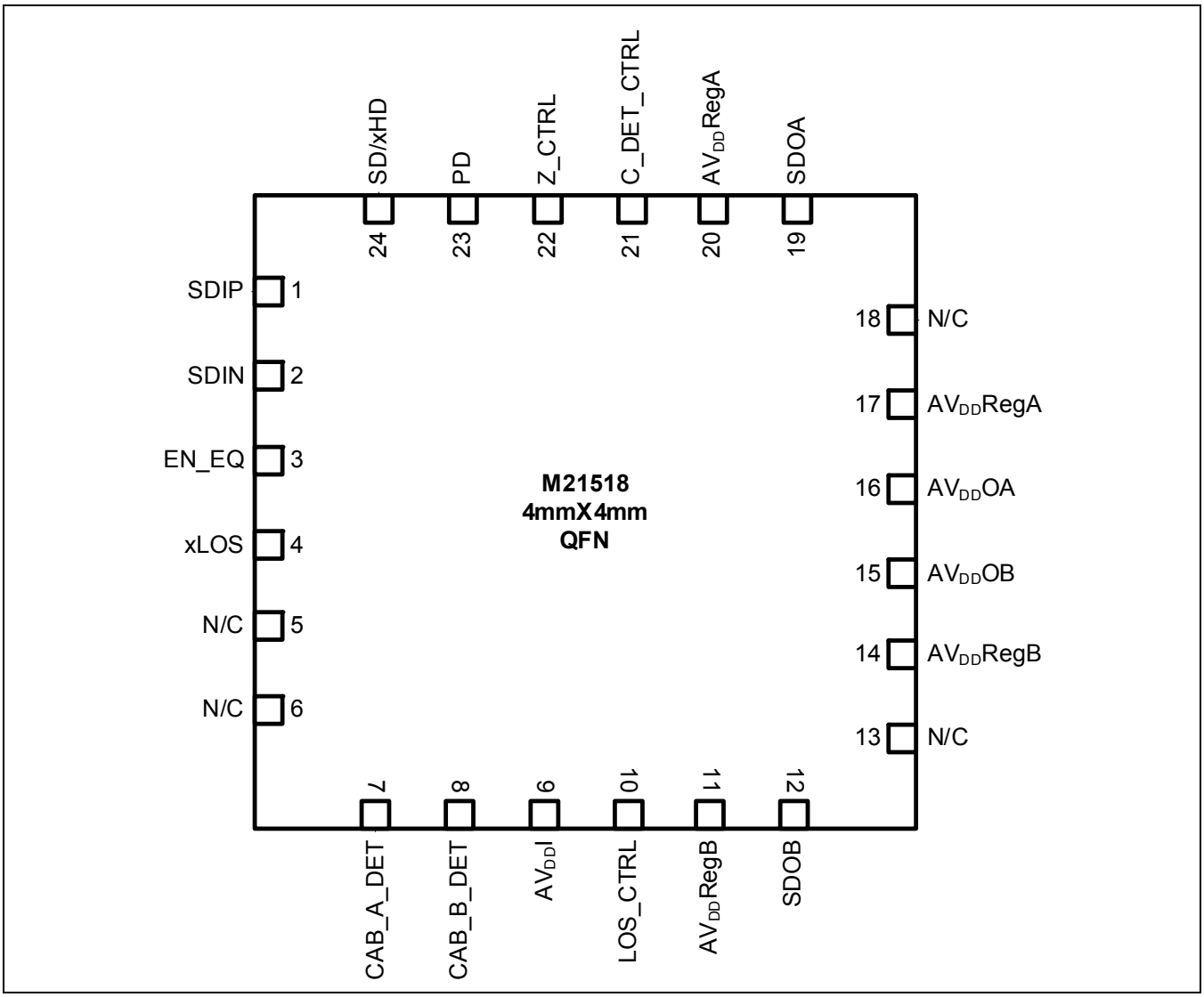


Table 3-1. Pin Description (1 of 2)

Pin Name	Pin Number	Type	Description
AV_{SS}	Center Ground Paddle	Power	Chip Ground
AV_{DDI}	9	Power	Positive supply for input circuitry
AV_{DD}RegA	17, 20	Power	RegulatorA bypass capacitor connection, positive supply for outputA
AV_{DD}RegB	11, 14	Power	RegulatorB bypass capacitor connection, positive supply for outputB
AV_{DD}OA	16	Power	Positive supply for reglatorA
AV_{DD}OB	15	Power	Positive supply for reglatorB
SDOA	19	O-Analog	High speed serial output A
SDOB	12	O-Analog	High speed serial output B
SDIP/N	1,2	I-Analog	High speed serial video data input
Z_CTRL	22	I-Analog	Sets output impedance through an external Z_CTRL resistor connected to AV_{SS} Z_CTRL=665 Ω to set 75 Ω output impedance Z_CTRL=250 Ω to set 50 Ω output impedance
SD/xHD	24	I-DIGITAL	Output slew rate control L = SDO has 3G/HD slew rate H = SDO has SD slew rate
CAB_A_DET	7	Open Drain Output with internal 100k pull up	Cable Detect Output for Output A L = Cable not detected on output A H = Cable detected on output A
CAB_B_DET	8	Open Drain Output with internal 100k pull up	Cable Detect Output for Output B L = Cable not detected on output B H = Cable detected on output B
PD	23	3-state/I-DIGITAL	Power down control L = SDOA on, SDOB power down F = Both outputs on H = Power down both outputs
C_DET_CTRL	21	3-state/I-DIGITAL	Cable Detect Control L = If any output is disconnected, device will be powered down F = Both outputs need to be disconnected for device to be powered down H = Power down upon cable detect disabled; cable detect outputs are active
LOS_CTRL	10	3-state/I-DIGITAL	Loss of Signal (LOS) control L = LOS circuit disabled F = LOS circuit enabled; device powers down on LOS H = LOS circuit enabled; no power down on LOS

Table 3-1. Pin Description (2 of 2)

Pin Name	Pin Number	Type	Description
EN_EQ	3	3-state/I-DIGITAL	Input equalization L = No Input Equalization on SDIP/N F = Medium Input Equalization on SDIP/N H = High Input Equalization on SDIP/N
xLOS	4	Open Drain Output with internal 100k pull up	Loss of input signal output (LOS) L = Signal not present H = Signal present

NOTES:

1. 3-state inputs have a default of F (floating).
2. A Z_CTRL resistance of 665Ω will also provide 800mVpp output swing.

Figure 3-2. Differential Input (SDIP, SDIN)

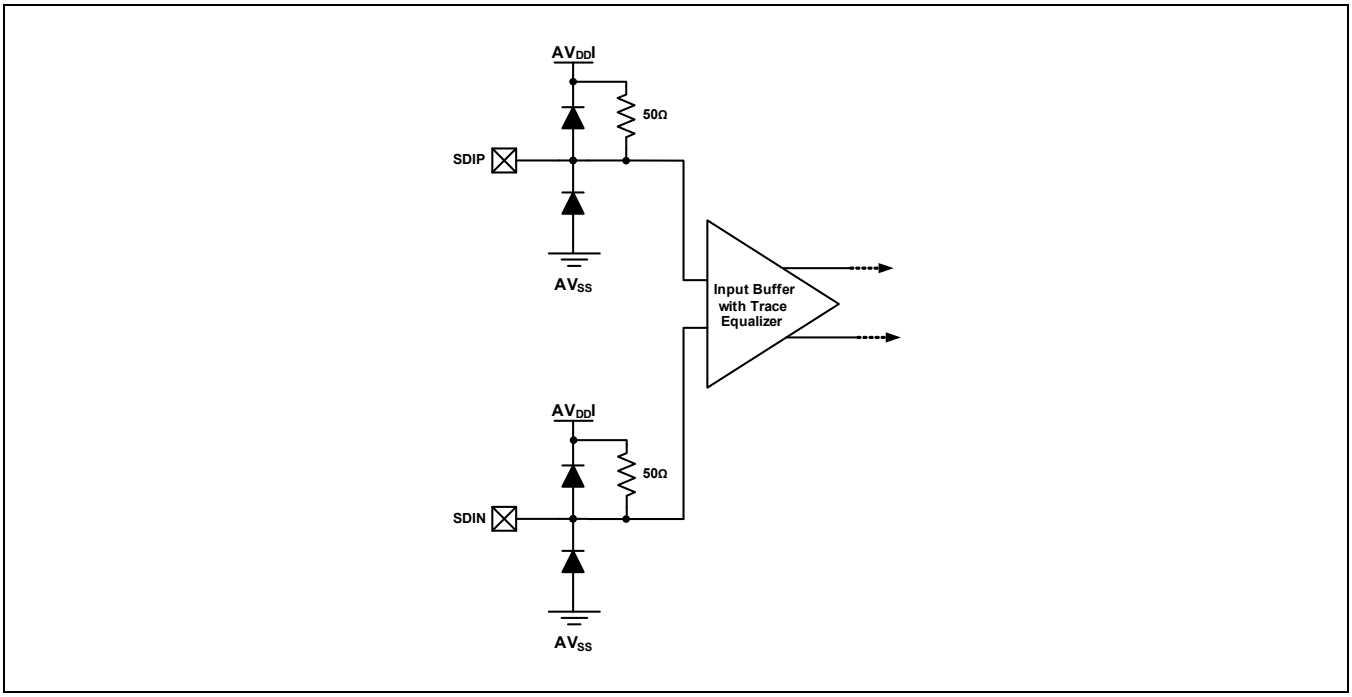


Figure 3-3. Single-Ended Output (SDOA, SDOB)

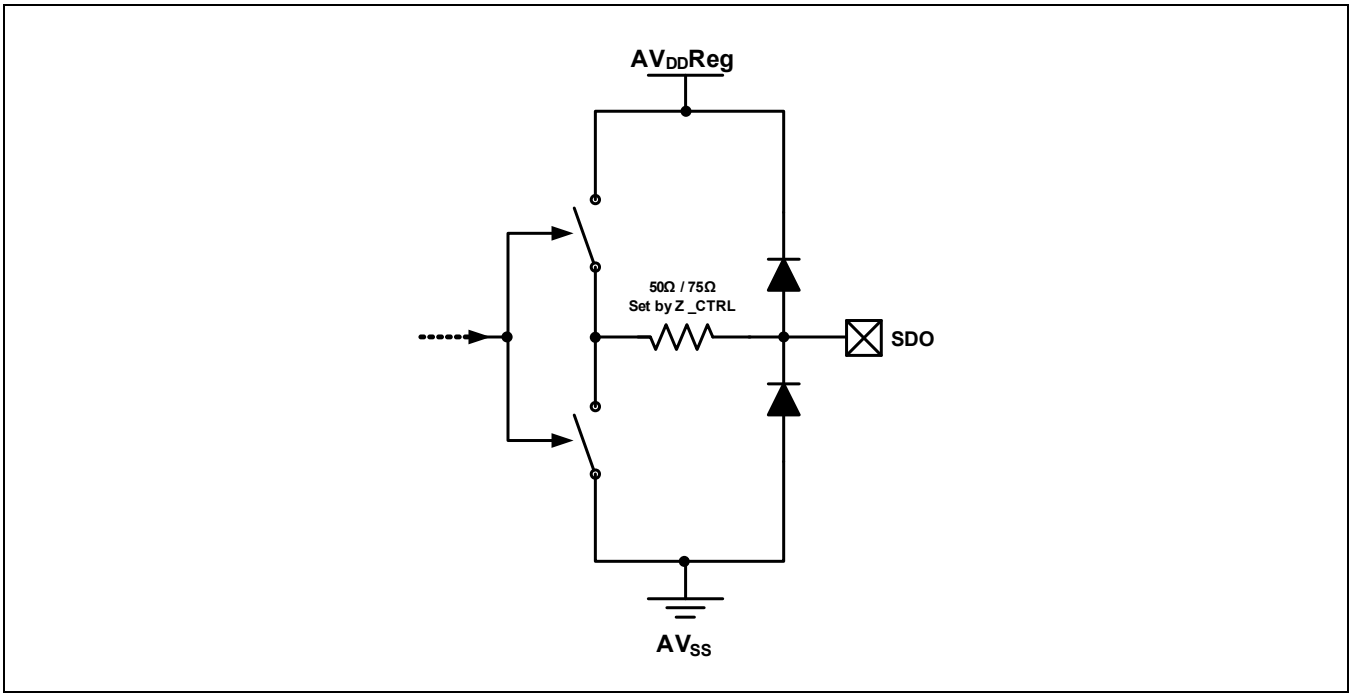


Figure 3-4. Digital Input Pin (SD/xHD)

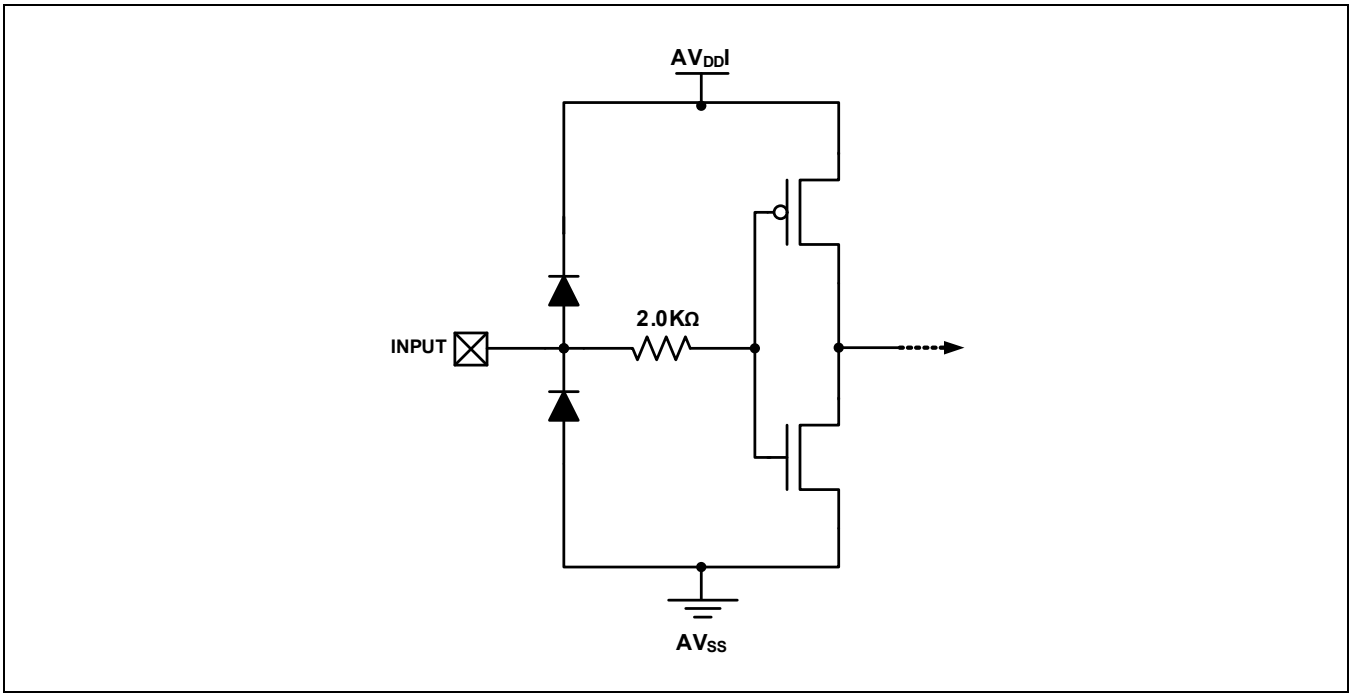


Figure 3-5. 3-State Logic Input (PD, C_DET_CTRL, LOS_CTRL, EN_EQ)

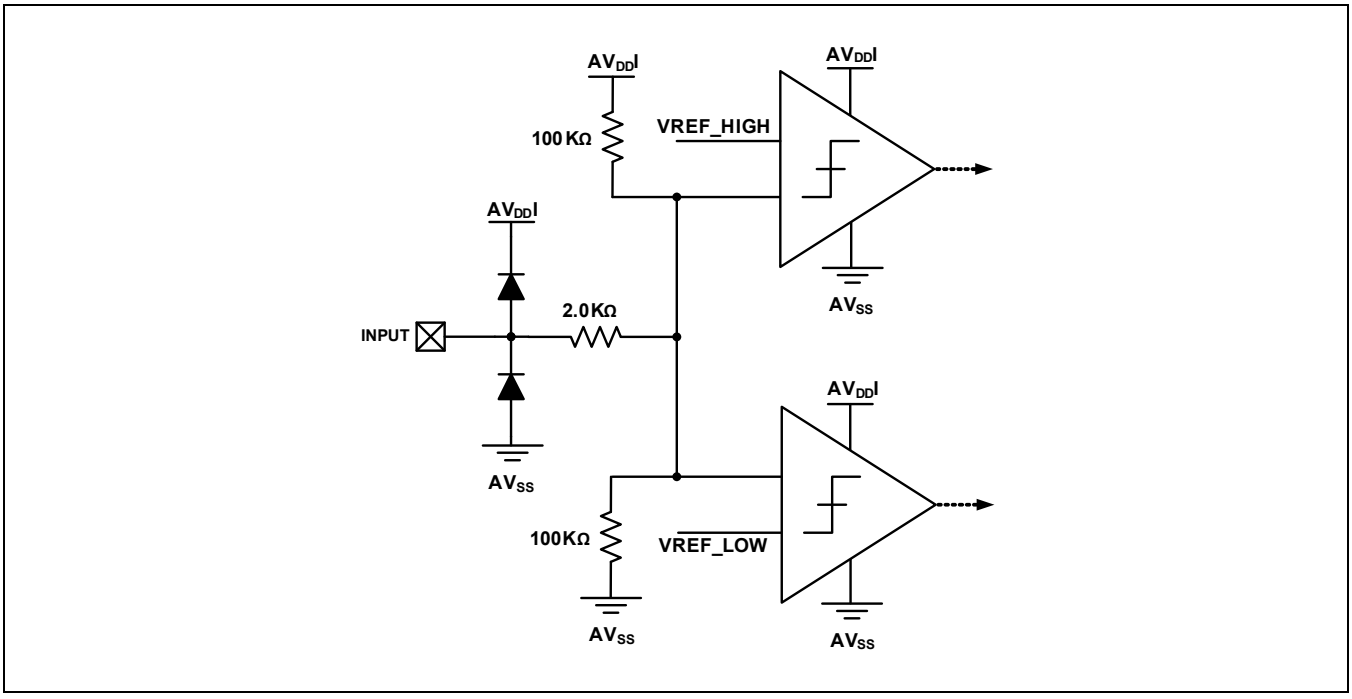
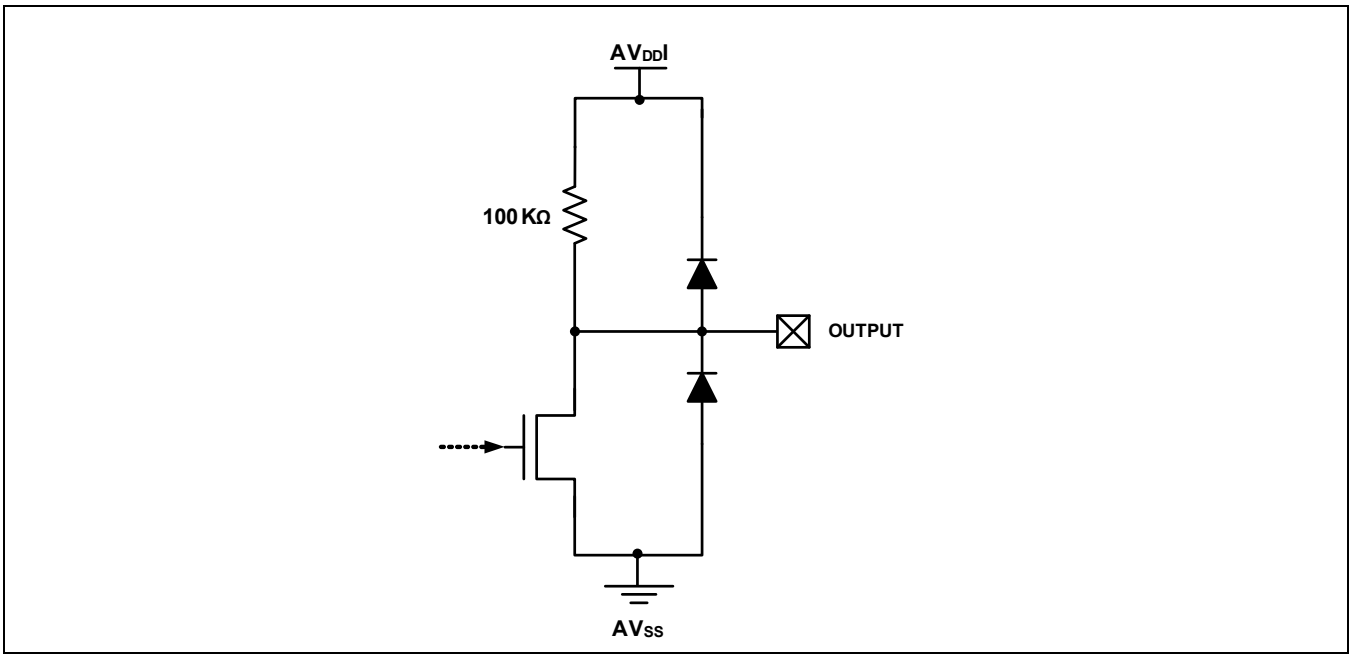


Figure 3-6. Open Drain Logic Output (CAB_A_DET, CAB_B_DET, xLOS)



The M21518 is assembled in 24-pin 4 mm x 4 mm Quad Flat No-Lead (QFN) package. The exposed die paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB ground. A cross-section of the QFN package can be found in Figure 3-7.

Figure 3-7. QFN Package Cross Section

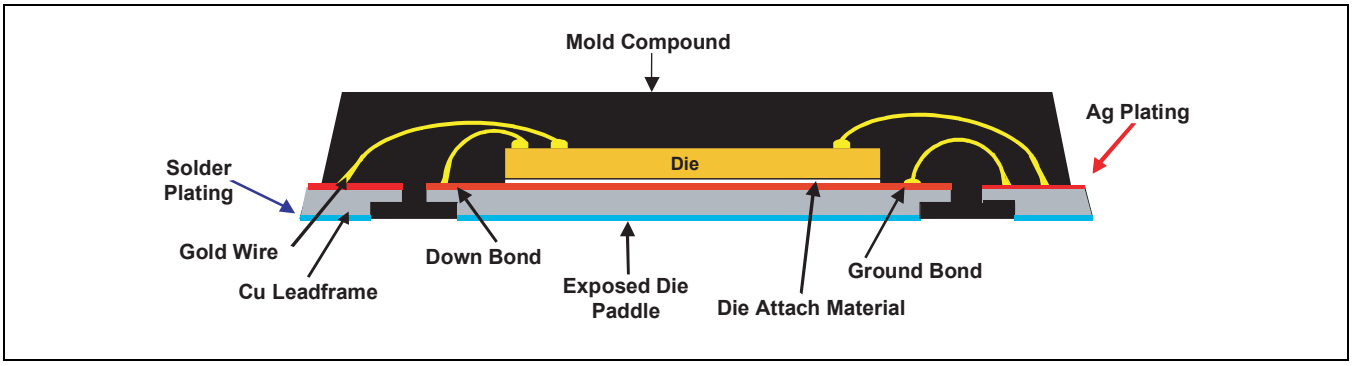
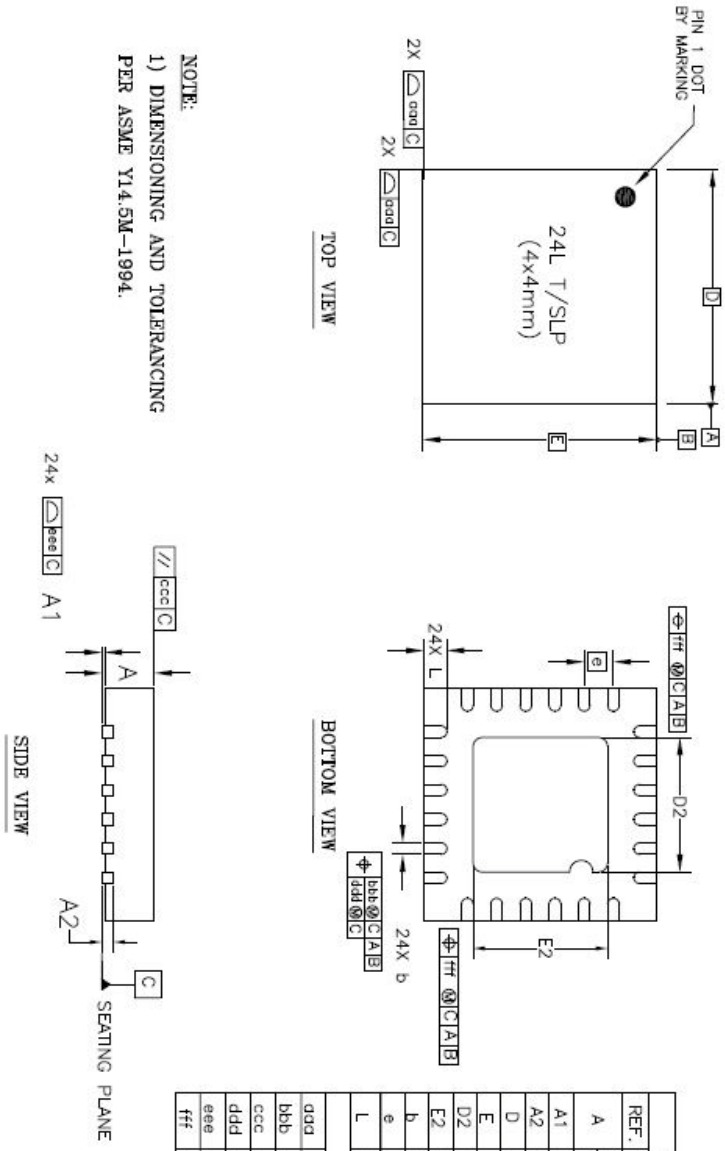


Figure 3-8. Package Drawing



Dimensional Ref.			
	REF.	Min.	Nom	Max.
A		0.800	0.850	0.900
A1		0.000	—	0.050
A2			0.203 REF	
D			4.000 BSC	
E			4.000 BSC	
D2		2.250	2.300	2.350
E2		2.250	2.300	2.350
b		0.150	0.200	0.250
e			0.500 BSC	
L		0.350	0.400	0.450
Dimensional Tol.				
aaa			0.050	
bbb			0.100	
ccc			0.050	
ddd			0.050	
eee			0.080	
fff			0.050	

1. For dimension reference A, Min. is 0.800, Nom. is 0.850 and Max. is 0.900.
2. New Unisem package and old Amkor package have the same footprint dimensions.

Figure 3-9. 24-Pin Package Dimensions

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
	0.700	0.750	0.800
A1	0.000	—	0.050
A2	0.203 REF		
D	4.000 BSC		
E	4.000 BSC		
D2	2.250	2.300	2.350
E2	2.250	2.300	2.350
b	0.150	0.200	0.250
e	0.500 BSC		
L	0.350	0.400	0.450
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

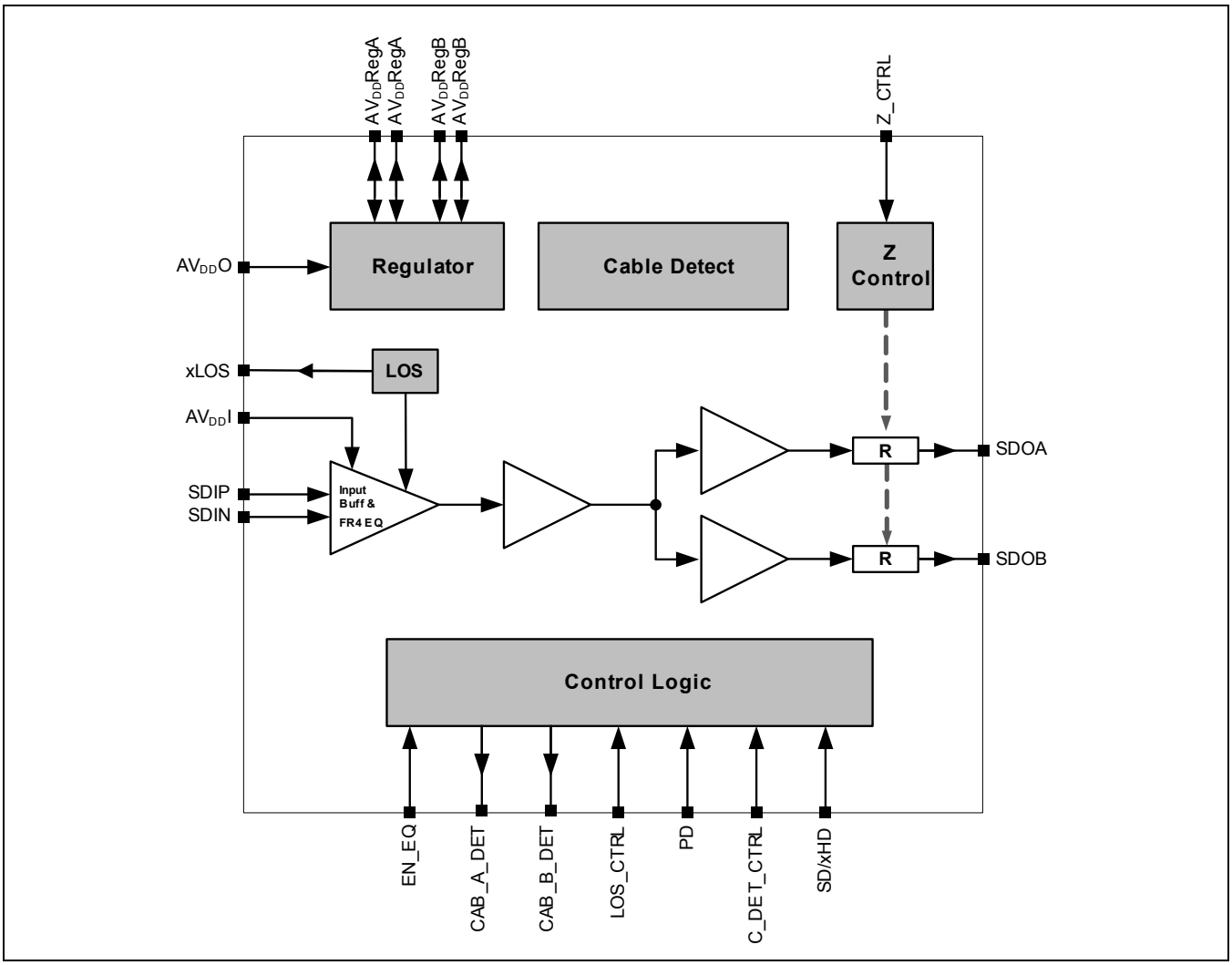
1. For dimension reference A, Min. is 0.800, Nom. is 0.850 and Max. is 0.900.
2. New Unisem package and old Amkor package have the same footprint dimensions.

4.0 Functional Description

4.1 Block Diagram

Figure 4-1 is the functional block diagram of the M21518. The subsequent sections provide additional detail on the operation of the device.

Figure 4-1. M21518 Functional Block Diagram



4.2 Input Description

The M21518 has a differential input, with integrated 50 Ω pull-up resistors to AV_{DDI}. AV_{DDI} may be supplied from a 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply. The input buffers are compatible with PCML, LVDS or LVPECL signal levels.

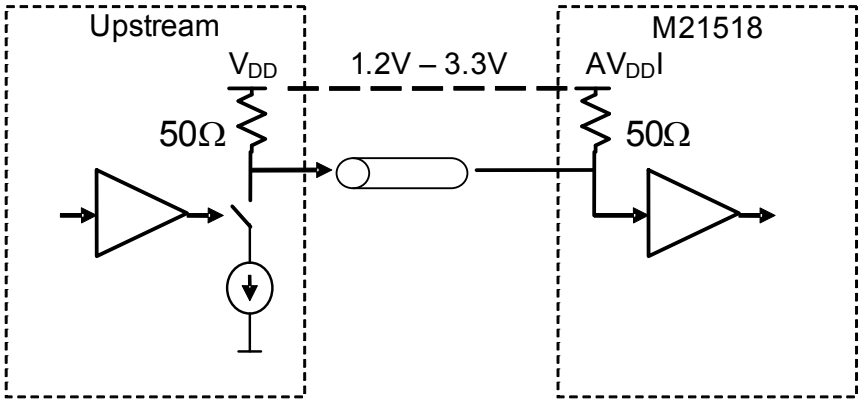
To improve signal integrity in large systems, the input has programmable input equalization (IE) with three gain levels: 0 dB, 4 dB, 6 dB.

Setting the gain to 0 dB effectively disables the IE feature. The pin EN_EQ allows for selecting the proper level of input equalization based on the board characteristics at the input. The maximum level of equalization compensates for up to 36” of FR4 trace. The operation of the EN_EQ pin is summarized in Table 4-1 below.

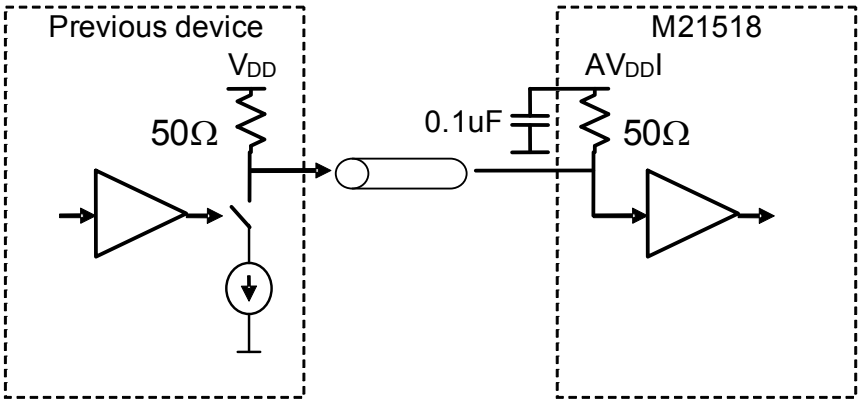
Table 4-1. Operation of EN_EQ Pin

Pin	Level	Function
EN_EQ	L	SDIP/N IE EQ gain = 0 dB
	F	SDIP/N IE EQ gain = 4 dB
	H	SDIP/N IE EQ gain = 6 dB

In 3G/HD/SD SDI applications, it is best to avoid AC coupling data interfaces between devices, if possible. DC coupling will result in increased system jitter margin. Also, DC coupling eliminates the requirement for additional components on the board. In order to accommodate DC coupling to the upstream device, the AV_{DDI} domain of the M21518 is electrically isolated from all other power domains on chip. This allows for it to be tied to the V_{DD} of the previous device’s output driver enabling a fully DC coupled system, as shown below.



Alternatively, a “self-biasing” scheme can be used at the input. This offers the benefit of having the V_{DD} of the previous device and the power domain(s) of the M21518 completely separated, while allowing dc coupling:



In this configuration, the minimum input common mode that can be tolerated, is 1.2 V.

If for any reason AC coupling is necessary, then a capacitor of 4.7 µF or greater must be used.

A Loss of Signal (LOS) detector circuit monitors the input and issues an alarm when the input signal goes below the detection threshold. The detection threshold is 90 mV_{PP} with +90 mV hysteresis. This means that if the input signal level drops below 90 mV_{PP}, then the LOS alarm is asserted. For the alarm to be de-asserted, the input signal must increase to greater than 180 mV_{PP}. This prevents the internal LOS alarm from chattering.

Depending on the state of the LOS_CTRL pin, the LOS alarm at the input can power down the associated signal path and forces the corresponding output to low level. The LOS alarm can be monitored at the xLOS pin, it is low when asserted.

4.3 Output Description

Unlike conventional SMPTE compliant cable drivers, the M21518 uses a voltage mode implementation as opposed to current mode. This allows for significant power savings when compared to previous generation cable drivers, with the additional benefit of two positive polarity outputs.

Internally, an output buffer drives a 1.6 V amplitude signal through an integrated impedance load. The impedance of the load is set by the external Z_CTRL resistor to AV_{SS}. For most applications Z_CTRL should be 665 Ω, which sets the output load to 75 Ω. If the application requires a 50 Ω output impedance, Z_CTRL may be 250 Ω. In both cases Z_CTRL must have 1% tolerance.

The M21518 can meet SMPTE Output Return Loss (ORL) specifications without the need for an external matching network. However, for additional margin a matching network consisting of a 75 Ω resistor and a 1 nH inductor may be used.

The device has a power down pin, PD. The operation of the PD pin is summarized in Table 4-2 below. When only SDOB is powered down, the signal at SDOB is set to low. When both SDOA and SDOB are powered down, both outputs are high impedance.

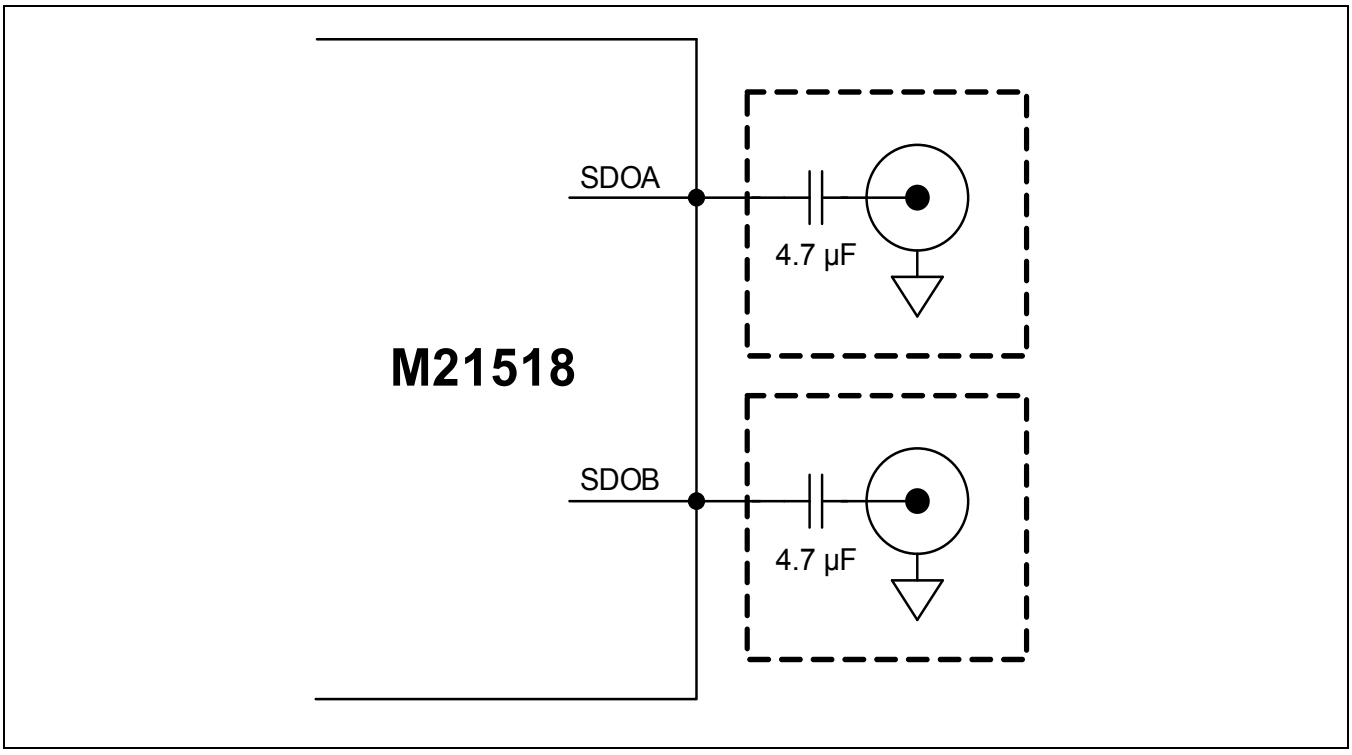
Table 4-2. Operation of PD Pin

Pin	Level	Function
PD	L	SDOA on, SDOB powered down
	F	Both SDOA and SDOB on
	H	Both SDOA and SDOB powered down

Figure 4-2 shows a typical output circuit.

When the cable detect function is enabled, only the outputs used need to be connected, while unused outputs may be left floating. However, if the cable detection function is disabled, the unused output must be powered down or properly terminated. When SDOB only is powered down, SDOB output will be approximately 75 Ω to ground. When both SDOA and SDOB are powered down, both outputs will be high impedance

Figure 4-2. Typical Output Circuit (all Outputs Connected)



4.4 Power Supply Description

The device features two internal regulators to supply the power for the drivers for each output. $AV_{DD}OA$ and $AV_{DD}OB$ supply the voltage to each output's respective regulator. These pins may be connected to DC voltages ranging from 1.8 V to 3.3 V. Each regulator pin requires an external 1 µF bypass capacitor to ground, which must be connected to $AV_{DD}RegA$ and to $AV_{DD}RegB$. It is recommended to add a secondary 10 nF bypass capacitor on each regulator output as close to pin as possible.

In addition to supplying the output stage for SDOB, $AV_{DD}OB$ is also used to power the core circuitry.

A completely separate supply domain, AV_{DDI}, provides the supply for the high-speed serial input pins. The input termination and ESD protection for the SDI pins and the digital control input pins are referenced to this supply. The isolated domain allows DC coupling to an upstream device that is running from a different supply voltage. For example, if, in order to save power, $AV_{DD}OA/B$ are connected to 1.8 V, but the cable driver must interface to a reclocker that uses a 3.3 V supply, then DC coupling can be achieved by simply connecting AV_{DDI} to the 3.3 V rail.

Figure 4-3 to 4-5 show three examples of how the cable driver can be configured. Note that even when only one output is enabled, both output regulators must be supplied with the correct voltage.

Figure 4-3. Supply Configuration, Both A and B Outputs Used

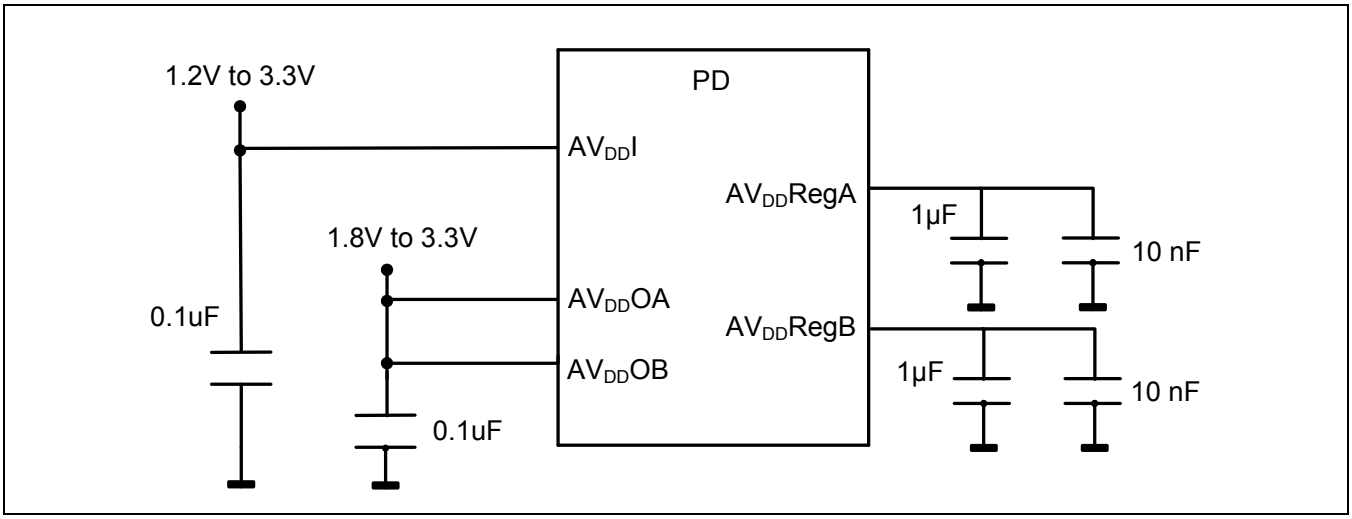


Figure 4-4. Supply Configuration, Output A Used, Output B Powered Down

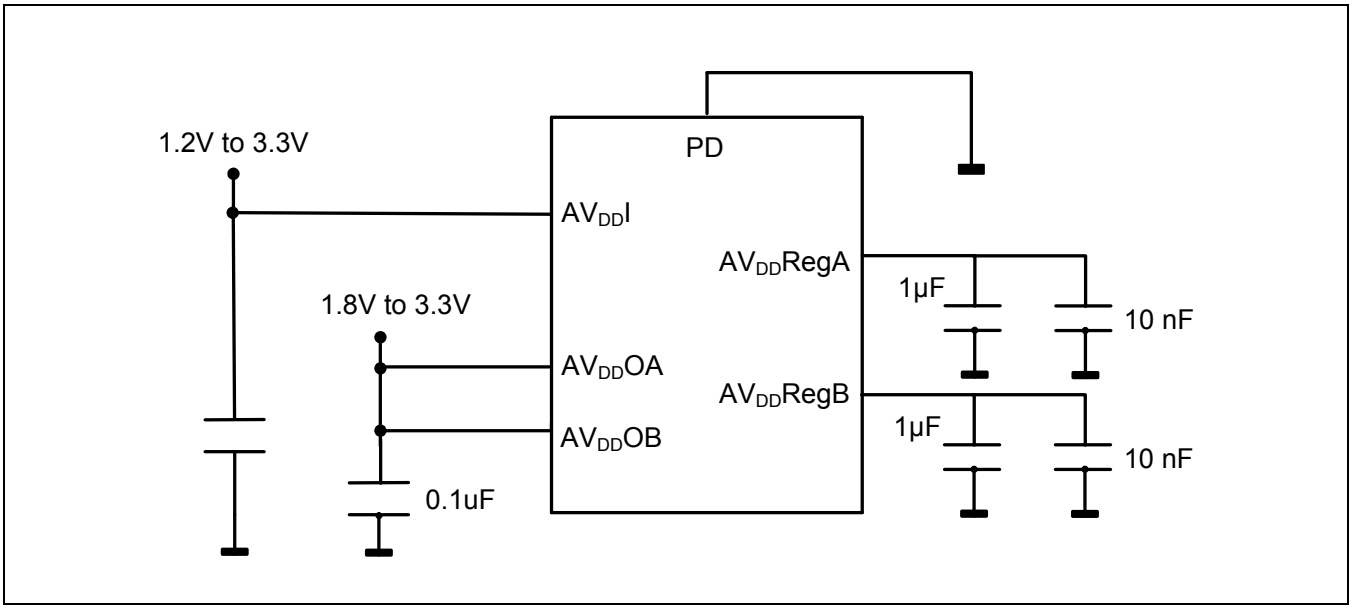
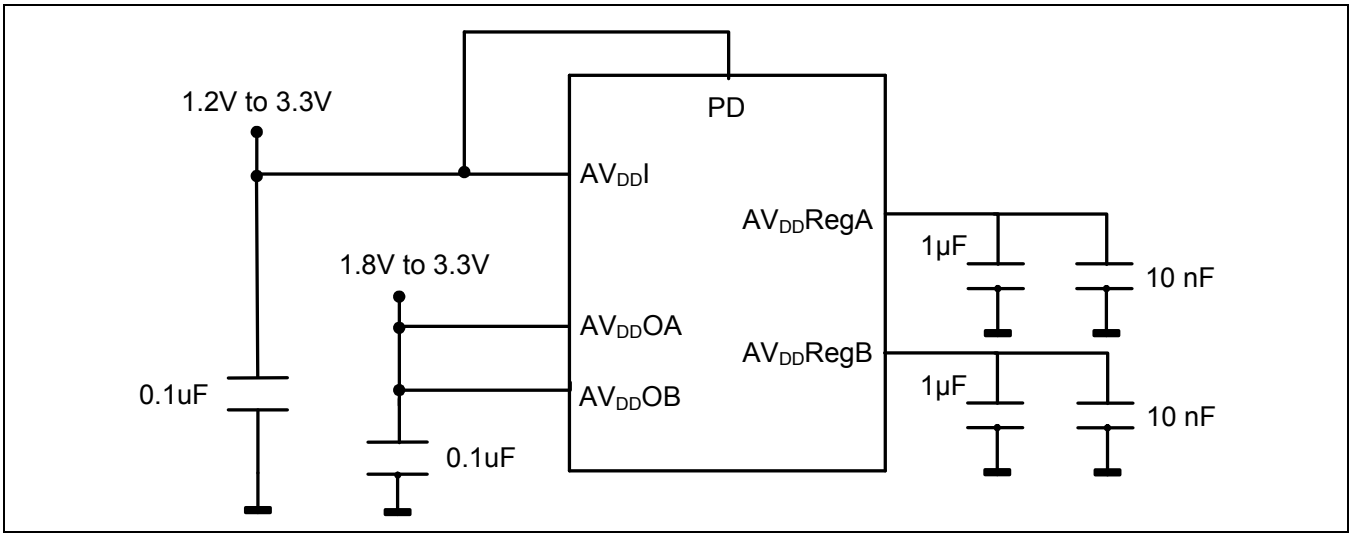


Figure 4-5. Supply Configuration, Power Down Mode



4.5 Logic Control Signals

The digital logic control signals are ESD protected and referenced to the AV_{DDI}. This allows the device to interface to many different logics levels from different supply domains.

Some pins have a state called "F"; this stands for "floating." To assert this state leave the pin unconnected or undriven.

4.5.1 Slew Rate Control (SD/xHD)

Pin SD/xHD controls the slew rate of the high-speed output. To comply with the SMPTE specification the slew rate is slowed down to approximately 600 ps when in SD mode. Note that there is no pull-up on the SD/xHD pin, so it should not be left floating.

Table 4-3. Slew Rate Control (SD/xHD)

Pin	Level	Function
SD/xHD	L	Set SDOA/B Slew rate to 3G/HD Levels
	H	Set SDOA/B Slew rate to SD Levels

4.5.2 Power Down Control

The PD pin can be used to power down one or both of the M21518 high-speed outputs. This control is independent of the cable detect and LOS power down controls.

Table 4-4. Operation of PD Pin

Pin	Level	Function
PD	L	SDOA on, SDOB powered down
	F	Both outputs on
	H	Power down both outputs

4.5.3 Cable Detect Control

The M21518 features an integrated near-end cable detector. This circuit can detect whether a cable has been disconnected from an output and whether or not it is reconnected without requiring any additional external components.

Utilizing the cable detection feature has several system level advantages such as:

- Reduced power consumption when no cable is connected to both outputs
- Reduced EMI
- Eliminates the requirement for external termination

If C_DET_CTRL pin = 'L' and either output A or B are disconnected, the device will automatically power down. If C_DET_CTRL pin = 'F' and both output A and B are disconnected, the device will automatically power down. In both cases the resulting power reduction is 50%.

Table 4-5. Cable Detection Functions

Pin	Level	Function
C_DET_CTRL	L	Powers down if any active output is disconnected.
	F	Powers down if all active outputs are disconnected.
	H	Power down disabled, but CAB_A_DET is active and if SDOB is enabled then CAB_B_DET is also active.

There are two cable detection outputs (CAB_A_DET and CAB_B_DET). These are always active and go to a logic low when SDOA and SDOB respectively are disconnected from a cable or matched load.

The cable detection power down function may be disabled by setting C_DET_CTRL = H. In this state CAB_A_DET and CAB_B_DET are still active.

4.5.4 Loss of Signal Control

As mentioned in Section 4.2, the M21518 features a Loss of Signal monitor on the high speed data input.

The LOS_CTRL pin controls this function as detailed in Table 4-6.

Table 4-6. Loss of Signal Control

Pin	Level	Function
LOS_CTRL	L	LOS circuit is disabled, xLOS output fixed high
	F	xLOS output active, power down on LOS assert
	H	xLOS output active, no power down on LOS assert