

## Description

M3xxx316 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible 35ns/35ns and 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually unlimited endurance and data retention, high performance and scalable memory technology.

M3xxx316 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

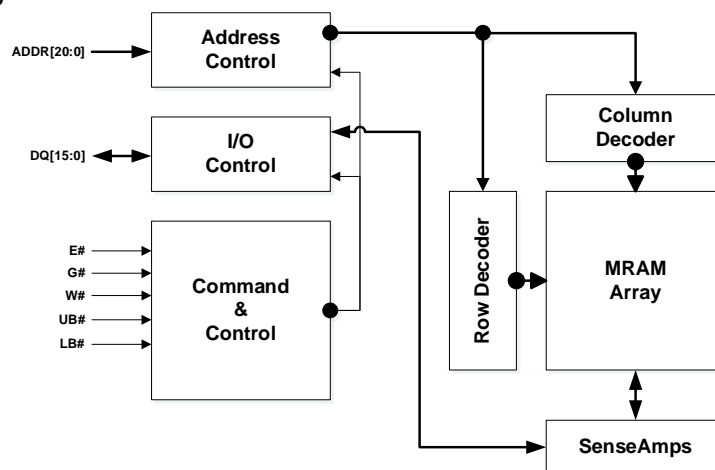
## Typical Applications

- Ideal for applications that must store and retrieve data without incurring large latency penalties
- Factory Automation
- Multifunction Printers
- Industrial Control And Monitoring
- Medical Diagnostics
- Data Switches And Routers
- Smart Meter

## Features

- Interface
  - Parallel Asynchronous x16
- Technology
  - 40nm pMTJ STT-MRAM
- Data Retention (see Table 16. Endurance and Data Retention Density)
  - 4Mb, 8Mb, 16Mb, 32Mb
- Operating Voltage Range
  - VCC: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C
- RoHS Compliant & REACH Compliant
- Packages
  - 44-pin TSOP (10mm x 18mm)
  - 54-pin TSOP (10mm x 22mm)
  - 48-ball FBGA (10mm x 10mm)
- Memory Array Organization
  - 4Mbit
    - 262,144 x 16
  - 8Mbit
    - 524,288 x 16
  - 16Mbit
    - 1,048,576 x 16
  - 32Mbit
    - 2,097,152 x 16

## Block Diagram



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### Performance

Device Operation	Typical Values	Units
Read Cycle Time	35.0 (minimum)	ns
Write Cycle Time	35.0 (minimum)	ns
Standby Current	1.7 (typical)*	mA
Read Current	12.0 (typical)	mA
Write Current	20.0 (typical)	mA

\*Number shown is for 16Mb device

## General Description

M3xxx316 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible 35ns/35ns and 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

**Table 1: Technology Comparison**

	SRAM	Flash	EEPROM	MRAM
<b>Non-Volatility</b>	-	√	√	√
<b>Write Performance</b>	√	-	-	√
<b>Read Performance</b>	√	-	-	√
<b>Endurance</b>	√	-	-	√
<b>Power</b>	-	-	-	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance, high performance and scalable memory technology.

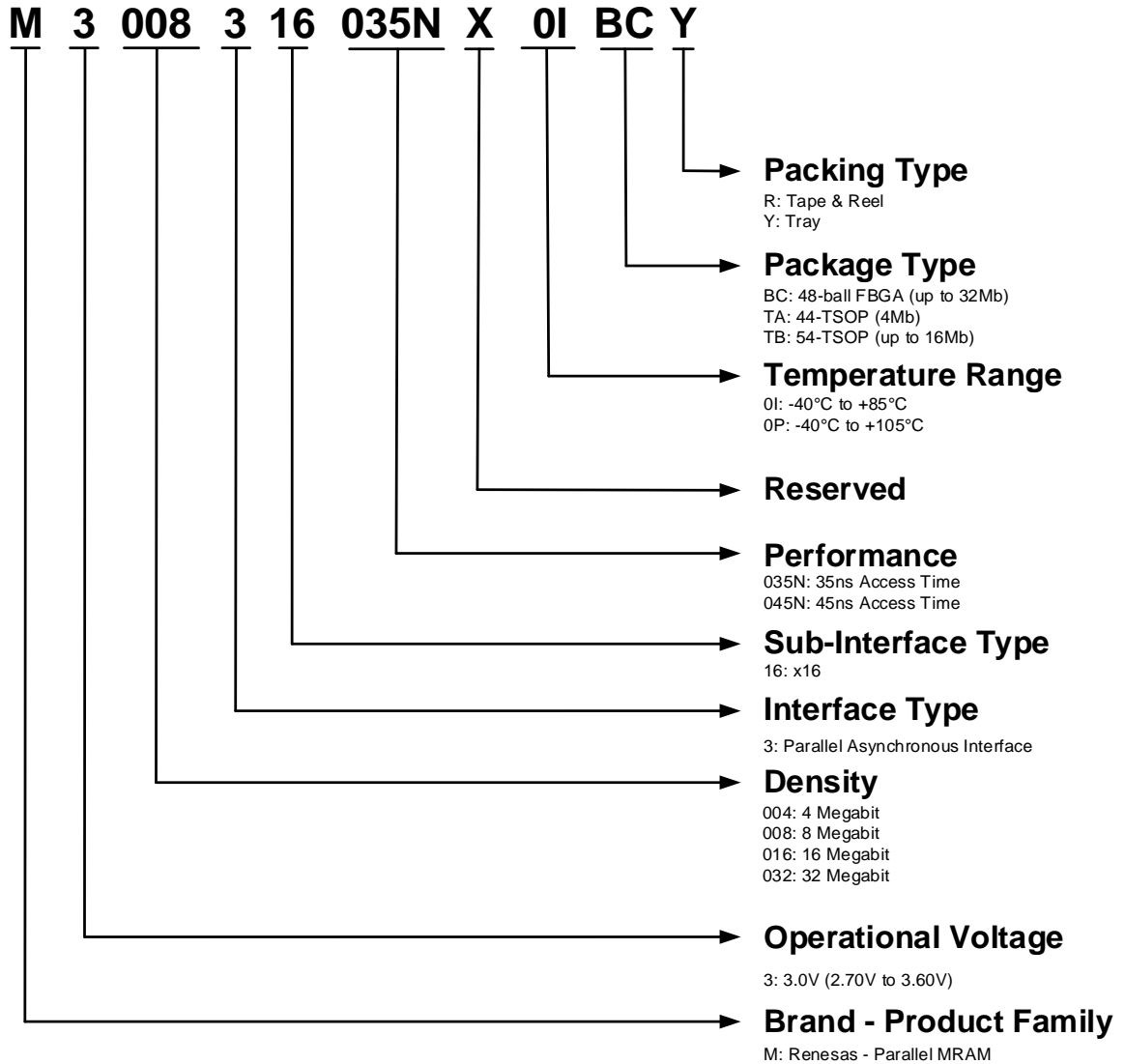
M3xxx316 is available in small footprint 54-pin TSOP (10mm x 22mm) and 48-Ball FBGA (10mm x 10mm) packages supporting densities ranging from 4Mb to 16Mb. The 48-Ball FBGA also supports the 32Mb. Density of 4Mb is also available in a small footprint 44-pin TSOP (10mm x 18mm). These packages are compatible with similar low-power volatile and non-volatile products.

M3xxx316 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

**Figure 1: Part Number Ordering System**



### Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 2: Valid Combinations List**

Valid Combinations – 35ns				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
M3004316035NX	0I, 0P	BC, TA, TB	R, Y	M3004316035NX0IBCR
				M3004316035NX0IBCY
				M3004316035NX0ITAR
				M3004316035NX0ITAY
				M3004316035NX0ITBR
				M3004316035NX0ITBY
				M3004316035NX0PBCR
				M3004316035NX0PBCY
				M3004316035NX0PTAR
				M3004316035NX0PTAY
				M3004316035NX0PTBR
M3004316035NX0PTBY				
M3008316035NX	0I, 0P	BC, TB	R, Y	M3008316035NX0IBCR
				M3008316035NX0IBCY
				M3008316035NX0ITBR
				M3008316035NX0ITBY
				M3008316035NX0PBCR
				M3008316035NX0PBCY
				M3008316035NX0PTBR
M3008316035NX0PTBY				
M3016316035NX	0I, 0P	BC, TB	R, Y	M3016316035NX0IBCR
				M3016316035NX0IBCY
				M3016316035NX0ITBR
				M3016316035NX0ITBY
				M3016316035NX0PBCR
				M3016316035NX0PBCY
				M3016316035NX0PTBR
M3016316035NX0PTBY				
M3032316035NX	0I, 0P	BC	R, Y	M3032316035NX0IBCR
				M3032316035NX0IBCY
				M3032316035NX0PBCR
				M3032316035NX0PBCY

Valid Combinations – 45ns				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
<b>M3004316045NX</b>	0I, 0P	BC, TA, TB	R, Y	M3004316045NX0IBCR
				M3004316045NX0IBCY
				M3004316045NX0ITAR
				M3004316045NX0ITAY
				M3004316045NX0ITBR
				M3004316045NX0ITBY
				M3004316045NX0PBCR
				M3004316045NX0PBCY
				M3004316045NX0PTAR
				M3004316045NX0PTAY
				M3004316045NX0PTBR
				M3004316045NX0PTBY
<b>M3008316045NX</b>	0I, 0P	BC, TB	R, Y	M3008316045NX0IBCR
				M3008316045NX0IBCY
				M3008316045NX0ITBR
				M3008316045NX0ITBY
				M3008316045NX0PBCR
				M3008316045NX0PBCY
				M3008316045NX0PTBR
M3008316045NX0PTBY				
<b>M3016316045NX</b>	0I, 0P	BC, TB	R, Y	M3016316045NX0IBCR
				M3016316045NX0IBCY
				M3016316045NX0ITBR
				M3016316045NX0ITBY
				M3016316045NX0PBCR
				M3016316045NX0PBCY
				M3016316045NX0PTBR
				M3016316045NX0PTBY
<b>M3032316045NX</b>	0I, 0P	BC	R, Y	M3032316045NX0IBCR
				M3032316045NX0IBCY
				M3032316045NX0PBCR
				M3032316045NX0PBCY

## Signal Description and Assignment

Figure 2: Device Pinout

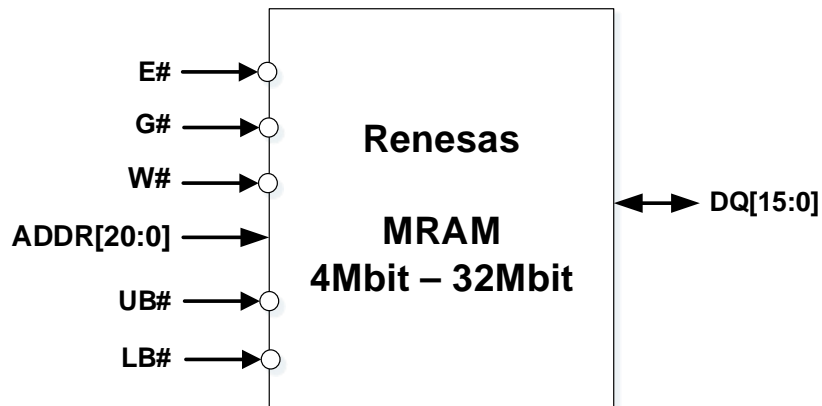


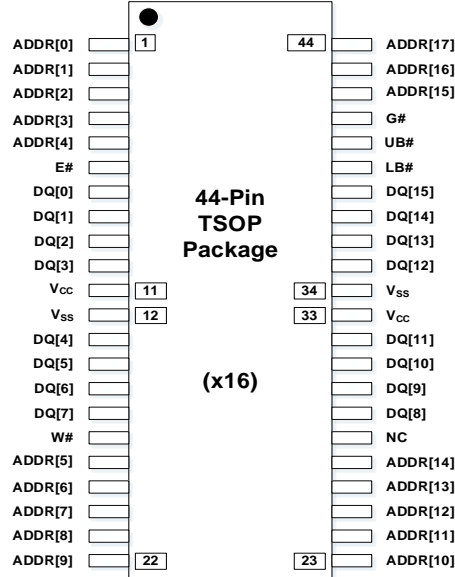
Table 3: Signal Description

Signal	Type	Description
<b>E#</b>	Input	<b>Chip enable:</b> Enables or disables the MRAM.
<b>G#</b>	Input	<b>Output enable:</b> Enables the output drivers in bidirectional data transfer I/Os.
<b>W#</b>	Input	<b>Write enable:</b> Transfers serial data from the host system to the MRAM when Low (Logic '0'). Transfers serial data from the MRAM to the host system when High (Logic '1').
<b>UB#</b>	Input	<b>Upper Byte Enable:</b> Enables or disables DQ[15:8].
<b>LB#</b>	Input	<b>Lower Byte Enable:</b> Enables or disables DQ[7:0].
<b>ADDR[20:0]</b>	Input	<b>Address:</b> I/Os for address transfer. 04M: ADDR[17:0] – 18 Address pins for 04M devices. 08M: ADDR[18:0] – 19 Address pins for 08M devices. 16M: ADDR[19:0] – 20 Address pins for 16M devices. 32M: ADDR[20:0] – 21 Address pins for 32M devices.
<b>DQ[15:0]</b>	Input / Output	<b>Data inputs/outputs:</b> The bidirectional I/Os transfer data.
<b>V<sub>cc</sub></b>	Supply	<b>V<sub>cc</sub>:</b> Core and I/O power supply.
<b>V<sub>ss</sub></b>	Supply	<b>V<sub>ss</sub>:</b> Core and I/O ground supply.
<b>NC</b>		<b>No connect:</b> NCs are not internally connected. They can be driven or left unconnected.
<b>DNU</b>		<b>Do not use:</b> DNUs must be left unconnected.

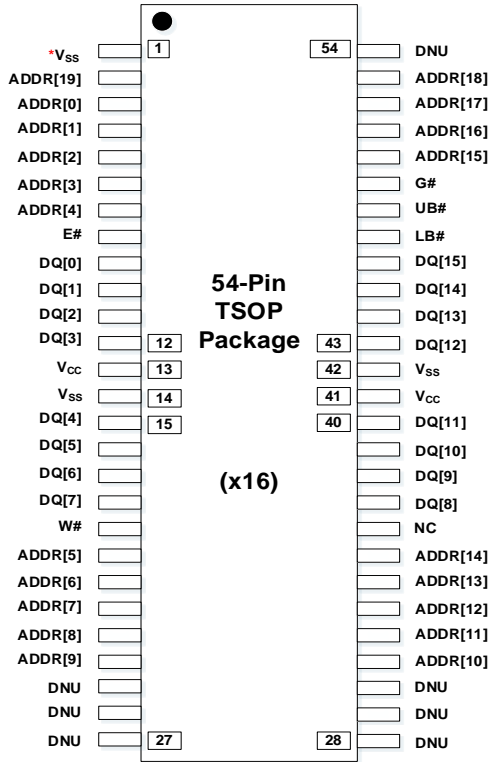


Package Options

44-Pin TSOP (4Mb) (Top View)

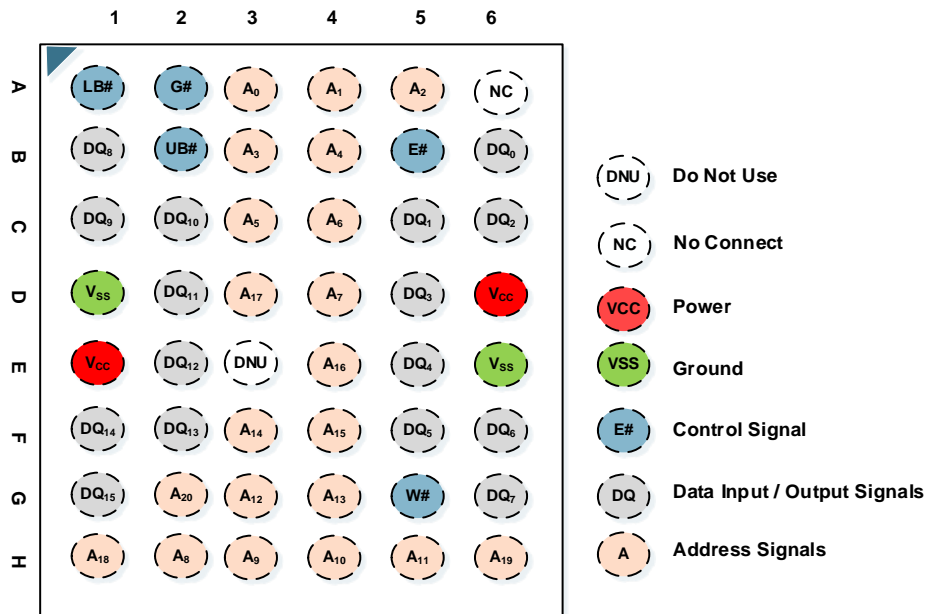


54-Pin TSOP (4-16Mb) (Top View)

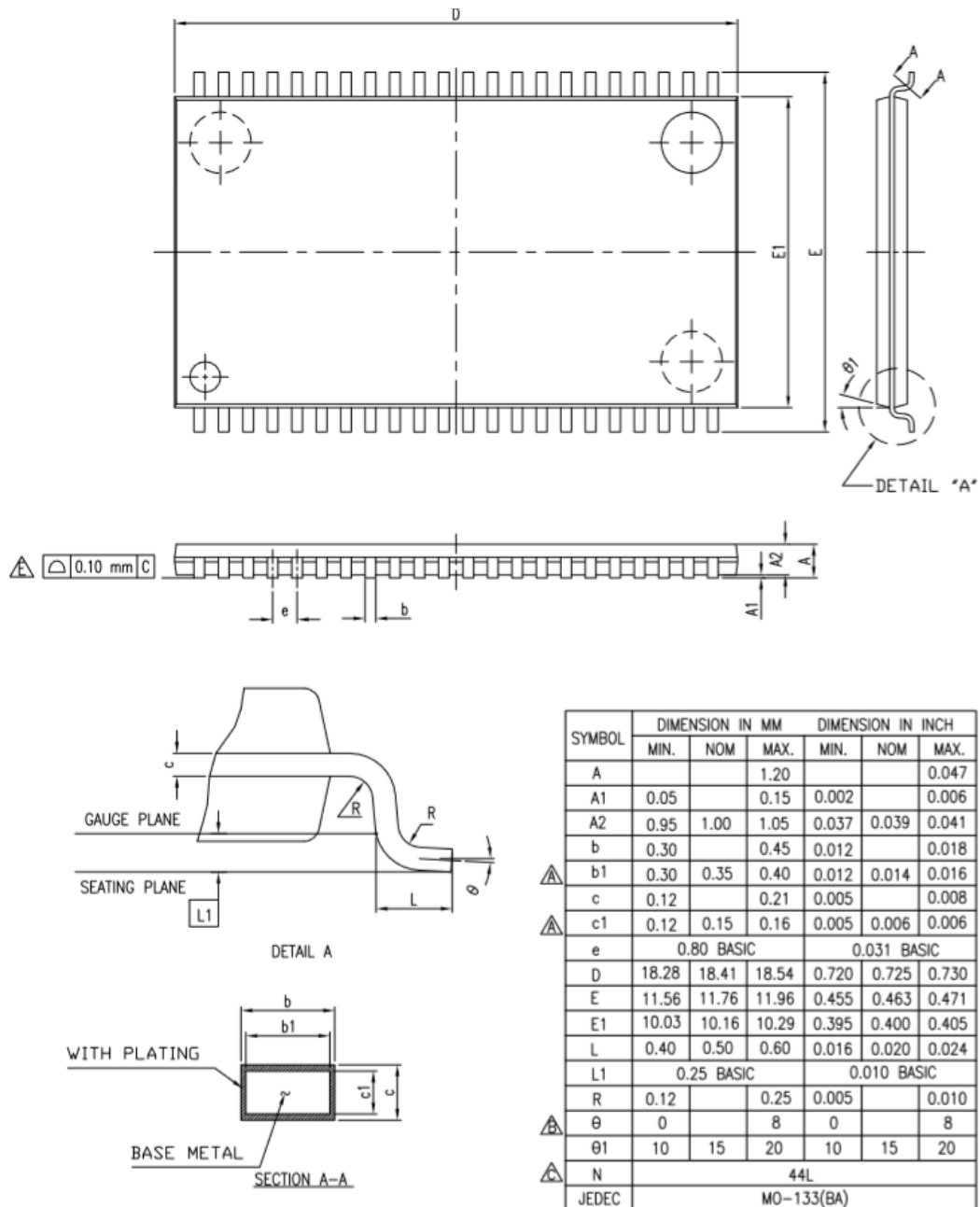


Note: \*VSS pin 1 must be held low, < VIL for the part to function properly.

48-Ball FBGA (4-32Mb) (Balls Down, Top View)

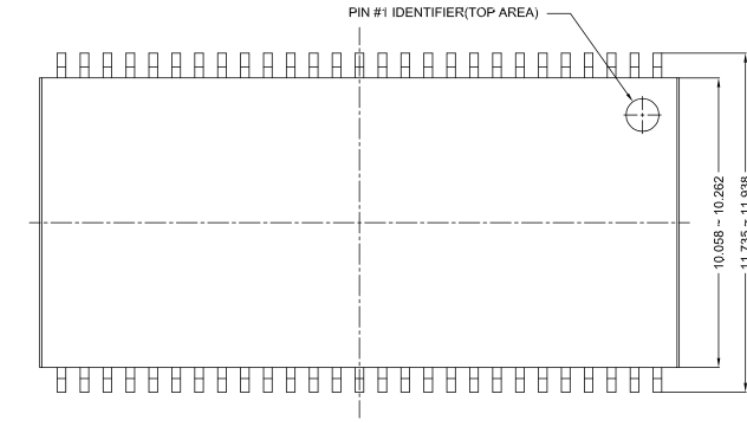


Package Drawings  
44-Pin TSOP

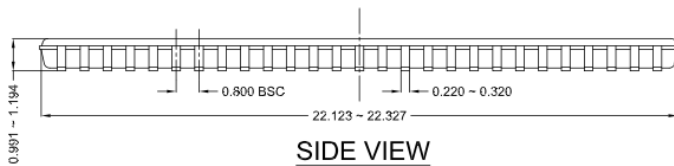


NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.  
D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

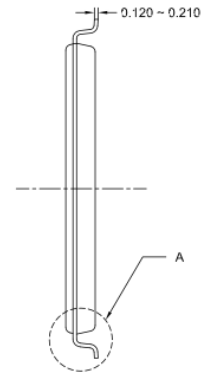
54-Pin TSOP



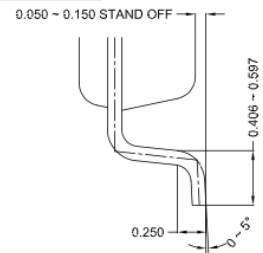
TOP VIEW



SIDE VIEW



SIDE VIEW

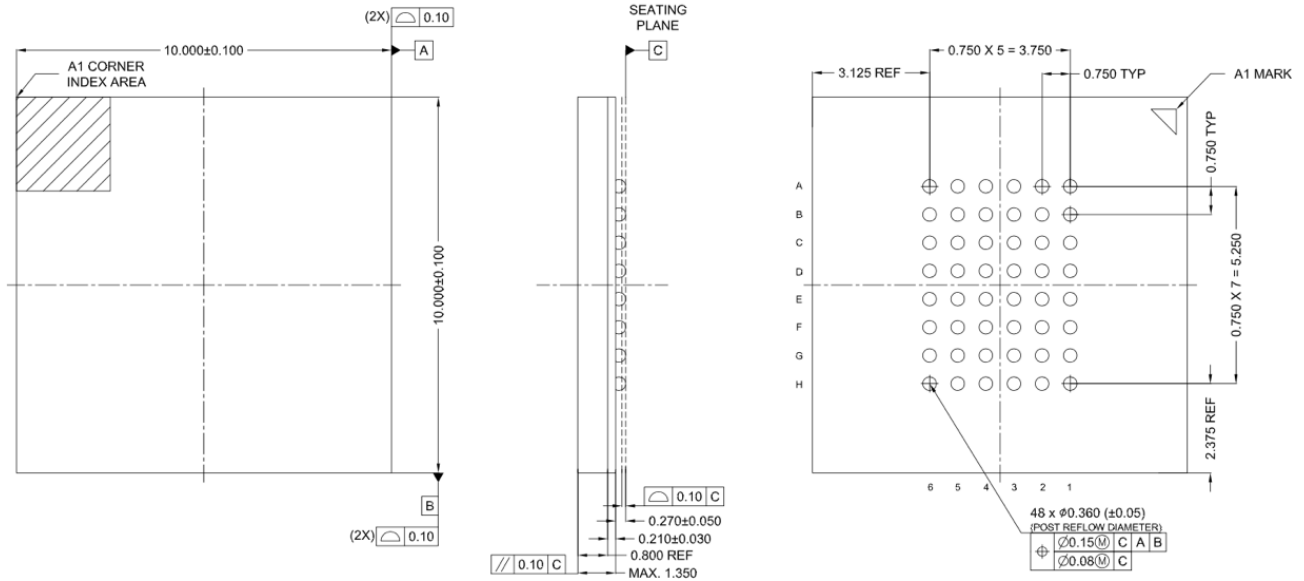


DETAIL "A"

(Unit : mm)

		COMMON DIMENSIONS		
		MIN	NOM	MAX
Package		54TSOP		
Body size	X	-	-	-
	Y	11.735	-	11.938
Mold size	X	22.123	-	22.327
	Y	10.058	-	10.262
Lead Pitch		0.800 BSC		
Total Thickness		0.991	-	1.194
Lead Frame Thickness		0.120	-	0.210
Stand Off		0.050	-	0.150
LEAD Width		0.220	-	0.320

### 48-Ball FBGA



(Unit : mm)

		COMMON DIMENSIONS		
		MIN	NOM	MAX
Package		48 FBGA		
Body size	X	9.900	10.000	10.100
	Y	9.900	10.000	10.100
Ball Pitch		0.750		
Total Thickness				1.350
Mold Thickness		0.800 Ref.		
Substrate Thickness		0.190	0.210	0.240
Ball Diameter (Raw Ball Size)		0.350		
Stand Off		0.220	0.270	0.320
Ball Width (Post Reflow size)		0.310	0.360	0.410
Package Edge Tolerance		0.100		
Mold Parallelism		0.100		
Coplanarity		0.100		
Ball Offset (Package)		0.150		
Ball Offset (Ball)		0.050		
Ball Count		63		
Edge Ball Center to Center	X	3.750		
	Y	5.250		

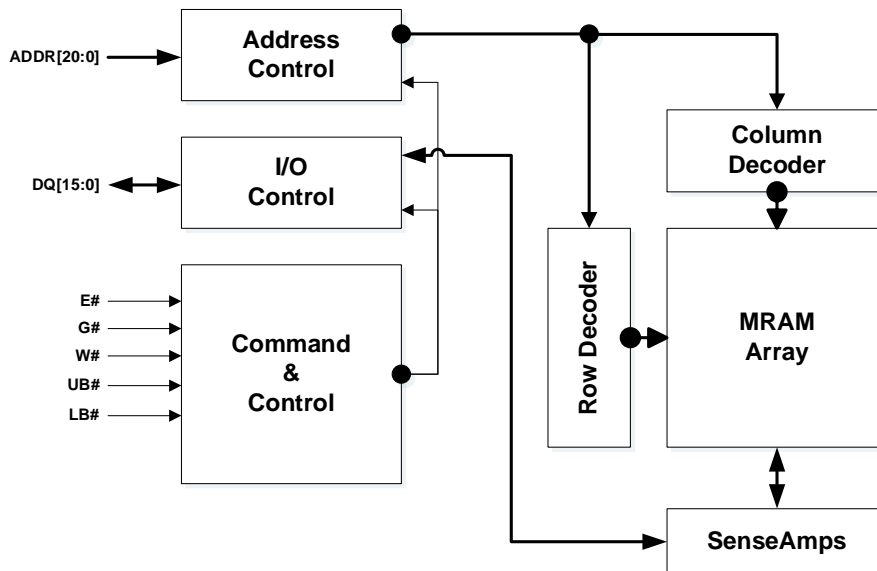
## Architecture

M3xxx316 is a high performance MRAM device. Writing to and reading from the device as follows:

To write to the device, bring Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[15]) to be written into the memory location specified by the address pins ADDR[0] through ADDR[20] (48-ball FBGA), ADDR[0] through ADDR[19] (54-pin TSOP) and ADDR[0] through ADDR[17] (44-pin TSOP).

To read from the device, bring Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins ADDR[0] through ADDR[20] (48-ball FBGA), ADDR[0] through ADDR[19] (54-pin TSOP) and ADDR[0] through ADDR[17] (44-pin TSOP) to appear on I/O pins (DQ[0] to DQ[15]).

**Figure 3: Functional Block Diagram**



**Table 4: Modes of Operation**

Mode	E#	G#	W#	UB#	LB#	Current	DQ[15:8]	DQ[7:0]
<b>Not Selected</b>	H	X	X	X	X	I <sub>SB</sub>	Hi-Z	Hi-Z
<b>Output Disabled</b>	L	H	H	X	X	I <sub>READ</sub>	Hi-Z	Hi-Z
<b>Output Disabled</b>	L	X	X	H	H	I <sub>READ</sub>	Hi-Z	Hi-Z
<b>Read Upper Byte</b>	L	L	H	L	H	I <sub>READ</sub>	Dataout	Hi-Z
<b>Read Lower Byte</b>	L	L	H	H	L	I <sub>READ</sub>	Hi-Z	Dataout
<b>Read Word</b>	L	L	H	L	L	I <sub>READ</sub>	Dataout	Dataout
<b>Write Upper Byte</b>	L	X	L	L	H	I <sub>WRITE</sub>	Datain	Hi-Z
<b>Write Lower Byte</b>	L	X	L	H	L	I <sub>WRITE</sub>	Hi-Z	Datain
<b>Write Word</b>	L	X	L	L	L	I <sub>WRITE</sub>	Datain	Datain

**Notes:**

H: High (Logic '1')

L: Low (Logic '0')

X: Don't Care

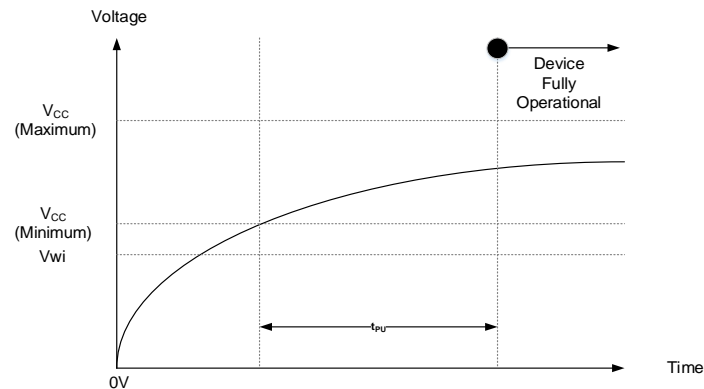
Hi-Z: High Impedance

### Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G#, must follow  $V_{CC}$  during power-up

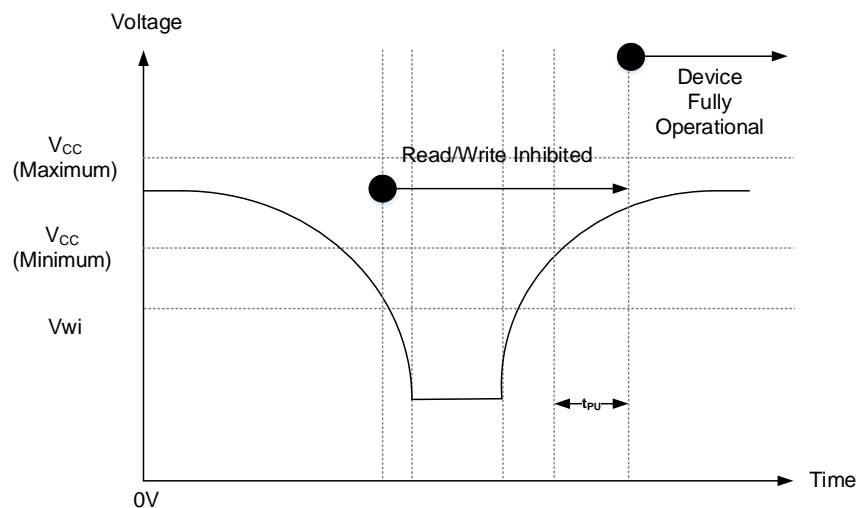
**Figure 4: Power-Up Behavior**



When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G#, must follow  $V_{CC}$  during power-down
- During power loss or brownout, where  $V_{CC}$  goes below  $V_{wi}$ , read/write operations are prohibited. The power-up timing needs to be observed after  $V_{CC}$  goes above  $V_{CC}$  (minimum)

**Figure 5: Power-Down Behavior**



**Table 5: Device Initialization Timing – 3.0V**

Parameter	Symbol	Test Conditions	3.0V			Units
			Minimum	Typical	Maximum	
<b>V<sub>CC</sub> Range</b>		All operating voltages and temperatures	2.7	-	3.6	V
<b>V<sub>CC</sub> Power Up to First Instruction</b>	t <sub>PU</sub>	All operating voltages and temperatures	1	-	-	ms



## Electrical Specifications

**Table 6: Recommended Operating Conditions**

Parameter / Condition	Minimum	Typical	Maximum	Units	
	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
V <sub>CC</sub> Supply Voltage	3.0V	2.7	3.0	3.6	V
V <sub>SS</sub> Supply Voltage		0.0	0.0	0.0	V
V <sub>wi</sub> Write Inhibit Voltage		2.1	2.3	2.5	V

**Table 7: Pin Capacitance**

Parameter	Symbol	Test Conditions	Density	Maximum	Units
Input Pin Capacitance	C <sub>IN</sub>	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V	4Mb - 16Mb	10.0	pF
			32b	20.0	
Input / Output Pin Capacitance	C <sub>INOUT</sub>	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V	4Mb - 16Mb	10.0	pF
			32Mb	20.0	

**Table 8: DC Characteristics**

Parameter	Symbol	Test Conditions	3.0V Device (2.7V-3.6V)			Units	
			Minimum	Typical	Maximum		
Read Current	I <sub>READ</sub>	V <sub>CC</sub> (max), I <sub>OUT</sub> =0mA	4Mb – 32Mb	-	12.0	30.0	mA
Write Current	I <sub>WRITE</sub>	V <sub>CC</sub> (max)	4Mb – 32Mb	-	20.0	30.0	mA
Standby Current Industrial (-40°C to 85°C)	I <sub>SB</sub>	E# = V <sub>IH</sub> , V <sub>CC</sub> (max)	4Mb-16Mb	-	1.5	2.5	mA
			32Mb	-	3.0	5.0	
Standby Current Industrial Extended (-40°C to 105°C)	I <sub>SB</sub>	E# = V <sub>IH</sub> , V <sub>CC</sub> (max)	4Mb-16Mb	-	1.7	3.5	mA
			32Mb	-	3.4	7.0	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub> (max)		-	-	±1.0	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>CC</sub> (max)		-	-	±1.0	μA
Input High Voltage	V <sub>IH</sub>			0.8xV <sub>CC</sub>	-	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>			-0.5	-	0.2xV <sub>CC</sub>	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> = -1.6mA		V <sub>CC</sub> -0.5	-	-	V
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA		-	-	0.4	V

**Table 9: Magnetic Immunity Characteristics**

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	$H_{\max\_write}$	24000	A/m
Magnetic Field During Read	$H_{\max\_read}$	24000	A/m

**Table 10: AC Test Conditions**

Parameter	Value
Input pulse levels	0.0V to $V_{CC}$
Input rise and fall times	5ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30pF

Write Operation

Figure 6: Write Operation (W# Controlled)

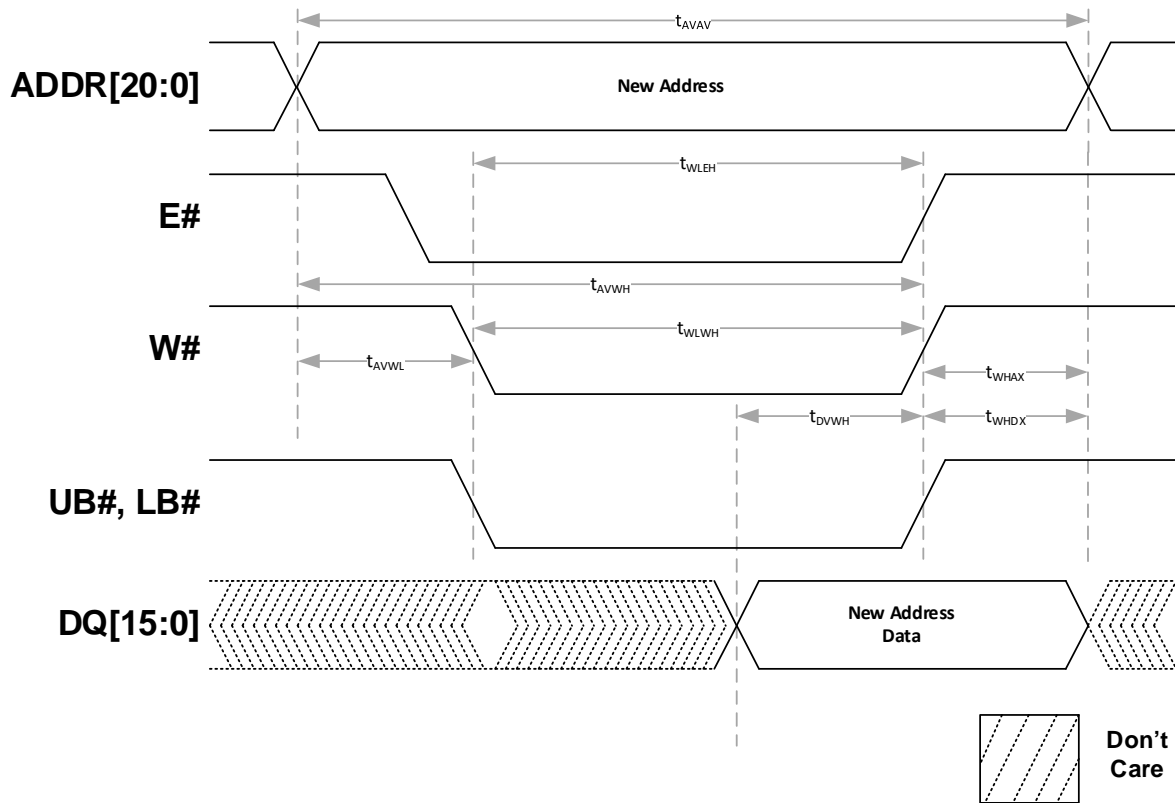


Table 11: Write Operation (W# Controlled)

Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	$t_{AVAV}$	35	45	-	ns
Address Set-Up Time	$t_{AVWL}$	0		-	ns
Address Valid to end of Write (G# High)	$t_{AVWH}$	18	28	-	ns
Address Valid to end of Write (G# Low)	$t_{AVWH}$	20	30	-	ns
Write Pulse Width (G# High)	$t_{WLVH}, t_{WLEH}$	15	25	-	ns
Write Pulse Width (G# Low)	$t_{WLVH}, t_{WLEH}$	15	25	-	ns
Data Valid to end of Write	$t_{DVWH}$	10	15	-	ns
Data Hold Time	$t_{WHDX}$	0		-	ns
Write recovery Time	$t_{WHAX}$	12		-	ns

Notes:

- G# is High (Logic '1') for Write operation
- Power supplies must be stable
- Addresses valid either before or at the same time as  $E\#$  goes low

Figure 7: Write Operation (E# Controlled)

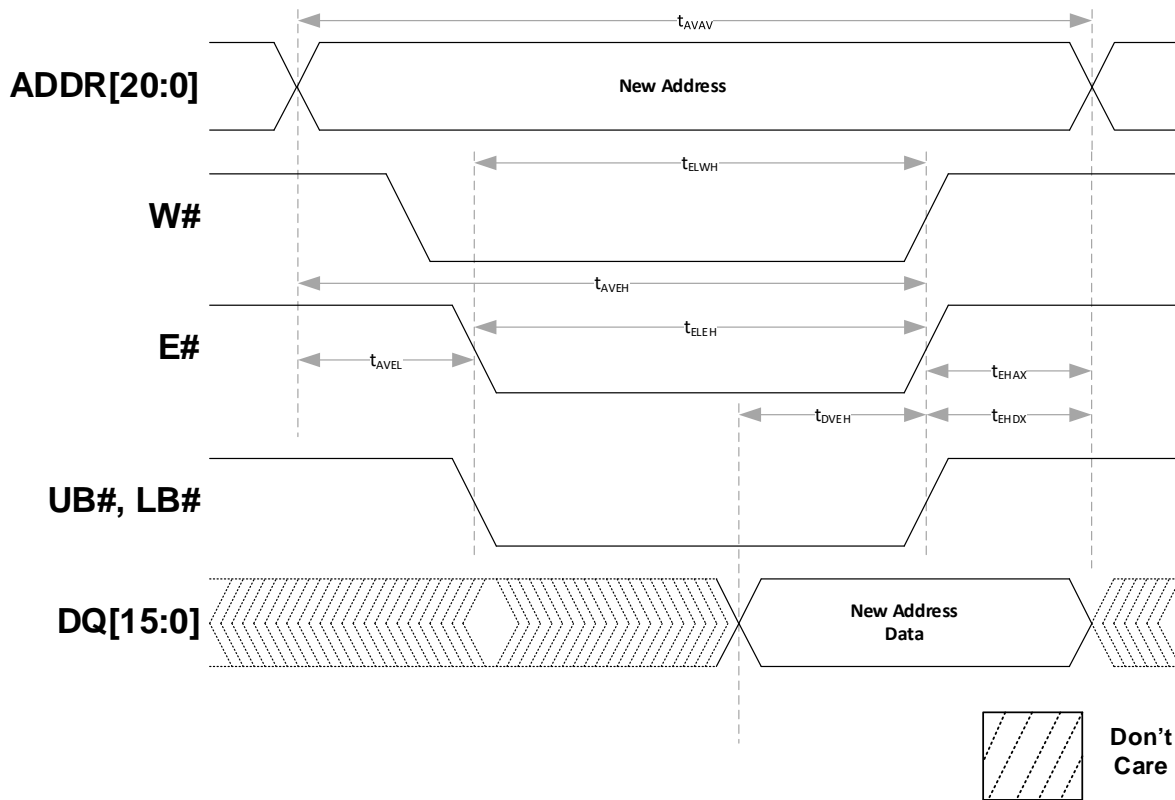


Table 12: Write Operation (E# Controlled)

Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	$t_{AVAV}$	35	45	-	ns
Address Set-Up Time	$t_{AVEL}$	0		-	ns
Address Valid to end of Write (G# High)	$t_{AVEH}$	18	28	-	ns
Address Valid to end of Write (G# Low)	$t_{AVEH}$	20	30	-	ns
Write Pulse Width (G# High)	$t_{ELWH}, t_{ELEH}$	15	25	-	ns
Write Pulse Width (G# Low)	$t_{ELWH}, t_{ELEH}$	15	25	-	ns
Data Valid to end of Write	$t_{DVEH}$	10	15	-	ns
Data Hold Time	$t_{EHDX}$	0		-	ns
Write recovery Time	$t_{EHAX}$	12		-	ns

Notes:

- G# is High (Logic '1') for Write operation
- Power supplies must be stable
- Addresses valid either before or at the same time as W# goes low

Bus Turnaround Operation - Read to Write

Figure 8: Bus Turnaround Operation

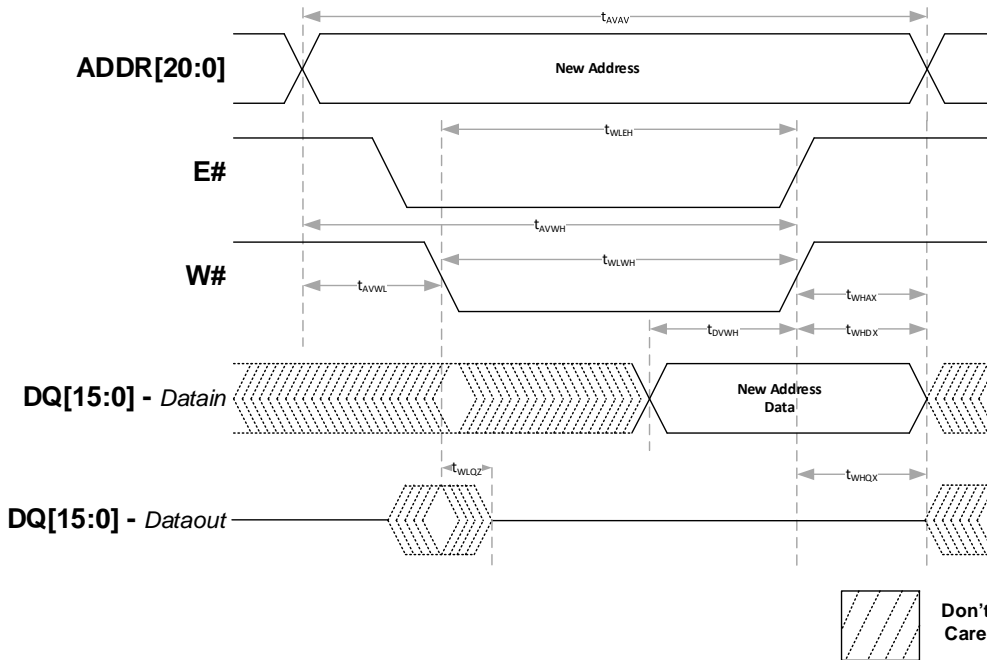


Table 13: Bus Turnaround

Parameter	Symbol	Minimum	Maximum		Units
			35ns	45ns	
<b>W# Low to Data Hi-Z</b>	$t_{WLQZ}$	0	12	15	ns
<b>W# High to Output Active</b>	$t_{WHQX}$	3	-		ns

Notes:

- Power supplies must be stable
- Addresses valid either before or at the same time as E# goes low

Read Operation

Figure 9: Read Operation

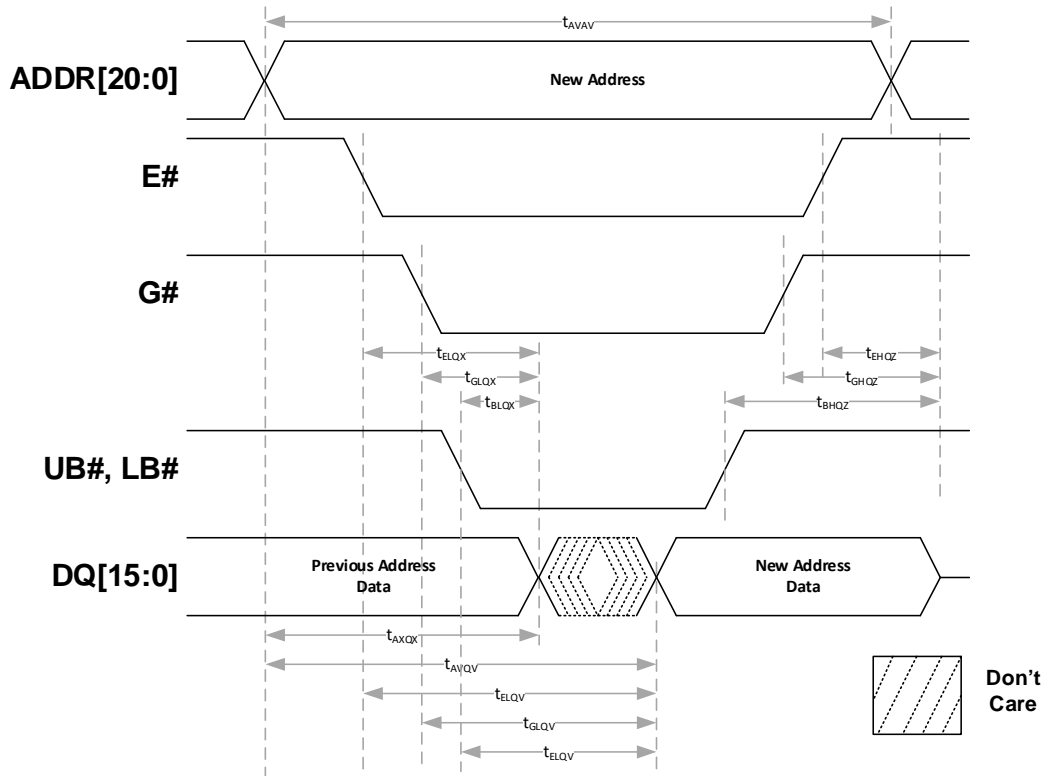


Table 14: Read Operation

Parameter	Symbol	Minimum		Maximum		Units
		35ns	45ns	35ns	45ns	
Read Cycle Time	$t_{AVAV}$	35	45	-	-	ns
Address Cycle Time	$t_{AVQV}$	-	-	35	45	ns
Chip Enable Access Time	$t_{ELQV}$	-	-	35	45	ns
Output Enable Access Time	$t_{GLQV}$	-	-	15	25	ns
Byte Enable Access Time	$t_{BLQV}$	-	-	15	25	ns
Output Hold From Address Change	$t_{AXQX}$	3	-	-	-	ns
Chip Enable Low to Output Active	$t_{ELQX}$	3	-	-	-	ns
Output Enable Low to Output Active	$t_{GLQX}$	0	-	-	-	ns
Byte Enable Low to Output Active	$t_{BLQX}$	0	-	-	-	ns
Chip Enable High to Output Hi-Z	$t_{EHQZ}$	0	-	15	-	ns
Output Enable High to Output Hi-Z	$t_{GHQZ}$	0	-	10	15	ns
Byte Enable High to Output Hi-Z	$t_{BHQZ}$	0	-	10	-	ns

Notes:

- W# is High (Logic '1') for Read operation
- Power supplies must be stable
- Addresses valid either before or at the same time as E# goes low

## Endurance and Data Retention

**Table 15: Endurance and Data Retention**

Parameter	Symbol	Test Conditions	Minimum	Units
<b>Write Endurance</b>	END	-	10 <sup>14</sup>	cycles
<b>Data Retention</b>	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

**Notes:**

W# is High (Logic '1') for Read operation

## Thermal Resistance

**Table 16: Thermal Resistance Specifications**

Parameter	Description	Test Conditions	44-pin TSOP	54-pin TSOP (4-16Mb)	48 Ball FBGA (4-16Mb)	48 Ball FBGA (32Mb)	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	40.05	52.78	42.67	43.98	°C/ W
$\theta_{JC}$	Thermal resistance (junction to case)		7.02	6.70	11.09	11.82	

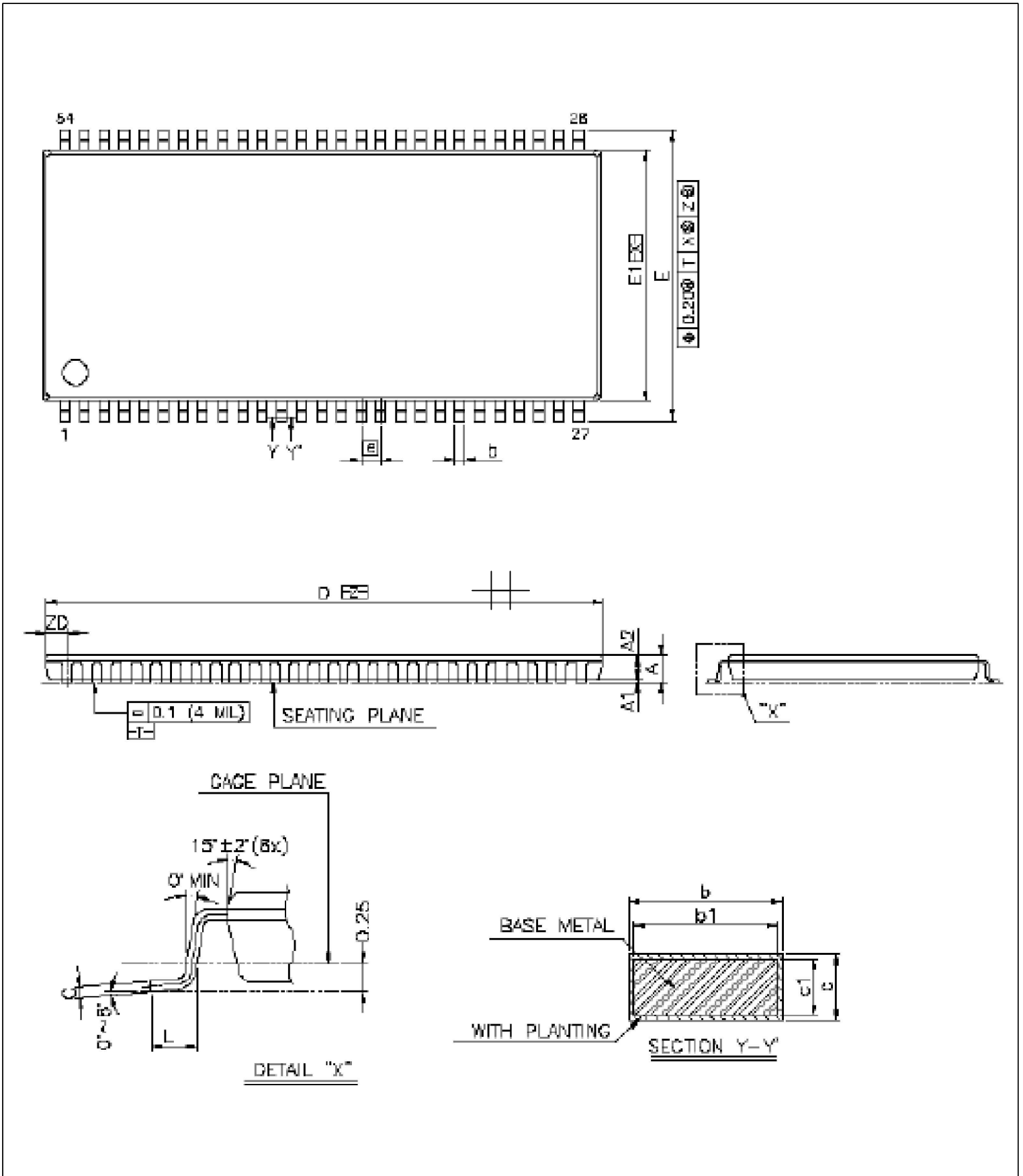
**Notes:**

1: These parameters are guaranteed by characterization; not tested in production.



### Revision History

Revision Date	Change Summary
Sept.03.21	Initial release

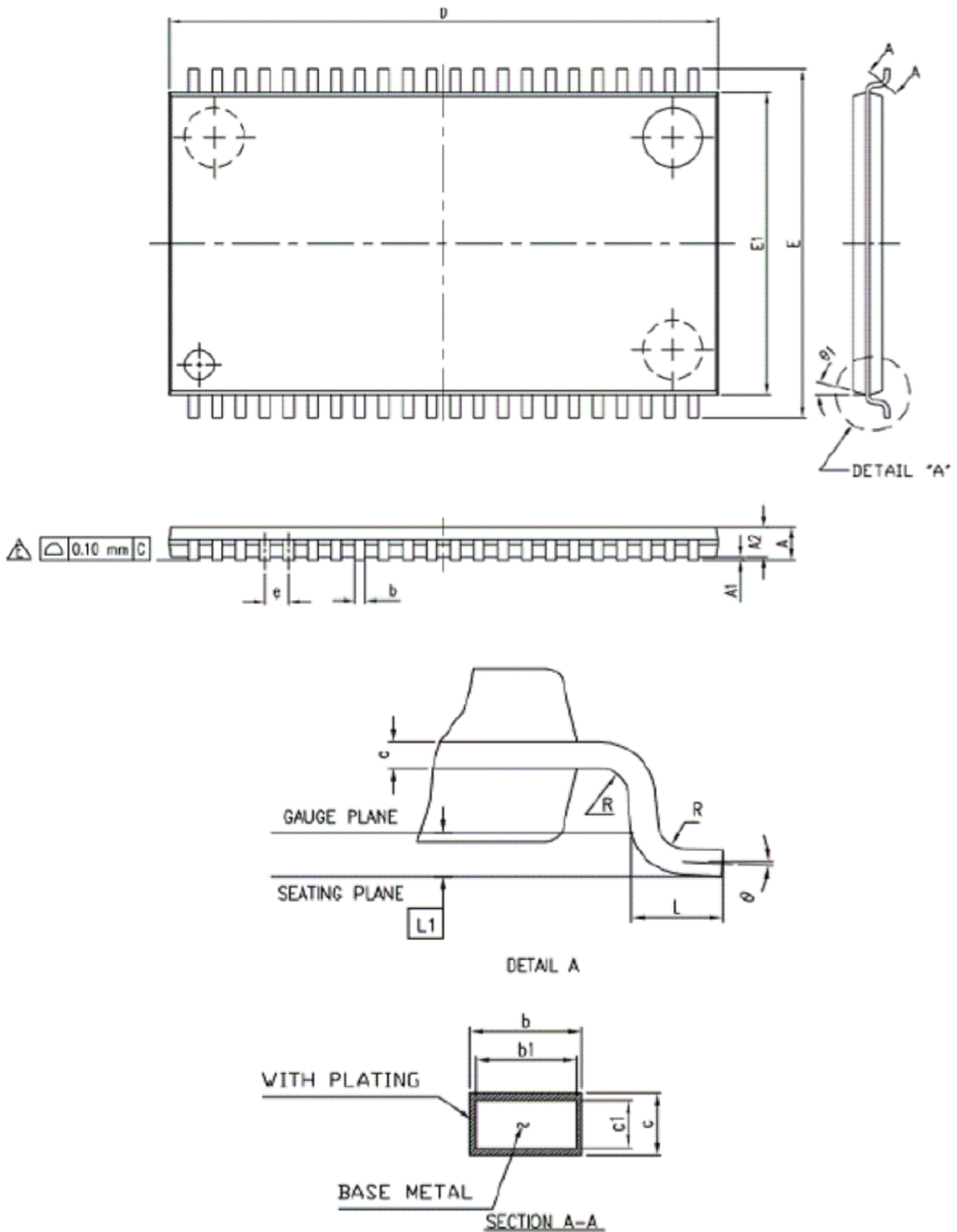


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			47
A1	0.05		0.15	2		6
A2	0.95	1.00	1.05	37	39	41
b	0.30		0.45	12		18
b1	0.30	0.35	0.40	12	14	16
c	0.12		0.21	5		8
c1	0.12	0.15	0.16	5	5,9	6
D	22.09	22.22	22.35	870	875	880
E	11.56	11.76	11.96	455	463	471
E1	10.03	10.16	10.29	395	400	405
e	0.75	0.80	0.85	29.5	31.5	33.5
L	0.35	0.50	0.65	14	20	26
ZD	0.56	0.71	0.86	22	28	34

**NOTE:**

1. REFER TO : JEDEC MS-024 FA
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION OR GATE BURRS.  
MOLD PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.  
DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSION.  
INTERLEAD MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.  
ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX. b DIMENSION BY MORE THAN 0.13mm  
DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MINIMUM b DIMENSION BY MORE THAN 0.07mm.
4. ALL DIMENSION IN MILIMETERS

Package Revision History		
Date Created	Rev No.	Description
June 28, 2020	00	Initial Release

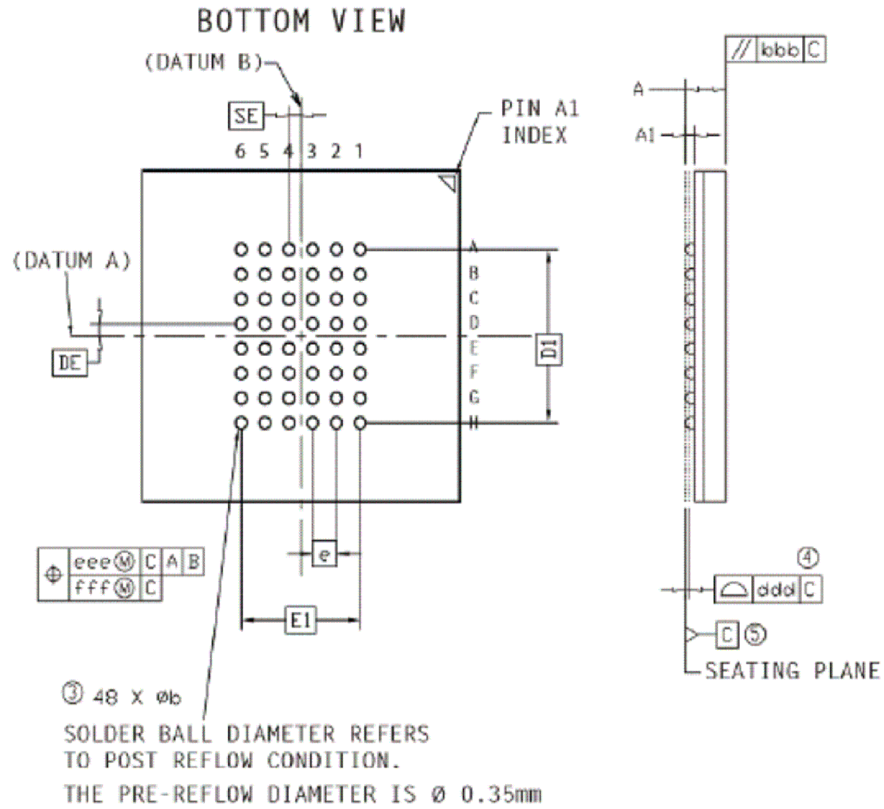


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
△ b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12		0.21	0.005		0.008
△ c1	0.12	0.15	0.16	0.005	0.006	0.006
e	0.80 BASIC			0.031 BASIC		
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
R	0.12		0.25	0.005		0.010
△ θ	0		8	0		8
θ1	10	15	20	10	15	20
△ N	44L					
JEDEC	MO-133(BA)					

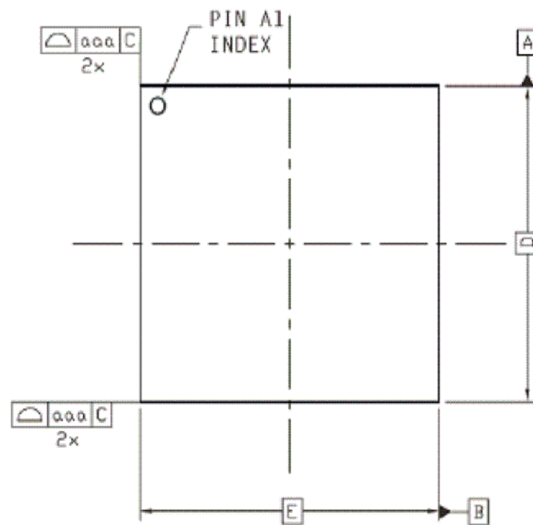
NOTE: DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.

D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

Package Revision History		
Date Created	Rev No.	Description
June 28, 2020	00	Initial Release



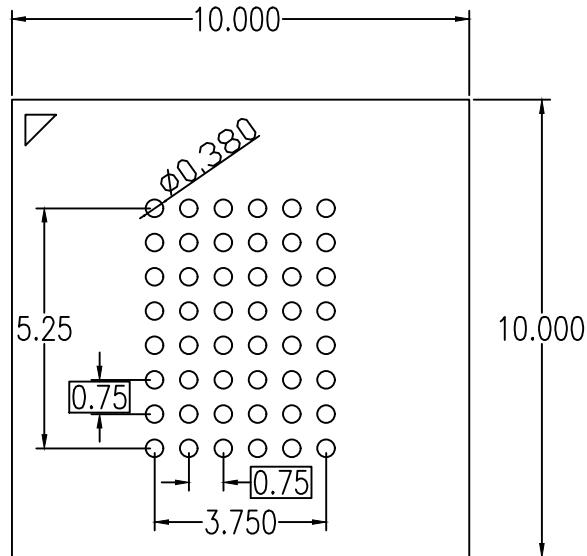
**TOP VIEW**



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D	10.00 BSC		
E	10.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
DE	0.375 BSC		
SE	0.375 BSC		
e	0.75 BSC		

Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.10
eee	0.15
fff	0.08

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
- ③ 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- ④ Dimension 'ddd' is measured parallel to primary datum C.
- ⑤ Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
June 28, 2020	00	Initial Release
July 20, 2020	01	Add Recommended Land Pattern