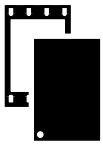
M34E04

4-Kbit Serial Presence Detect (SPD) EEPROM compatible with JEDEC EE1004

Datasheet - production data



UFDFPN8 (MC)
2 x 3 mm

Features

- 512-byte Serial Presence Detect EEPROM compatible with JEDEC EE1004 specification
- Compatible with SMBus serial interface:
  - up to 1 MHz transfer rate
- EEPROM memory array:
  - 4 Kbits organized as two pages of 256 bytes each
  - Each page is composed of two 128-byte blocks
- Software data protection for each 128-byte block
- Write:
  - Byte Write within 5 ms
  - 16 bytes Page Write within 5 ms
- Noise filtering:
  - Schmitt trigger on bus inputs
  - Noise filter on bus inputs
- Single supply voltage:
  - 1.7 V to 3.6 V
- Operating temperature range:
  - from 0 °C up to +95 °C
- Enhanced ESD/latch-up protection
- More than 4million Write cycles
- More than 200-year data retention
- RoHS-compliant and halogen-free 8-lead ultra thin fine pitch dual flat no lead package (ECOPACK2®)

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1 Description

The M34E04 is a 512-byte EEPROM device designed to operate the SMBus bus in the 1.7 V - 3.6 V voltage range, with a maximum of 1 MHz transfer rate in the 2.2 V - 3.6 V voltage range, over the JEDEC defined ambient temperature of 0°C / 95°C.

The M34E04 includes a 4-Kbit serial EEPROM organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is composed of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write-protected in one or more memory blocks.

The M34E04 device is protocol-compatible with the previous generation of 2-Kbit devices, M34E02. The page selection method allows commands used with legacy devices such as M34E02 to be applied to the lower or upper pages of the EEPROM.

Individually locking a 128-byte block may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific SMBus sequence, each block may be protected from writes until the write protection is electrically reversed using a separate SMBus sequence which also requires V_{HV} on input SA0. The write protection for all four blocks is cleared simultaneously.

Figure 1. Logic diagram

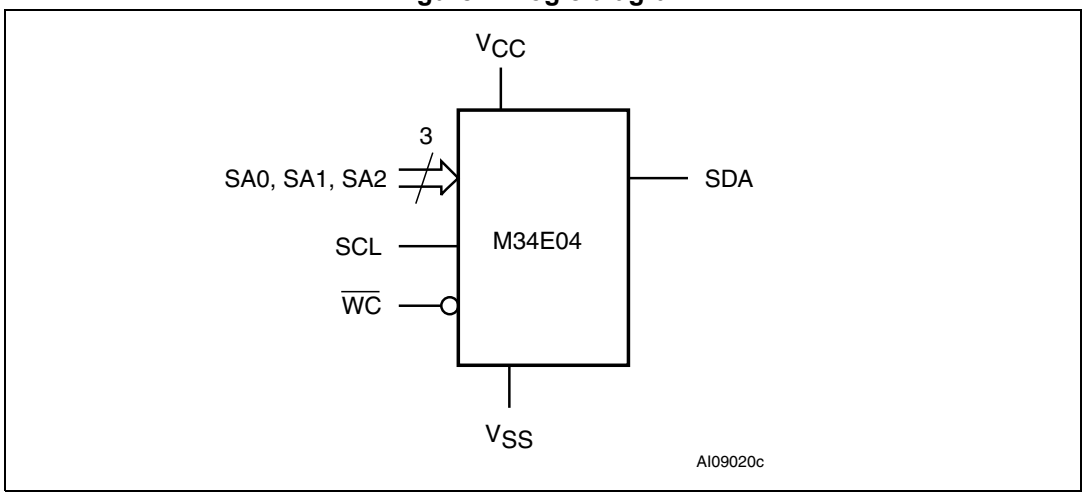
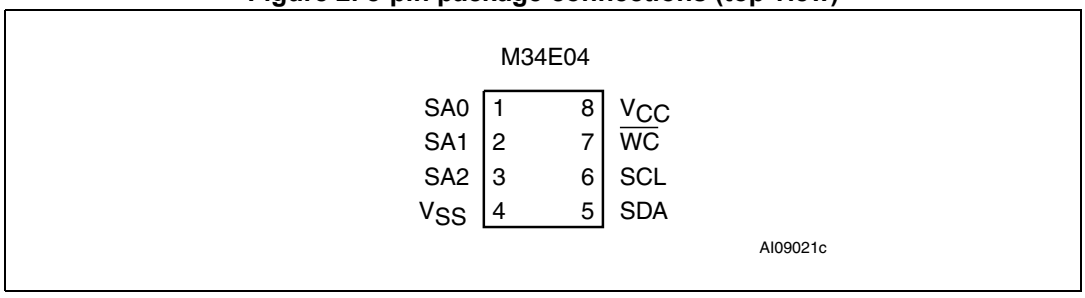


Figure 2. 8-pin package connections (top view)



1. See the *Package mechanical data* section for package dimensions, and how to identify pin 1.

Table 1. Signal names

Signal names	Description
SA2, SA1, SA0	Slave address
SDA	Serial data
SCL	Serial clock
$\overline{WC}$	Write control
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

2.1 Serial clock (SCL)

The signal applied on this input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

If SCL is driven low for tTIMEOUT (see *Table 13*) or longer, the M34E04 is set back in Standby mode, ready to receive a new START condition.

2.2 Serial data (SDA)

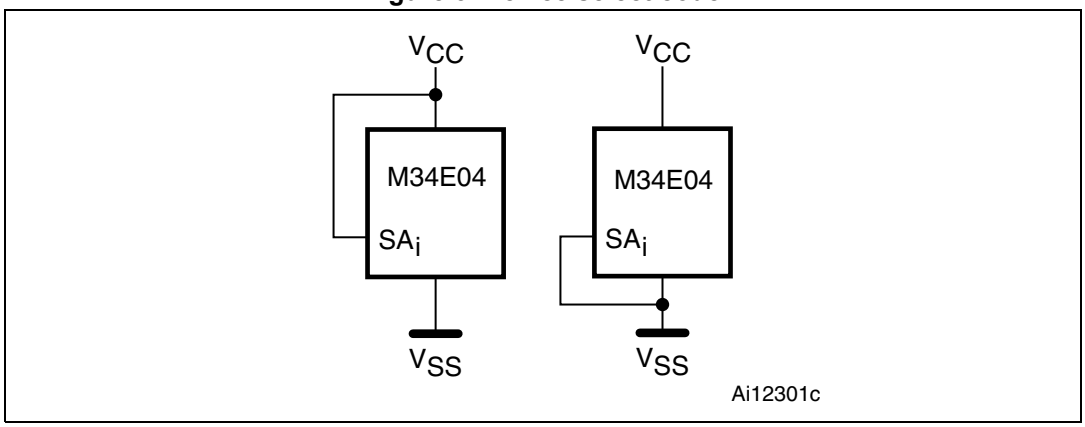
SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 12* indicates how the value of the pull-up resistor can be calculated).

2.3 Slave address (SA2, SA1, SA0)

(SA2,SA1,SA0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Type Identifier Code (DTIC, see *Table 2*). These inputs must be tied to V_{CC} or V_{SS}, as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0).

The SA0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction.

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is provided for protecting the contents of the whole memory from inadvertent write operations. Write Control ($\overline{WC}$) is used to enable (when driven low) or disable (when driven high) write instructions to the entire memory area.

When Write Control ($\overline{WC}$) is tied low or left unconnected, the write protection of the memory is determined by the status defined by the execution of the previous SWPi instructions.

2.5 Supply voltage (V_{CC})

2.5.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.5.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8* and the rise time must not vary faster than 1 V/µs.

2.5.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8*).

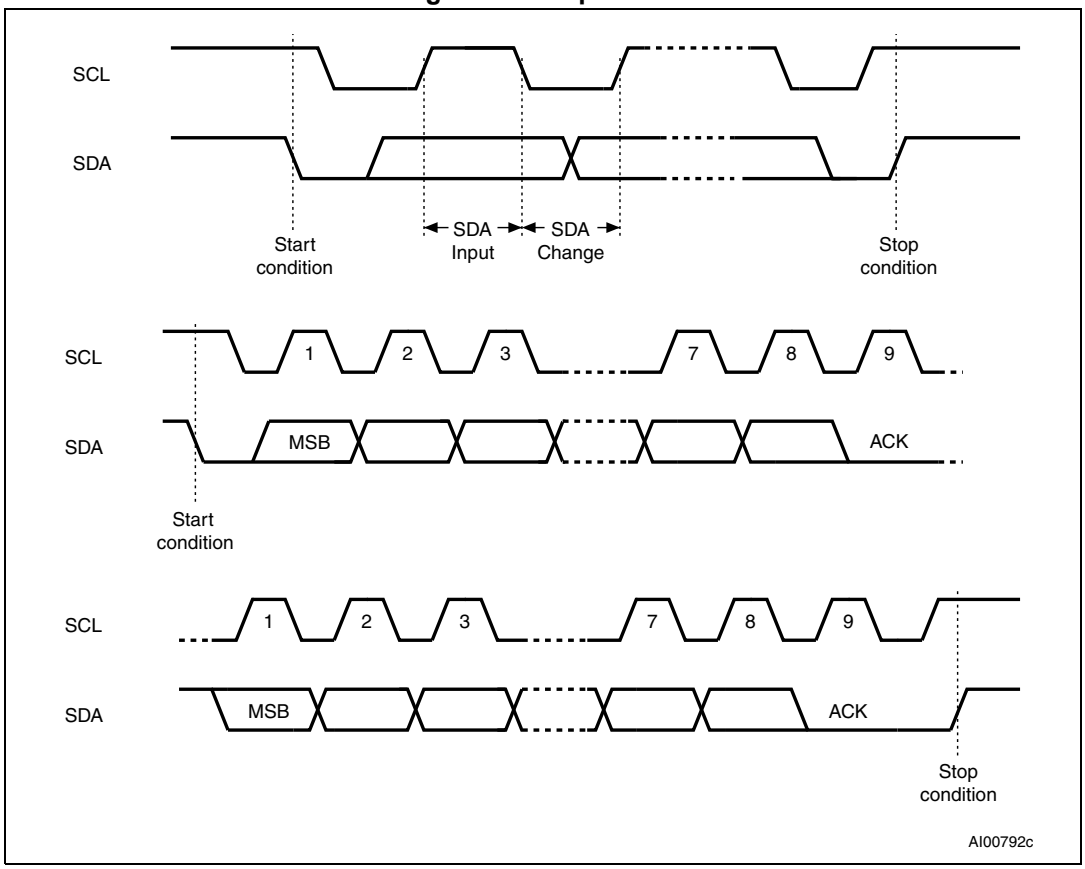
When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. However, the device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

2.5.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

Figure 4. Bus protocol



3 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 4*. Any device that sends data onto the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus master, and the other device is known as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether a bus master or a slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

3.5 Memory addressing

To start a communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

The Device Type Identifier Code (DTIC) consists of a 4-bit device type identifier, and a 3-bit slave address (SA2, SA1, SA0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

Table 2. Device Type Identifier Code (DTIC)

	Abbr	Device type identifier (1)				Select address (2) (3)			R_W_n	SA0 pin (4)
		b7	b6	b5	b4	b3	b2	b1	b0	
Read	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0 (5)	RPS0					0	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 1 (5)	RPS1					1	0	0	1	0, 1 or V_{HV}
Read Protection Status, block 2 (5)	RPS2					1	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 3 (5)	RPS3					0	0	0	1	0, 1 or V_{HV}
Set Page Address to 0 (6)	SPA0					1	1	0	0	0, 1 or V_{HV}
Set Page Address to 1 (6)	SPA1					1	1	1	0	0, 1 or V_{HV}
Read Page Address (7)	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	-					All other encodings				

1. The most significant bit, b7, is sent first.
2. Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins.
3. For backward compatibility with M34E02 devices, the order of block select bits (b3 and b1) is not a simple binary encoding of the block number.
4. SA0 pin is driven to Vss, Vcc or VHV.
5. Reading the block protection status results in Ack when the block is not write-protected, and results in NoAck when the block is write-protected.
6. Setting the EE page address to 0 selects the lower 256 bytes of EEPROM; setting it to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.
7. Reading the EE page address results in Ack when the current page is 0, and NoAck when the current page is 1.

Up to eight memory devices can be connected on a single serial bus. Each one is given a unique 3-bit code on the slave address (SA2, SA1, SA0) inputs. When the device select code is received, the device only responds if the slave address is the same as the value on the slave address (SA2, SA1, SA0) inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

3.6 Write operations

Following a Start condition, the bus master sends a device select code with the RW bit reset to 0. The device acknowledges this, as shown in *Figure 5*, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

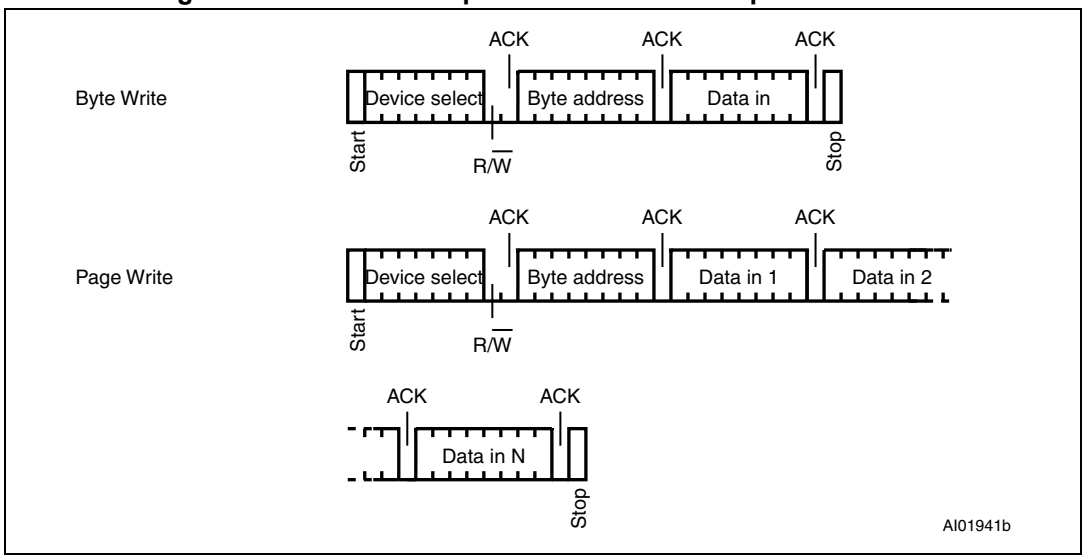
When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10th bit" time slot), either at the end of a Byte write or a Page write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

3.6.1 Byte write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 5*.

Figure 5. Write mode sequences in a non write-protected area



3.6.2 Page write

The Page write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control (WC) is low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address

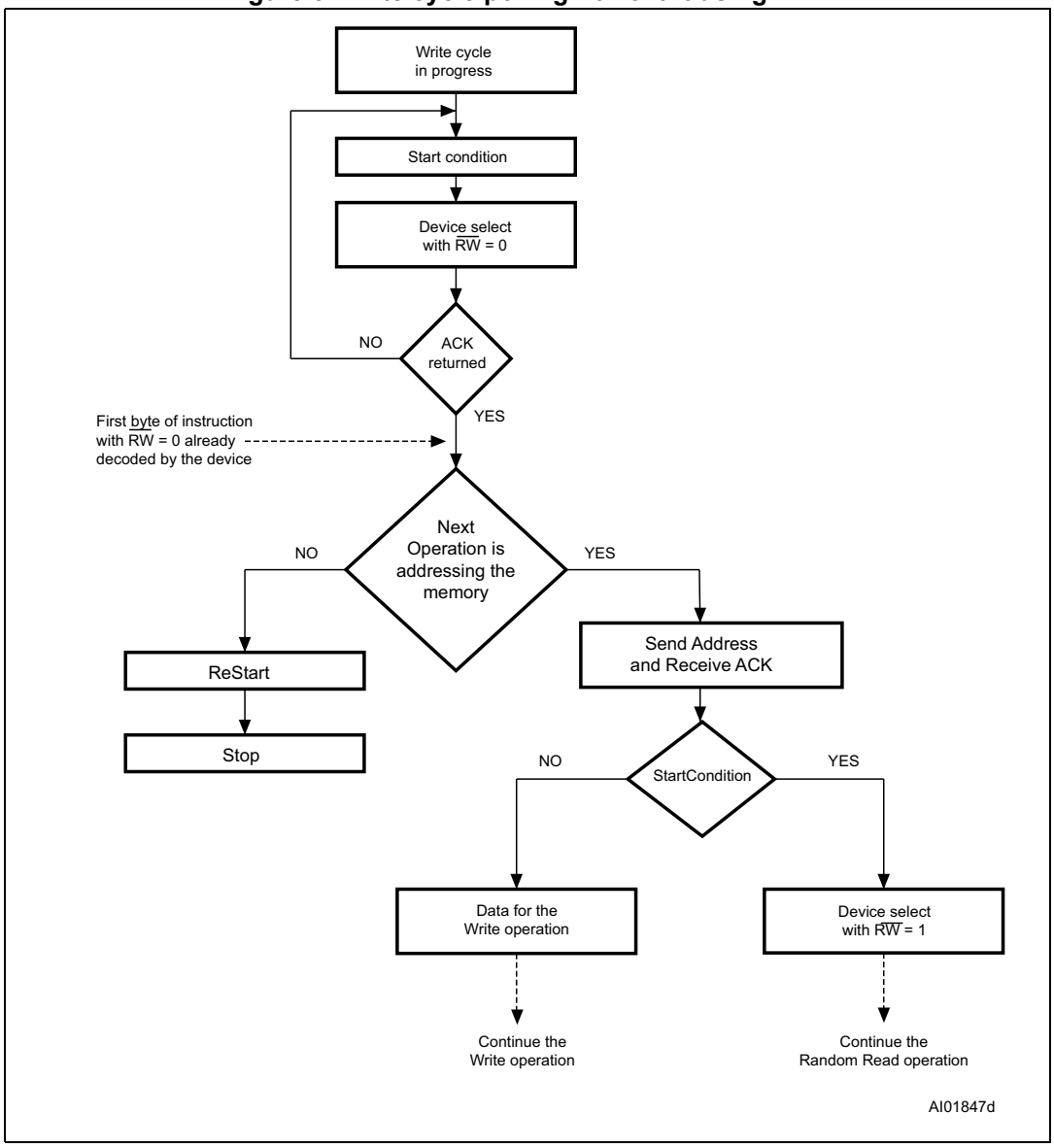
bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

3.6.3 Minimizing system delays by polling on ACK

The sequence, as shown in *Figure 6*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 6. Write cycle polling flowchart using ACK



During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 13*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

3.7 Read operations

Read operations are performed independently of whether a hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

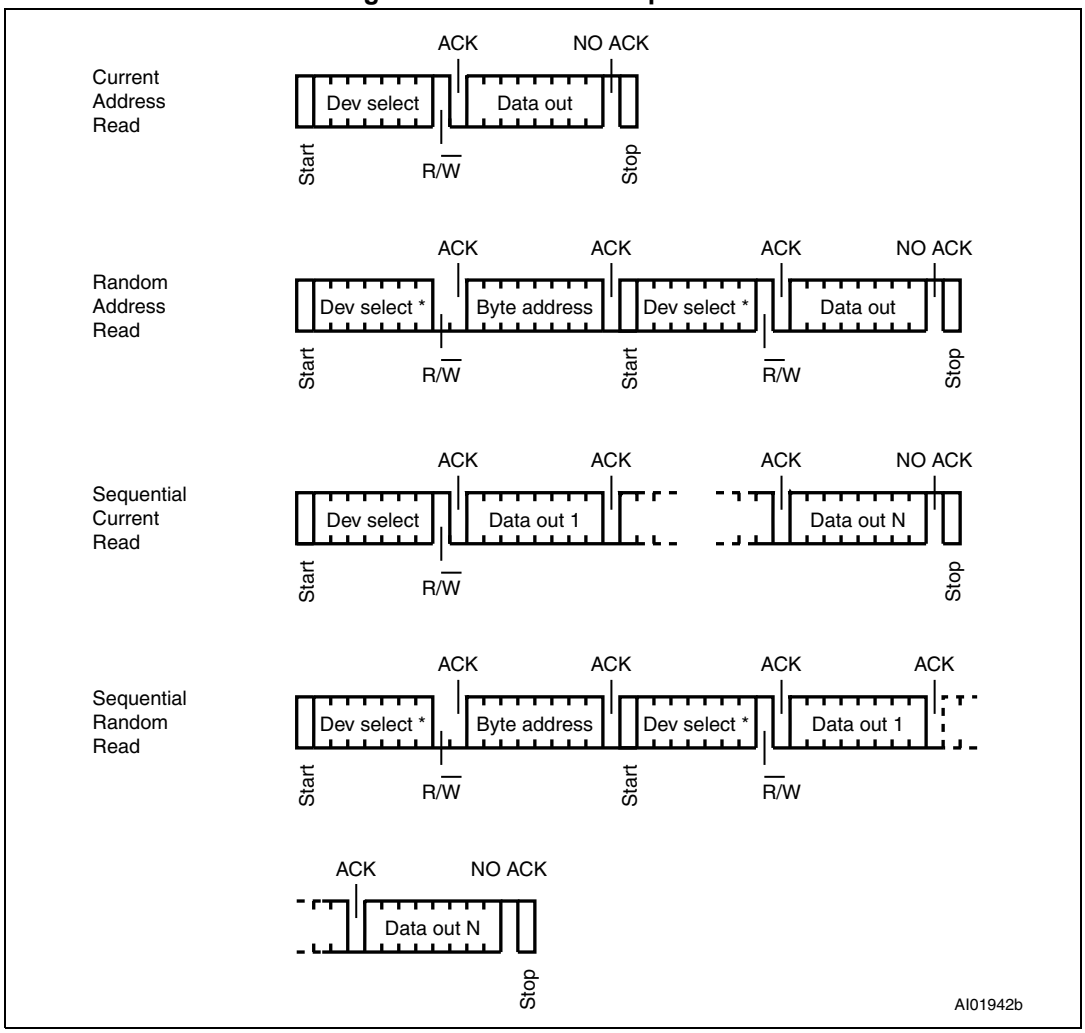
3.7.1 Random address read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 1*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.7.2 Current address read

For the Current address read operation, following a Start condition, the bus master only sends a device select code with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 1*, *without* acknowledging the byte.

Figure 7. Read mode sequences



3.7.3 Sequential read

This operation can be used after a Current address read or a Random address read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 1*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.7.4 Acknowledge in read mode

For all Read commands, after each byte read, the device waits for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

Note: The seven most significant bits of the device select code of a Random Read (in the 1st and 3rd bytes) must be identical.

3.8 Setting the write protection

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 1

The device has three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection status for block n

The level of write protection (set or cleared), that has been defined using these instructions, remains defined even after a power cycle.

The DTICs of the SWP, CWP and RPS instructions are defined in *Table 2*.

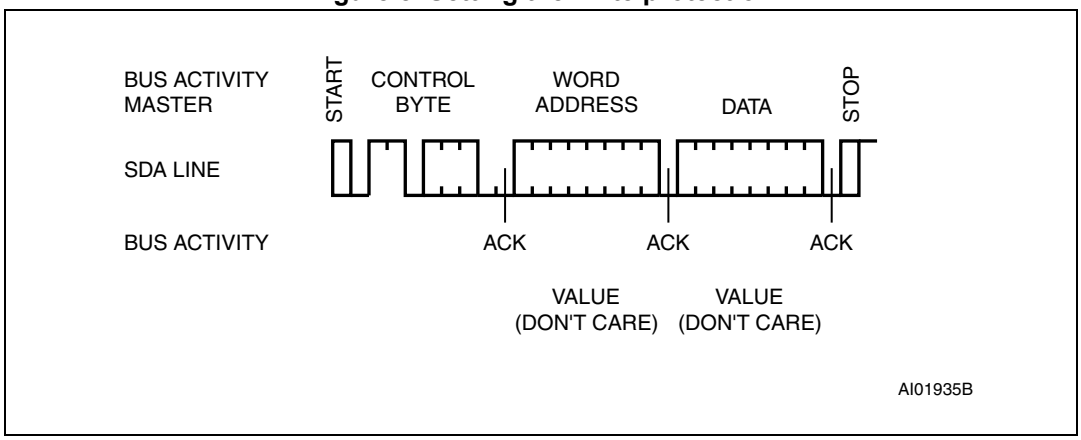
3.8.1 Set and clear the write protection (SWPn and CWP)

If the software write protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.

When decoded, SWPn and CWPn trigger a write cycle lasting t_W (see *Table 13*).

The DTICs of the SWP and CWP instructions are defined in *Table 2*.

Figure 8. Setting the write protection



3.8.2 Read the protection status (RPSn)

The serial bus master issues an RPSn command specifying which block to report upon. If the software write protection has not been set, the device replies to the data byte with an Ack. If it has been set, the device replies to the data byte with a NoAck.

The DTIC of the RPSn instruction is defined in *Table 2*.

3.8.3 Set the page address (SPAn)

The SPAn command selects the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the page address is always 0, selecting the lower 256 bytes.

The DTIC of the SPAn instruction is defined in *Table 2*.

3.8.4 Read the page address (RPA)

The RPA command determines if the currently selected page is 0 (device returns Ack) or 1 (device returns NoAck).

The DTIC of the RPA instruction is defined in *Table 2*.

4 Initial delivery state

The device is delivered with all bits in the memory array set to ‘1’ (each byte contains FFh).

5 Use within a DDR4 DRAM module

In the application, the M34E04 is soldered directly in the printed circuit module. The three slave address inputs (SA2, SA1, SA0) must be connected to V_{SS} or V_{CC} directly (that is without using a serial resistor) through the DRAM module connector (see *Table 3* and *Figure 3*). The pull-up resistor on SDA is connected on the SMBus of the motherboard (as shown in *Figure 9*).

The Write Control ($\overline{WC}$) of the M34E04 can be left unconnected. However, connecting it to V_{SS} is recommended, to maintain full read and write access.

Table 3. DRAM DIMM connections

DIMM position	SA2	SA1	SA0
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

5.1 Programming the M34E04

The situations in which the M34E04 is programmed can be considered under two headings:

- when the DDR4 DRAM is isolated (not inserted on the PCB motherboard)
- when the DDR4 DRAM is inserted on the PCB motherboard

5.1.1 Isolated DRAM module

With a specific programming equipment, it is possible to define the M34E04 content, using Byte and Page write instructions, and the write-protection SWP(n) and CWP instructions. To issue the SWP(n) and CWP instructions, the signal applied on SA0 must be driven to V_{HV} during the whole instruction.

5.1.2 DRAM module inserted in the application motherboard

Table 4 and *Table 5* show how the Ack bits can be used to identify the write-protection status.

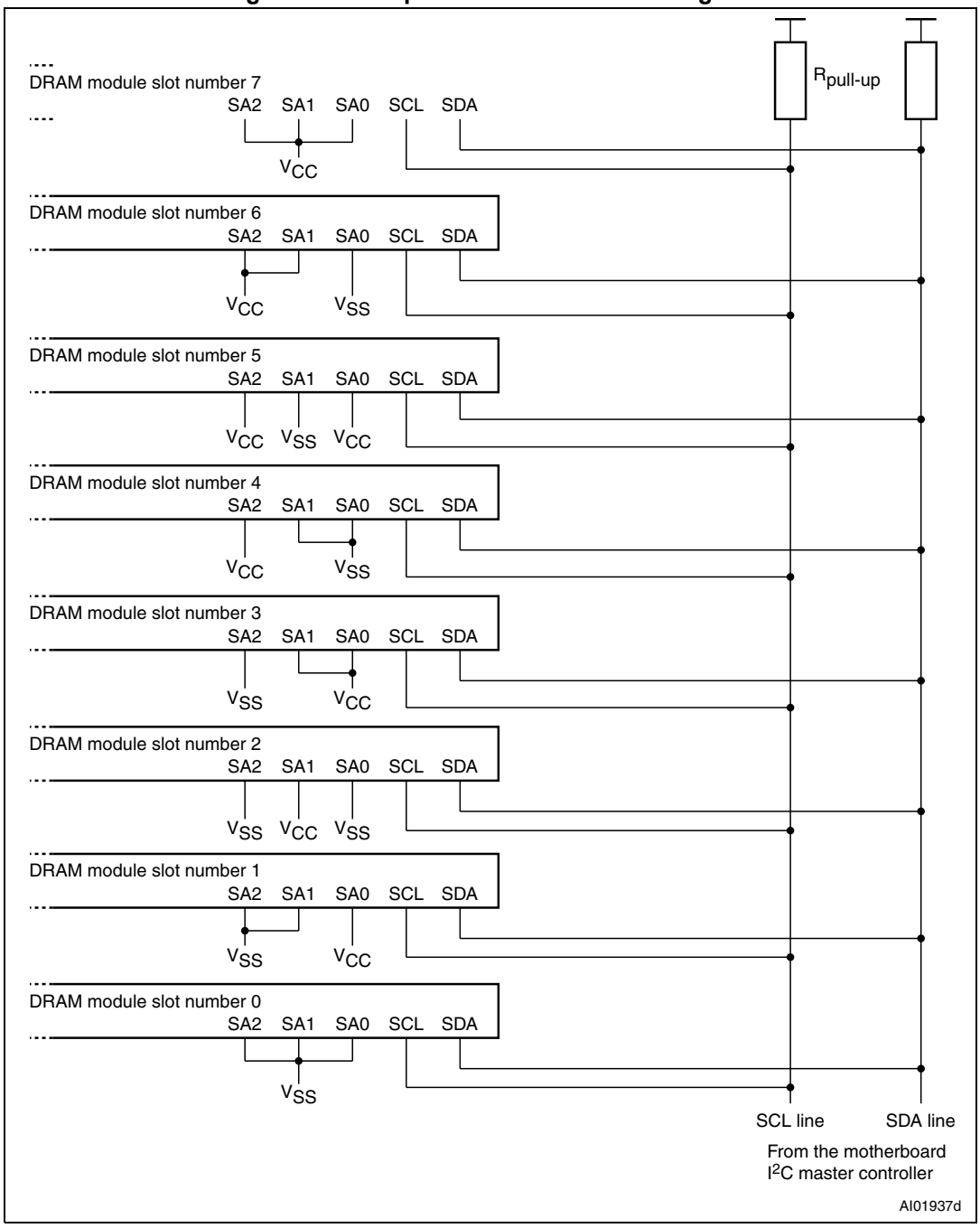
Table 4. Acknowledge when writing data or defining the write-protection status (instructions with R/W bit = 0)

Status	Instruction	Ack	Address	Ack	Data byte	Ack	Write cycle (t_W)
Protected	SWPn	NoAck	Not significant	NoAck	Not significant	NoAck	No
	CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write in protected block	Ack	Address	Ack	Data	NoAck	No
Not Protected	SWPn or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write	Ack	Address	Ack	Data	Ack	Yes

Table 5. Acknowledge when reading the protection status (instructions with R/W bit = 1)

SWPn Status	Instruction	Ack	Address	Ack	Data byte	Ack
Set	RPSn	NoAck	Not significant	NoAck	Not significant	NoAck
Not set	RPSn	Ack	Not significant	NoAck	Not significant	NoAck

Figure 9. Serial presence detect block diagram



1. SA0, SA1 and SA2 are wired at each DRAM module slot in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.

6 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and the device operation at these conditions or at any other conditions above those indicated in the operating sections of this specification is not implied. An exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
	Ambient temperature with power applied		-55	130	°C
T_{STG}	Storage temperature		-65	150	°C
V_{IO}	Input or output range	SA0 Others	-0.50 -0.50	11.0 6.5	V
I_{OL}	DC output current (SDA = 0)		-	20	mA
V_{CC}	Supply voltage		-0.5	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model) (1)		-	3500 (2)	V

1. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, and R2 = 500 Ω).
2. Positive and negative pulses applied on different combinations of pin connections, according to AECQ100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω).

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions (for temperature range 8 devices)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	3.6	V
T_A	Ambient operating temperature	0	+95	°C

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	SCL input rise and fall time, SDA input fall time	-	50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC measurement I/O waveform

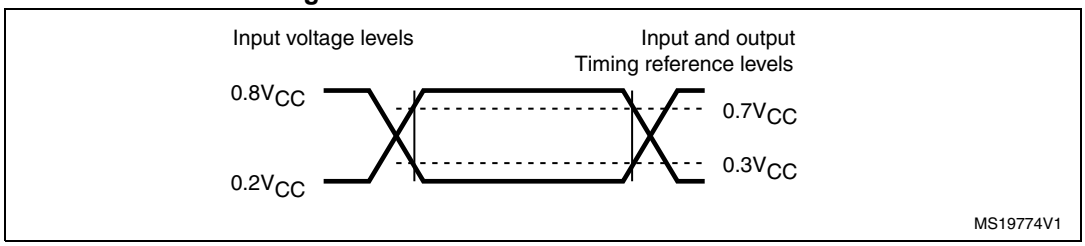


Table 9. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_{EiL}	SA0, SA1, SA2 input impedance	$V_{IN} < 0.3V_{CC}$	30	-	kΩ
Z_{EiH}	SA0, SA1, SA2 input impedance	$V_{IN} > 0.7V_{CC}$	800	-	kΩ
Z_{WCL}	$\overline{WC}$ input impedance	$V_{IN} < 0.3V_{CC}$	5	-	kΩ
Z_{WCH}	$\overline{WC}$ input impedance	$V_{IN} > 0.7V_{CC}$	500	-	kΩ
t_{NS}	Pulse width ignored (input filter on SCL and SDA)	-	-	100	ns

1. Characterized, not tested in production.

Table 10. Cycling performance

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance	$T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycle
		$T_A = 85$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1,200,000	

Table 11. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	$T_A = 55$ °C	200	Year

1. The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.

Table 12. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 7*)	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA, SA0, SA1, SA2)	$V_{IN} = V_{SS}$ or V_{CC}	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (read)	f_c = 400 kHz or 1 MHz	-	1	mA
I_{CC0}	Supply current (write)	During t_W, $V_{IN} = V_{SS}$ or V_{CC}	-	1 (1)	mA
I_{CC1}	Standby supply current	Device not selected (2), $V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} \geq 2.2$ V	-	2	µA
		Device not selected (2), $V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} < 2.2$ V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	-	-0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	-	0.7V_{CC}	V_{CC}+1	V
V_{HV}	SA0 high voltage detect	$V_{CC} < 2.2$ V	7	10	V
		$V_{CC} \geq 2.2$ V	V_{CC} +4.8 V	10	V
V_{OL}	Output low voltage	I_{OL} = 20 mA, $V_{CC} \geq 2.2$ V	-	0.4	V
		I_{OL} = 6 mA, $V_{CC} \leq 2$ V	-	0.6	V
		I_{OL} = 3 mA, $V_{CC} \leq 2$ V	-	0.4	V
V_{POR}	Power on reset threshold	-	-	1.4 (1)	V
V_{PDR}	Power down reset threshold	-	0.7 (1)	-	V

1. Measured during characterization, not tested in production.
2. The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write command).

Table 13. AC characteristics

Symbol		Parameter	V_{CC} < 2.2 V		V_{CC} ≥ 2.2 V				Unit
			100 kHz		400 kHz		1000 kHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	f_C	Clock frequency	10	100	10	400	10	1000	kHz
t_{HIGH}	t_{CHCL}	Clock pulse width high time	4000	-	600	-	260	-	ns
t_{LOW} (1)	t_{CLCH}	Clock pulse width low time	4700	-	1300	-	500	-	ns
$t_{TIMEOUT}$ (2)		Detect clock low timeout	25	35	25	35	25	35	ms
t_R (3)	t_{XH1XH2}	SDA rise time	-	1000	20	300	-	120	ns
t_F (3)	t_{QL1QL2}	SDA(out) fall time	-	300	20	300	-	120	ns
$t_{SU:DAT}$	t_{DXCH}	Data in setup time	250	-	100	-	50	-	ns
$t_{HD:DI}$	t_{CLDX}	Data in hold time	0	-	0	-	0	-	ns
$t_{HD:DAT}$	t_{CLQX}	Data out hold time	200	3450	200	900	0	350	ns
$t_{SU:STA}$ (4)	t_{CHDL}	Start condition setup time	4700	-	600	-	260	-	ns
$t_{HD:STA}$	t_{DLCL}	Stop condition hold time	4000	-	600	-	260	-	ns
$t_{SU:STO}$	t_{CHDH}	Stop condition setup time	4000	-	600	-	260	-	ns
t_{BUF}	t_{DHDL}	Time between Stop Condition and next Start Condition	4700	-	1300	-	500	-	ns
t_W		Write time	-	5	-	5	-	5	ms
t_{POFF} (3)		Time ensuring a Reset when V_{CC} drops below V_{PDR}(min)	100	-	100	-	100	-	µs
t_{INIT} (3)		Time from V_{CC}(min) to the first command	0	-	0	-	0	-	µs

1. Initiate clock stretching, which is an optional SMBus bus feature.
2. A timeout condition can only be ensured if SCL is driven low for $t_{TIMEOUT}$(Max) or longer; then the M34E04 is set in Standby mode and is ready to receive a new START condition. If SCL is driven low for less than $t_{TIMEOUT(}$Min), the M34E04 internal state remains unchanged.
3. Measured during characterization, not tested in production.
4. To avoid spurious START and STOP conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.

Figure 11. AC waveforms

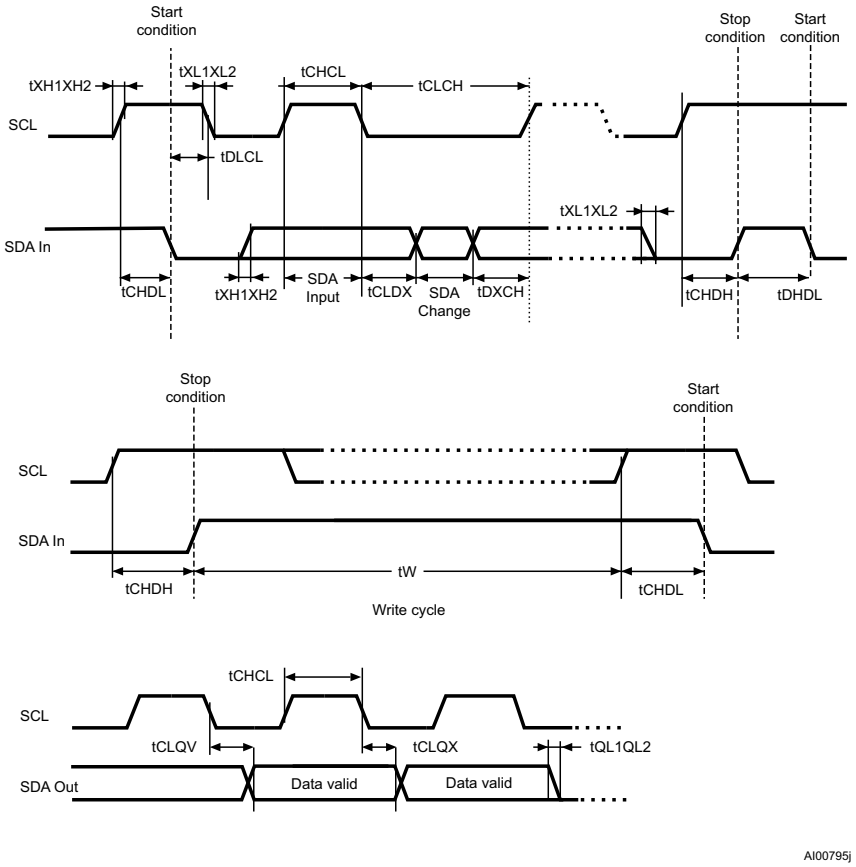


Figure 12. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 1 MHz

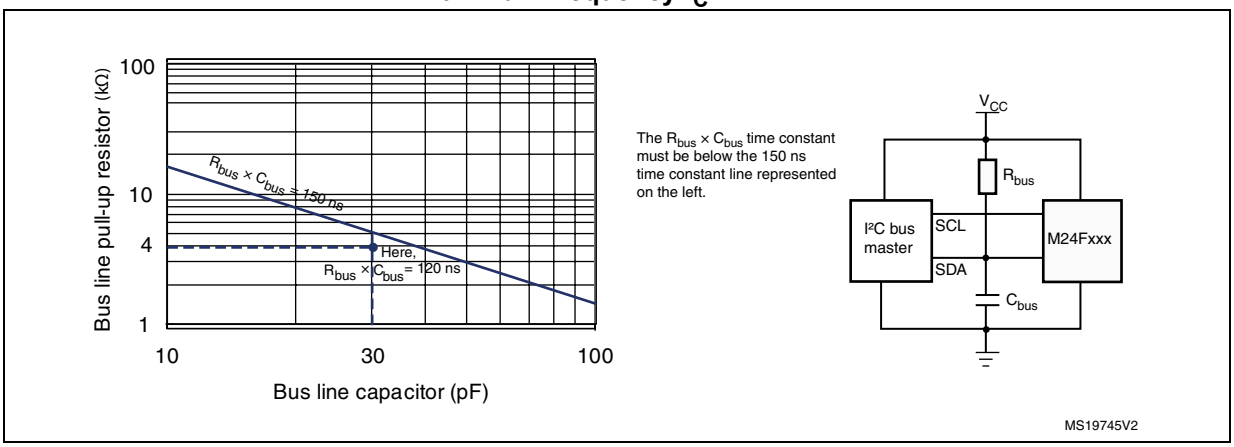
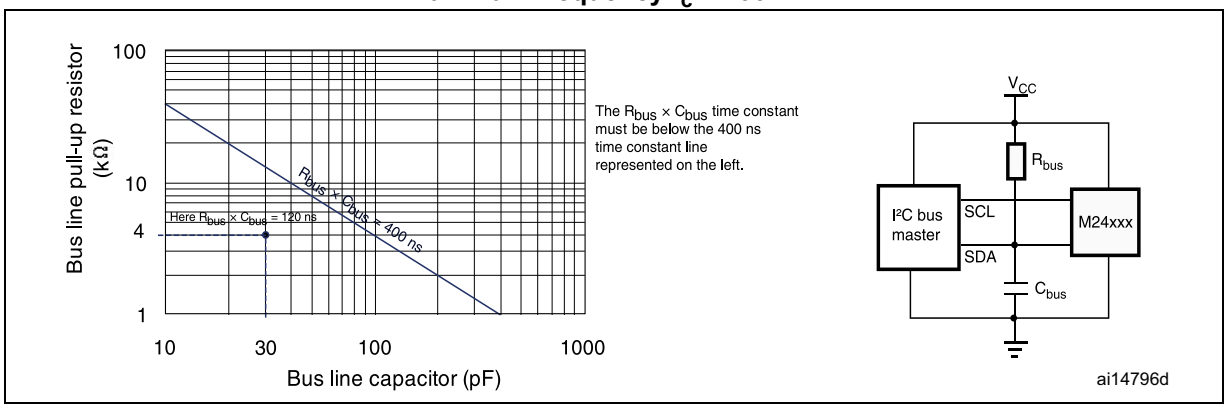


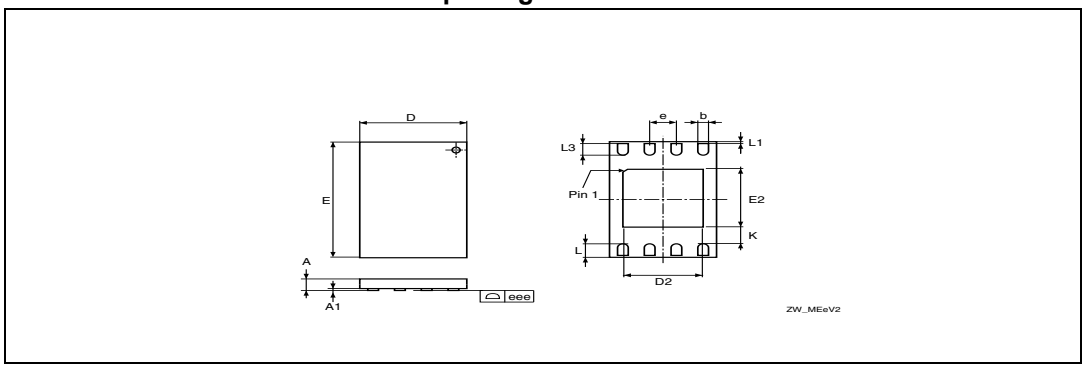
Figure 13. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_c = 400 kHz



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat no lead, package outline



1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 14. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)	-	1.200	1.600	-	0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)	-	1.200	1.600	-	0.0472	0.0630
e	0.500	-	-	0.0197	-	-
K (rev MC)	-	0.300	-	-	0.0118	-
L	-	0.300	0.500	-	0.0118	0.0197
L1	-	-	0.150	-	-	0.0059
L3	-	0.300	-	-	0.0118	-
eee (2)	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

9 Part numbering

Table 15. Ordering information scheme

Example: M34E04 - F MC 9 T G

Device type

M34 = Application specific I^2C serial access EEPROM

Device function

E04 = 4 Kbit (512 × 8) SPD (serial presence detect)

Operating voltage

F = V_{CC} = 1.7 to 3.6 V over 0 °C to 95 °C

Package(1)

MC= UFDFPN8 (MLP8)

Temperature range

9 = 0 °C to 95 °C

Option

T = Tape and reel packing

blank = Tube packing

Plating technology

G = ECOPACK2®

1. All package are ECOPACK2® (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Engineering Sample

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

10 Revision history

Table 16. Document revision history

Date	Revision	Changes
20-Jun-2012	1	Initial release
04-Dec-2012	2	Updated the supply voltage, temperature range and data retention in the list and *Table 15*. Updated the first paragraph in *Section 1*. Moved *Table 2* from section 2.5.4 to *Section 3.5*. and added note (5). Moved former section 3.6 to the end of *Section 3* and updated it. Updated V_{IO} Max., V_{ESD} Max. and I_{OL} Max. values in *Table 6*. Removed text from 1st paragraph of *Section 7*. Updated *Table 7*, *Table 9* and *Table 12*. Updated different symbols, values and note (2) in *Table 13*. Updated *Figure 12*.
22-May-2013	3	Changed Datasheet status to *Datasheet - production data*. Updated UFDFPN8 silhouette on the cover page. Updated f_c and V_{PDR} values, added I_{CC0} row and updated note (1) in *Table 12: DC characteristics*. Updated f_{POFF} and t_{INIT} and corresponding notes in *Table 13: AC characteristics*. Updated UFDFPN8 in *Table 15: Ordering information scheme*. Changed the temperature range from ‘6’ to ‘8’.
21-Jun-2013	4	Updated *Table 15: Ordering information scheme*. Temperature range: changed from ‘8’ to ‘9’. Plating technology: kept ‘G’ but removed ‘T’.
03-Feb-2014	5	Added Specification JEDEC EE1004. Updated *Figure 11*.
27-Jun-2014	6	On Cover page updated Write cycles value and years data retention value. Added *Table 10: Cycling performance* and *Table 11: Memory cell data retention*.
12-Nov-2014	7	Updated: – ECOPACK2® on cover page – *Section 2.1: Serial clock (SCL)* – note 2 on *Table 13* – note 1 on *Table 15* Added: – Sentence about Engineering samples after *Table 15*