

Distributed Low Noise Amplifier

9 kHz - 20 GHz



MAAL-011181

Rev. V1

Features

- Gain: 15 dB
- Noise Figure: 2.5 dB
- Output IP3: 29 dBm
- 5 V Drain Supply
- 5 mm, 32 lead PQFN Package
- Halogen-Free “Green” Mold Compound
- RoHS* Compliant

Applications

- Multi Market
- ISM

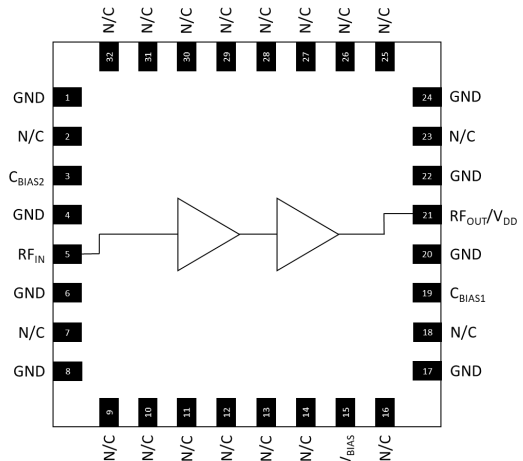
Description

The MAAL-011181 is a wideband distributed low noise amplifier with an operating frequency range of 9 kHz to 20 GHz. This LNA typically has a 2.5 dB noise figure, 15 dB gain, 29 dBm output IP3, 19 dBm output P1dB, and 21 dBm P3dB. Only a single bias supply voltage of 5 V is required to bias the LNA. The typical current draw is 125 mA.

No external matching components are required, but external biasing components are needed. Large capacitors for bypassing are required on C_{BIAS1} and C_{BIAS2} for low frequency operation. An RF choke and blocking capacitor should be added to the RF output pin to bias the amplifier. 5 V must be applied to V_{BIAS} while V_{DD} can vary.

The MAAL-011181 is designed for wideband low noise applications such as test equipment. The 5 mm, 32 lead PQFN package is lead free and RoHS compliant. This LNA is also available in die form under part number MAAL-011181-DIE.

Block Diagram



Pin Configuration^{1,2}

Pin #	Pin Name	Description
1,4,6,8,17,20,22,24	GND	Ground
2,7,9-14,16,18,23,25-32	N/C	No Connection
3	C_{BIAS2}	Bypass Capacitor 2
5	RF_{IN}	RF Input
15	V_{BIAS}	Bias Voltage
19	C_{BIAS1}	Bypass Capacitor 1
21	RF_{OUT}/V_{DD}	RF Output/Voltage Supply

1. It is recommended that all NC (No Connect) pins be grounded.
2. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground.

Ordering Information

Part Number	Package
MAAL-011181-TR0500	500 Piece Reel
MAAL-011181-SMB	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: $V_{DD} = +5\text{ V}$, $V_{BIAS} = +5\text{ V}$, $T_A = 25^\circ\text{C}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	1 GHz 10 GHz 20 GHz	dB	13.5 12.5 11.0	15.5 14.5 13.0	—
Gain Flatness	9 kHz - 20 GHz	dB	—	+/-0.5	—
Gain Variation vs. Temperature	10 GHz	dB/°C	—	0.02	—
Noise Figure	10 GHz 20 GHz	dB	—	2.0 4.0	2.8 5.0
Input Return Loss	9 kHz - 20 GHz	dB	—	15	—
Output Return Loss	9 kHz - 20 GHz	dB	—	10	—
P1dB	10 GHz 20 GHz	dBm	15.0 9.5	17.5 12.5	—
P3dB	10 GHz 20 GHz	dBm	—	20 15	—
IP3	10GHz 20 GHz -20 dBm per tone, 10 MHz spacing	dBm	—	30 25	—
Quiescent Current	9 kHz - 20 GHz	mA	—	125	165

Maximum Operating Conditions

Parameter	Maximum
Input Power	25 dBm
Junction Temperature ^{3,4}	+160°C
Operating Temperature	-40°C to +85°C

3. Operating at nominal conditions with $T_J \leq +160^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.

4. TX Junction Temp. (T_J) = $T_C + \Theta_{jc} * ((V * I) - (P_{OUT} - P_{IN}))$.

Typical TX thermal resistance (Θ_{jc}) = 65°C/W.

a) For $T_C = +85^\circ\text{C}$, $T_J = 125.6^\circ\text{C}$ @ 5 V, 125 mA

b) For $T_C = +25^\circ\text{C}$, $T_J = 65.6^\circ\text{C}$ @ 5 V, 125 mA

Absolute Maximum Ratings^{5,6}

Parameter	Absolute Maximum
Input Power	27 dBm
Junction Temperature ⁷	+180°C
Storage Temperature	-55°C to +150°C

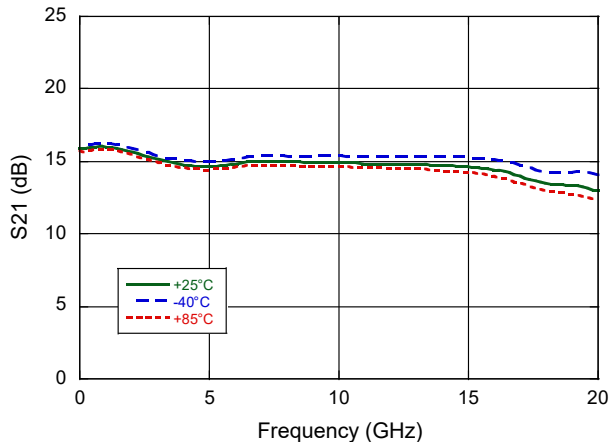
5. Exceeding any one or combination of these limits may cause permanent damage to this device.

6. MACOM does not recommend sustained operation near these survivability limits.

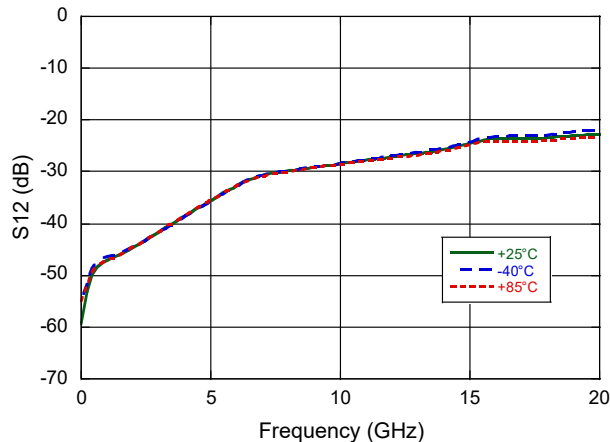
7. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Typical Performance Curves

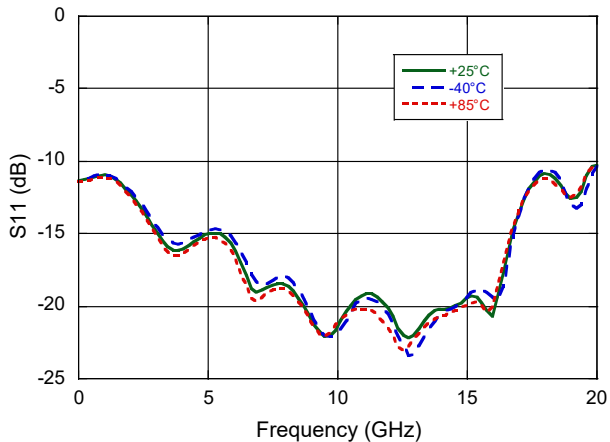
Gain



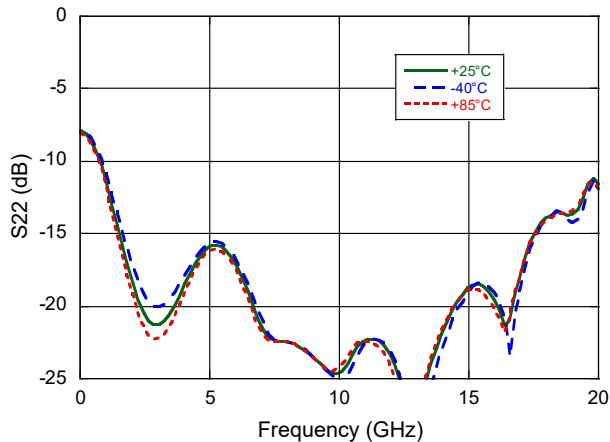
Isolation



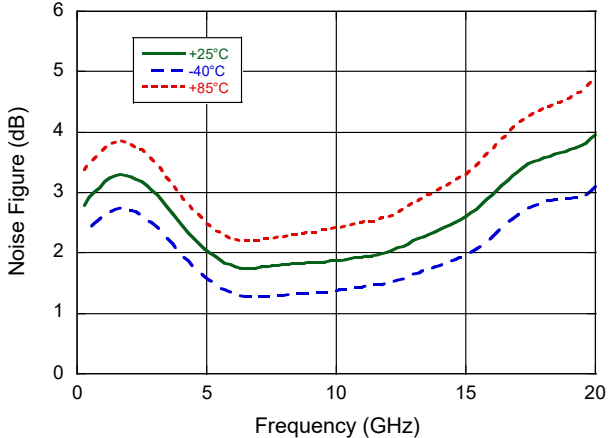
Input Return Loss



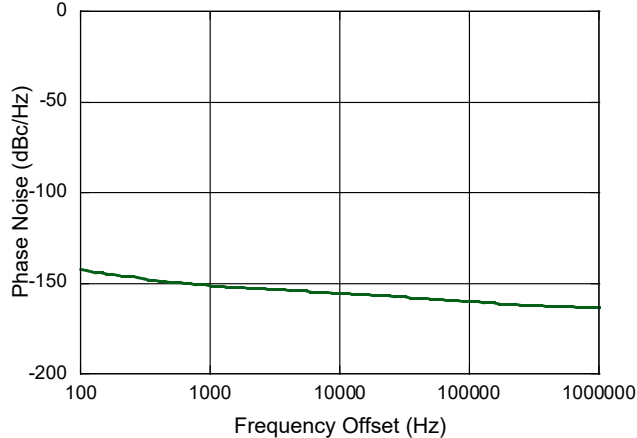
Output Return Loss



Noise Figure

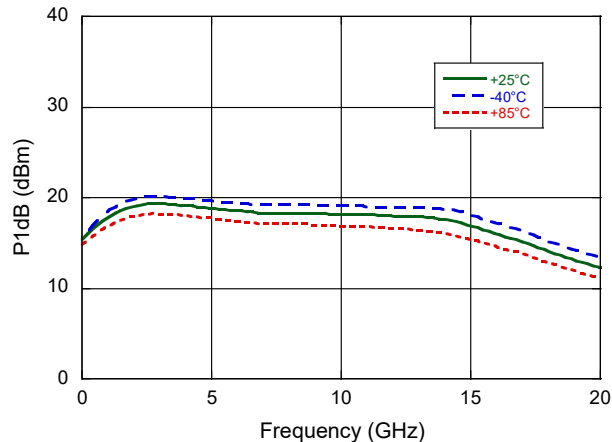


Phase Noise (Pin = -10 dBm @ 12 GHz)

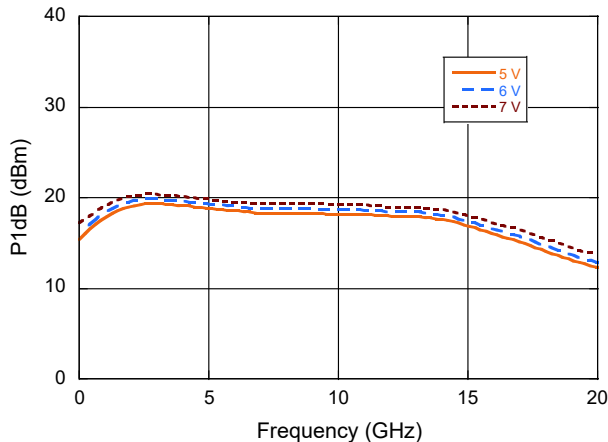


Typical Performance Curves

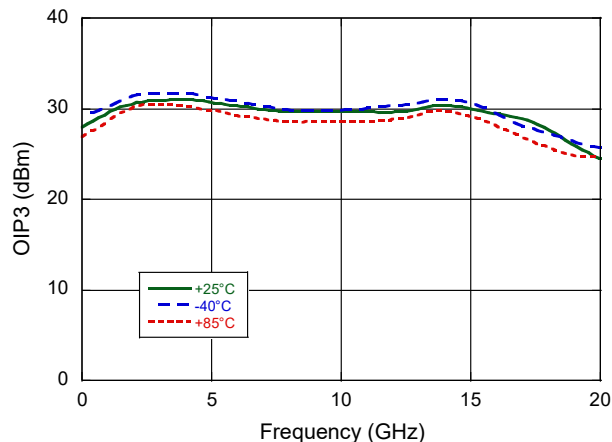
P1dB over Temperature



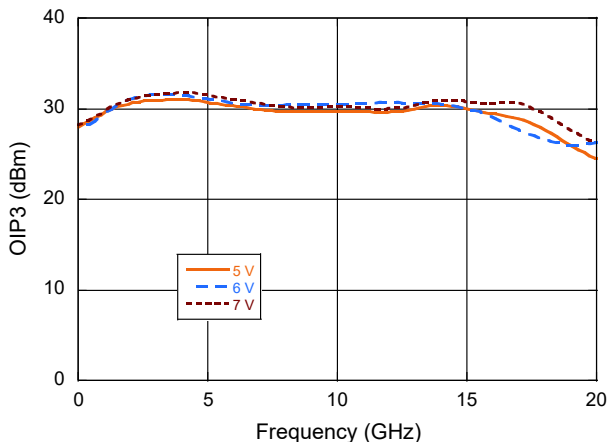
P1dB over Voltage (Vbias = +5V)



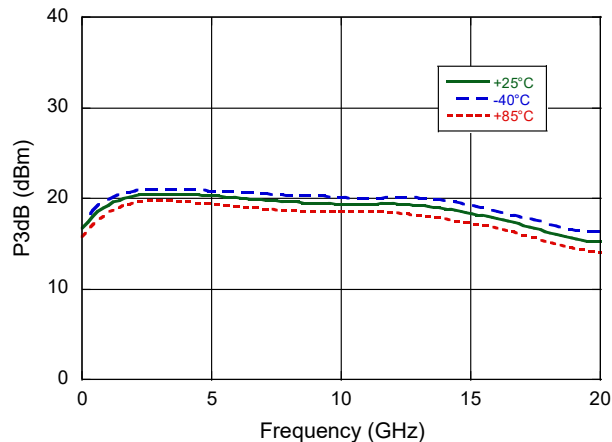
Output IP3 over Temperature



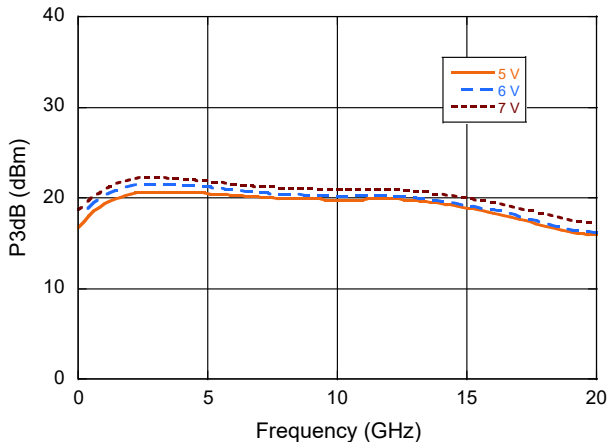
Output IP3 over Voltage (Vbias = +5V)



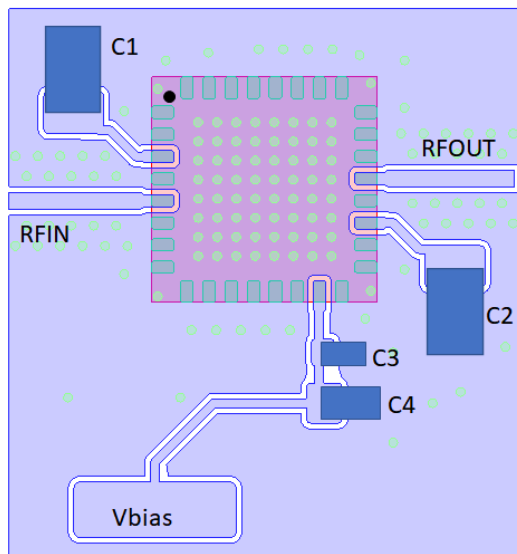
P3dB over Temperature



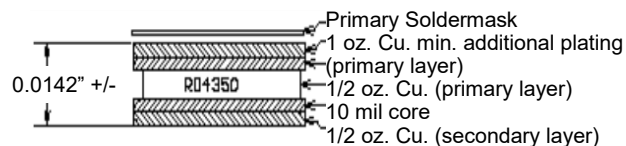
P3dB over Voltage (Vbias = +5V)



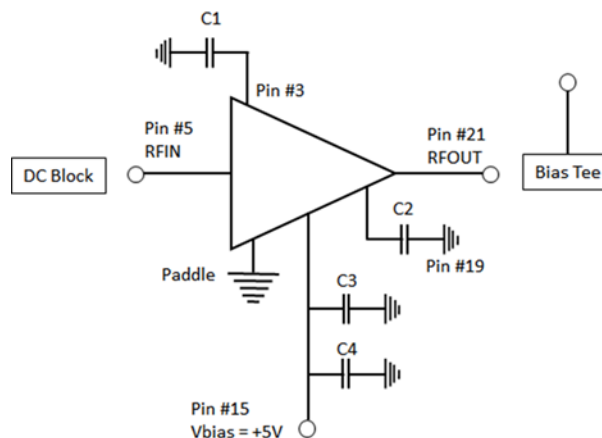
Recommended PCB Layout⁸



8. The DC blocking capacitor on RF_{IN} and Bias Tee on RF_{OUT} were connected externally on the MACOM Evaluation board and are not shown in this layout.



Application Schematic



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1B devices.

Parts List

Part	Value	Case Style	Manufacturer	Manufacturer's Part Number
C1,C2	1 μ F	0805	TDK	C2012X5R1C106M085AC
C3	100 pF	0402	Murata	GCM1555C1H101JA16
C4	1000 pF	0603	Murata	GCM188R72A102KA37

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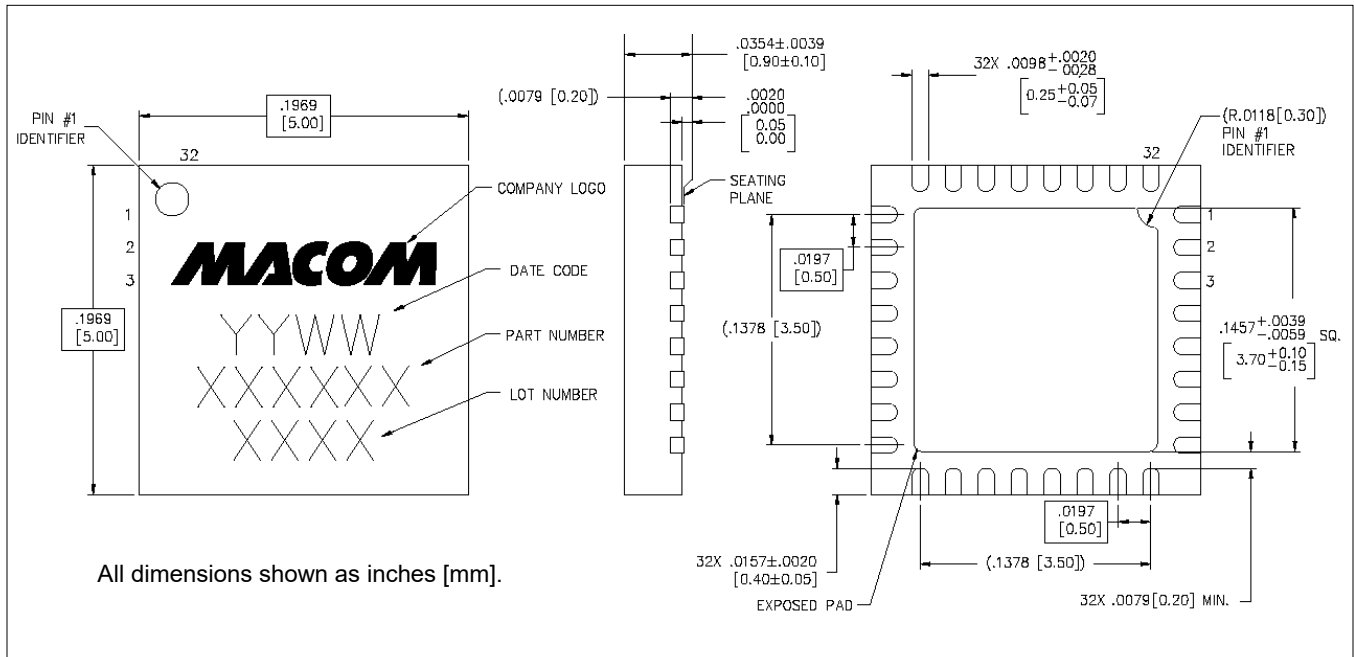
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Lead-Free 5 mm 32-Lead PQFN[†]



[†] Reference Application Note S2083 for lead-free solder reflow recommendations.
 Meets JEDEC moisture sensitivity level 1 requirements.
 Plating is NiPdAuAg.