

Wideband Amplifier 10 MHz - 40 GHz

Rev. V2

Features

- 13 dB Gain
- 50 Ω Input / Output Match
- +18 dBm Output Power
- +5 V DC, 190 mA
- Lead-Free 5 mm 9-lead LGA Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAM-011109 is an easy-to-use, wideband amplifier that operates from 10 MHz - 40 GHz. The device features 13 dB gain and +18 dBm of output power. Matching is 50 Ω with typical return loss better than 15 dB. This amplifier requires dual DC supplies: 5 V (190 mA) and a low current -5 V (<1 mA).

The MAAM-011109 integrates an ultra-broadband bias choke, DC blocking and bypass capacitors. Other features include a gate bias adjust pin to change current setting for power or temperature, a gain trim control pin that allows 15 dB of gain control (0 to -1V), and a temperature compensated detector pin that provides a DC voltage in relation to output power.

The MAAM-011109 is ideally suited for any application that requires 50 Ω gain from 10 MHz to 40 GHz. It is useful in applications where the incoming signal varies over a broad bandwidth such as laboratory, instrumentation, and defense applications.

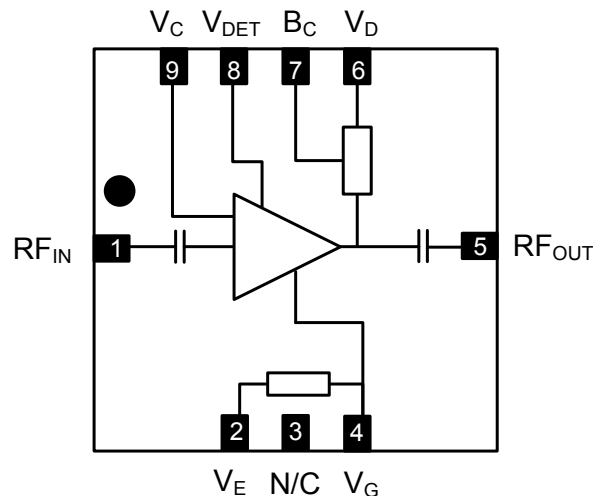
This device is housed in a leadless 5 X 5 X 1.3 mm package that can be handled and placed with standard pick and place assembly equipment. The package base is a two layer laminate with overmold fully compatible with PCB environment and wash conditions. The module includes a GaAs MMIC that is fully passivated for performance and reliability.

Ordering Information^{1,2}

Part Number	Package
MAAM-011109	bulk quantity
MAAM-011109-TR1000	1000 piece reel
MAAM-011109-001SMB	Sample board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Function
1	RF _{IN}	RF Input
2	V _E	-5 V Supply
3	N/C	No Connection
4	V _G	Gate Adjust (optional)
5	RF _{OUT}	RF Output
6	V _D	+5 V Supply
7	B _C	V _D Bypass (optional) No Connection
8	V _{DET}	Power Detector
9	V _C	Gain Control
10	Paddle ³	Ground

3. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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Electrical Specifications: $T_A = +25^\circ\text{C}$, $V_D = +5\text{ V}$, $V_E = -5\text{ V}$, $V_C = \text{Open}$, $Z_{IN} = Z_{OUT} = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	0.1 GHz	dB	—	12.0	—
	2 GHz		11.0	13.0	
	12 GHz		10.0	12.0	
	20 GHz		10.0	11.5	
	32 GHz		8.0	11.0	
	40 GHz		—	8.0	
Isolation	0.01 - 40 GHz	dB	—	22	—
Input Return Loss	0.01 - 40 GHz	dB	—	13	—
Output Return Loss	0.01 - 40 GHz	dB	—	9	—
Noise Figure	0.01 - 40 GHz	dB	—	3.5	—
P1dB	0.1 GHz	dBm	—	+18	—
	10 GHz			+17	
	40 GHz			+13	
Output IP3	0.1 GHz	dBm	—	+26	—
	10 GHz			+24	
	40 GHz			+16	
Bias Current	$V_D = +5\text{ V}$, $V_E = -5\text{ V}$	mA	—	170	—

Absolute Maximum Ratings^{4,5,6}

Parameter	Absolute Max.
Input Power	+17 dBm
Drain Supply Voltage	+8 Volts
Junction Temperature ⁷	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Operating at nominal conditions with $T_J \leq 150^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.
- Junction Temperature (T_J) = $T_C + \Theta_{JC} * ((V * I) - (P_{OUT} - P_{IN}))$
Typical thermal resistance (Θ_{JC}) = 21°C/W
 - For $T_C = 25^\circ\text{C}$,
 $T_J = 43^\circ\text{C}$ @ 5 V, 190 mA, $P_{OUT} = 20\text{ dBm}$, $P_{IN} = 7\text{ dBm}$
 - For $T_C = 85^\circ\text{C}$,
 $T_J = 103^\circ\text{C}$ @ 5 V, 190 mA, $P_{OUT} = 20\text{ dBm}$, $P_{IN} = 7\text{ dBm}$

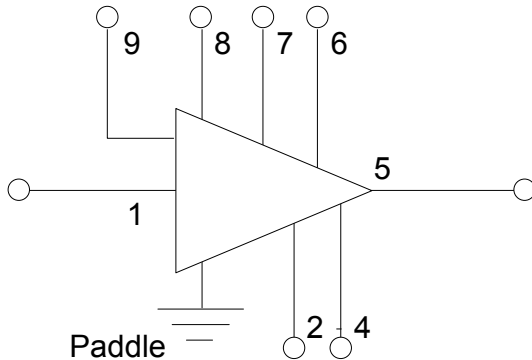
Handling Procedures

Please observe the following precautions to avoid damage:

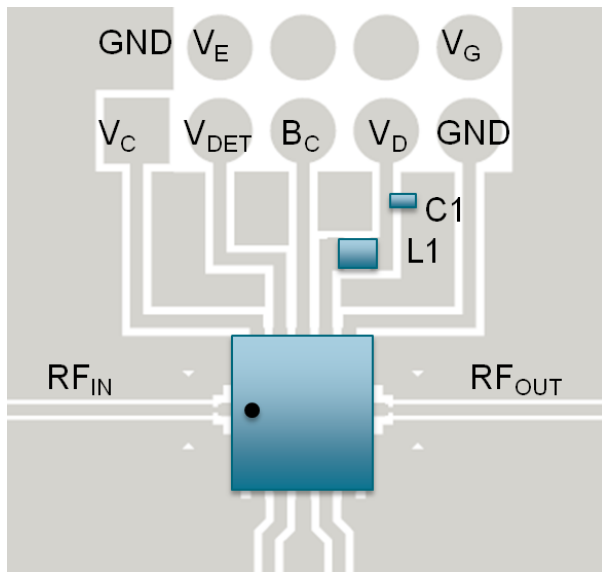
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1B devices.

Application Schematic



Recommended PCB Layout



Parts List

Component	Value	Package
C1	0.22 μ F	0201
L1	470 Ω	0603

Application Information for DC & pins

For proper MAAM-011109 operation a DC voltage must be applied at the V_E (-5 V) and V_D (+5 V) pins *in that order*. The optional V_G pin may be used to override the automatic V_E bias network to hard set the gate. Adjusting V_G from -0.2 V to -0.6 V will change the quiescent current. If V_G is used, V_E should be left unconnected.

The V_C pin is typically left unconnected unless gain control or output power limiting is desired. Please refer to the “Variable Gain/Limiting” section for detailed usage.

The V_D pin should be bypassed with at least 0.1 μ F for stability. For operation below 100 MHz a ferrite bead (Murata BLM18BB471) must be inserted between the V_D pin and bypass capacitor. The V_G and V_C pins must also be bypassed with a 0.1 μ F capacitor if operating below 100 MHz.

The V_{DET} pin is typically left unconnected unless a voltage reference is desired that is correlated to the output power. Please refer to the “Internal Detector” section for detailed usage.

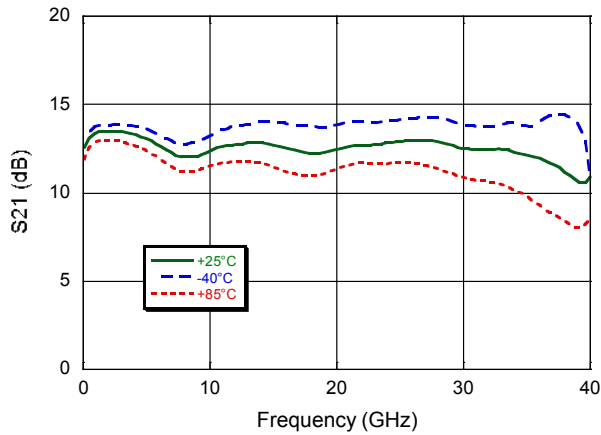
The B_C pin is typically left unconnected unless gain bandwidth and shape change is desired. Please refer to an application note on this pin.

The input and output pins are internally DC blocked. No more than +/- 12 V should ever be present on these RF only pins.

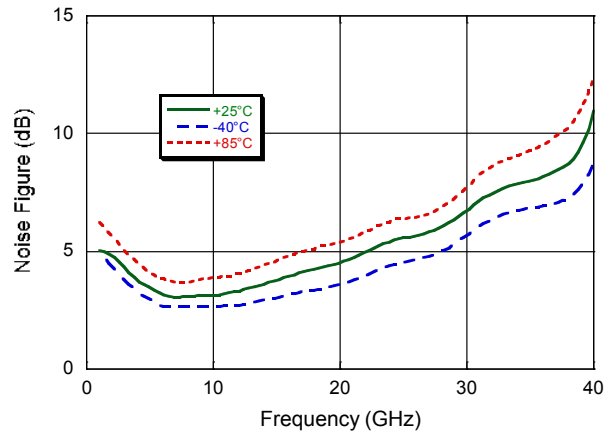
The backside paddle of the MAAM-011109 should be connected to ground with as many vias as possible to maximize high frequency performance, thermal dissipation, and stability.

Typical Performance Curves over Temperature

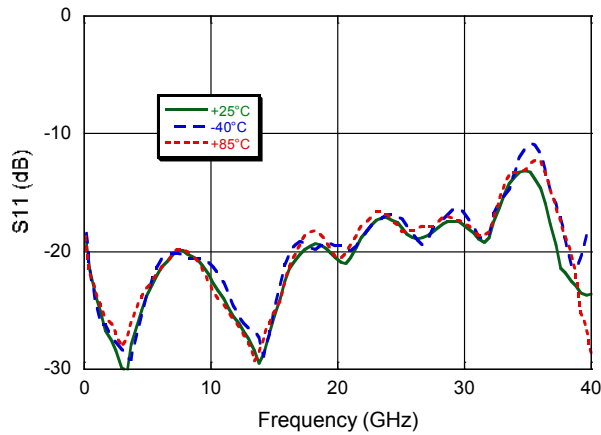
Gain



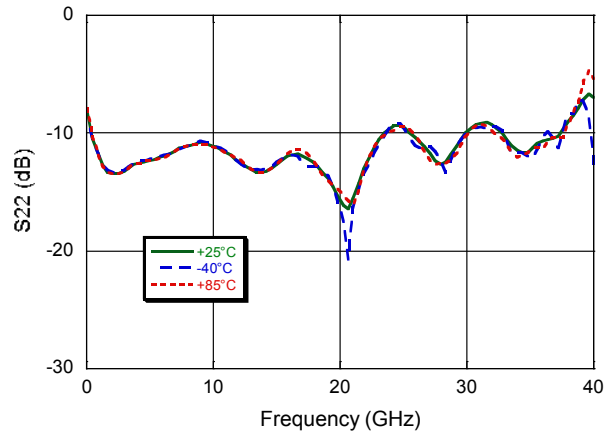
Noise Figure



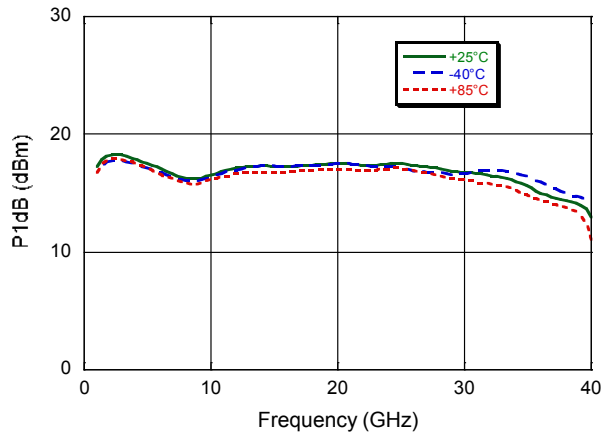
Input Return Loss



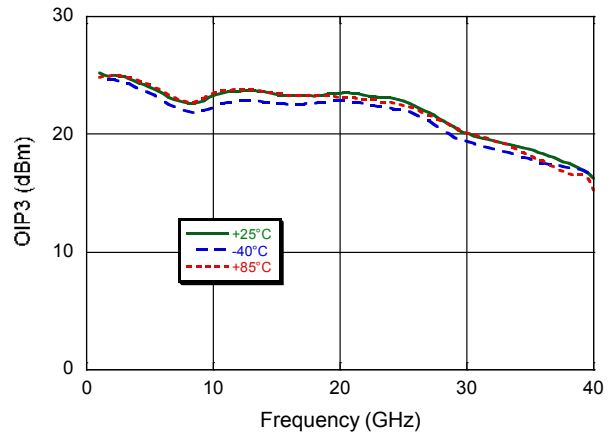
Output Return Loss



Output P1dB

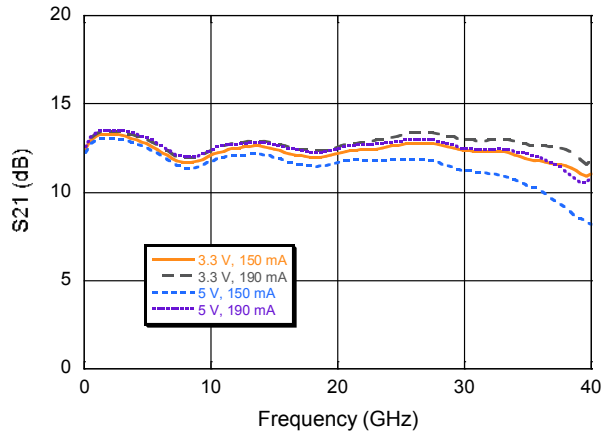


Output IP3

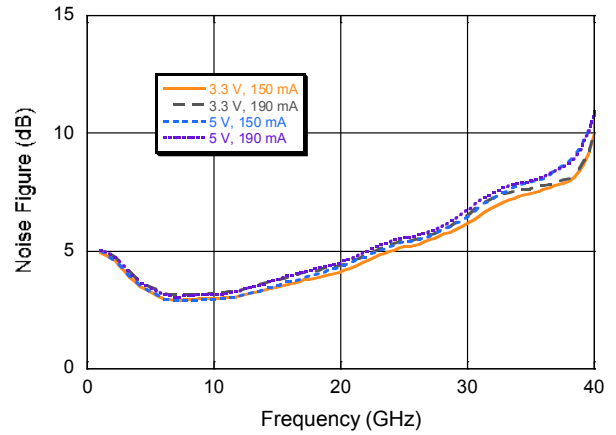


Typical Performance Curves vs. Voltage and Current

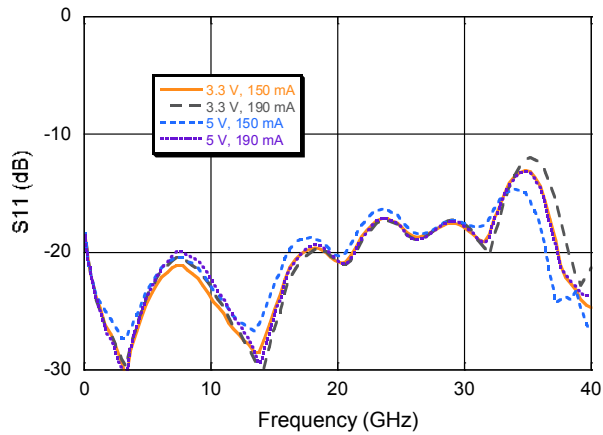
Gain



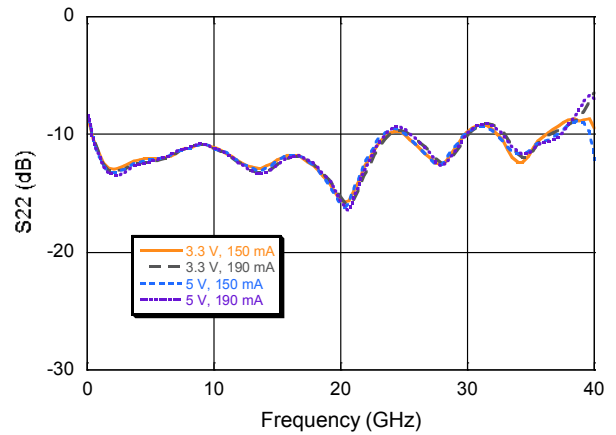
Noise Figure



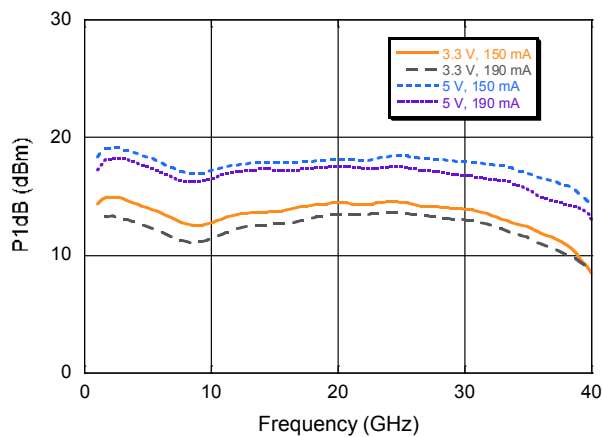
Input Return Loss



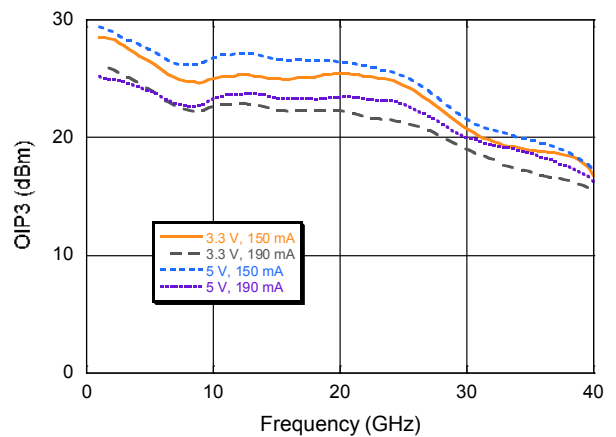
Output Return Loss



Output P1dB

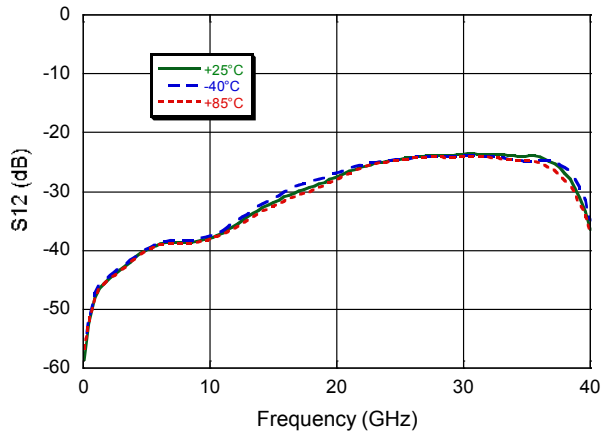


Output IP3

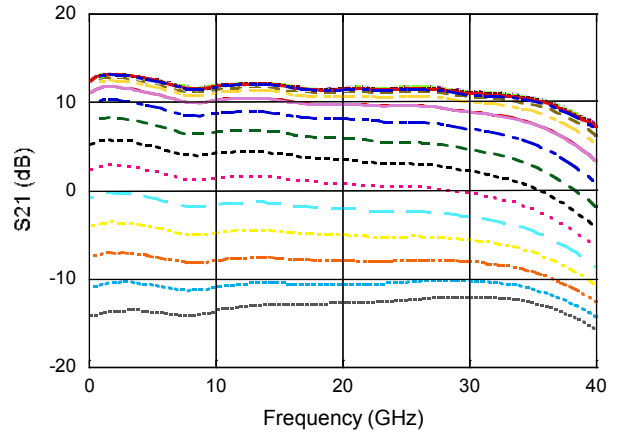


Typical Performance Curves

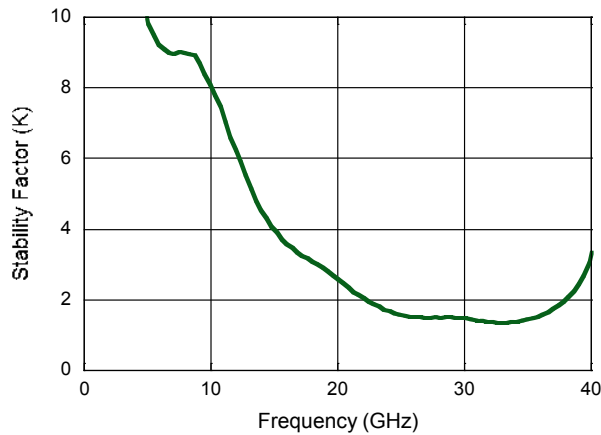
Isolation



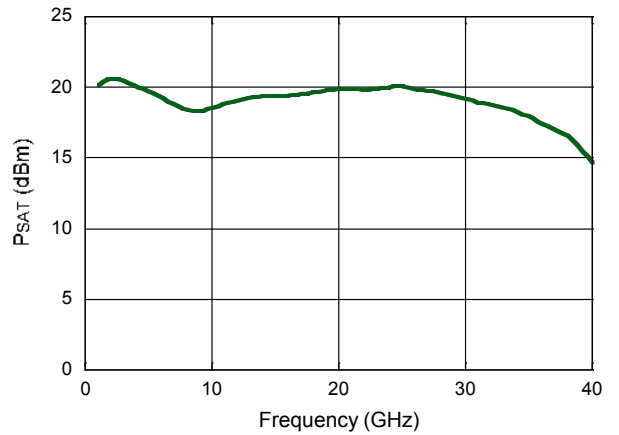
Gain vs. Frequency, $V_c = -0.9$ to 1.1 V



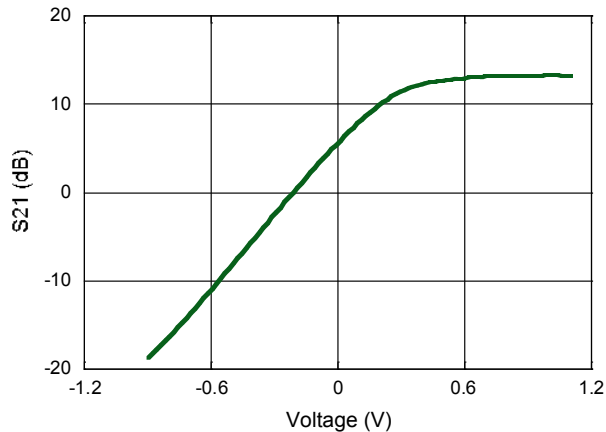
Stability Factor



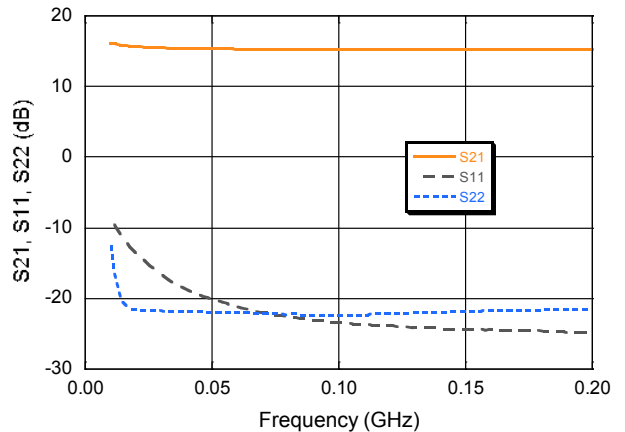
Output Saturated Power



Gain @ 5 GHz vs. Control Voltage

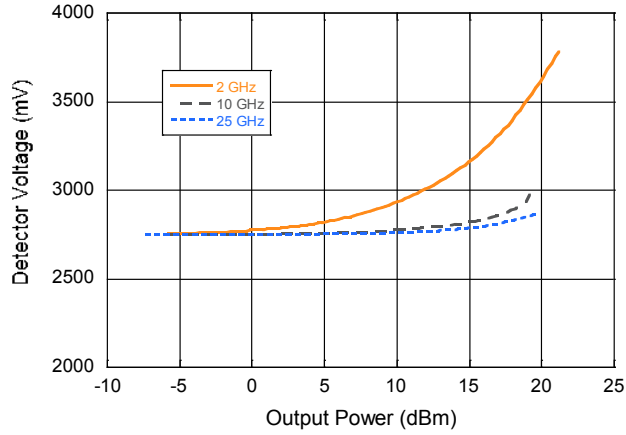


Low Frequency Response

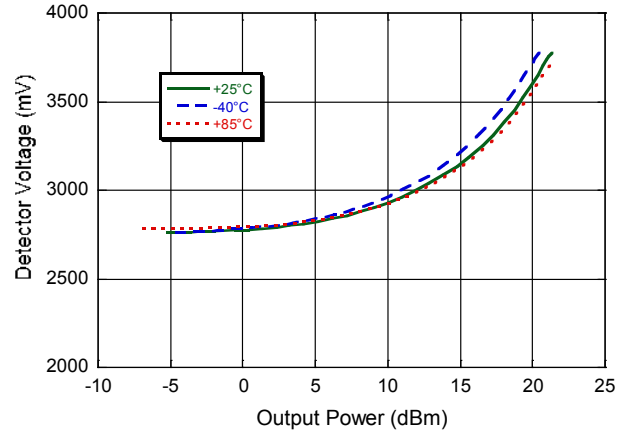


Typical Performance Curves

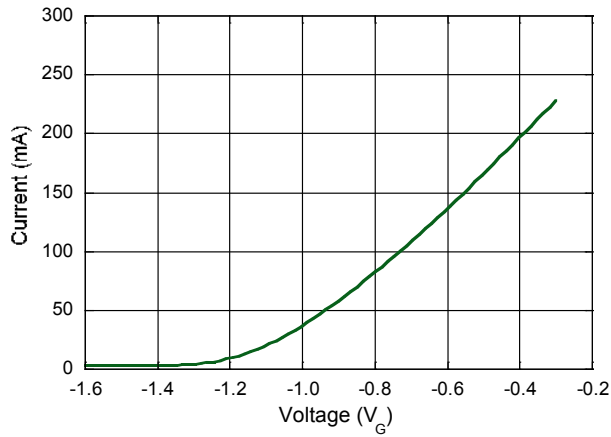
V_{DET} vs. Output Power



V_{DET} vs. Output Power @ 2 GHz



Current vs. Gate Voltage



Current vs. Control Voltage

