

1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



MAAP-011232

Rev. V3

Features

- Gain: 24.5 dB
- P_{-1dB} : 29 dBm
- P_{SAT} : 30 dBm
- PAE at P_{SAT} : 40%
- OIP3: 40 dBm
- Bias Conditions: 9 V, 265 mA
- Fully Matched Output
- Lead-Free 3 mm 16-LD PQFN package
- RoHS* Compliant

Applications

- LMR
- MILCOM
- SATCOM
- Sensors & Telemetry
- Test & Measurement

Description

The MAAP-011232 is a 2-stage power amplifier with gain shut off, operating from 100 MHz to 3 GHz. For operation in the 100 MHz to 1 GHz frequency range no I/O matching is required. Internal DC blocking is provided at the input, while the RF output port is DC coupled through an external bias-tee. Bias current, RF gain and output power are controlled with a gate bias voltage (V_G). Typical current consumption is <300 mA at maximum output power.

The MAAP-011232 is well suited to both power and driver requirements for multiple applications.

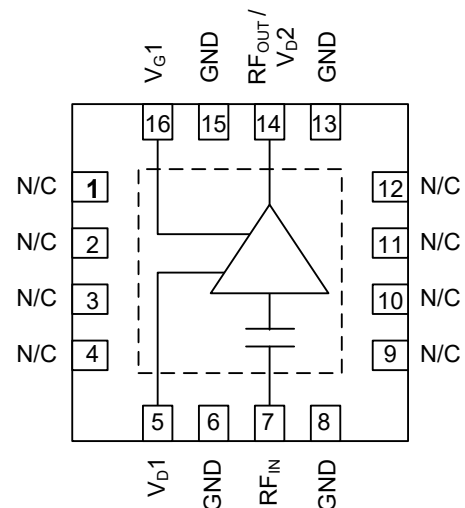
The MAAP-011232 is fabricated using a GaAs D-mode high breakdown process which features full passivation for increased performance and reliability.

Ordering Information^{1,2}

| Part Number | Package |
|--------------------|---------------------|
| MAAP-011232 | Bulk |
| MAAP-011232-TR0500 | 500 Piece Reel |
| MAAP-011232-TR1000 | 1000 Piece Reel |
| MAAP-011232-001SMB | Sample Board Type A |
| MAAP-011232-002SMB | Sample Board Type B |

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration^{3,4}

| Pin # | Function |
|---------------|------------------------------------|
| 1 - 4, 9 - 12 | No Connection |
| 5 | Drain Voltage V_{D1} |
| 6, 8, 13, 15 | Ground |
| 7 | RF Input |
| 14 | RF Output & Drain Voltage V_{D2} |
| 16 | Shut Off Voltage V_G |

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

¹ * Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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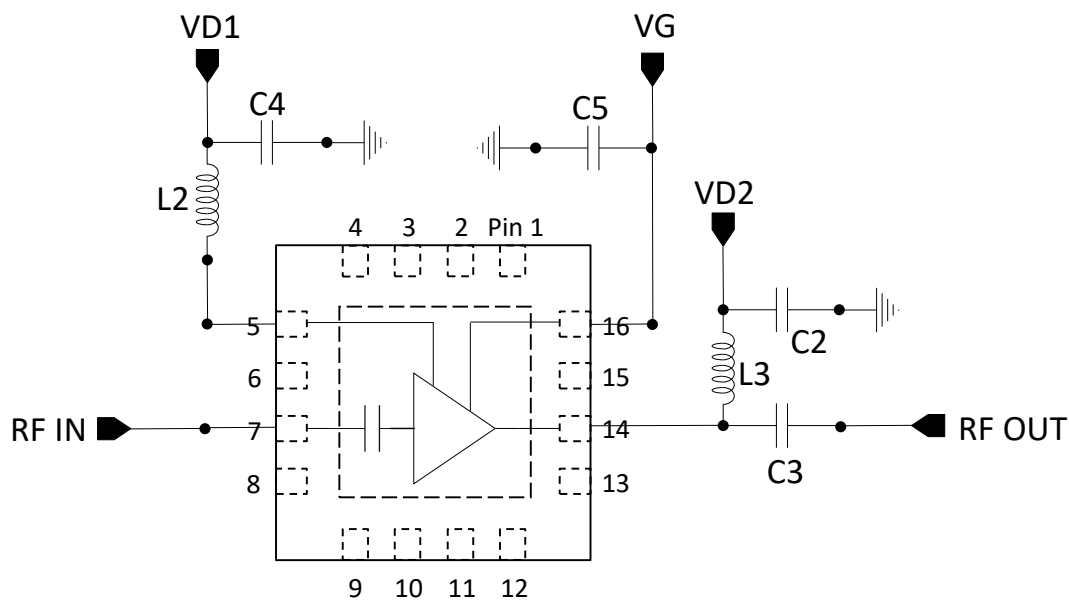
Rev. V3

Electrical Specifications:

Freq. = 1 GHz, $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, V_G pulsed with 1 ms pulse width and 10% duty cycle

| Parameter | Symbol | Test Conditions | Units | Min. | Typ. | Max. |
|---------------------------------|-------------------|-----------------------------|-------|-------|-------|-------|
| Small-Signal Gain | SSG | -10 dBm input drive level | dB | 23 | 24.5 | — |
| Output Power at 1dB compression | $P_{-1\text{dB}}$ | — | dBm | — | 29 | — |
| Saturated Output Power | P_{SAT} | 3 dB Gain compression | dBm | 28.5 | 30 | — |
| Power Added Efficiency | PAE | 3 dB Gain compression | % | 35 | 40 | — |
| Reverse Isolation | S12 | -10 dBm input drive level | dB | — | 50 | — |
| Input Return Loss | IRL | -10 dBm input drive level | dB | — | 8 | — |
| Output Return Loss | ORL | -10 dBm input drive level | dB | — | 12 | — |
| Output Third Order Intercept | OIP3 | -13 dBm/tone, F1-F2 = 6 MHz | dBm | — | 40 | — |
| Gate Bias Voltage | V_G | 3 dB Gain compression | V | -0.75 | -0.55 | -0.30 |
| Quiescent Drain Current | I_{DQ1} | — | mA | — | 65 | — |

Schematic of the Production Test Board



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Rev. V3

Absolute Maximum Ratings^{5,6}

| Parameter | Absolute Maximum |
|-------------------------------------|------------------|
| RF Input Power | 20 dBm |
| Gate Voltage | -4 V to 0 V |
| Drain Voltage VD1 | 10 V |
| Drain Voltage VD2 | 10 V |
| Junction Temperature ^{7,8} | +150°C |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +150°C |

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq +150^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.
8. Junction Temperature ($T_J = T_C + \Theta_{JC} * [(V * I) - (P_{OUT} - P_{IN})]$)
Typical thermal resistance (Θ_{JC}) = 29°C/W.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these (HBM) Class 1A devices.

Operating the MAAP-011232

To operate the device, follow these steps:

1. Set VG to -2 V.
2. Turn on VD1 and VD2 to 5-9 V.
3. Adjust VG to set I_{DQ2} (I_{DQ1} varies).
4. Turn off in reverse order with VG last.

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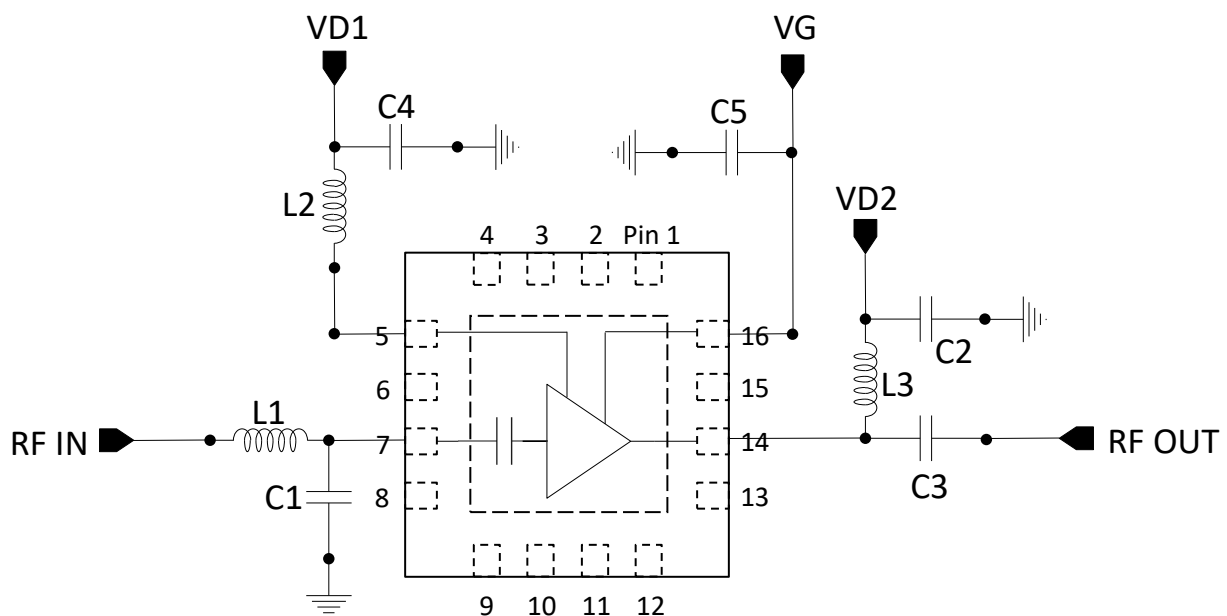
Rev. V3

Typical Electrical Specifications: Test Board A: 100 - 1600 MHz Input Tuning

$T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

| Parameter | Symbol | Test Conditions | Units | Typical Values | | | |
|---------------------------------|-------------------|-----------------------------|-------|----------------|-----|------|------|
| Frequency | F | — | MHz | 100 | 700 | 1100 | 1600 |
| Small-Signal Gain | SSG | -10 dBm input drive level | dB | 16 | 26 | 25 | 21 |
| Output Power at 1dB compression | $P_{-1\text{dB}}$ | 1 dB Gain compression | dBm | 29 | 29 | 30 | 29 |
| Saturated Output Power | P_{SAT} | 3 dB Gain compression | dBm | 30 | 30 | 30.5 | 30 |
| Power Added Efficiency | PAE | 3 dB Gain compression | % | 32 | 40 | 45 | 37 |
| Reverse Isolation | S12 | -10 dBm input drive level | dB | 79 | 56 | 55 | 53 |
| Input Return Loss | IRL | -10 dBm input drive level | dB | 4 | 17 | 28 | 7 |
| Output Return Loss | ORL | -10 dBm input drive level | dB | 17 | 16 | 15 | 14 |
| Output Third Order Intercept | OIP3 | -13 dBm/tone, F1-F2 = 6 MHz | dBm | 41 | 44 | 43 | 40 |
| Gate Bias Voltage | V_G | — | V | -0.55 | | | |
| Quiescent Drain Current | I_{DQ1} | — | mA | 65 | | | |

Schematic of the Test Board Type A: 100-1600 MHz Input Tuning



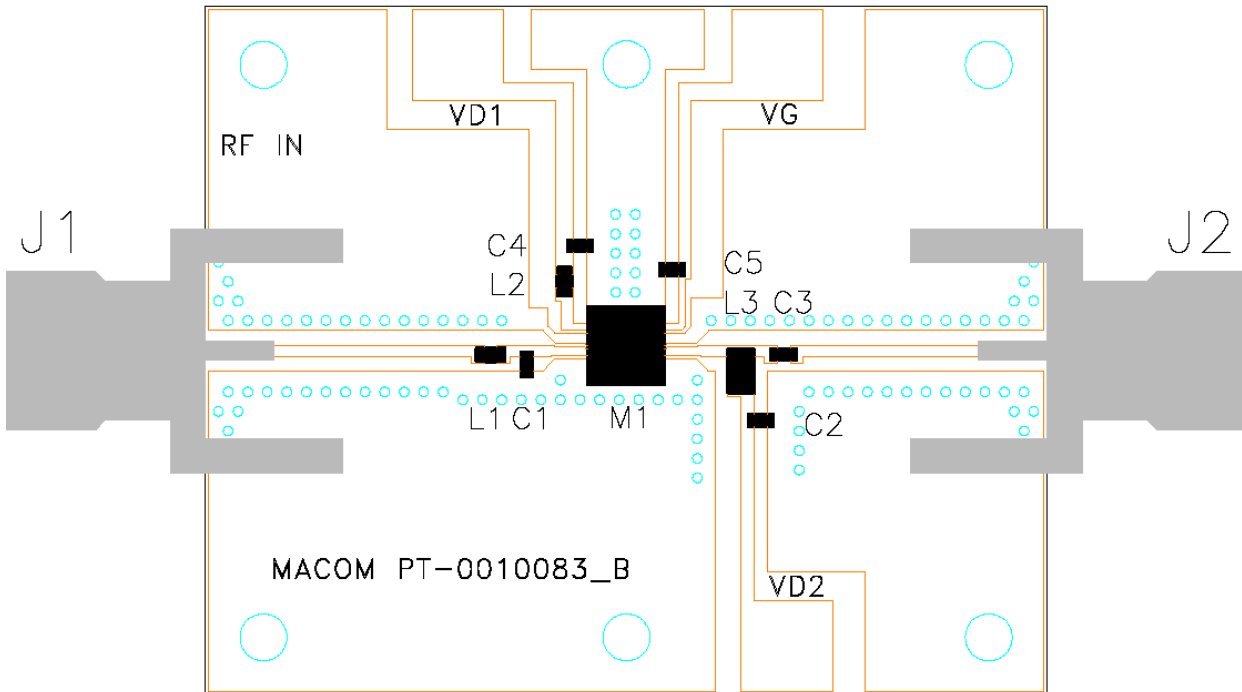
1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



MAAP-011232
Rev. V3

Test Board Type A: 100 - 1600 MHz Input Tuning



PCB Material: R4003C LoPro, 0.008" THICK, Solid Copper filled vias

Parts List

| Part | Description | Value | Size | Manufacturer |
|--------|---------------|-------------|------|----------------------|
| C1 | Capacitor | 0.6 pF | 0402 | Murata |
| C2, C4 | Capacitor | 0.1 μ F | 0402 | Murata |
| C3 | Capacitor | 100 pF | 0402 | Murata |
| C5 | Capacitor | 10 nF | 0402 | Murata |
| L1 | Inductor | 7.5 nH | 0402 | 0402CS, Coilcraft |
| L2 | Inductor | 560 nH | 0402 | 0402AF, Coilcraft |
| L3 | Inductor | 110 nH | 0603 | 0603HP, Coilcraft |
| J1, J2 | SMA Connector | — | — | 142-0701-881 Emerson |

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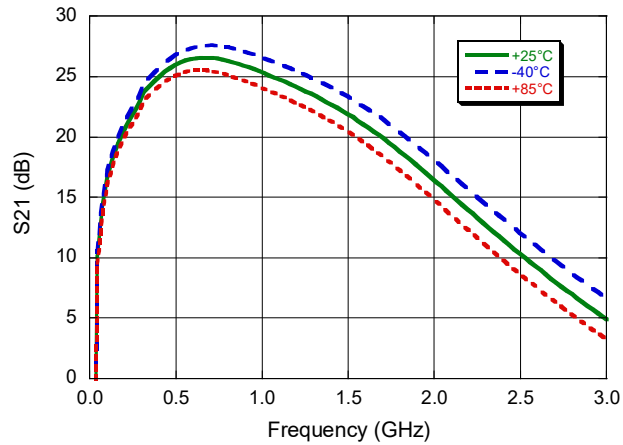
MAAP-011232

Rev. V3

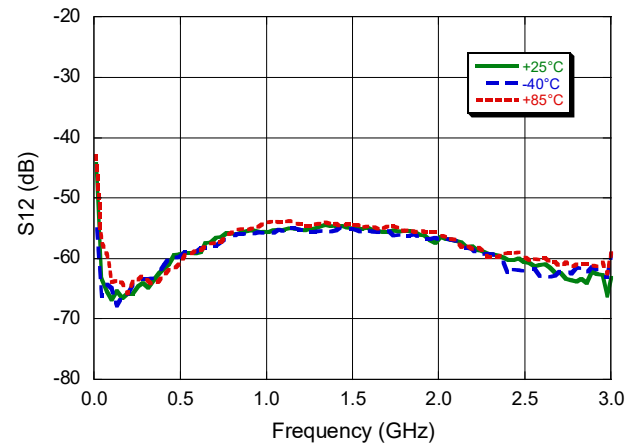
Test Board Type A: S-parameters over Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

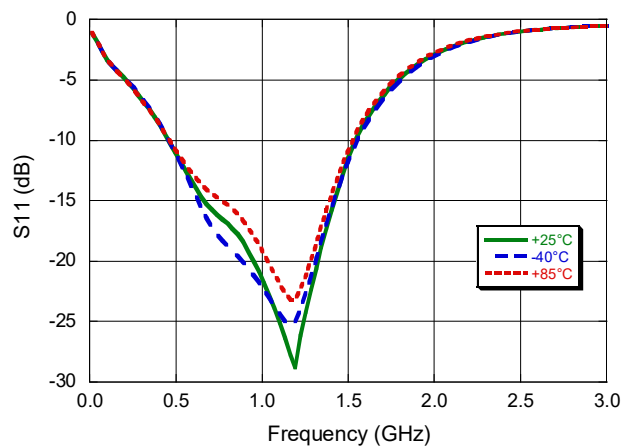
Insertion Gain vs. Frequency



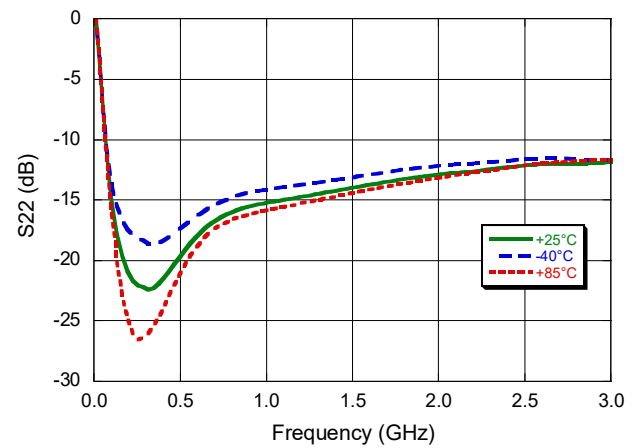
Isolation vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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0.1 - 3.0 GHz



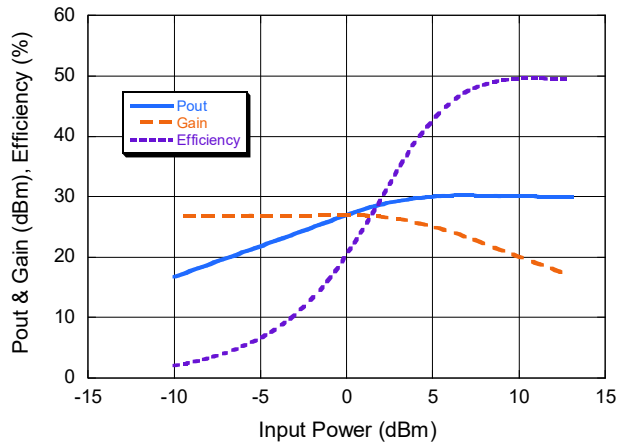
MAAP-011232

Rev. V3

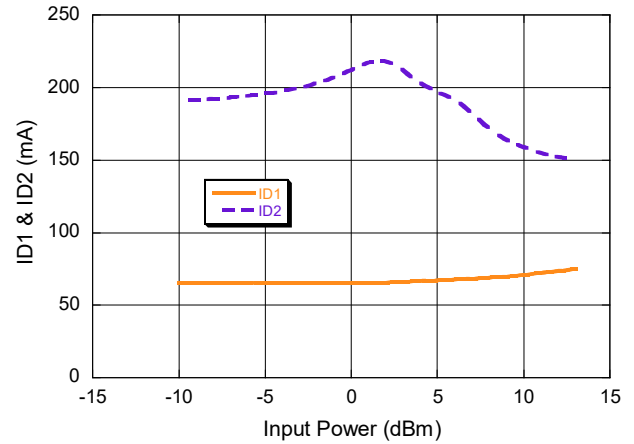
Test Board Type A - Power Performance @ Room Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

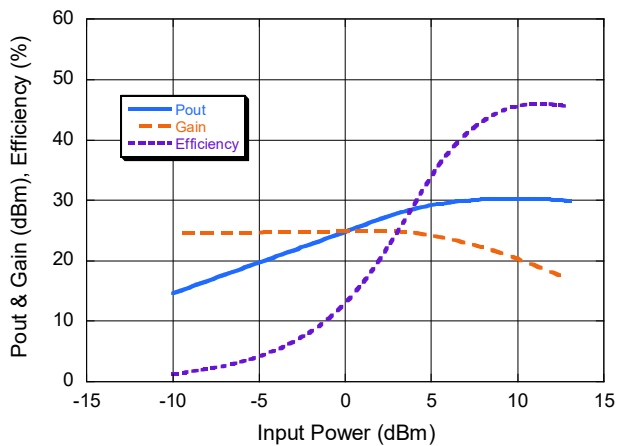
P_{OUT} , Gain and Efficiency vs. P_{IN} @ 700 MHz



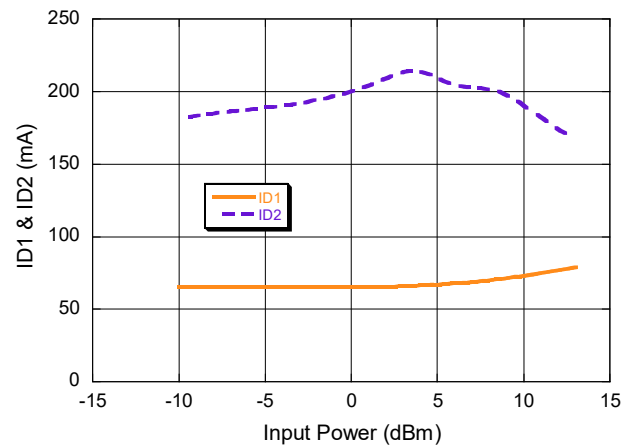
Bias Current vs. P_{IN} @ 700 MHz



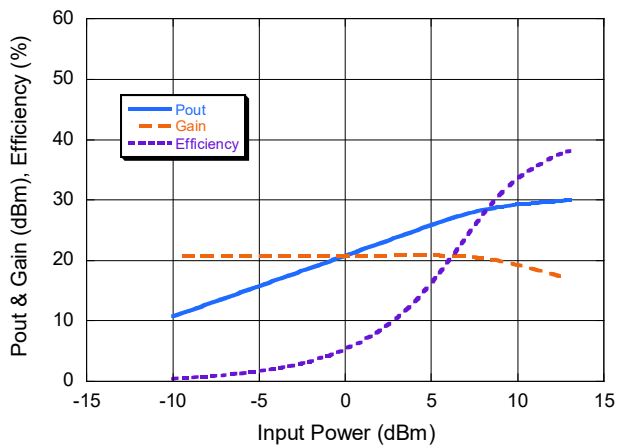
P_{OUT} , Gain and Efficiency vs. P_{IN} @ 1100 MHz



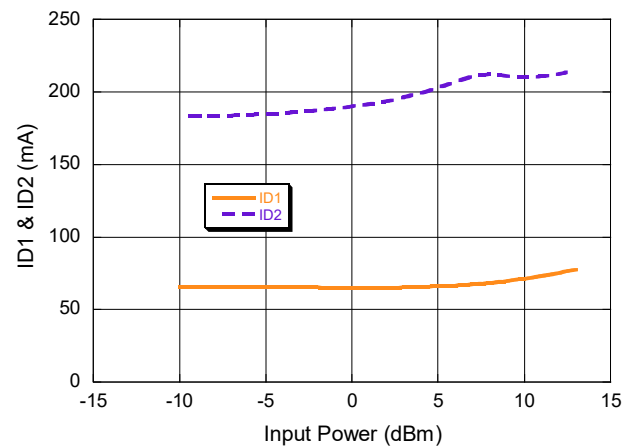
Bias Current vs. P_{IN} @ 1100 MHz



P_{OUT} , Gain and Efficiency vs. P_{IN} @ 1600 MHz



Bias Current vs. P_{IN} @ 1600 MHz



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0.1 - 3.0 GHz



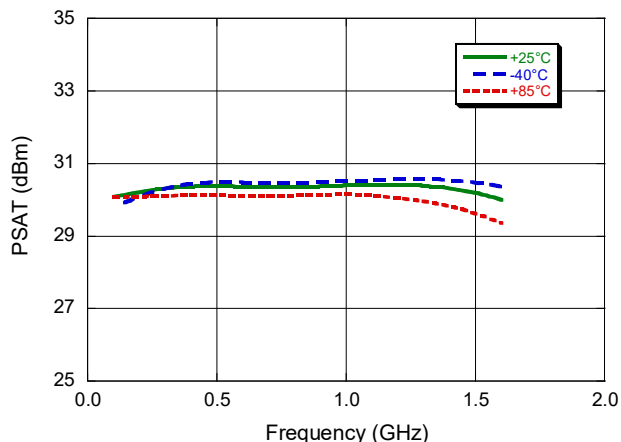
MAAP-011232

Rev. V3

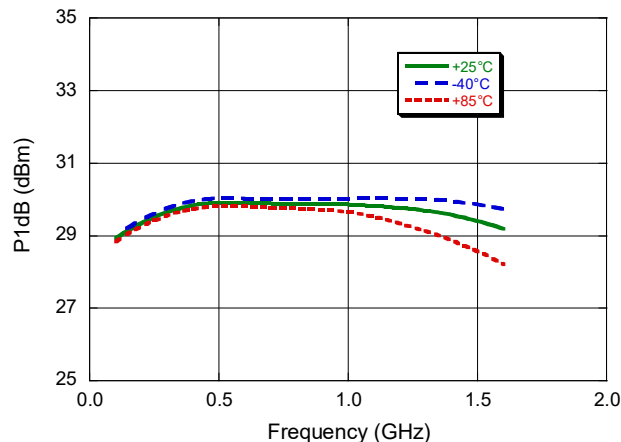
Test Board Type A - Power Performance over Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

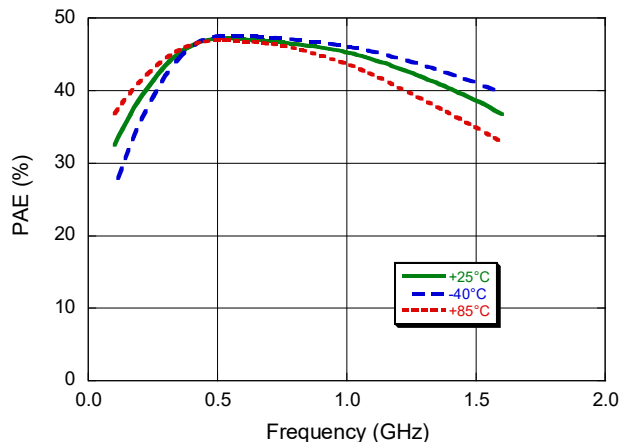
Saturated Power vs. Frequency



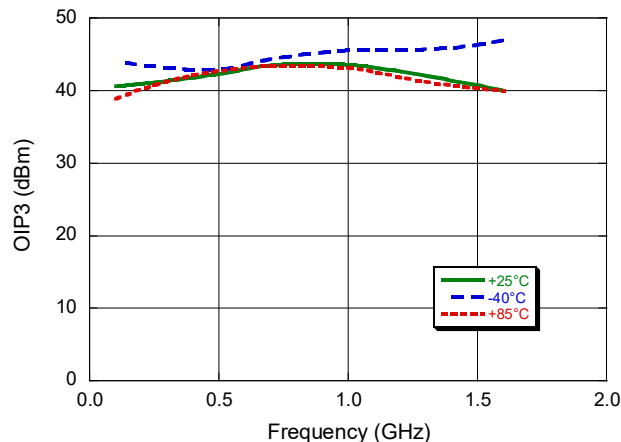
P1dB vs. Frequency



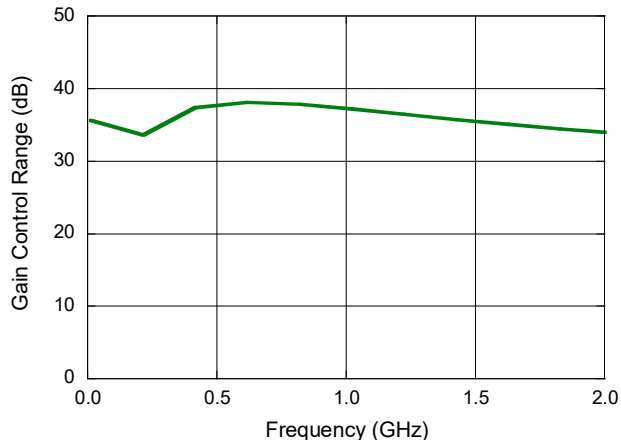
PAE vs. Frequency



Output IP3 vs. Frequency



Gain Control Range vs. Frequency



$P_{IN} = -13\text{ dBm/ tone}$, tone separation = 6 MHz

Measured for V_G between -0.4 V and -1.4 V

1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



MAAP-011232

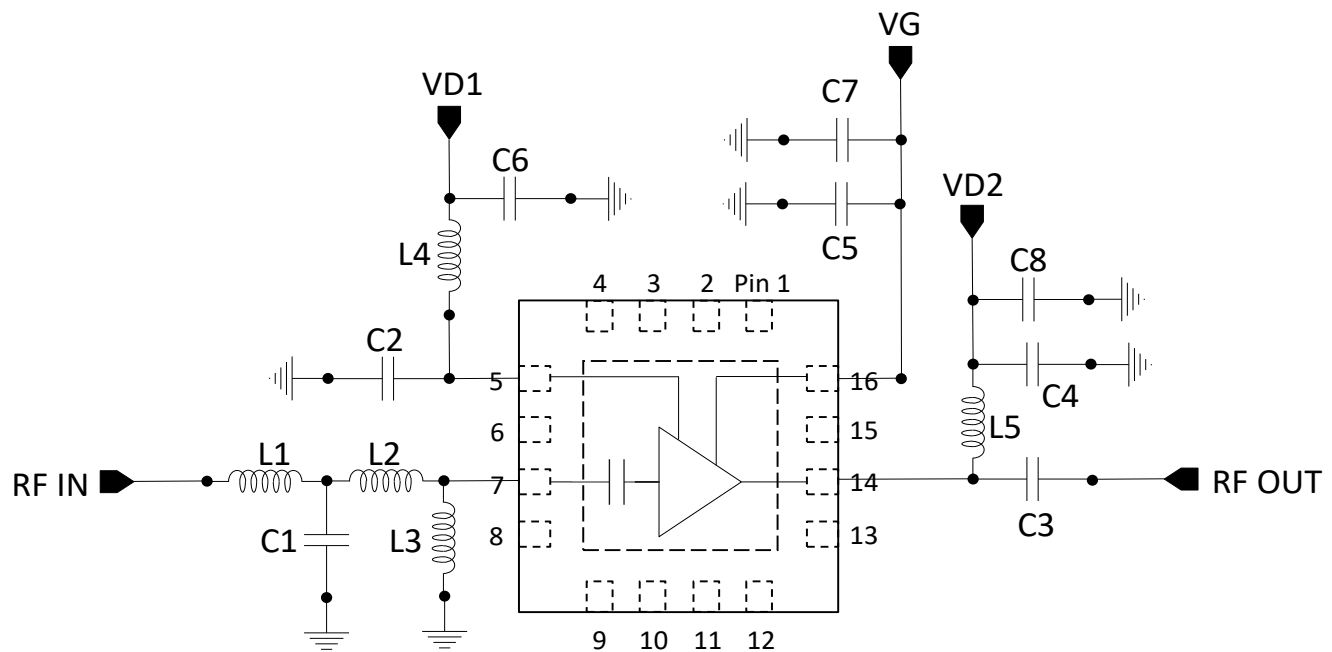
Rev. V3

Typical Electrical Specifications: Test Board B: 1600 - 3000 MHz Input Tuning

$T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

| Parameter | Symbol | Test Conditions | Units | Typical Values | | |
|--------------------------------|-------------------|-----------------------------|-------|----------------|------|------|
| Frequency | F | — | MHz | 2000 | 2500 | 3000 |
| Small-Signal Gain | SSG | -10 dBm input drive level | dB | 24 | 24 | 17 |
| Output Power @ 1dB compression | $P_{-1\text{dB}}$ | 1 dB Gain compression | dBm | 29 | 29 | 30 |
| Saturated Output Power | P_{SAT} | 3 dB Gain compression | dBm | 30 | 30 | 30.5 |
| Power Added Efficiency | PAE | 3 dB Gain compression | % | 37 | 40.5 | 37 |
| Reverse Isolation | S12 | -10 dBm input drive level | dB | 51 | 52 | 54 |
| Input Return Loss | IRL | -10 dBm input drive level | dB | 9 | 11 | 2 |
| Output Return Loss | ORL | -10 dBm input drive level | dB | 10 | 9 | 9 |
| Output Third Order Intercept | OIP3 | -13 dBm/tone, F1-F2 = 6 MHz | dBm | 40 | 42 | 40 |
| Gate Bias Voltage | V_G | — | V | -0.55 | | |
| Quiescent Drain Current | I_{DQ1} | — | mA | 65 | | |

Schematic of the Test Board Type B: 1600-3000 MHz Input Tuning



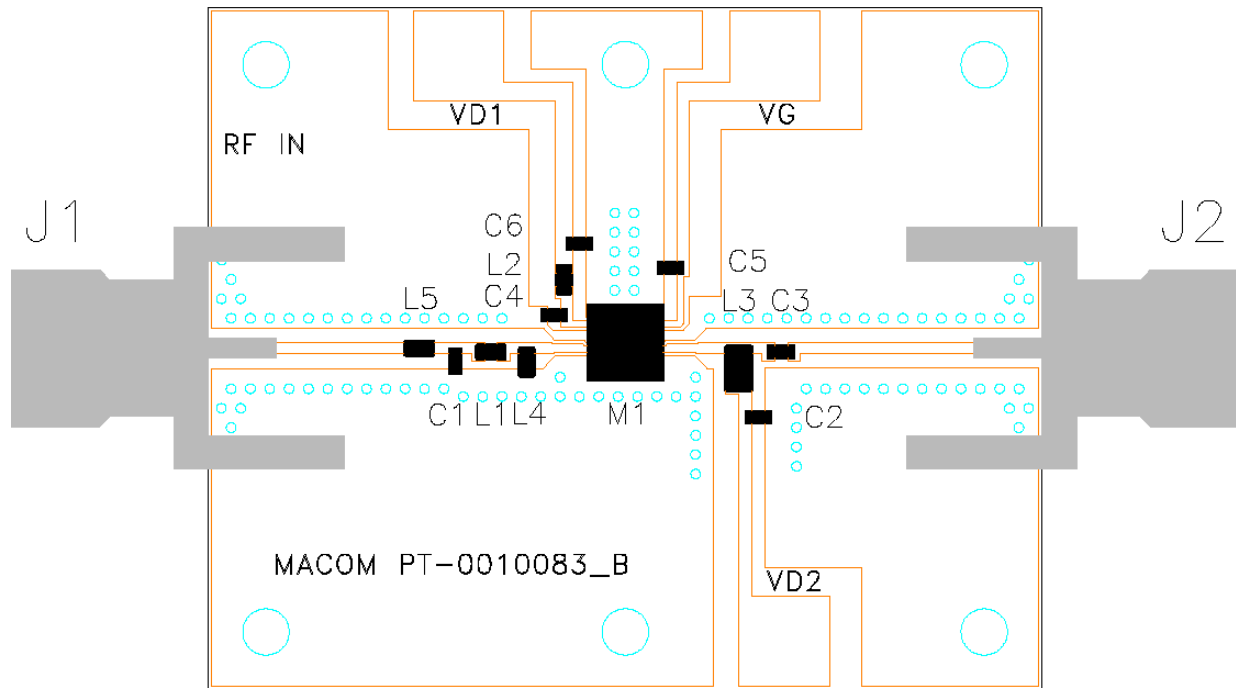
1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



MAAP-011232
Rev. V3

Test Board Type B: 1600 - 3000 MHz Input Tuning



PCB Material: R4003C LoPro, 0.008" THICK, Solid Copper filled vias

Parts List

| Part | Description | Value | Size | Manufacturer |
|--------|---------------|-------------|------|----------------------|
| C1 | Capacitor | 1.2 pF | 0402 | PPI |
| C4, C5 | Capacitor | 10 nF | 0402 | Murata |
| C2, C6 | Capacitor | 0.1 μ F | 0402 | Murata |
| C3 | Capacitor | 100 pF | 0402 | Murata |
| L1 | Inductor | 5.6 nH | 0402 | 0402HP, Coilcraft |
| L2 | Inductor | 560 nH | 0402 | 0402AF, Coilcraft |
| L3 | Inductor | 110 nH | 0603 | 0603HP, Coilcraft |
| L4 | Inductor | 10 nH | 0402 | 0402HP, Coilcraft |
| L5 | Inductor | 3.3 nH | 0402 | 0402HP, Coilcraft |
| J1, J2 | SMA Connector | — | — | 142-0701-881 Emerson |

1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



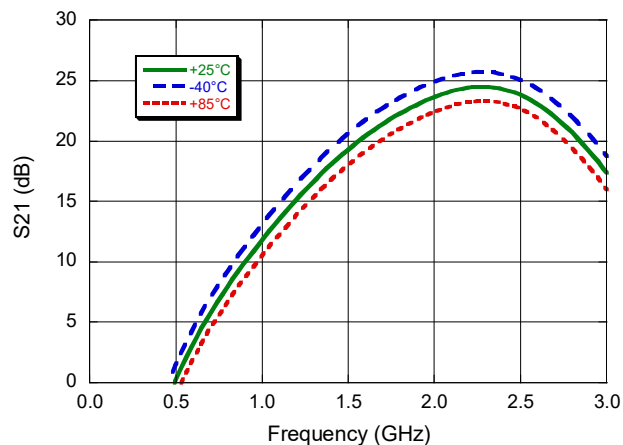
MAAP-011232

Rev. V3

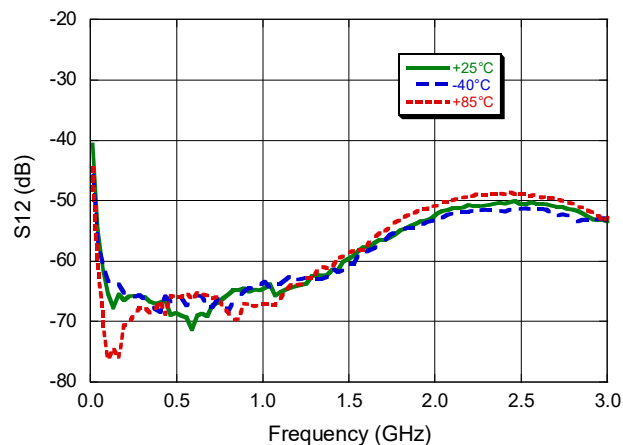
Test Board Type B: S-parameters over Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

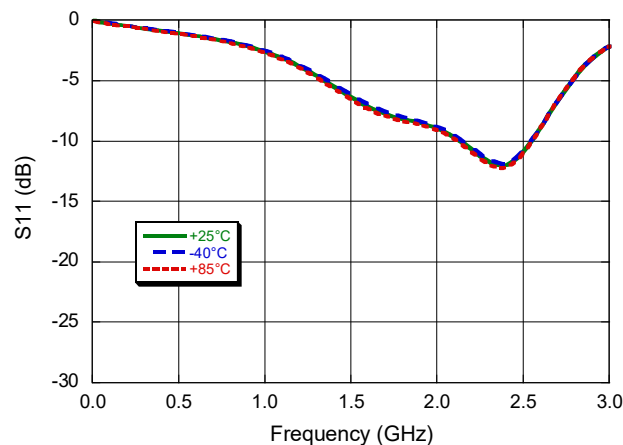
Insertion Gain vs. Frequency



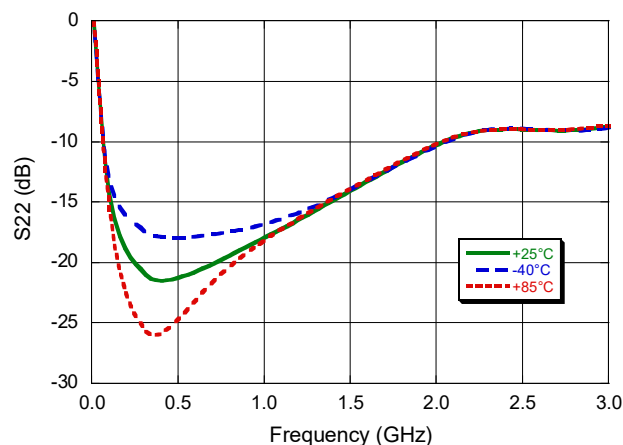
Isolation vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



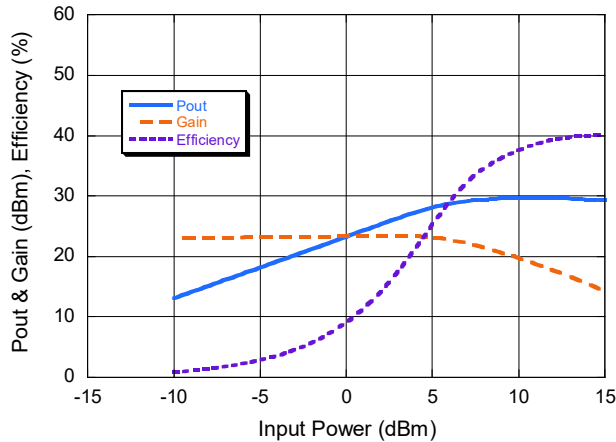
MAAP-011232

Rev. V3

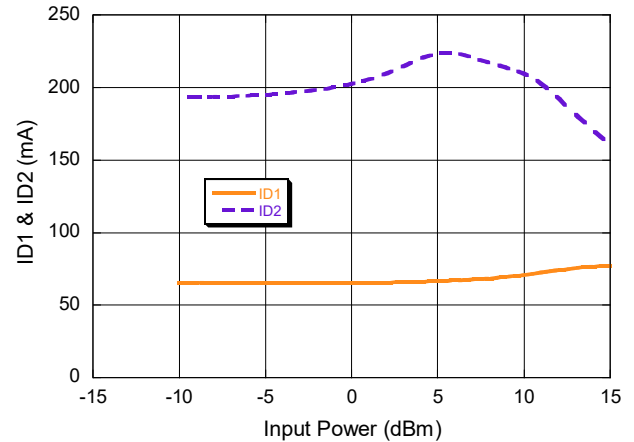
Test Board Type B - Power Performance @ Room Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

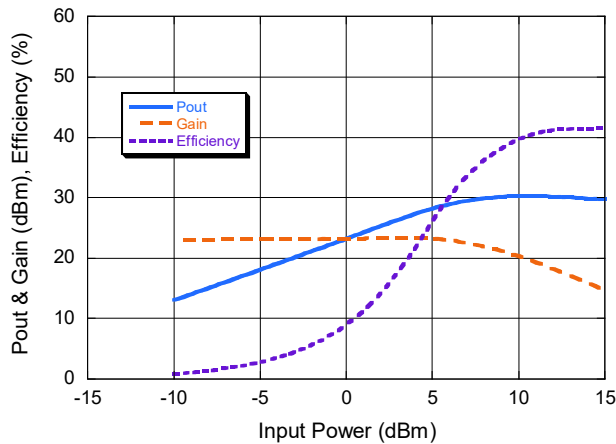
P_{OUT} , Gain and Efficiency vs. P_{IN} @ 2 GHz



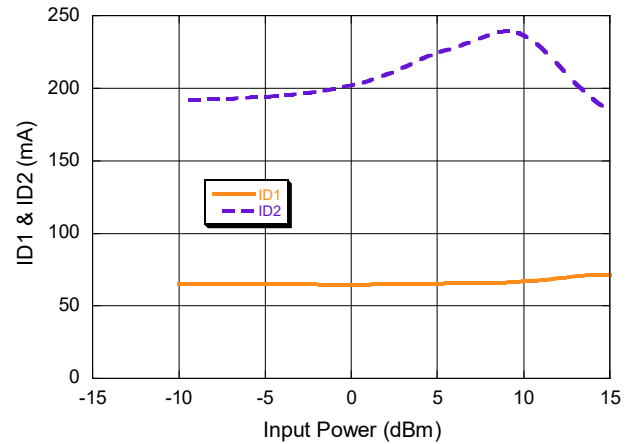
Bias Current vs. P_{IN} @ 2 GHz



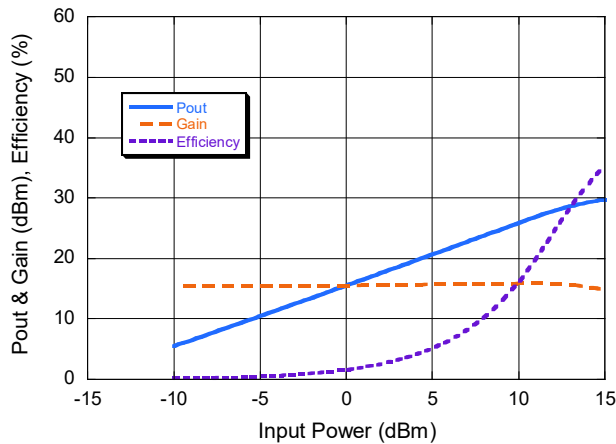
P_{OUT} , Gain and Efficiency vs. P_{IN} @ 2.5 GHz



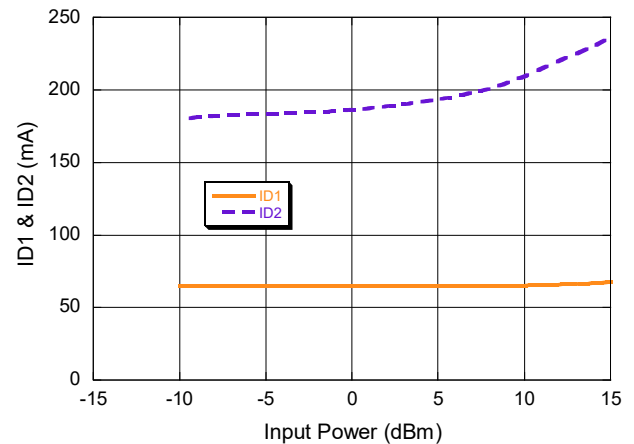
Bias Current vs. P_{IN} @ 2.5 GHz



P_{OUT} , Gain and Efficiency vs. P_{IN} @ 3 GHz



Bias Current vs. P_{IN} @ 3 GHz



1 W Driver Amplifier with VG Enable

0.1 - 3.0 GHz



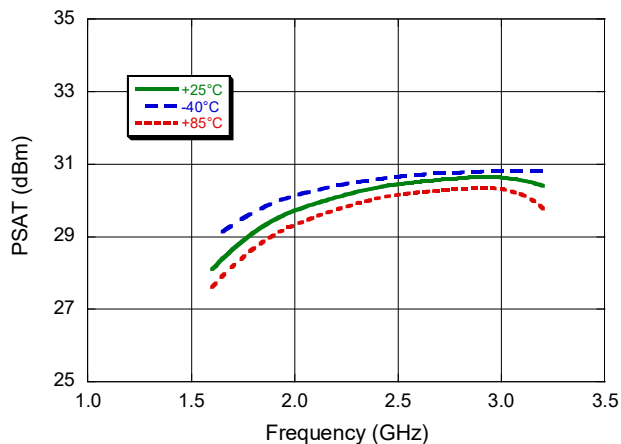
MAAP-011232

Rev. V3

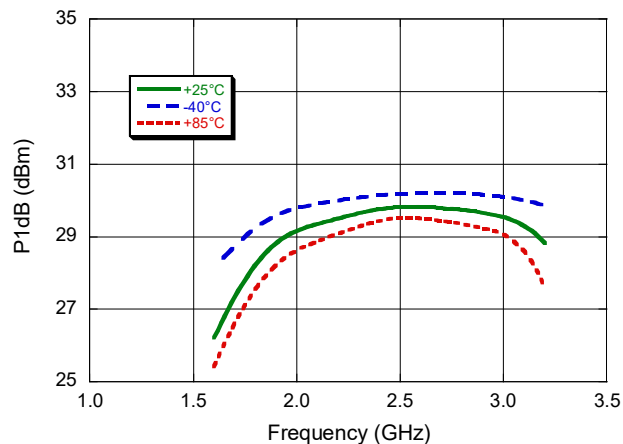
Test Board Type B - Power Performance over Temperature

Test Conditions: $T_A = +25^\circ\text{C}$, $V_{D1} = V_{D2} = 9\text{ V}$, $I_{DQ1} = 65\text{ mA}$, $I_{DQ2} = 200\text{ mA}$, $Z_0 = 50\ \Omega$, CW

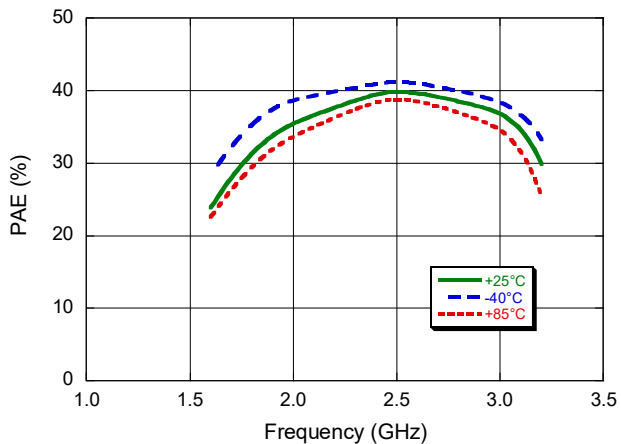
Saturated Power vs. Frequency



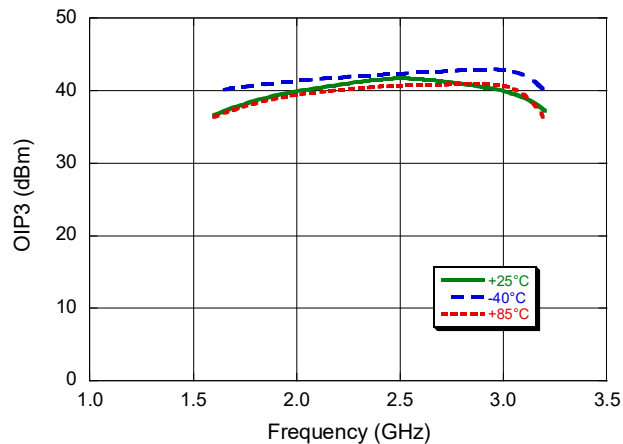
P1dB vs. Frequency



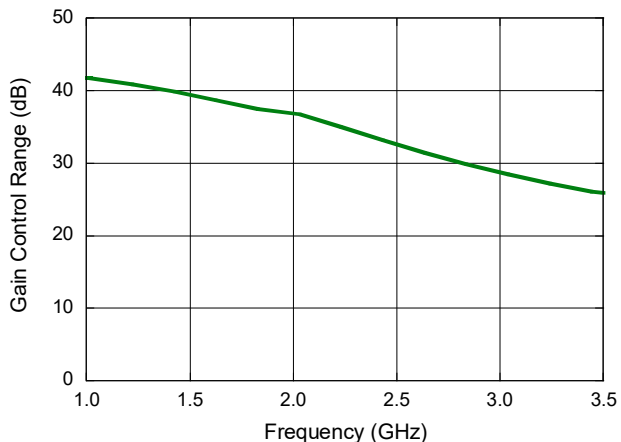
PAE vs. Frequency



Output IP3 vs. Frequency



Gain Control Range vs. Frequency



$P_{IN} = -13\text{ dBm/tone}$, tone separation = 6 MHz

Measured for V_G between -0.4 V and -1.4 V

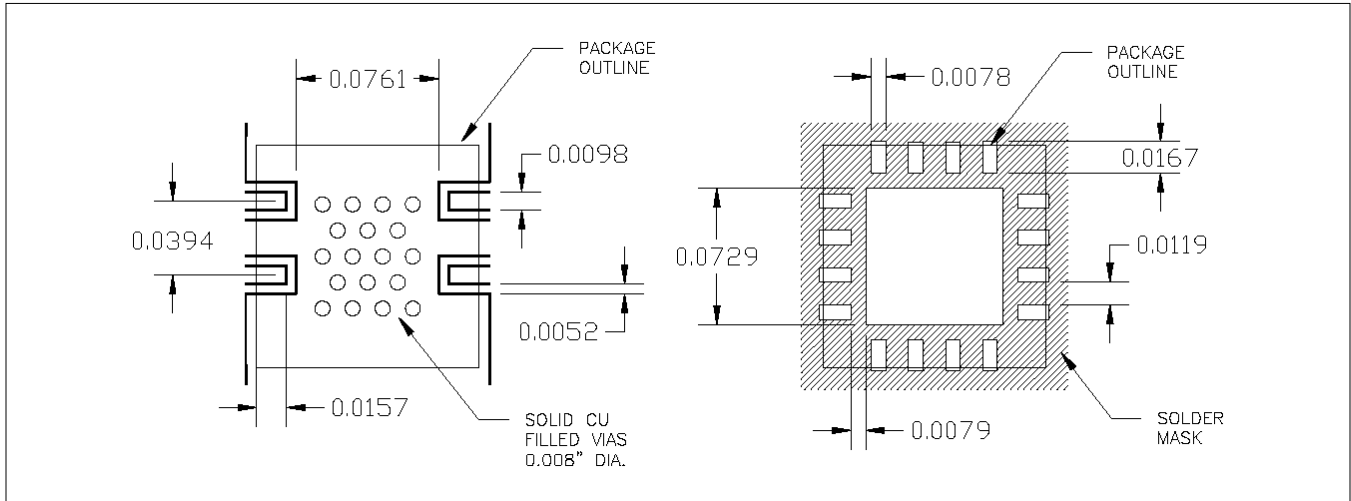
1 W Driver Amplifier with VG Enable

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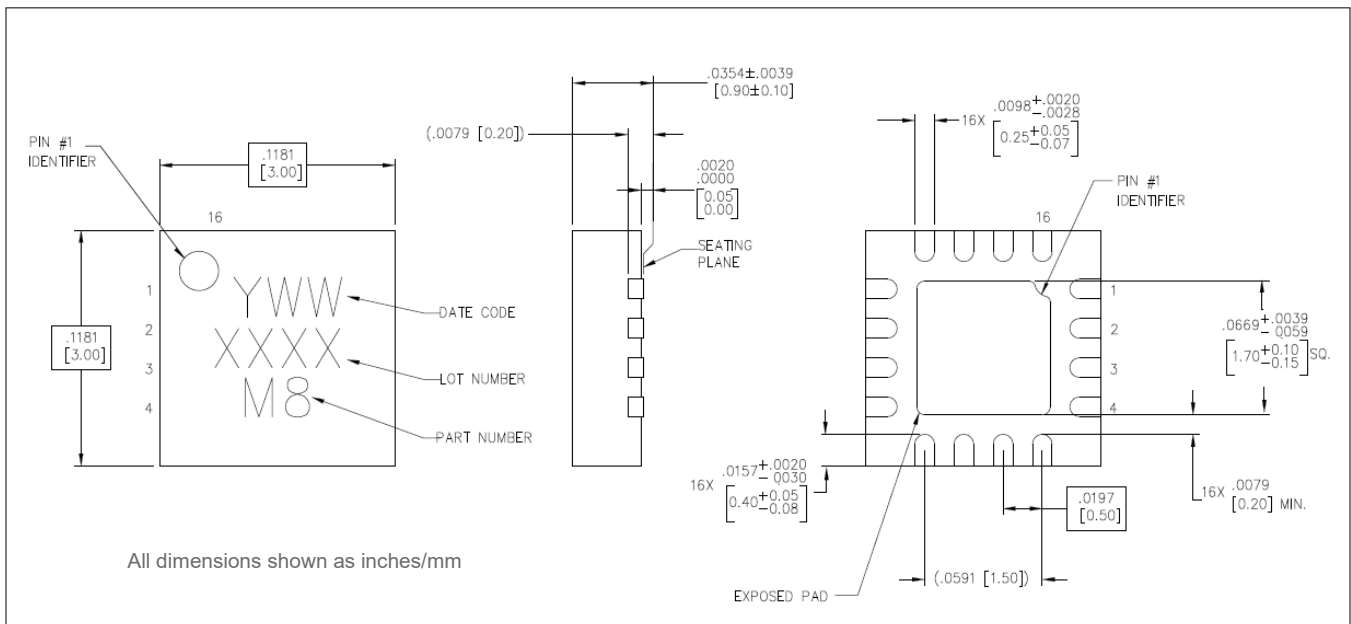
MAAP-011232
Rev. V3

Recommended Landing Pattern^{9,10}



9. All dimensions are in inches.
10. Landing pattern indicates solder mask opening. Cu-filled via-holes under the ground are used for optimal thermal performance. Recommended pattern: 8-mil diameter, 8-mil spacing.

Lead-Free 3 mm 16-Lead PQFN[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.