MAAP-015024-DIE

Power Amplifier, 8 W
14.5 - 17.5 GHz

Rev. V6

Features

- 8 W Power Amplifier
- 20 dB Small Signal Gain
- 39 dBm Saturated Pulsed Output Power
- Dual Sided Bias Architecture
- 100% On-wafer DC & RF Power Tested
- 100% Visual Inspection to MIL-STD-833
- Bare Die

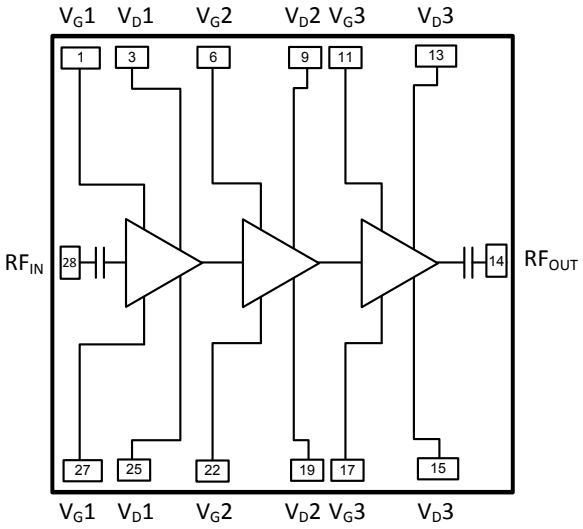
Description

The MAAP-015024-DIE three stage 14.5 - 17.5 GHz GaAs MMIC power amplifier has a saturated pulsed output power of 39 dBm and a small signal gain of 20 dB. The power amplifier must be biased directly on both sides of the die.

This MMIC uses MACOM's GaAs pHEMT device technology and is based upon optical gate lithography to ensure high repeatability and uniformity. The chip has surface passivation for protection and backside via holes and gold metallization to allow a conductive epoxy die attach process.

This device is well suited for communication and radar applications.

Functional Schematic



Pad Configuration

Pad #	Function	Description
1	V_G1	1st Stage Gate Voltage
3	V_D1	1st Stage Drain Voltage
6	V_G2	2nd Stage Gate Voltage
9	V_D2	2nd Stage Drain Voltage
11	V_G3	3rd Stage Gate Voltage
13	V_D3	3rd Stage Drain Voltage
14	RF_{OUT}	RF Output
15	V_D3	3rd Stage Drain Voltage
17	V_G3	3rd Stage Gate Voltage
19	V_D2	2nd Stage Drain Voltage
22	V_G2	2nd Stage Gate Voltage
25	V_D1	1ST Stage Drain Voltage
27	V_G1	1st Stage Gate Voltage
28	RF_{IN}	RF Input

Ordering Information

Part Number	Package
MAAP-015024-DIE	Die in vacuum release gel pack
MAAP-015024-DIER	Diced Wafer on Grip Ring
MAAP-015024-DIEEV1	Direct gate bias sample board
MAAP-015024-DIEEV2	On chip gate bias sample board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Power Amplifier, 8 W
14.5 - 17.5 GHz

Electrical Specifications:

Freq. = 14.5 - 17.5 GHz, T_A = +25°C, Duty Cycle = 5%, P_{IN} = 23 dBm

Parameter	Units	Min.	Typ.	Max.
Gain	dB	—	21.0	—
Gain Flatness	dB	—	+/-1.0	—
Input Return Loss	dB	—	10.0	—
Output Return Loss	dB	—	6.0	—
Reverse Isolation	dB	—	50.0	—
Saturated Output Power 14.5 - 15.0 GHz 15.0 - 17.5 GHz	dBm	 35.0 37.5	 37.5 39.0	—
Drain Bias Voltage	V	—	8.0	—
Gate Bias Voltage	V	—	-0.9	—
Current	A	—	5.0	7.0

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Input Power	30 dBm
Gate Voltage	-0.5 V < V_G < -2 V
Supply Voltage	8.5 Vdc
Supply Current	7.5 A
Storage Temperature	-65°C to +165°C
Operating Temperature	-40°C to +85°C
Junction Temperature[3]	+175°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.
3. Operating at nominal conditions with $T_J \leq$ +175°C will ensure MTTF > 1 x 10^6 hours.

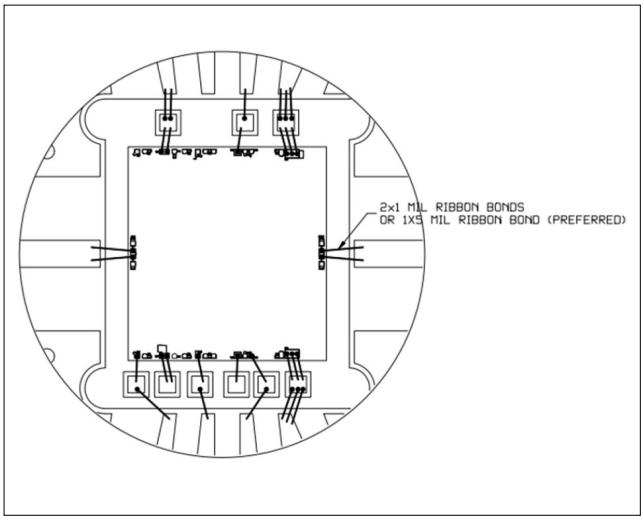
Handling Procedures

Please observe the following precautions to avoid damage:

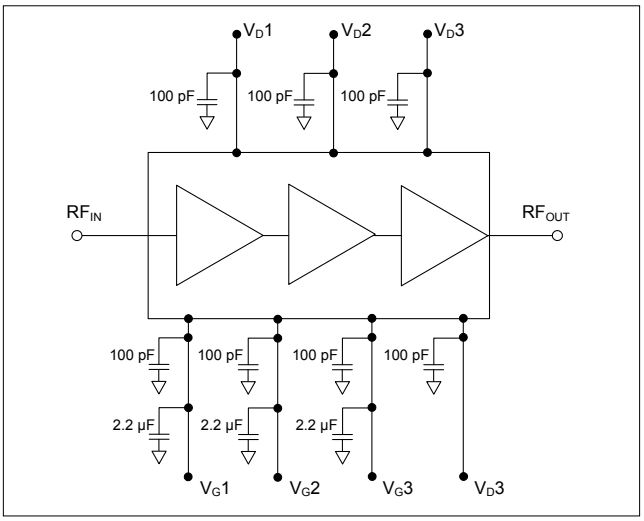
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

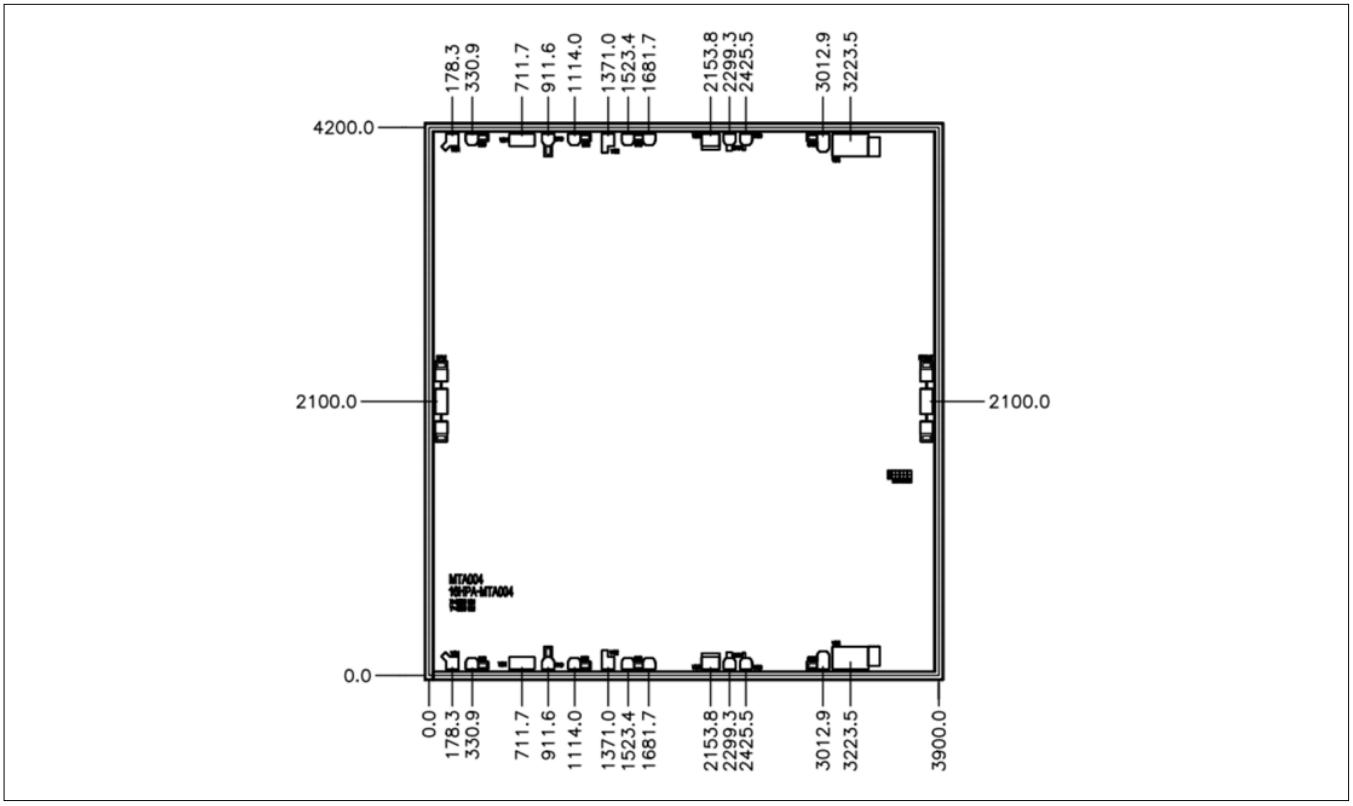
Bonding Diagram



Schematic

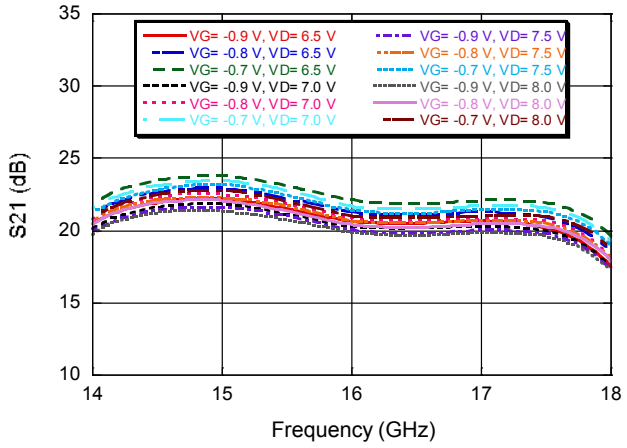


MMIC Bare Die

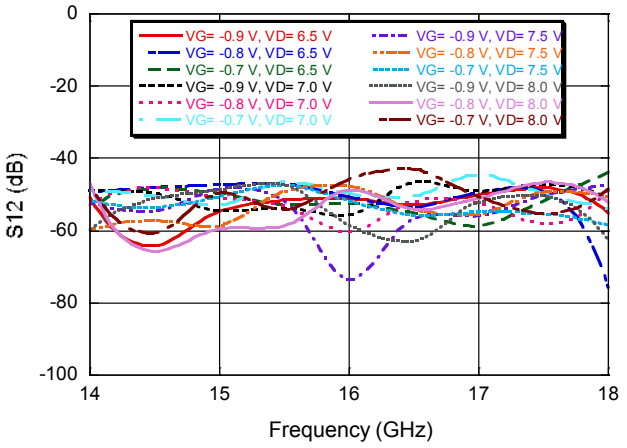


Typical Performance Curves

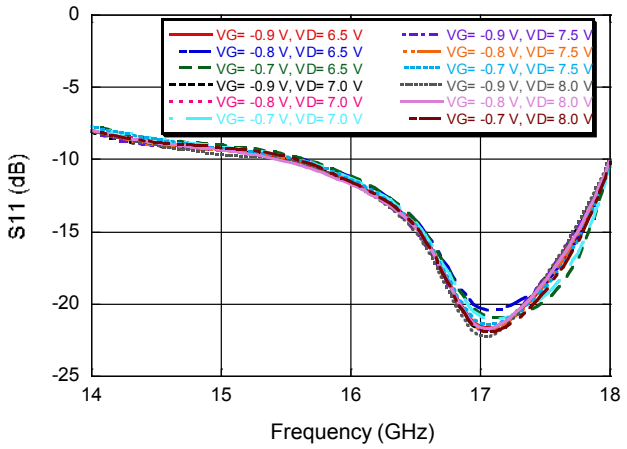
Gain vs. Frequency



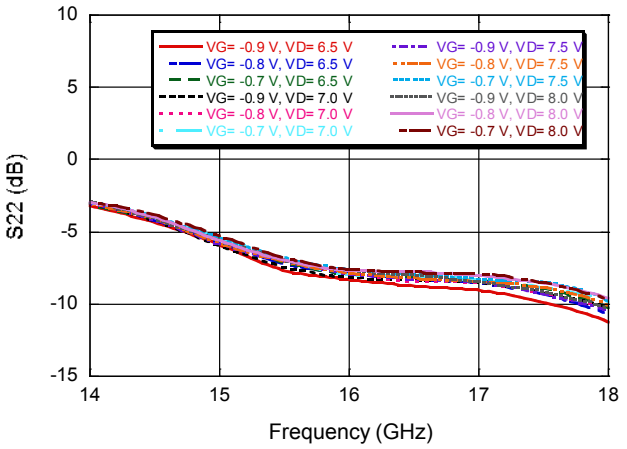
Reverse Isolation vs. Frequency



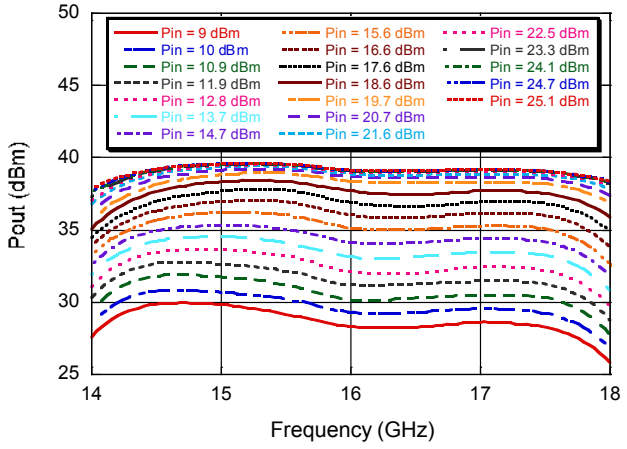
Input Return Loss vs. Frequency



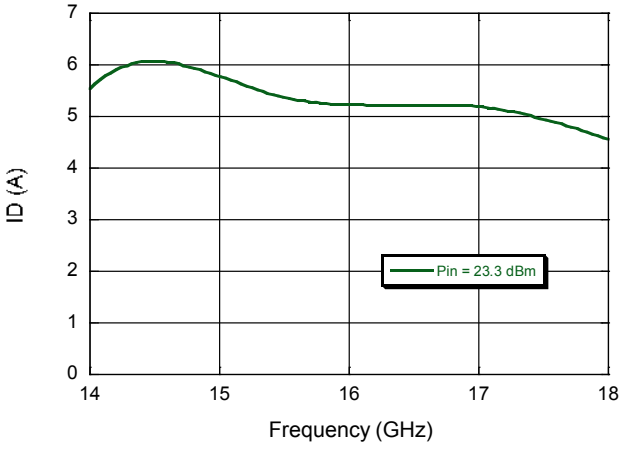
Output Return Loss vs. Frequency



Output Power vs. Frequency, V_G = -0.9 V, V_D = 8 V

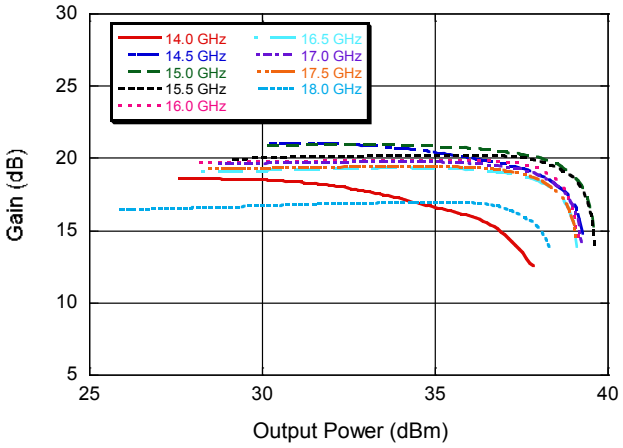


Current vs. Frequency, V_G = -0.9 V, V_D = 8 V

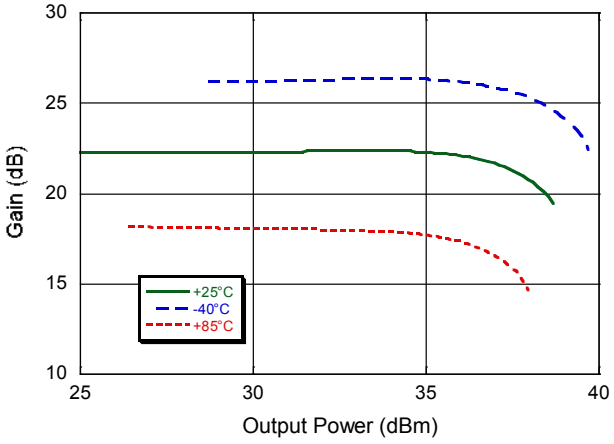


Typical Performance Curves

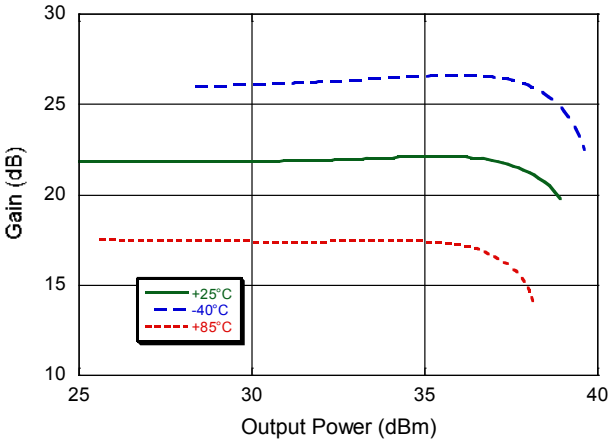
Gain vs. Output Power



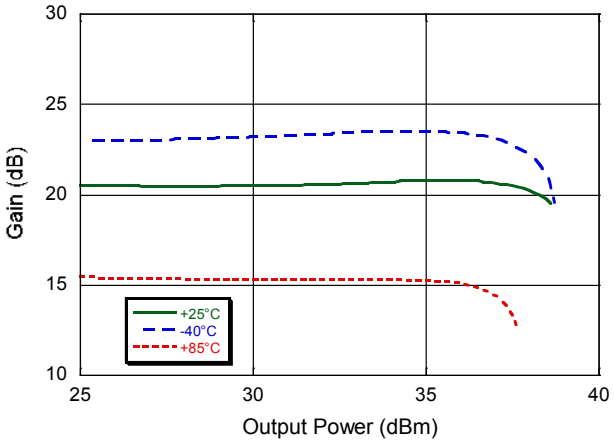
Gain @ 14.5 GHz vs. Output Power



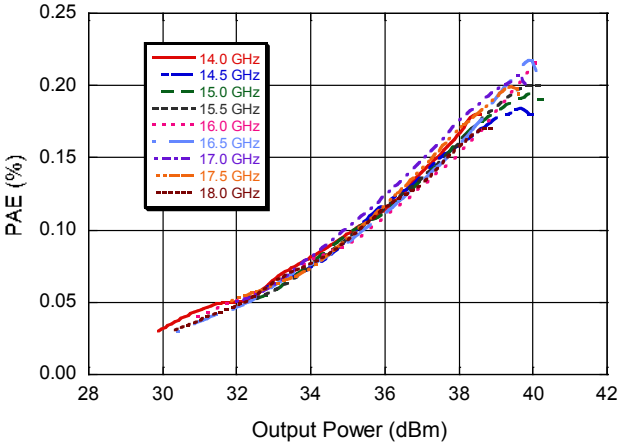
Gain @ 15.0 GHz vs. Output Power



Gain @ 15.5 GHz vs. Output Power



PAE vs. Output Power



Applications Section

Application Notes

Note 1 - Biasing
The MAAP-015024-DIE is biased directly through the gates (V_G1, V_G2 and V_G3) of the power amplifier (PA). The V_G should be biased on one side of the PA. The V_D3 must be biased on both sides of the PA. The V_D1 and V_D2 should only be biased on one side of the PA. The PA is biased typically with V_G = -0.9 V and V_D = 8 V.

The bias (V_G1, V_G2, V_G3) should always be applied before the drain voltage (V_D1, V_D2, V_+3) is applied and when switching off the PA the drain voltage must be switched off first before the gate voltage. It is strongly recommended to pulse the drain voltage of the PA so the heat can be dissipated from the device.

Note 2 - Bias Arrangement
Each DC pin (V_D and V_G) needs to have DC bypass capacitance of 100 pF as close to the device as possible. In addition the V_G must have 2.2 µF on the side the gate voltage is applied. It is recommended to also use a further capacitance of 0.01 µF on the DC pins.

Note 3 - Pulse Operation
The performance of the MAAP-015024-DIE is characterized under pulsed conditions with a pulse width of 5 µS and a duty cycle of 5%. The measurements were taken while the drain voltage was pulsed. It is strongly recommended to ensure the heat generated is dissipated from the die with an adequate thermal solution. If this thermal path is not provided this will result in reduced performance/ lifetime and possible thermal runaway that will permanently damage the PA. It is not recommended to operate this PA in CW operation unless the bias is reduced.

Applications Section

Handling and Assembly

Die Attachment

This product is 0.075 mm (0.003") thick and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280ºC (note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/- 10ºC. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding

Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5 - 2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.