-10 V to -25 V Driver for PIN Diode Switches

MADR-011022
Rev. V2

Features

- -10 V to -25 V Back Bias
- 25 mA Sinking Current
- 20 mA Sourcing Current
- Propagation Delay <130 ns Driving 100 pF Capacitive Load
- Quiescent Currents <1 mA
- TTL Logic Control
- Internal Active Pull Down for All Logic Controls
- Internal Power Sequencer Eliminates External Power Sequencing
- 4 mm 16-Lead PQFN Package
- RoHS* Compliant

Applications

- Aerospace & Defense
- ISM

Description

The MADR-011022 switch driver is designed to work with MACOM's HMIC 20 W CW SPDT PIN diode switches. This driver has complementary outputs which can provide up to 25 mA sinking and 20 mA sourcing bias current to a SPDT PIN diode switch. An all-off RF state can be achieved with the EN pin of this driver. An extra control C2 with driver select DS are provided to allow two drivers working together to drive a SP3T or SP4T switch.

The back bias voltage can be selected to be any voltage between -10 V and -25 V. This switch driver can be easily controlled by standard TTL logic. With low quiescent current, this driver has a typical delay of <130 ns when driving a 100 pF capacitive load.

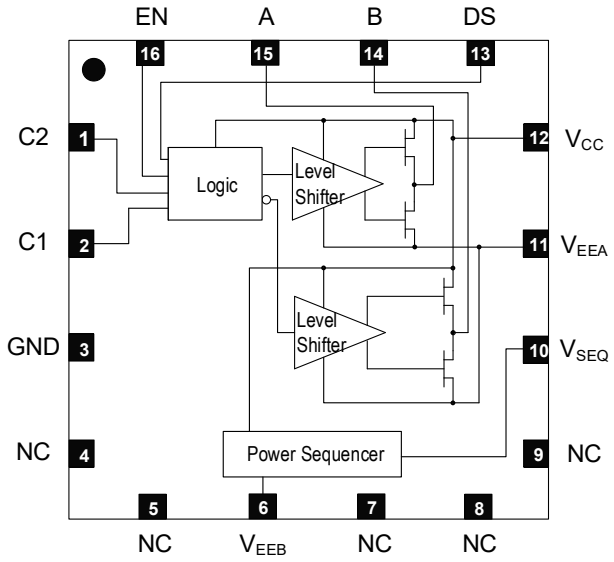
This driver is packaged in a lead-free 4 mm 16-lead PQFN package and is available in tape and reel packaging for high volume applications.

Ordering Information[1]

Part Number	Package
MADR-011022-TR1000	1000 Piece Reel

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration

Pin #	Function	Description of Function
1	C2	Logic Control Input
2	C1	Logic Control Input
3	GND	Ground
4,5,7,8,9	NC[2]	No Connection
6	V_{EEB}	Negative Bias for Sequencer Die
10	V_{SEQ}	Power Sequencer Die Output
11	V_{EEA}	Negative Bias for Driver Die
12	V_{CC}	Positive Bias
13	DS	Driver Select
14	B	Inverted Driver Output
15	A	Non-inverted Driver Output
16	EN	Enable
17	Paddle[3]	Ground

2. NC pins should be left open.
3. MACOM recommends connecting the exposed pad centered on the package bottom to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Recommended Operating Conditions[4]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{CC}	—	V	4.5	5.0	5.5
V_{EEA} and V_{EEB}	—	V	-25	—	-10
C1, C2, EN, DS	Logic "0" Logic "1"	V	0.0 2.0	0.0 V_{CC}	0.8 V_{CC}
I_{SINK}, Sinking Current per Output	—	mA	—	—	25
I_{SOURCE}, Sourcing Current per Output	—	mA	—	—	20
Total Capacitive load per Output (Operating)	—	pF	—	—	100
Rise / Fall Time of V_{CC} and V_{EEB}	—	µs	1	—	—
Operating Temperature	—	°C	-40	+25	+85

4. Negative bias should be applied to V_{EEB} (pin 6). The sequencer output V_{SEQ} should be connected to the driver die negative bias V_{EEA}. A 47 pF shunt capacitor shall be placed close to pin 11 (V_{EEA}).

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
V_{CC}	-0.5 V ≤ V_{CC} ≤ +7 V
V_{EEA}, V_{EEB}	-30 V ≤ V_{EEA},V_{EEB} ≤ +0.5 V
C1, C2, EN, DS	-0.5 V ≤ V_{CC} ≤ +7 V
Sinking Current per Output	35 mA
Sourcing Current per Output	30 mA
Capacitive Load per Output[7]	125 pF
Operating Temperature	-40°C to +110°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Capacitive load above 125 pF can cause peak current exceeding power limit for the MOSFETs in the output buffer.

Logic Truth Table[8,9]

Inputs				Outputs	
EN	DS	C2	C1	A	B
1	X	X	X	H	H
0	0	0	0	L	H
0	0	0	1	H	L
0	0	1	0	H	H
0	0	1	1	H	H
0	1	0	0	H	H
0	1	0	1	H	H
0	1	1	0	L	H
0	1	1	1	H	L

8. The actual output low voltage can be calculated by: $V_{OL} = V_{EEB} + I_{SINK} \times R_{Pull\text{-}Down}$.
9. The actual output high voltage can be calculated by: $V_{OH} = V_{CC} - I_{SOURCE} \times R_{Pull\text{-}Up}$.

Electrical Specifications: T_A = 25°C, V_{CC} = 5 V, V_{EEB} = -25 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{CC} Quiescent Current	C1 = 5 V, C2 = DS = EN = 0 V	mA	—	0.4	0.5
V_{EEB} Quiescent Current	C1 = 5 V, C2 = DS = EN = 0 V	mA	—	0.4	0.5
Control Input Leakage Current[10]	Control = 5 V	µA	—	20	25
$R_{PULL-UP}$, Output Pull-up On Resistance	20 mA Load	Ω	—	19	25
$R_{PULL-DOWN}$, Output Pull-down On Resistance	25 mA Load	Ω	—	19	25
Switching Speed Driving 100 pF Capacitors[11] T_{ON} T_{OFF} T_{RISE} T_{FALL}	 50% control to 90% Voltage 50% control to 10% Voltage 10% to 90% Voltage 90% to 10% Voltage	ns	—	 56 68 31 29	—
Switching Speed Driving MASW-002103 Switch[12] T_{ON} T_{OFF} T_{RISE} T_{FALL}	 50% control to 90% Voltage 50% control to 10% Voltage 10% to 90% Voltage 90% to 10% Voltage	ns	—	 75 69 22 50	—
Power Sequencer Threshold Voltage	Note 13	V	—	2.5	—
Power Sequencer Power On Time	Note 14	µs	—	25	—
Driver Die Power Up Time	Note 15	µs	—	1	—
Driver Die Power Down Time	Note 16	µs	—	1	—

10. This leakage current is due to an active pull-down NMOS FET at the control input.
11. Tested with a 100 pF capacitive load at each output (no current load).
12. MACOM MASW-002103 is a 50 MHz to 20 GHz SPDT HMIC Pin Diode Switch. Measured at 10 GHz, 16 dBm, V_{CC} = +5 V, V_{EEB} = -15 V, and 20 mA forward bias current. The control input was a 0.8 V to 2 V pulse with rise and fall time of 6 ns.
13. When V_{CC} is below this threshold, the internal power sequencer will pull its output V_{SEQ} to ground.
14. This is the delay between the moment when V_{CC} is above the power sequencer threshold to V_{SEQ} reaches 90% of steady state value. This is measured with a 47 pF shunt capacitor off V_{EEA}.
15. This is the time needed for the driver to function properly after V_{CC} and V_{EEA} reach 90% of their stable value.
16. This is the time needed for the internal bias voltages to discharge to 10% of their steady state value after V_{CC} and V_{EEA} are powered down.

Internal Power Sequencer

For normal operation, negative bias should be applied to V_{EEB} (pin 6). The sequencer output V_{SEQ} should be connected to the driver die negative bias V_{EEA}, with a 47 pF shunt capacitor, as shown in the application schematic next page. The voltage rating of this 47 pF capacitor should be sufficient according to the operating V_{EEB}.

When detected V_{CC} is above the power sequencer threshold, the negative bias V_{EEB} will be passed to the driver. When detected V_{CC} is below the power sequencer threshold, the power sequencer will pull V_{EEA} to ground to disable the driver.

Driving SPDT Switches

When driving SPDT switches, use C1 and EN as the control inputs. Output A is the non-inverting output, and output B is the inverting output. The unused controls DS and C2 can be left open due to the internal active pull-down. If an all-off RF state is not required, leaving the EN pin open will automatically enable the driver due to the internal active pull-down. The truth table is simplified as follows when DS and C2 are left open:

Truth Table for Driving SPDT

EN	C1	A	B
1	X	H	H
0	0	L	H
0	1	H	L

Handling Procedures

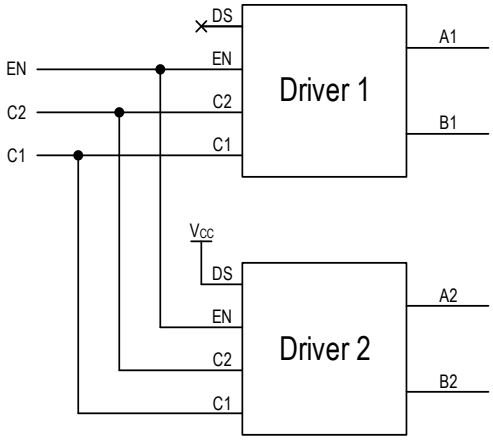
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1B devices.

Driving SP3T and SP4T Switches

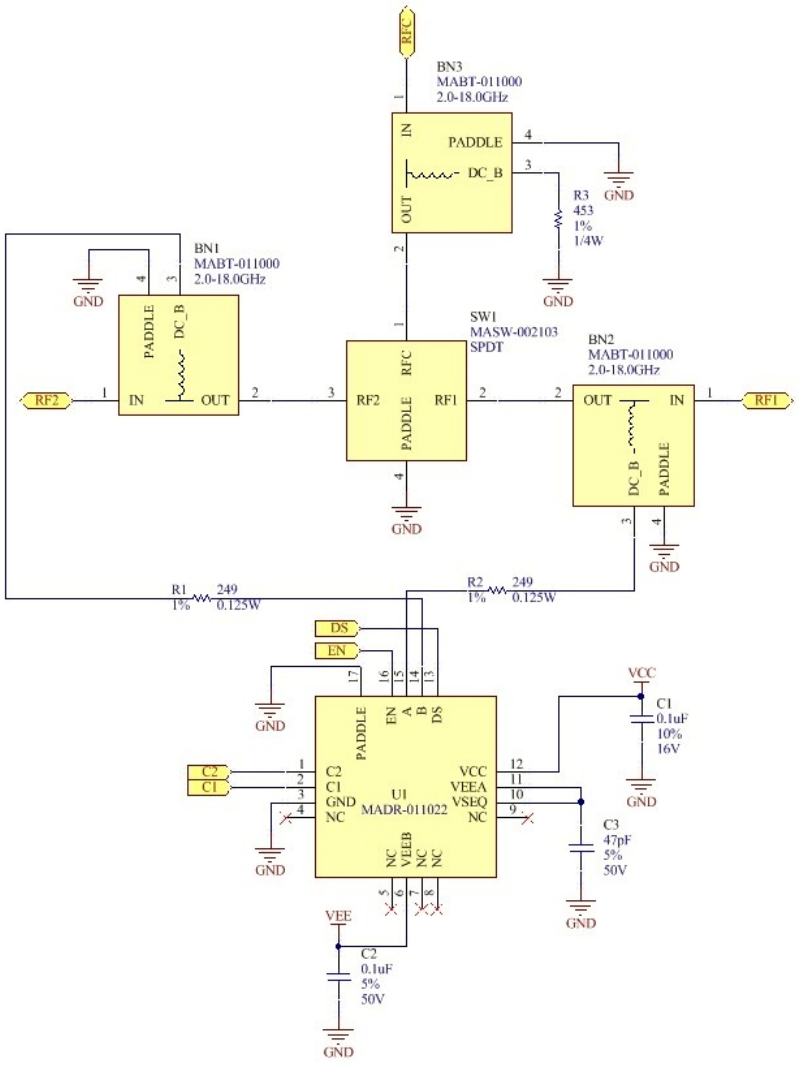
Two drivers are needed to drive a SP3T or SP4T switch. The DS pin of the first driver can be left open due to the internal active pull-down. Connect the DS pin of the second driver to V_{CC}. See the figure below for how to connect C1, C2, and EN. The combined truth table is below:



Truth Table for Driving SP3T and SP4T

Inputs			Outputs			
EN	C2	C1	A1	B1	A2	B2
1	X	X	H	H	H	H
0	0	0	L	H	H	H
0	0	1	H	L	H	H
0	1	0	H	H	L	H
0	1	1	H	H	H	L

Application Schematic Driving MASW-002103[17, 18]



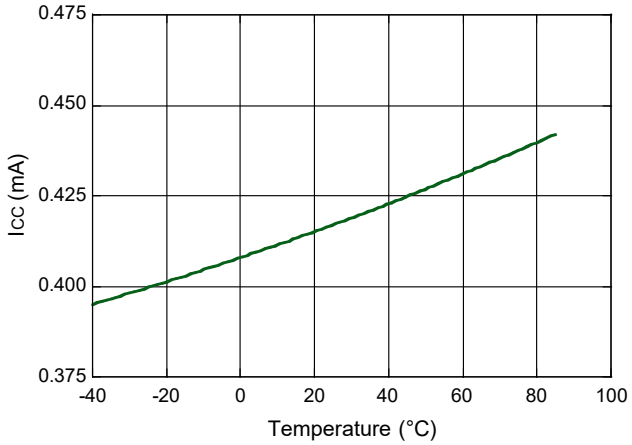
Parts List[18]

Part	Value
U1	MADR-011022, -10 V to -25 V Driver
SW1	MASW-002103, HMIC, SPDT Switch
BN1, BN2, BN3	MABT-011000, Bias Tee, 2 to 18 GHz
R1, R2	Resistor, 0805, 249 Ω, 1%, 1/8 W
R3	Resistor, 1206, 453 Ω, 1%, 1/4 W
C1	Capacitor, 0805, 16 V, X7R, 10%, 0.1 µF
C2	Capacitor, 0805, 50 V, X7R, 5%, 0.1 µF
C3	Capacitor, 0805, 50 V, X7R, 5%, 47 pF

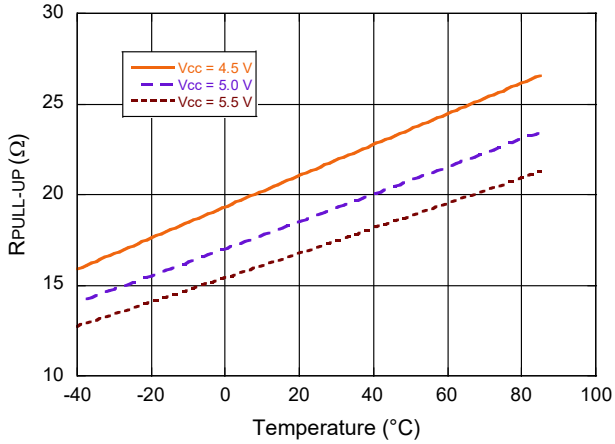
17. If all-off state is not needed, just leave C2, DS, and EN floating and use C1 as the switch control. See the Truth Table for Driving SPDT on the previous page. If all-off state is needed, leave C2 and DS floating, and use C1 and EN as the switch controls.
18. The voltage rating of C2 and C3 should be at least two times of V_{EE}.

Typical Performance Curves

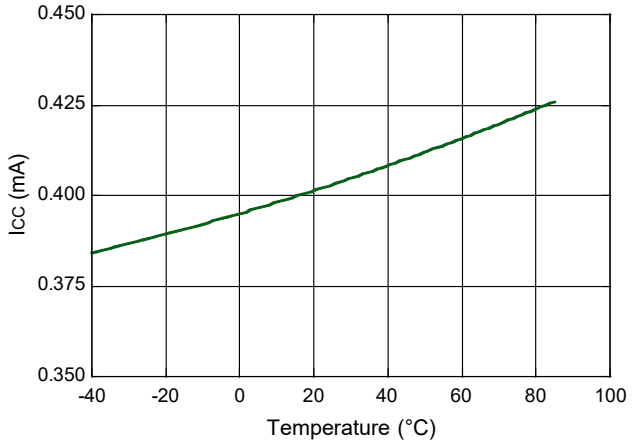
Quiescent I_{CC}: V_{CC} = +5 V, V_{EEB} = -25 V



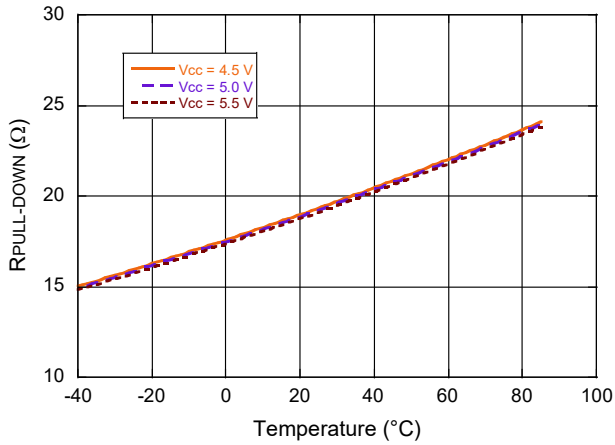
Output Pull-Up On Resistance[19]



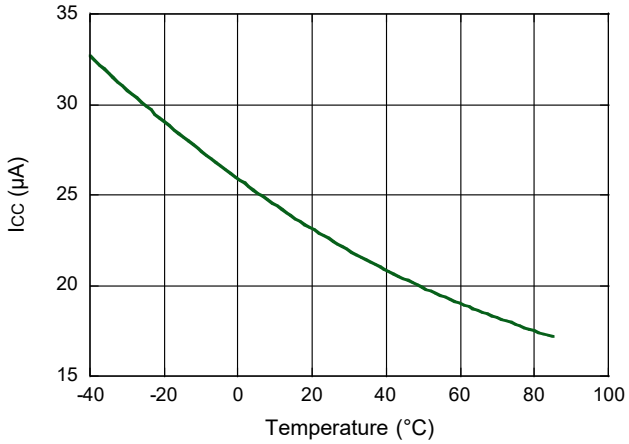
Quiescent I_{EEB}: V_{CC} = +5 V, V_{EEB} = -25 V



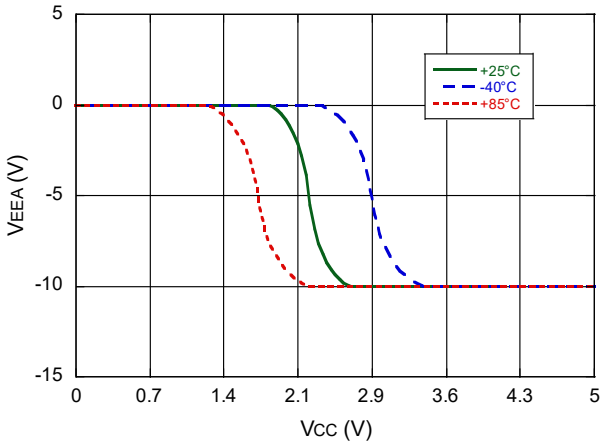
Output Pull-Down On Resistance[19]



Control Leakage Current: V_{CC} = C = +5 V, V_{EEB} = -25 V



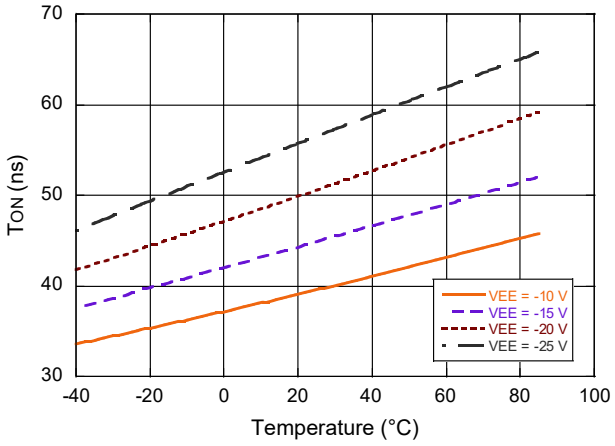
Power Sequencer Threshold:



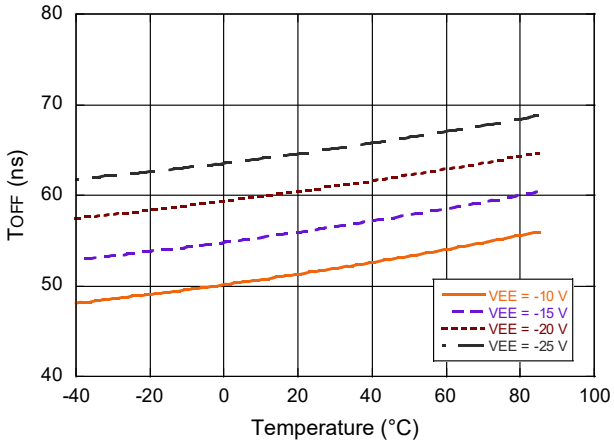
19. The output on resistance does not change with different V_{EEB} voltage levels.

Typical Performance Curves[20]

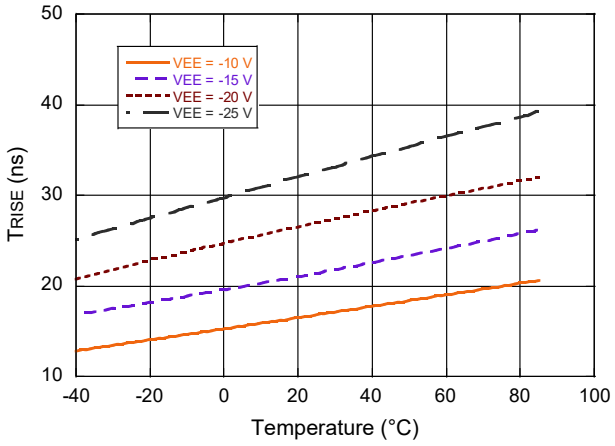
Switching Speed Driving 100 pF Capacitor: T_{ON}



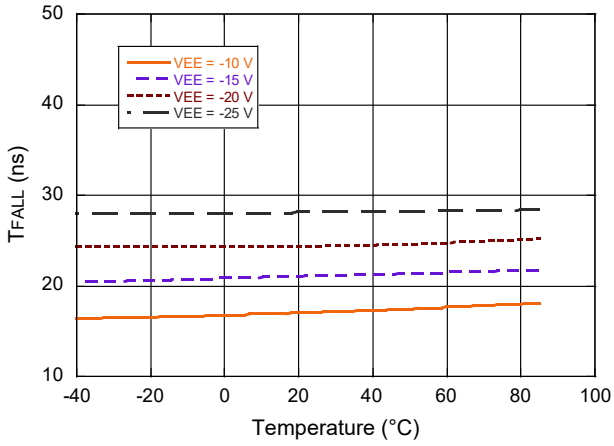
Switching Speed Driving 100 pF Capacitor: T_{OFF}



Switching Speed Driving 100 pF Capacitor: T_{RISE}



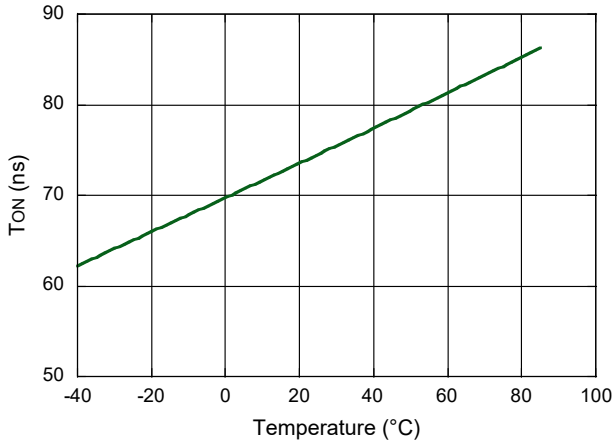
Switching Speed Driving 100 pF Capacitor: T_{FALL}



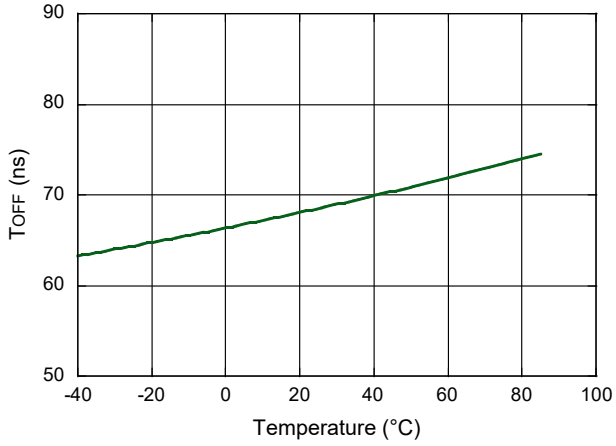
20. Tested with a 100 pF capacitor at each output (no current load), V_{CC} = +5 V, 0.8 V to 2 V control with rise and fall time of 6 ns.

Typical Performance Curves[21]

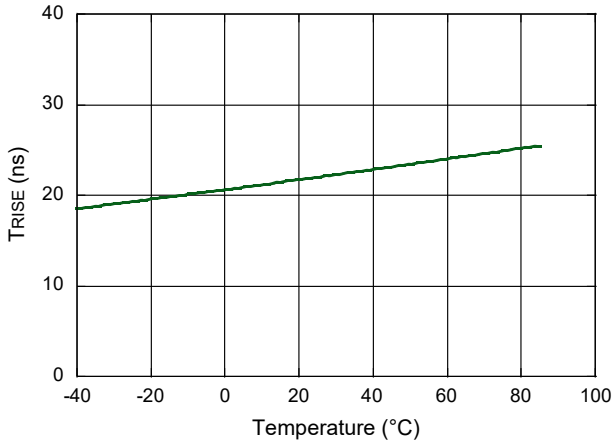
Switching Speed Driving MASW-002103: T_{ON}



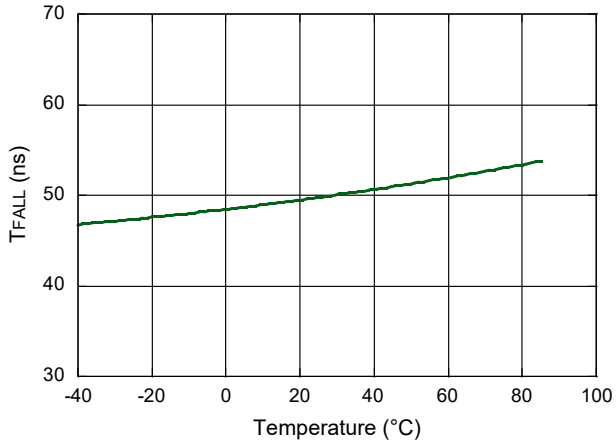
Switching Speed Driving MASW-002103: T_{OFF}



Switching Speed Driving MASW-002103: T_{RISE}

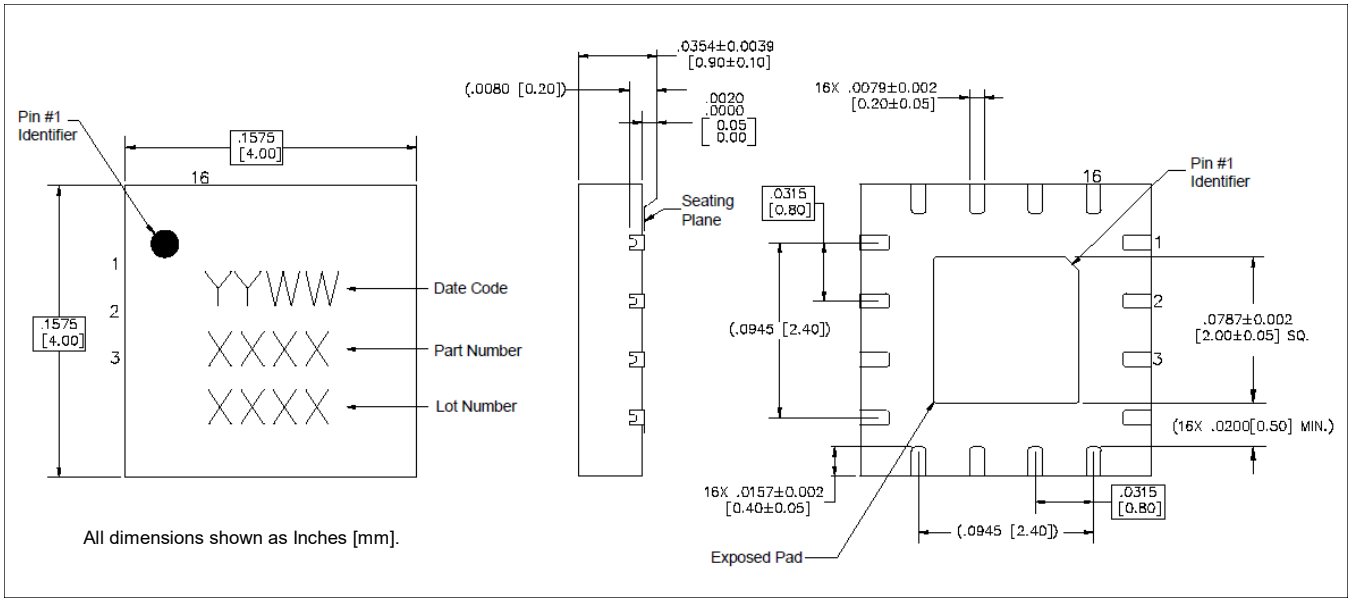


Switching Speed Driving MASW-002103: T_{FALL}



21. MACOM MASW-002103 is a 50 MHz to 20 GHz SPDT HMIC Pin Diode Switch. Measured at 10 GHz, 16 dBm, V_{CC} = +5 V, V_{EEB} = -15 V, and 20 mA forward bias current. The control input was a 0.8 V to 2 V pulse with rise and fall time of 6 ns.

Lead-Free 4 mm 16-Lead PQFN†



† This is not a JEDEC standard package.
Meets JEDEC moisture sensitivity level (MSL) 1 requirements.
Plating is NiPdAu.