MAMF-011015

X-Band Multifunction MMIC
8 - 11 GHz

Rev. V4

Features

- T_X Gain: 11 dB
- T_X P_{SAT}: 23 dBm
- R_X Gain: 24 dB
- R_X Noise Figure: 2 dB
- Lead-Free 7 mm 44-Lead PQFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant

Description

The MAMF-011015 is an 8 - 11 GHz multifunction GaAs MMIC designed for communication radar and weather applications. It functions in combination with an advanced Si serial-controller which addresses the GaAs chip for the necessary R_X/T_X selection path and the required signal controls, along with several other functionalities.

The MAMF-011015's GaAs chip utilizes a 0.25 µm pHEMT GaAs process which has been optimized for RF power, low noise, and RF signal control applications which is ideal for high levels of integration on a single IC. This GaAs MMIC includes a "Common path" circuit where it incorporates a 4-BIT digital attenuator, a 6-BIT digital phase shifter, and a T/R SPDT switch for R_X/T_X selection. The "R_X path" incorporates a low noise amplifier and 2 additional higher attenuation bits. The "T_X path" driver amplifier is designed to deliver sufficient RF power and gain for an outside power amplifier.

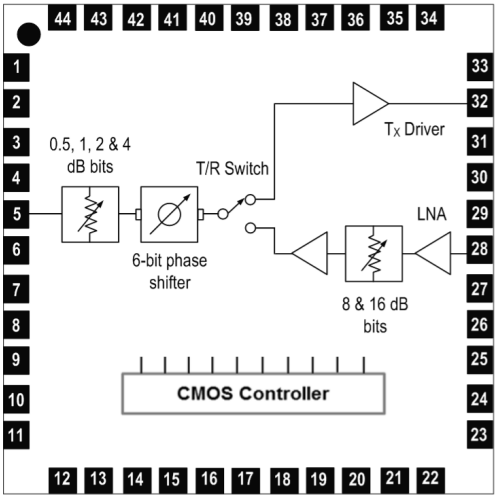
The MAMF-011015's Si serial-controller chip is designed to address the GaAs chip's common path signal control components along with several other functionalities such as external G/D control enabling or disabling internal gate/drain switching of the LNA or driver amplifier. When internal gate switching is disabled, external drain switching may be used for fast T/R switching (pulsing).

Ordering Information[1]

Part Number	Package
MAMF-011015-TR0500	500 Piece Reel
MAMF-011015-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration[2]

Pin	Function	Pin	Function
1 - 3	No Connection	25	V_{OPT2}
4	Ground	26	V_G_LNA
5	Common	27	Ground
6	Ground	28	R_x IN
7	V_{EE}	29	Ground
8	Ground	30	V_{CC1}
9 - 11	No Connection	31	Ground
12	V_{CC2}	32	T_x OUT
13	SER IN	33	Ground
14	CLK	34	DET
15	LE	35	REF
16	RS	36	No Connection
17	TR	37	V_{DD2}
18	EN	38	V_{DD1}
19	No Connection	39	No Connection
20	SWEN2	40	TEMP SENSE
21	SER OUT	41	V_G_PA12
22	V_{EE}	42	No Connection
23	SW2A50	43	G/D
24	SW2B50	44	No Connection
		45[3]	Ground

2. MACOM recommends connecting unused (no connection) pins to RF and DC ground.
3. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Description of Pin Functions

Pin	Function	Description of Function
4, 6	Ground	RF and DC Ground (RF Launch)
5	Common	RF Common Port - See Block Diagram
7	V_{EE}	Negative Supply for Logic Driver (Defines negative Voltages for GaAs switch outputs)
8	Ground	ED Ground
12	V_{CC2}	Positive Supply for Logic Driver
13	SER IN	Serial Input for Data Stream
14	CLK	Clock for Data Stream
15	LE	Load Enable for Data Stream
16	RS	Register Select - Selects from two interleaved data streams
17	TR	Transmit/Receive Switch Select; Works with “EN” to enable or disable LNA or driver amp
18	EN	The enable control can disable all amplifiers; Works with “TR” to disable amplifiers in path that is off
20	SWEN2	Determines if External PIN switch is driven (see truth table)
21	SER OUT	Serial Output for Data Stream
22	V_{EE}	Negative Supply for Logic Driver (Defines negative Voltage for PIN switch outputs)
23	SW2A50	Control for external PIN diode switch
24	SW2B50	Control for external PIN diode switch (complement of SW2A50)
25	V_{OPT2}	Positive Supply for Logic Driver (Defines positive Voltage for PIN switch outputs)
26	V_G_LNA	Provides gate bias (negative voltage) for LNA (this is a fixed, not adjustable voltage)
27, 29	Ground	RF and DC Ground (RF Launch)
28	R_X IN	Receive RF input - See block diagram
30	V_{CC1}	Positive bias for LNA
31, 33	Ground	RF and DC Ground (RF Launch)
32	T_X OUT	Transmit RF output - See block diagram
34	DET	Detector output, which monitors transmit power
35	REF	Reference output for the detector (using a differential amplifier, this is used to compensate for the temperature drift of the detector output)
37	V_{DD2}	Bias for the second stage of the driver amplifier
38	V_{DD1}	Bias for the first stage of the driver amplifier
40	TEMP SENSE	Temperature sensor to output the variation of chip temperature. The temperature sensor is located on chip, close to the driver amplifiers
41	V_G_PA12	Gate bias (negative voltage) for first two driver amp stages (this is a fixed, not adjustable voltage)
43	G/D	G/D Select switch; if the LNA (R_x path) and Driver Amplifier (T_x Path) are gate switched (by CMOS driver) or drain switched (using external MOSFETs)
45	Ground	Exposed pad centered on the package bottom must be connected to RF and DC ground

Electrical Specifications: Freq. = 8.5, 9.5, 10.5 GHz, T_A = 25°C, Z_0 = 50 Ω[4,5,6,7]

T_X State bias:

V_{DD1}= V_{DD2} = 5 V , V_G_PA12 = -5 V, V_{CC1} = 3.3 V, V_{G_LNA} = -5 V, V_{CC2}= V_{OPT2}[8]= 5 V, V_{EE}[9] = -5 V, TR = 5 V, SWEN2 = G/D = 0 V

Symbol	Parameter	Conditions	Units	Min.	Typ.	Max.
T_X Gain	Transmit Gain (Common to T_{X_OUT})	R_X Amplifier OFF, (0 dB ATT, 0°Phase) Freq. 8 - 9.5 GHz Freq. 10.5 GHz	dB	10 9	11	—
T_X IN RL	Transmit Input Return Loss	"	dB	10	14	—
T_X OUT RL	Transmit Output Return Loss	"	dB	8	9	—
T_X P1dB	Transmit P1dB	"	dBm	21.5	23	—
DPS	Phase Shifter (6-Bit) LSB	R_X Amplifier OFF, (0 dB ATT)	deg	—	5.625	—
DPS_Phase_Er	RMS Phase Error	"	deg	—	3.0	—
DPS_Amp_Er	RMS Amplitude Error	"	dB	—	0.6	—
DAT	Attenuator (4-Bit) LSB	R_X Amplifier OFF, (0°Phase)	dB	—	0.5	—
DPS_DAT_Er	RMS Attenuation Accuracy Error	"	dB	—	0.4	—
T_X Idq	Total T_X Drain Current (V_{DD1}, V_{DD2})	"	mA	—	140	—
I_{DD1}	Quiescent supply current of V_{DD1}	R_X Amplifier OFF, (0 dB ATT, 0°Phase)	mA	28	43	60
I_{DD2}	Quiescent supply current of V_{DD2}	"	mA	60	98	125
I_G_PA12	Quiescent supply current of V_{G_PA12}	"	mA	—	10	—
I_{CC1}	Quiescent supply current of V_{CC1}	"	mA	—	0	—
I_G_LNA	Quiescent supply current of V_{G_LNA}	"	mA	—	0	—
I_{CC2}	Quiescent supply current of V_{CC2}	"	µA	—	0.1	—
I_{EE}	Quiescent supply current of V_{EE}	"	mA	—	1	2
I_{OPT2}[10]	Quiescent supply current of V_{OPT2}	"	µA	—	0.1	—

RF Specifications: Freq. = 8.5, 9.5, 10.5 GHz, T_A = 25 °C, Z_0 = 50 Ω[4,5,6,7]

R_X State bias:

V_{DD1} = V_{DD2} = 5 V, V_G_PA12 = -5 V, V_{CC1}= 3.3 V, V_G_LNA = -5 V, V_{CC2}= V_{OPT2}[8] = 5 V, V_{EE}[9] = -5 V, TR = SWEN2 = G/D = 0 V

Symbol	Parameter	Conditions	Units	Min.	Typ.	Max.
R_X Gain	Receive Gain (R_X IN to Common)	T_X Amplifier OFF (0 dB ATT, 0° Phase)	dB	21	24	—
R_X IN RL	Receive Input Return Loss	"	dB	10	15	—
R_X OUT RL	Receive Output Return Loss	"	dB	8	14	—
R_X NF	Receive Noise Figure	"	dBm	—	2	2.5
R_X OIP3	Receive Output OIP3	"	dBm	15	18	—
DPS	Phase Shifter (6-Bit) LSB	T_X Amplifier OFF (0 dB ATT)	deg	—	5.625	—
DPS_Phase_Er	RMS Phase Error	"	deg	—	3.0	—
DPS_Amp_Er	RMS Amplitude Error	"	dB	—	0.6	—
DAT	Attenuator (4-Bit) LSB	T_X Amplifier OFF (0°Phase)	dB	—	0.5	—
DPS_DAT_Er	RMS Attenuation Accuracy Error	"	dB	—	0.4	—
I_{DD1}	Quiescent supply current of V_{DD1}	T_X Amplifier OFF, (0 dB ATT, 0° Phase)	mA	—	0	0.5
I_{DD2}	Quiescent supply current of V_{DD2}	"	mA	—	0.5	1.5
I_G_PA12	Quiescent supply current of V_{G_PA12}	"	mA	—	10	—
I_{CC1}	Quiescent supply current of V_{CC1}	"	mA	80	110	135
I_G_LNA	Quiescent supply current of V_{G_LNA}	"	mA	—	10	—
I_{CC2}	Quiescent supply current of V_{CC2}	"	mA	—	0	1
I_{EE}	Quiescent supply current of V_{EE}	"	mA	—	1	—
I_{OPT2}[10]	Quiescent supply current of V_{OPT2}	"	µA	—	0.2	—

Controls for PIN Driver[4,5,6,7,8,9,10]

Electrical Specifications: Freq. = 8.5, 9.5, 10.5 GHz, T_A = 25 °C, Z_0 = 50 Ω

Symbol	Parameter	Conditions	Units	Min.	Typ.	Max.
R_{PSW50}	Output Pull-up FET On Resistance for SWnA50 and SWnB50 Ports at 25°C	V_{CC2} = V_{OPT2} = +5 V, V_{EE} = -5 V, 50 mA load	Ω	—	18	—
R_{NSW50}	Output Pull-down FET On Resistance for SWnA50 and SWnB50 Ports at 25°C	V_{CC2} = V_{OPT2} = +5 V, V_{EE} = -5 V, 50 mA load	Ω	—	15	—
V_{IH}	Input High Voltage	—	V	0.7xV_{CC2}	V_{CC}	V_{CC2}
V_{IL}	Input Low Voltage	—	V	GND	GND	0.3xV_{CC2}
V_{OHS}	Output High for Serial Out	I_{OH} = -1 mA	V	—	V_{CC} - 0.1	—
V_{OLS}	Output Low for Serial Out	I_{OL} = +1 mA	V	—	0.1	—
I_{SOURCE}	DC Output Sourcing Current for SWnA50 and SWnB50 Ports	V_{CC2} = V_{OPT2} = +5 V, V_{EE} = -5 V	mA	—	—	50
I_{SINK}	DC Output Sinking Current for SWnA50, SWnB50 Ports	V_{CC2} = V_{OPT2} = +5 V, V_{EE} = -5 V	mA	—	—	50

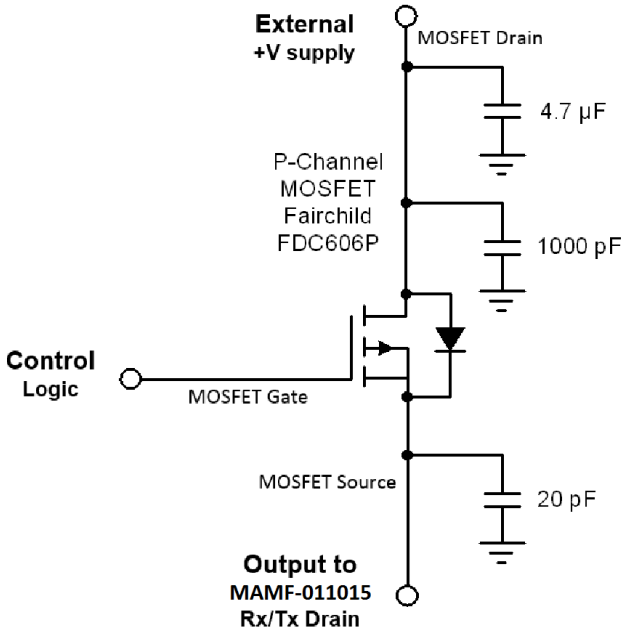
4. V_{CC1}, V_{DD1}, and V_{DD2} should be turned on after V_G_LNA and V_G_PA12 have been turned on. When turning power off, turn off V_{CC1}, V_{DD1}, and V_{DD2} prior to turning off V_G_LNA and V_G_PA12.
5. Unused logic inputs must be tied to either ground or V_{CC2}.
6. All voltages are relative to ground.
7. 0.01 µF decoupling capacitors are required on the power supply lines.
8. V_{OPT2} determines the output high voltage for the external PIN driver output, and is usually tied to V_{CC2}. When the PIN driver section is unused, V_{OPT2} should be grounded and SW2A50 and SW2B50 should be left open.
9. V_{EE} is tied to the substrate of the die and should be the most negative voltage potential. V_{EE} should never be biased higher than any other power supplies.
10. I_{OPT2} and I_{EE} are determined by the external PIN diode switches. They should not exceed 50 mA.

Electrical Pulsing Specifications[11]:
Freq. = 8.5, 9.5, 10.5 GHz, T_A = 25 °C, Z_0 = 50 Ω

Symbol	Parameter	Conditions	Units	Min.	Typ.	Max.
Gate Switching Mode[12]						
T_x T_{ON}	Transmit Turn-on Time	50% Control to 90% RF	ns	—	240	—
T_x T_{OFF}	Transmit Turn-off Time	50% Control to 10% RF	ns	—	100	—
R_x T_{ON}	Receive Turn-on Time	50% Control to 90% RF	ns	—	200	—
R_x T_{OFF}	Receive Turn-off Time	50% Control to 10% RF	ns	—	90	—
Drain Switching Mode[13]						
T_x T_{ON}	Transmit Turn-on Time	50% Control to 90% RF	ns	—	50	—
T_x T_{OFF}	Transmit Turn-off Time	50% Control to 10% RF	ns	—	30	—
R_x T_{ON}	Receive Turn-on Time	50% Control to 90% RF	ns	—	40	—
R_x T_{OFF}	Receive Turn-off Time	50% Control to 10% RF	ns	—	20	—

11. When switching states, it is important to avoid having T_X and R_X on at the same time, which could potentially lead to undesired spurious signals or a damaging oscillation.
12. When gate switching, we recommend lingering in the idle state for 20 ns when transitioning between T_X and R_X to ensure that the T_X and R_X amplifiers are not both on at the same.
13. Typical drain switching times are with the control applied to the gate of the recommended external MOSFETS, including the recommended bypass capacitors.

T_X / R_X Drain Switching circuit Recommendation



T_X / R_X Drain Switching Truth Table

Path State	External +V supply	Control Logic	Output to
T_X_ON	+5.0 V	0 V	V_{DD1}, V_{DD2}
T_X_OFF		+5.0 V	
R_X_ON	+3.3 V	0 V	V_{CC1}
R_X_OFF		+3.3 V	

Absolute Maximum Ratings[14,15,16,17,18,19]

Symbol	Parameter	Min.	Max.	Unit
V_{DD1}, V_{DD2}	T_X Amplifier Bias	-0.5	+7.0	V
V_G_LNA	Gate Bias to R_X Amplifier	-6.0	+0.5	V
V_G_PA12	Gate Bias to T_X Amplifier	-6.0	+0.5	V
V_{CC1}	Positive DC Supply Voltage LNA	-0.5	+5.0	V
V_{CC2}	Positive DC Supply Voltage Driver	-0.5	+7.0	V
V_{OPT2}	Optional DC Output Supply Voltage	-0.5	V_{CC} +0.5, or +7.0 Whichever is less	V
V_{EE}	Negative DC Supply Voltage[16]	-7	Note 16	V
V_{IN}	Digital Input Voltage[17]	-0.5 Note 17	V_{CC} +0.5 or +7.0 Whichever is less	V
I_{OH}	Output High Current for SER OUT	-10	0	mA
I_{OL}	Output Low Current for SER OUT	0	+10	mA
R_X IN	Receive RF Input	—	24	dBm
I_{SOURCE}	DC Output Sourcing Current for SW2A50 and SW2B50 Ports	0	60	mA
I_{SINK}	DC Output Sinking Current for SW2A50, SW2B50 Ports	0	60	mA
T_{OPER}	Operating Temperature	-40	+125	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_J	Junction Temperature[18, 19]	—	+150	°C

14. Exceeding any one or combination of these limits may cause permanent damage to this device.
15. MACOM does not recommend sustained operation near these survivability limits.
16. The absolute maximum rating for V_{EE} is the minimum of "V_{OPT2} + 0.5 V", "V_{CC2} +0.5 V", and "+0.5 V".
17. If $V_{CC2} \geq 6.5$ V, then the minimum for V_{IN} is V_{CC2} - 7.0 V.
18. Operating at nominal conditions with $T_J \leq +150$°C will ensure MTTF > 1 x 10^6 hours.
19. Junction Temperature (T_J) = T_C + Θ_{JC} * ((P_{DC}) - (P_{OUT} - P_{IN}))
    Typical Thermal Resistance in T_X mode (Θ_{JC}) = 67.0°C/W
    Typical Power Dissipation in the T_X state at 25°C is 0.6 W
    Typical Power Dissipation in the R_X state at 25°C is 0.27 W
    Typical Power Dissipation in the idle state at 25°C is 0.01 W

12-bit Serial to Parallel Driver

The phase shifting and attenuation settings are controlled by a serial data stream. Two states are entered in a single 24-bit data stream, 12-bit for each complete set of phase and attenuation settings.

The 24-bit serial interface (SERIN, CLK, LE, SER-OUT) is compatible with SPI protocol. The two 12-bit control words are loaded with MSB first. Note that the bits for the two states are interlaced, as shown in the "serial Input Bits Order and Function Table". When LE is high, the 24-bit data in the serial input register will be transferred to a 24-bit latch, and one of the two control words will be loaded to the complementary An and Bn outputs based on the logic state of RS control. "State A" uses the "A" bits while "State B" uses the "B" bits from the 24-bit stream. The RS control line allows fast toggling between the two states settings.

CLK will be masked to prevent data transition when LE is high. SEROUT is the SERIN delayed by 24 clock cycles.

Please refer to application note AN-0004028 for more detailed instructions on the driver operation. AN-0004028 also includes instructions to interface with USB-910H [USB-to-SPI/I2C embedded system interface] for quick operation of the device.

Register Select Truth Table [20]

RS	Bits Selected
0	"A" Bits
1	"B" Bits

20. See V_{IH} and V_{IL} for logic levels

Attenuator and Phase Shifter Control

The 6-bit attenuator and 6-bit phase shifter are controlled by serial input bits C1 ~ C12. The serial input bits order and control function are listed in following tables.

Serial Input Bits Order & Function Table

Function	Bit	RS = 0 State A	RS = 1 State B
-180° Phase Shift	C12B (MSB)	- -	State B
	C12A	State A	- -
-90° Phase Shift	C11B	- -	State B
	C11A	State A	- -
-45° Phase Shift	C10B	- -	State B
	C10A	State A	- -
-22.5° Phase Shift	C9B	- -	State B
	C9A	State A	- -
-11.25° Phase Shift	C8B	- -	State B
	C8A	State A	- -
-5.6° Phase Shift	C7B	- -	State B
	C7A	State A	- -
16 dB Attenuator	C6B	- -	State B
	C6A	State A	- -
8 dB Attenuator	C5B	- -	State B
	C5A	State A	- -
4 dB Attenuator	C4B	- -	State B
	C4A	State A	- -
2 dB Attenuator	C3B	- -	State B
	C3A	State A	- -
1 dB Attenuator	C2B	- -	State B
	C2A	State A	- -
0.5 dB Attenuator	C1B	- -	State B
	C1A (LSB)	State A	- -

T/R Switches Control

Switch drivers are designed to drive the SP2T switch in the MMIC which switch the T/R module between transmit and receive modes.

The SW2A50 and SW2B50 outputs are designed to drive PIN diode SP2T switches (External to the module). They are able to sink and source 50 mA current and provide back bias voltage as high as -5.5 V. They can be used to drive GaAs switches to improve the intermodulation performance and achieve higher P1dB at low frequencies.

For applications where an external PIN switch is used, SWEN2 is set to 0 V. In most cases, V_{OPT2} would be set to 0 V if an external GaAs switch is used.

T/R Switches Control Truth Table[21]

INPUTS		OUTPUTS			
SWEN2	TR	SW2A50	SW2B50	R_x Path	T_x Path
0	0	V_{EE}	V_{OPT2}	ON	OFF
0	1	V_{OPT2}	V_{EE}	OFF	ON
1	X	V_{OPT2}	V_{EE}	N/A	N/A

21. If no external switch is used, set SWEN2 high to conserve current.

Gate/Drain Switching Truth Table

G/D	Function
0 V	Drain Switching[22]
V_{EE}	Gate Switching[23]

22. When set in the drain switching mode, external MOSFETs will be needed to supply the bias voltage.
23. When gate switching, the internal driver will enable/disable the LNA (Receive amplifier) and Driver Amplifier (Transmit amplifier).

T/R Amplifiers Control

The combination of TR and EN inputs will be able to turn on/off the MMIC receive path LNAs and transmit path PAs.

T/R Amplifiers Control Truth Table [20, 24]

INPUTS			T_x or R_x Switch STATE	OUTPUTS	
G/D	EN	TR		PA	LNA
V_{EE}	0	0	Receive	OFF	OFF
V_{EE}	0	1	Transmit	OFF	OFF
V_{EE}	1	0	Receive	OFF	ON
V_{EE}	1	1	Transmit	ON	OFF
0 V	N/A	0	Receive	Note 25	Note 25
0 V	N/A	1	Transmit	Note 25	Note 25

24. In this table, the transmit or receive state signifies the how the switches are set. It does not mean that the amplifiers are enabled (ON).
25. The PA and LNA are enable/disabled depending on if external MOSFETs are “ON” or “OFF”. See the suggested T_X and R_X drain switching circuits.

Handling Procedures

Please observe the following precautions to avoid damage:

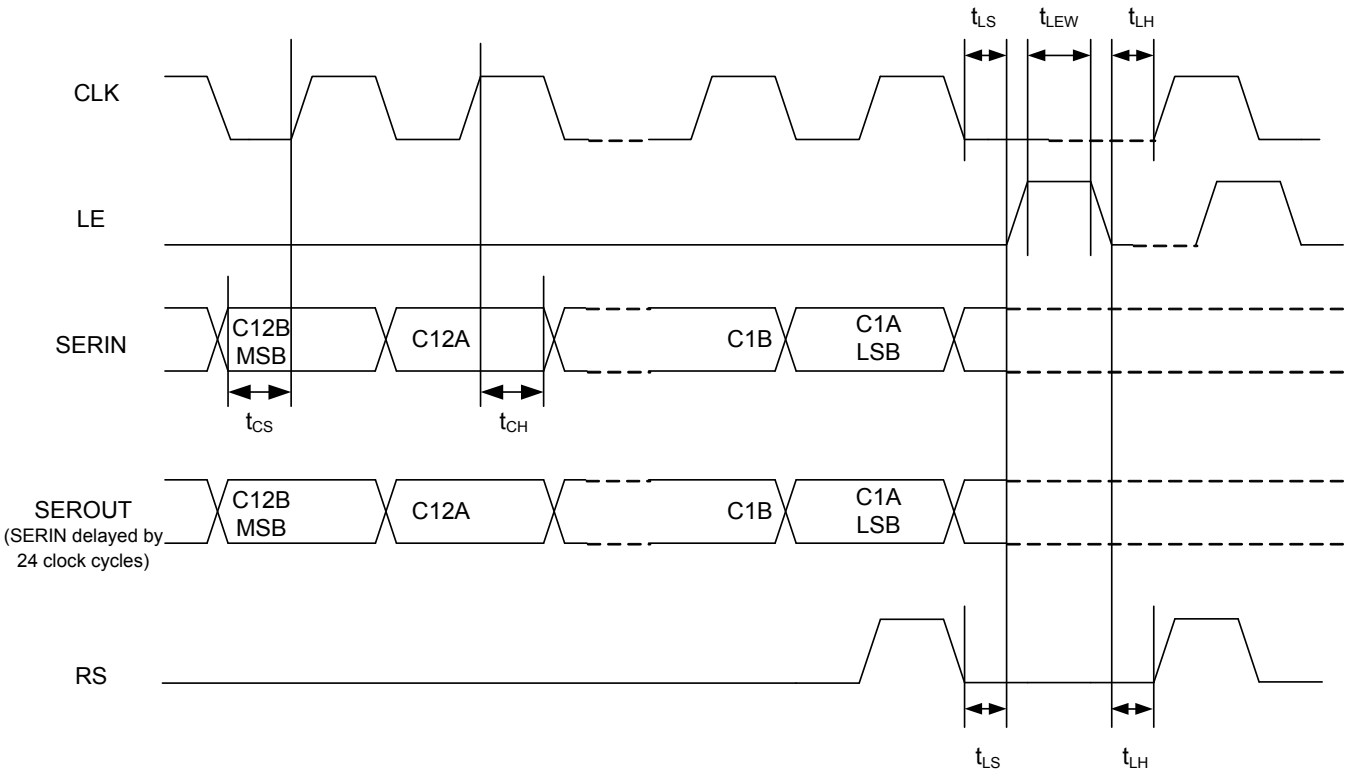
Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance	Unit
f_{data}	Max. Clock Rate for Shifting Serial Data	>80	MHz
t_{CS}	Min. Control Set-up Time	3.5	ns
t_{CH}	Min. Control Hold Time	3.5	ns
t_{LS}	Min. LE Set-up Time	3.5	ns
t_{LEW}	Min. LE Pulse Width	20.0	ns
t_{LH}	Min. LE Hold Time from CLK	3.5	ns
f_{RS}	Frequency for RS control, 50% Duty Cycle	25.0	MHz

Serial Interface Timing Diagram

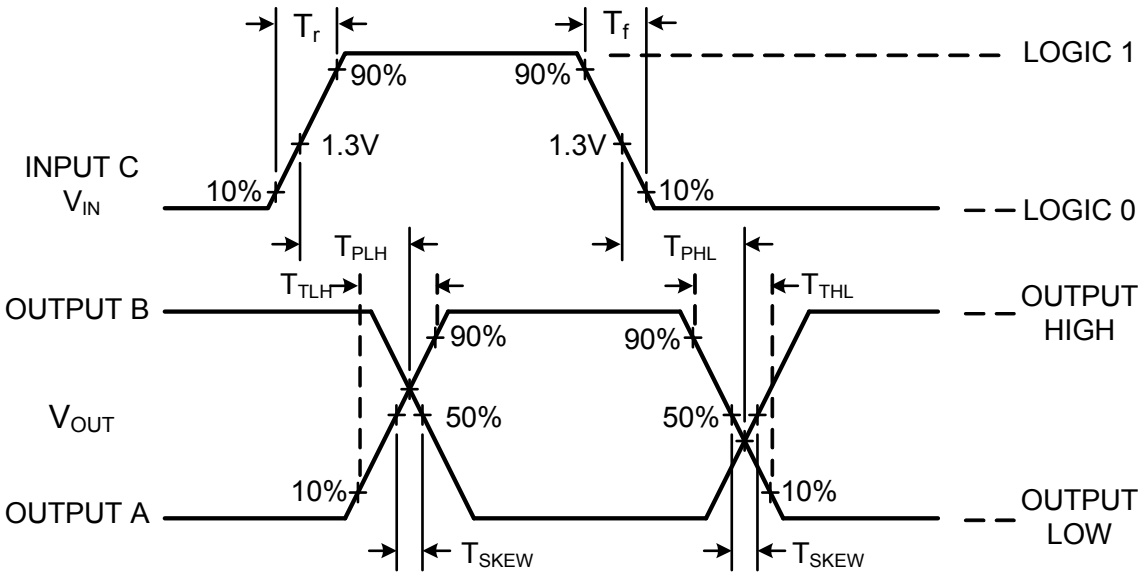


PIN Diode Driver Switching Speed:[26]

Symbol	Parameter	Typical performance	Unit
T_{PLH}	Propagation Delay	13	ns
T_{PHL}	Propagation Delay	13	ns
T_{TLH}	Output Transition Time (Rising Edge)	8	ns
T_{THL}	Output Transition Time (Falling Edge)	4.5	ns

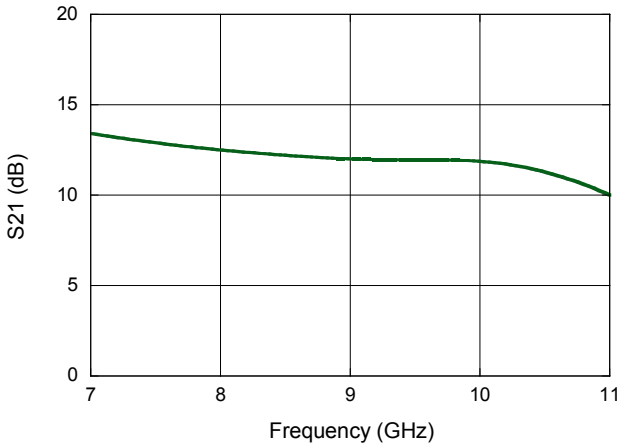
26. $V_{CC2} = V_{opt2} = 3.0$ V, $V_{EE} = -5.0$ V, $C_L = 24$ pF, input LOGIC1 = 3 V, LOGIC0 = 0 V, T_{RISE}, $T_{FALL} = 6$ ns.

Switching Waveforms

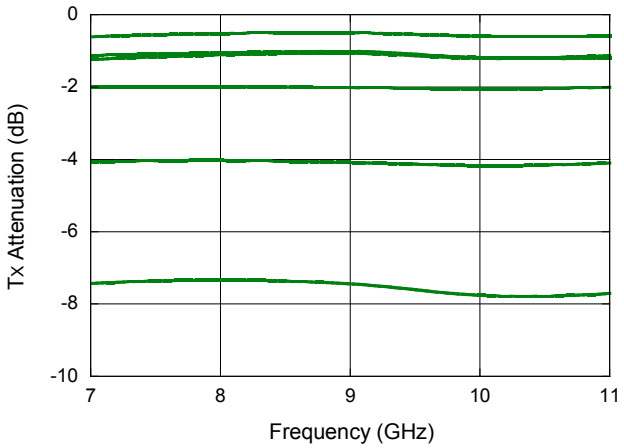


Typical Performance Curves

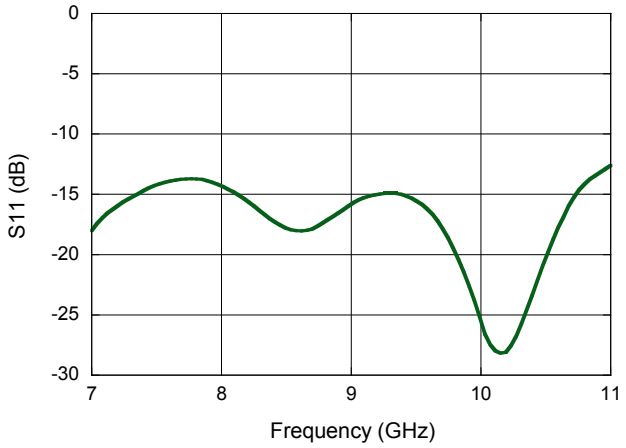
T_x Gain



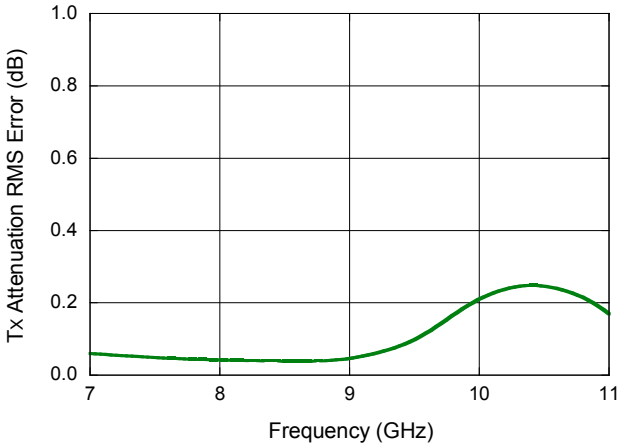
T_x Attenuation - Major Bits



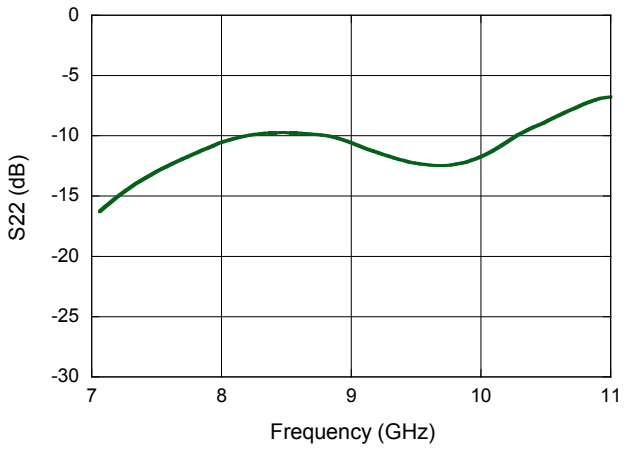
T_x Input Return Loss



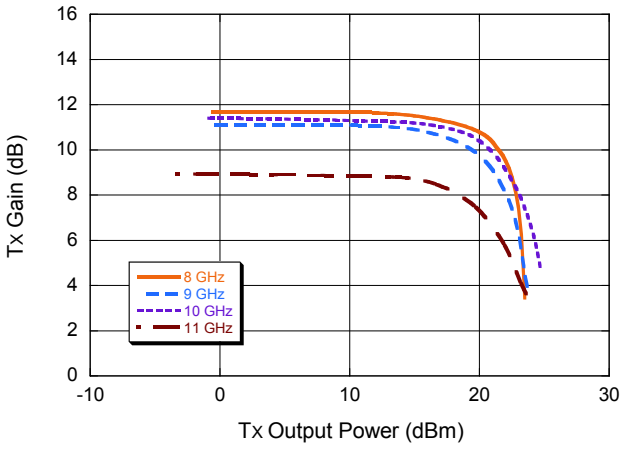
T_x Attenuation RMS Error



T_x Output Return Loss

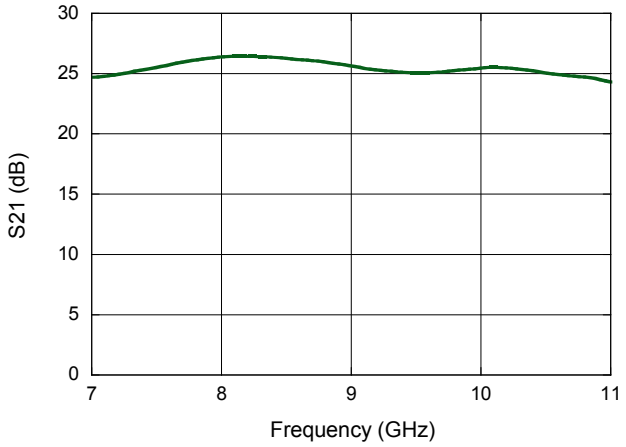


T_x Output P_{SAT}

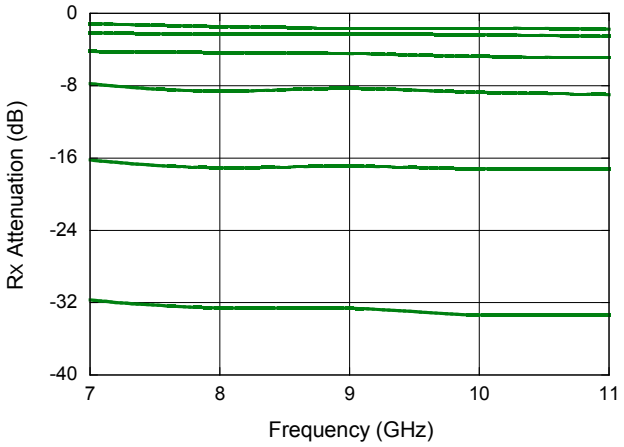


Typical Performance Curves

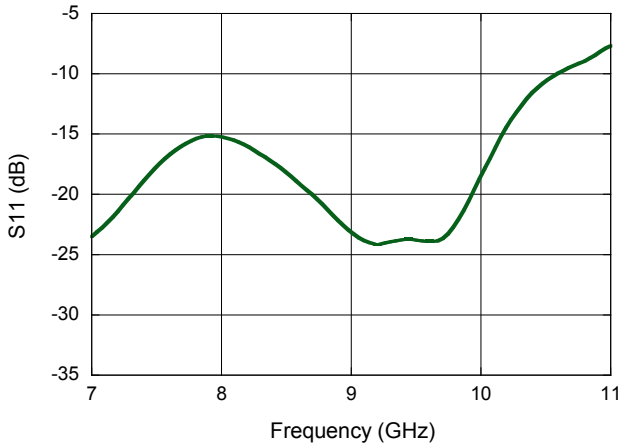
Rx Gain



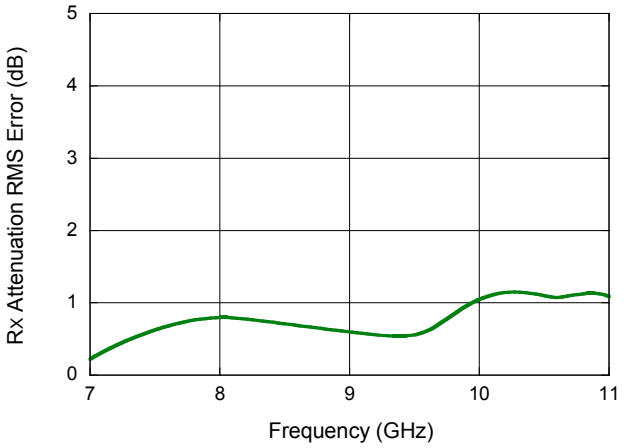
Rx Attenuation - Major Bits



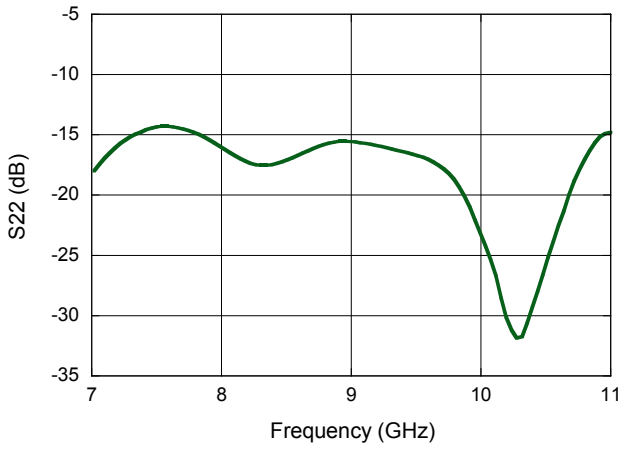
Rx Input Return Loss



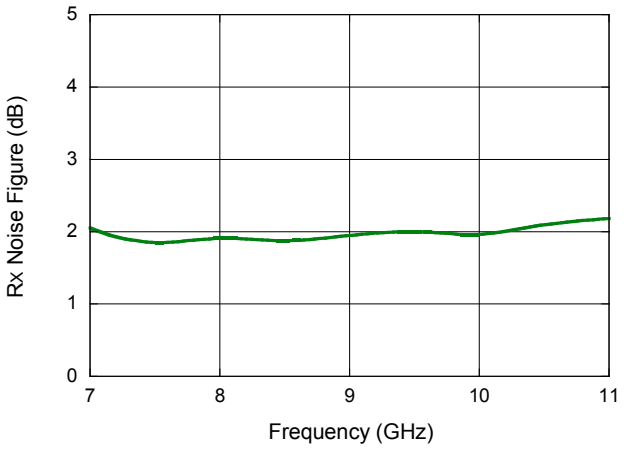
Rx Attenuation RMS Error



Rx Output Return Loss

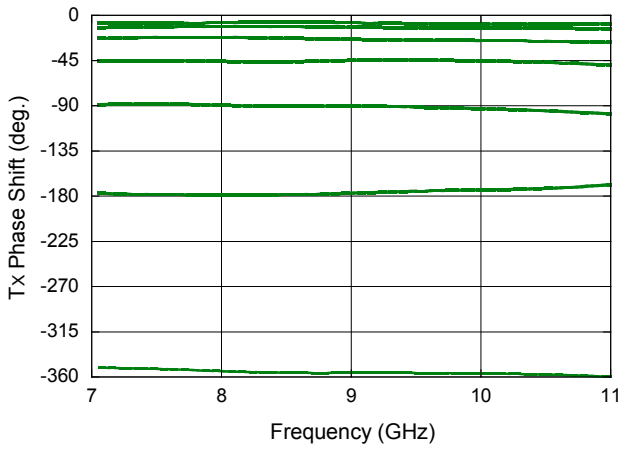


Rx Noise

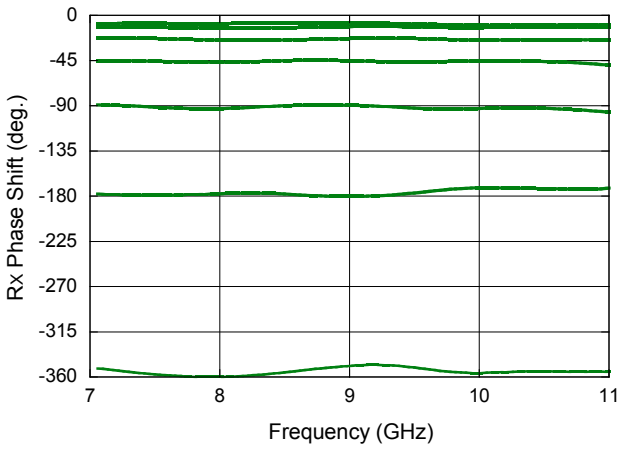


Typical Performance Curves

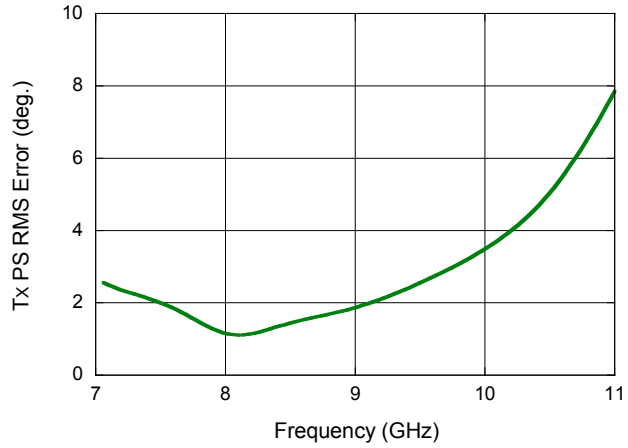
Tx Phase Shift



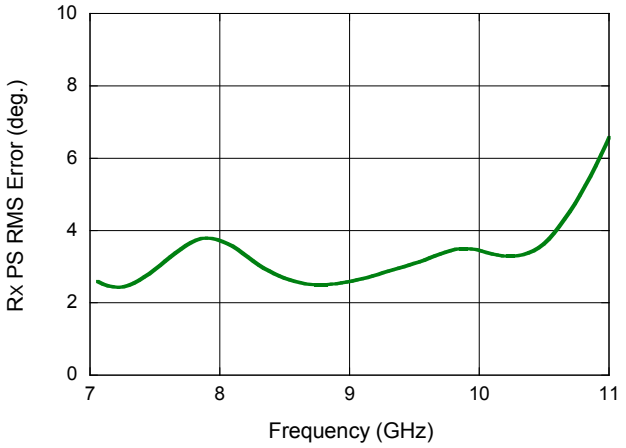
Rx Phase Shift



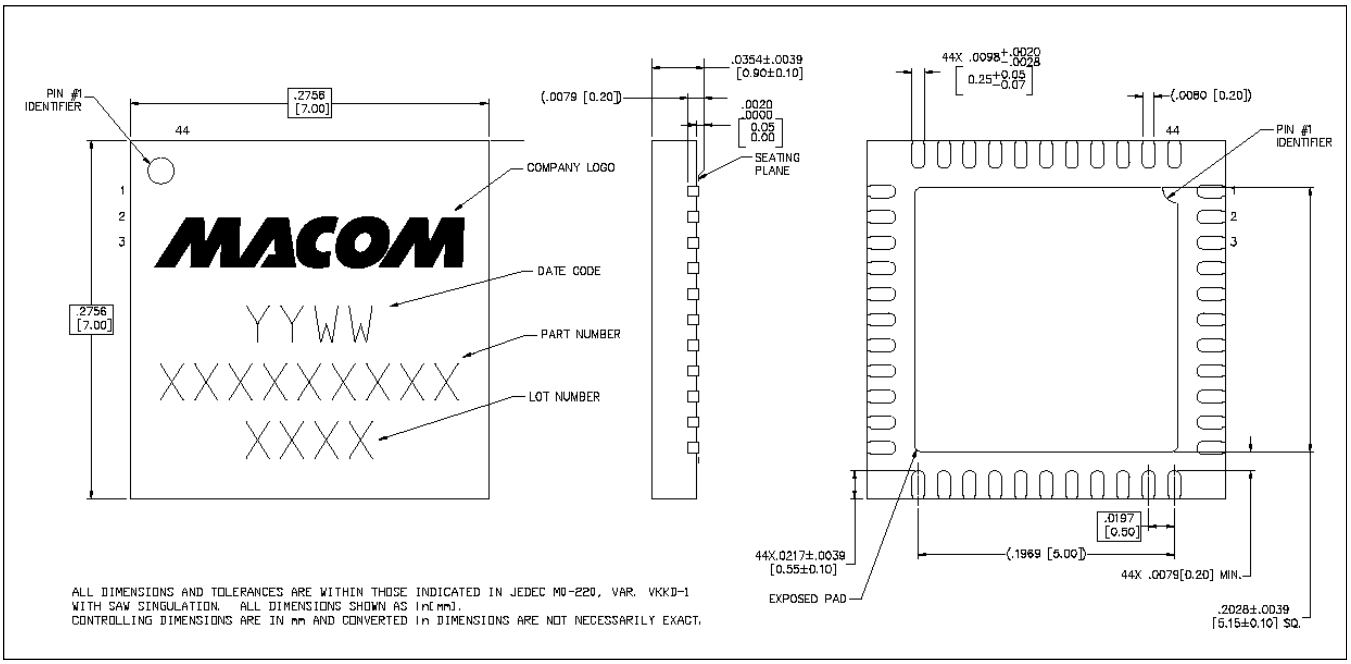
Tx PS RMS Error (deg.)



Rx PS RMS Error (deg.)



Lead Free 7 mm 44-lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
JEDEC moisture sensitivity levels MSL 3.
Plating is NiPdAu.