MAX11284 Evaluation Kit

Evaluates: MAX11284

General Description

The evaluation kit (EV kit) demonstrates the MAX11284 dual 24-bit, dual-channel, 16ksps Delta-Sigma ADCs with integrated PGA. The EV kit includes a graphical user interface (GUI) that provides communication from the target device to the PC. The EV kit can operate in multiple modes:

1) **Standalone Mode:** In "standalone" mode, the EV kit is connected to the PC through a USB cable and performs a subset of the complete EV kit functions. Sample rate and sample size are limited.
2) **FPGA Mode:** In FPGA mode, the EV kit is connected to an Avnet ZedBoard™ through a low-pin-count FMC connector. The ZedBoard features a Xilinx® Zynq®-7000 SOC that connects to the PC through an Ethernet port, which allows the GUI to perform different operations with full control over mezzanine card functions. The EV kit with FPGA platform performs the complete suite of evaluation tests for the target IC.
3) **User-Supplied SPI Mode:** In addition to the USB and FMC interfaces, the EV kit provides two 12-pin Pmod -style headers for user-supplied SPI interface, to connect the signals for SYNC, $\overline{RDYB}$, SCLK, DIN, DOUT, and $\overline{CS}$.

The EV kit includes Windows XP®, Windows® 7, and Windows 8-compatible software to utilize the features of the IC. The EV kit GUI allows different sample sizes, adjustable sampling rates, on-board or external reference options, and graphing software that includes the FFT and histogram of the sampled signals with the ability to save plots in .jpg or .csv formats.

The ZedBoard accepts a +12V AC-DC wall adapter. The EV kit can be powered by either the ZedBoard or a local 12V supply. The EV kit has on-board transformers and digital isolators to separate the IC from the ZedBoard/ on-board processor.

The MAX11284 EV kit comes with a MAX11284ETL+ in a 40-pin TQFN package installed.

ZedBoard is a trademark of Avnet, Inc.

Xilinx and Zynq are registered trademarks and Xilinx is a registered service mark of Xilinx, Inc.

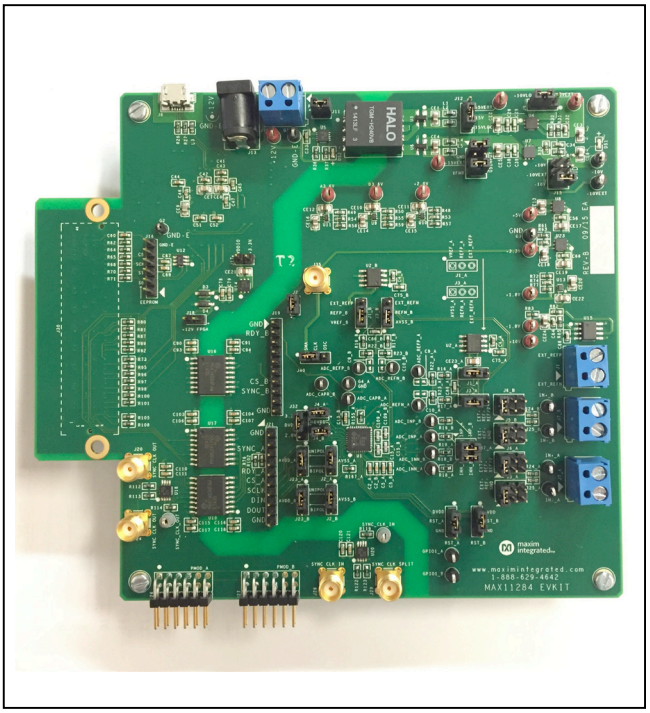
Windows and Windows XP are registered trademarks and registered service marks of Microsoft Corporation.

Features

- High-Speed USB, FMC Connector, and Pmod connectors
- 5MHz SPI Interface
- Various Sample Sizes and Sample Rates
- Collects Up to 1 Million Samples (with FPGA platform)
- Time Domain, Frequency Domain, and Histogram Plotting
- Sync In and Sync Out for Coherent Sampling for Higher Input Frequency (with FPGA platform)
- On-Board 2.5V Voltage References (MAX6126)
- Proven PCB Layout
- Fully Assembled and Tested
- Windows XP, Windows 7 and Windows 8-Compatible Software

***Ordering Information* appears at end of data sheet.**

MAX11284 EV Kit Photo



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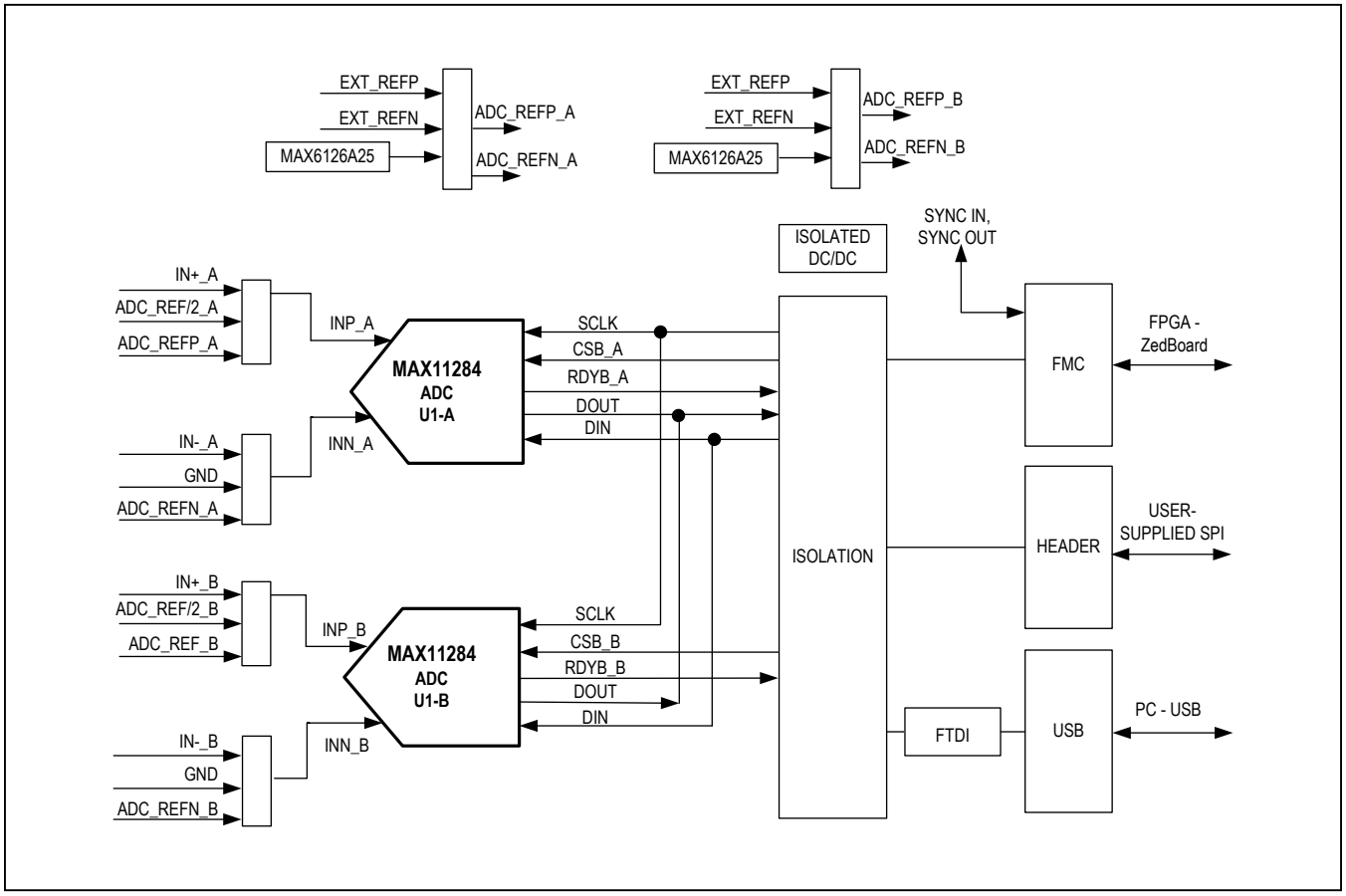
System Block Diagram



MAX11284 EV Kit Files

FILE	DECRIPTION
MAX11284EVKitSetupVx.x.exe	Application Program (GUI)
Boot.bin	ZedBoard Firmware (SD Card to boot Zynq)

Quick Start

Required Equipment

- MAX111284 EV kit
- +12V (500mA) power supply
- Micro-USB cable
- ZedBoard development board with Vivado Design Suite 14.3 or higher (optional – **Not Included** with EV kit)
- Function generator (Audio Precision 2700 series, additional channels required for unipolar mode)
- Windows XP, Windows 7 or Windows 8 PC with a spare USB port

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV system software. Text in **bold and underline** refers to items from the Windows operating system.

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

1) Visit **www.maximintegrated.com/evkitsoftware** to download the latest version of the EV kit software, MAX11284EVKit.ZIP. Save the EV kit software to a temporary folder and uncompressed the ZIP file.
2) Install the EV kit software and USB driver on your computer by running the MAX11284EVKitSetupVx.x.exe program inside the temporary folder. The program files are copied to your PC and icons are created in the Windows **Start | Programs** menu. At the end of the installation process the installer will launch the installer for the FTDI Chip CDM drivers.

For Standalone mode:

3) Verify that all jumpers are in their default positions for the EV kit (Table 1)
4) Connect the micro-USB cable from the PC to the J8 connector of the EV kit.
5) Connect the +12V adapter to the J13 connector of the EV kit.
6) Start the EV kit software by opening its icon in the **Start | Programs** menu. The EV kit software appears as shown in Figure 1. Verify that the lower-right status bar indicates the EV Kit hardware is **Connected**.
7) From the Device menu select **Standalone** and click **Search for USB Device**. Then select **Standalone** again and select a device in the list. Verify that the lower left status bar indicates the EV Kit hardware is **Connected**.

For FPGA mode (when connected to a ZedBoard):

8) Connect the Ethernet cable from the PC to the J11 connector of the ZedBoard and configure the **Internet Protocol Version 4 (TCP/Ipv4)** properties in the local area Connection to IP address **192.168.1.2** and subnet Mask to **255.255.255.0**.

Note: If an ethernet port is not available on the PC, then please use the option of ethernet to USB port adapter.

9) Verify that the J12 slot of the ZedBoard SD card contains the boot.bin file for the MAX11284 EV Kit.
10) Connect the EV Kit FMC connector (J2) to the ZedBoard FMC connector (J1). Gently press them together.
11) Verify that all jumpers are in their default positions for the ZedBoard (Table 2) and EV kit (Table 1).
12) Connect the +12V wall adapter power supply to the J20 connector of the ZedBoard. Leave the ZedBoard powered off. Connect the PC to the ZedBoard with an Ethernet cable.
13) Enable the power supply of the ZedBoard by sliding SW8 to on.
14) Start the EV kit software by opening its icon in the **Start | Programs** menu. The EV kit software appears as shown in Figure 1. From the **Device** menu select **FPGA**. Verify that the lower-right status bar indicates the EV Kit hardware is **Connected**.

For either Standalone or FPGA Mode:

15) Within the **Delta-Sigma Modulator** group box, select **Unipolar**, **Offset Binary**, and **24-Bit** within the **Format** dropdown list, and and **Continuous** within the **Conversion Mode** dropdown list.
16) Connect the positive terminal of the first signal source to the IN+A test point on the EV kit. Connect the negative terminal of the second signal source to the IN-A test point on the EV kit. The ground of the signal sources must be connect to the ground of the EV kit board.
17) Configure the first signal source to generate a 32.7148Hz, 1.25VP-P sinusoidal wave with +1.875V offset.
18) Configure the second signal source to generate a 32.7148Hz, 1.25V_{P-P} sinusoidal wave with +0.625V offset.
19) Enable both signal sources simultaneously on the function generator.
20) In the **Calibration** group box, select **Self Offset/ Gain** in the drop down list and then click **Calibrate**.
21) Click on the **Scope** tab.
22) Check the **Remove DC** checkbox to remove the DC component of the sampled data.
23) Click the **Capture** button to read sampled data from the ADC.
24) The EV kit software appears as shown in Figure 1 for standalone mode or Figure 2 for FPGA mode.
25) Verify the Frequency is approximately 32.7148Hz displayed on the right. The scope graph has buttons in the upper-right corner that allow zooming in to detail.

Table 1. MAX11284 EV Kit User Configuration Jumper Settings

JUMPER	SHUNT POSITION	DESCRIPTION
J1_A	1-2*	Drive IC REFP_A pin with onboard voltage reference.
	2-3	Drive IC REFP_A pin with external voltage reference.
J1_B	1-2*	Drive IC REFP_B pin with onboard voltage reference.
	2-3	Drive IC REFP_B pin with external voltage reference.
J2	1-2*	Power oscillator (U21) with +3.3V supply.
	Open	Disable U21 by removing power.
J2_A	1-2*	Connect IC AVSS_A to GND (unipolar mode – also set J23_A for unipolar).
	2-3	Connect IC AVSS_A to -1.8V (bipolar mode – also set J23_A for bipolar).
J2_B	1-2*	Connect IC AVSS_B to GND (unipolar mode – also set J23_B for unipolar).
	2-3	Connect IC AVSS_B to -1.8V (bipolar mode – also set J23_B for bipolar).
J3_A	1-2*	Drive IC REFN_A pin with onboard voltage reference.
	2-3	Drive IC REFN_A pin with external voltage reference.
J3_B	1-2*	Drive IC REFN_B pin with onboard voltage reference.
	2-3	Drive IC REFN_B pin with external voltage reference.
J4_A	1-2*	Connect IC to the DVDD_A voltage selection jumper J32.
	open	Attach amp meter between pins 1-2 to measure current consumed by IC DVDD.
J4_B	1-2*	Connect IC to the DVDD voltage selection jumper J32.
	open	Attach amp meter between pins 1-2 to measure current consumed by IC DVDD.
J5_A	1-2	Apply external analog signal to IN-_A.
	3-4	Connect IN-_A to REFN_A.
	5-6	Connect IN-_A to GND.
J5_B	1-2	Apply external analog signal to IN-_B.
	3-4	Connect IN-_B to REFN_B.
	5-6	Connect IN-_B to GND.
J6_A	1-2	Apply analog signal to IN+_A.
	3-4	Connect IN+_A to REFP_A.
	5-6	Connect IN+_A to REF/2_A.
J6_B	1-2	Apply analog signal to IN+_B.
	3-4	Connect IN+_B to REFP_B.
	5-6	Connect IN+_B to REF/2_B.
J9	1-2	Connects the +10V rail to test point +10VEXT for external power
	2-3*	Connects the +10V rail to LDO U4
J11	1-2*	Enables main power supply (U5)
	Open	Disables main power supply (U5)
J12	1-2	Connects the +15V rail to test point +15EXT for external power (powers U4)
	2-3*	Connects the +15V rail to isolation transformer (powers U4)
J14	1-2	Connects U7 input to GND
	3-4	Connects U7 input to test point -15VEXT for external power
	5-6*	Connects U7 input to isolation transformer
J15	5-6*	Connects U7 output to GND, which sets the reference for the -10V supply
J17	1-2*	Connects on-board FTDI chip to 3.3V, necessary for standalone mode
	Open	Disconnects on-board FTDI chip power. This jumper does not interfere with ZedBoard

Table 1. MAX11284 EV Kit User Configuration Jumper Settings (continued)

JUMPER	SHUNT POSITION	DESCRIPTION
J23_A	1-2*	Connect IC AVDD_A to 3.6V (unipolar mode)
	2-3	Connect IC AVDD_A to +1.8V (bipolar mode)
J23_B	1-2*	Connect IC AVDD_B to 3.6V (unipolar mode)
	2-3	Connect IC AVDD_B to +1.8V (bipolar mode)
J32	1-2	Set IC DVDD_A and DVDD_B to +3.3V
	2-3*	Set IC DVDD_A and DVDD_B to +2.0V
J37_A	1-2, 3-4*	Connect IN+_A and IN+_B, and IN-_A and IN-_B together. Used when both channel A and B needs same signal source.
	open	Disconnects IN+_A from IN+_B, and IN-_A from IN-_B. User must apply different signal sources to channel A and B.
J40	1-2	Drive IC CLK pin with signal from SMA connector J35
	2-3*	Drive IC CLK pin with signal from onboard oscillator U21
RST_A	1-2*	Connect IC RSTB_A to DVDD (normal operation)
	2-3	Connect IC RSTB_A to GND (reset state)
RST_B	1-2*	Connect IC RSTB_B to DVDD (normal operation)
	2-3	Connect IC RSTB_B to GND (reset state)

**Default position.*

Table 2. ZedBoard Jumper Settings (optional)

JUMPER	SHUNT POSITION	DESCRIPTION
J18	1-2	VDDIO set for 3.3V
JP11	2-3	Boot from SD card
JP10	1-2	
JP9	1-2	
JP8	2-3	
JP7	2-3	
JP10	—	
J12	n/a	SD card installed
J20	n/a	Connected to 12V wall adapter
SW8	Off	ZedBoard power switch, off while connecting boards

Table 3. MAX11284 EV Kit Connectors

JUMPER	DESCRIPTION
J8	USB connector for standalone mode
J1	External reference input
J7_A	External input for ADC channel A's IN+ and IN-
J7_B	External input for ADC channel B's IN+ and IN-
J10, J13	External power connections, 12V. Both wall adapter and screw terminals are provided. When ZedBoard is used these connectors are not necessary if jumper J18 is installed.
J20, J24	Sync clock out
J26	Pmod A, connects to ADC A
J27	Pmod B, connects to ADC B
J28	Sync clock input, SMA
J29	Split Sync clock in, SMA
J30	FMC connector for use with ZedBoard
J35	External clock input, SMA

General Description of Software

The main window of the EV kit software contains several tabs: **ADC Config**, **Scope**, **DMM**, **Histogram**, **FFT** and **ADC Registers**. The **ADC Config** tab and **ADC Registers** tab provide control to communicate with the MAX11284 registers. The other four tabs are used for evaluating the sample data read from the ADC.

ADC Config Tab

The **ADC Config** tab provides an interface for configuring the IC from a functional perspective. See Figure 1 for standalone mode and Figure 2 for FPGA mode. The main block provides for channel selection(s), calibration, GPIO control, Input path selection, data format, filtering, power, clocking, and sync out clock (FPGA mode only). To begin, select the IC populated on the EV Kit with the drop-down list. To read all the configuration settings, click the **Read All** button in the **Serial Interface** block. When a setting is changed, the register associated with that setting is automatically written. The **Status Log** at the bottom of the GUI shows the value and register that was changed.

The primary mode for calibration is using the drop down list to select a calibration mode, followed by clicking the **Calibrate** button. The checkboxes for **Self Offset**, **Self Gain**, **System Offset** and **System Gain** allow for the user to enable or disable the calibration values. The calibration values can also be changed manually by entering a hex value in the SPI numeric box. Please see the *System Offset and Gain* section of the data sheet for detailed system calibration.

The **Power** block allows the user to put the part in a sleep or standby state by selecting one of these options in the drop down list. The configuration settings can be reset back to default by clicking the **Reset Registers** button. For the **Clock** Source selection, the IC internal clock (default) is always a valid option; make sure a shunt is not on jumper J2 that disables the on-board oscillator. If the external clock is selected, a clock must be applied at the IC CLK pin. For jumper J40, if a shunt is placed on the 1-2 position, it selects the user-supplied clock signal that is applied at the SMA (J35) connector. Please make sure that a shunt is removed from jumper J2 to disable the on-board oscillator. The EV kit has another external option of using the on-board oscillator (U21). Place a shunt to the 2-3 position of jumper J40 and make sure jumper J2 is installed to power on-board oscillator. Once the above configurations are completed, start conversion by clicking the **Convert** button in the **Serial Interface** block. To read the data and status, click the **Read Data and Status** button on the lower-right of the GUI.

To save a configuration, select **Save ADC Config As…** in the **File** menu. This saves all the ADC register values to a XML file. To load a configuration, select **Load ADC Config** in the **File** menu. When the XML file is loaded, all the register values in the file are written to the ADC.

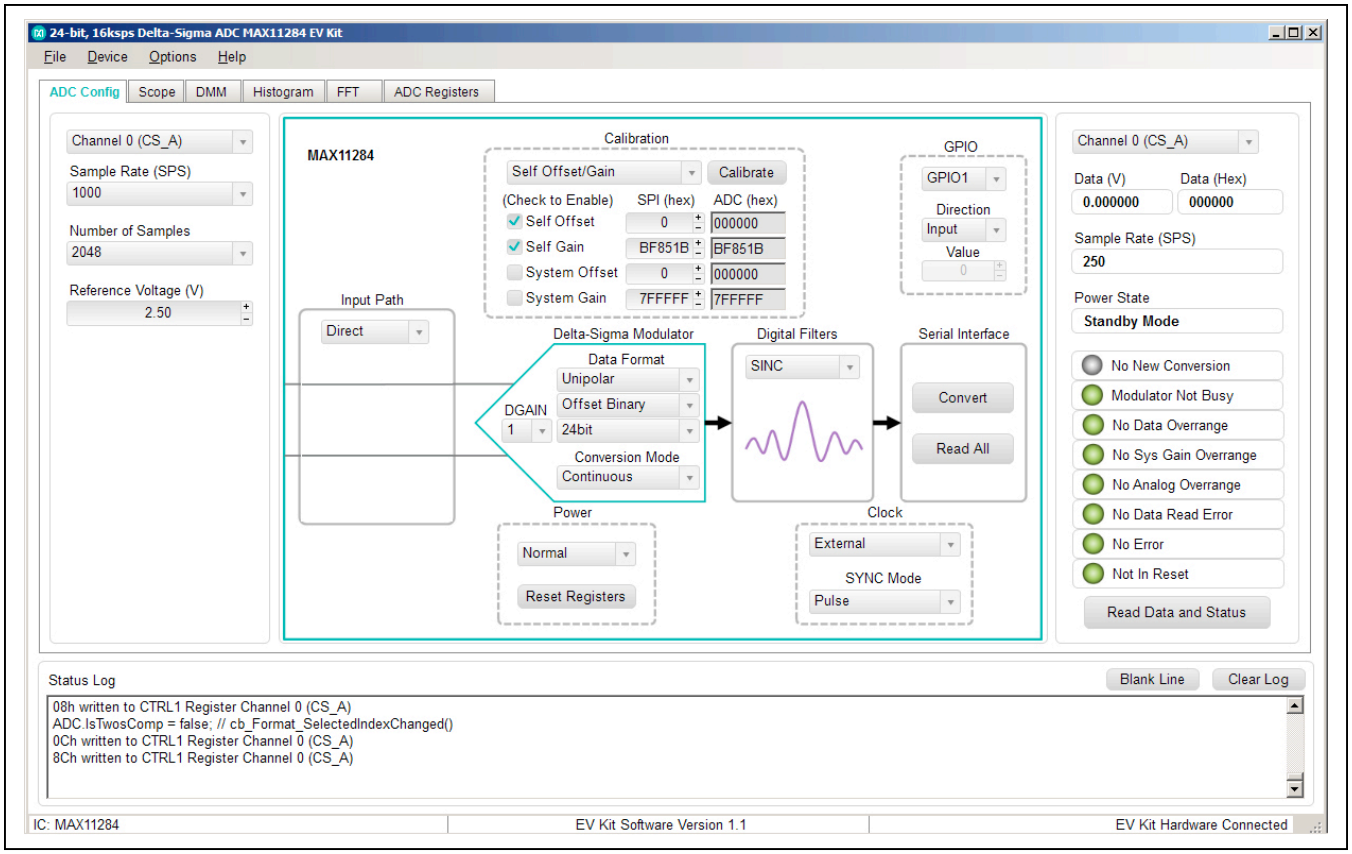


Figure 1. MAX11284 EV Kit Software (Standalone, ADC Config Tab)

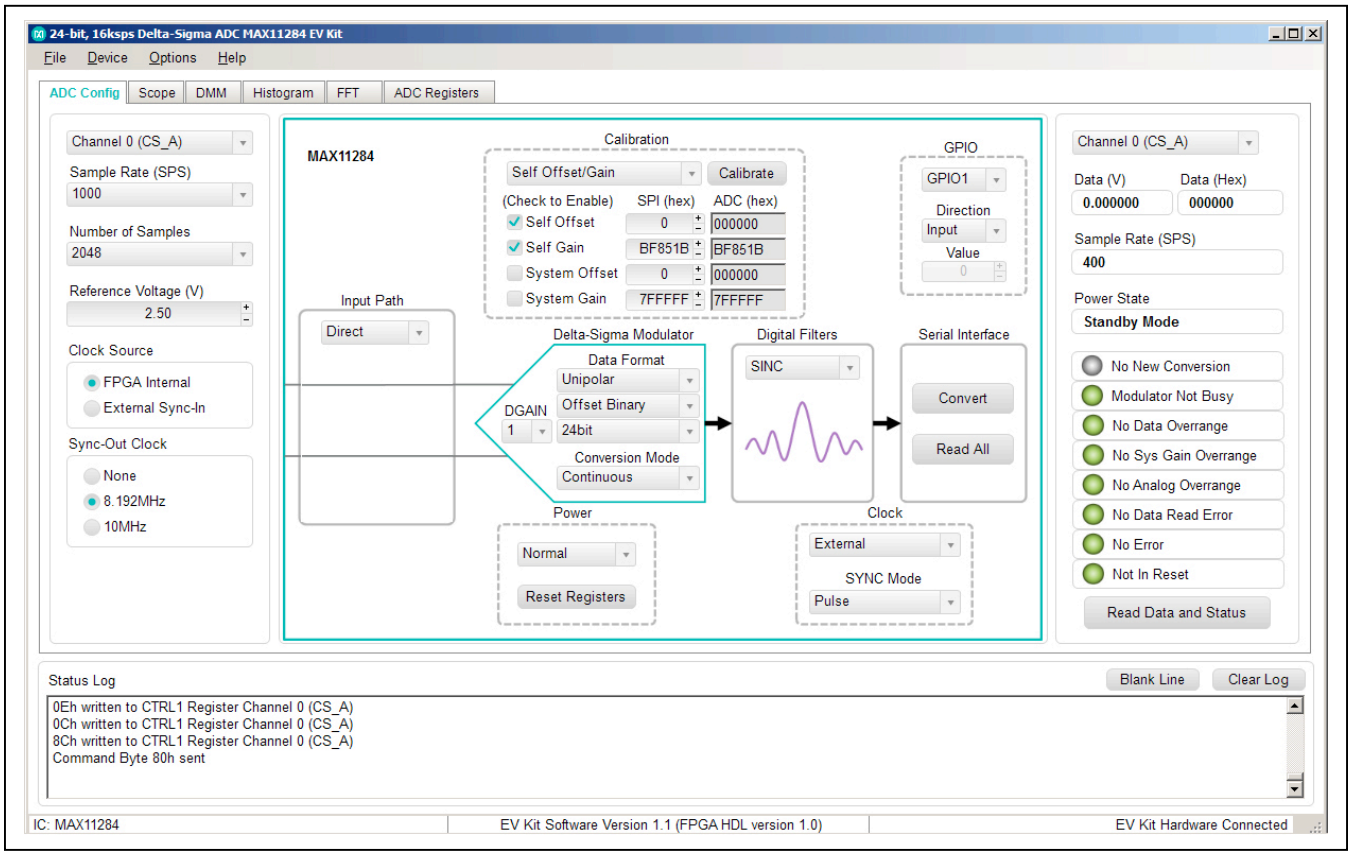


Figure 2. MAX11284 EV Kit Software (FPGA, ADC Config Tab)

Scope Tab

The **Scope** tab sheet is used to capture data and display it in the time domain. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. The **Display Unit** drop-down list allows counts and voltages. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the waveform, such as average, standard deviation, maximum, minimum, and fundamental frequency. Figure 3 displays the ADC data when a sinusoidal signal is applied at the inputs on the EV kit.

To save the captured data to a file, go to **Options > Save Graph > Scope**. This saves the setting on the left and the data captured to a CSV file.

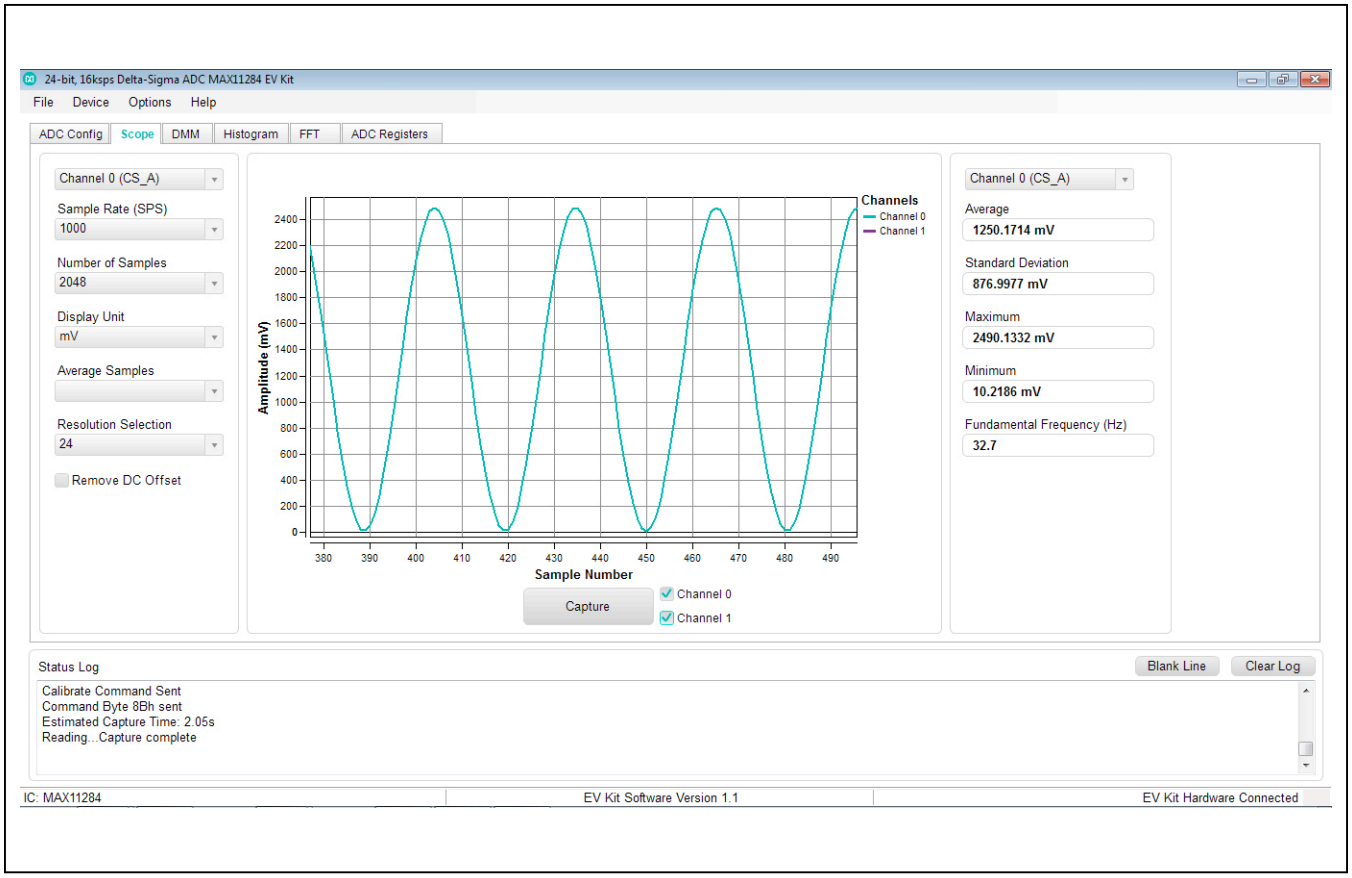


Figure 3. MAX11284 EV Kit Software (Scope Tab)

DMM Tab

The **DMM** tab sheet displays conversion data in a format similar to that of a digital multimeter. Once the desired configuration is set and input is applied, click on the **Capture** button. Figure 4 displays the results shown by the **DMM** tab when IN+A and IN-A are set to ADC_REF/2_A, see Table 1 for jumper positions. The same principle applies for channel B of the device.

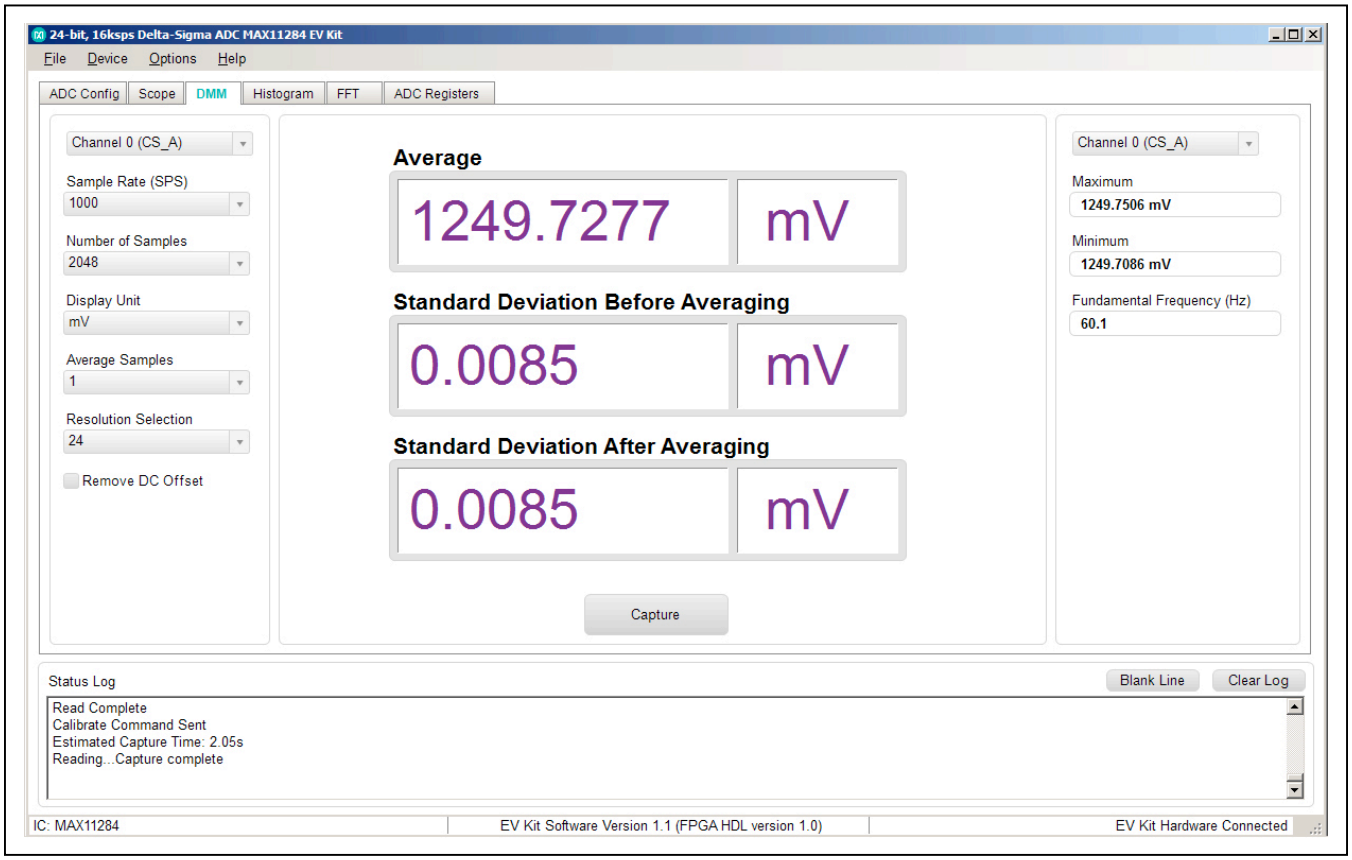


Figure 4. MAX11284 EV Kit Software (DMM Tab)

Histogram Tab

The **Histogram** tab sheet is used to display a histogram of the captured data. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the histogram such as average, standard deviation, maximum, minimum, peak-to-peak noise, effective resolution, and noise-free resolution. To use this histogram feature, apply a DC voltage at the input. Figure 5 displays the results of input referred noise when ADC_INP_A and ADC_INN_A test points are connected to ground. The same principle applies for channel B of the ADC.

To save the histogram data to a file, go to **Options > Save Graph > Histogram**. This saves the setting on the left and the histogram data captured to a CSV file.

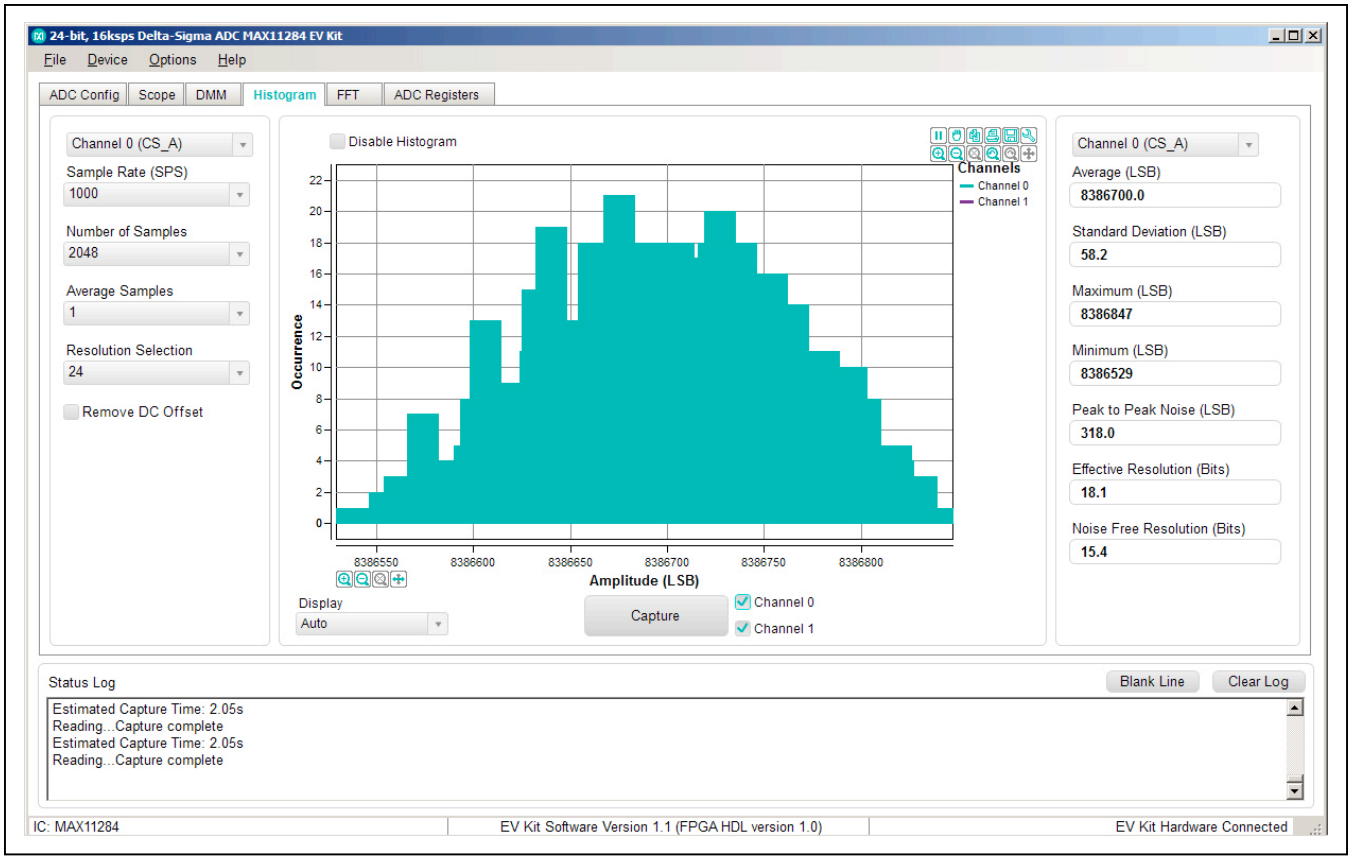


Figure 5. MAX11284 EV Kit Software (Histogram Tab)

FFT Tab

The **FFT** tab sheet (Figure 6) is used to display the FFT of the data. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. Once the desired configuration is set, click on the **Capture** button. The right side of the tab displays the performance based on the FFT, such as fundamental frequency, THD, SNR, SINAD, SFDR, ENOB, and noise floor. The same principle applies for channel B of the ADC.

To save the FFT data to a file, go to **Options > Save Graph > FFT**. This saves the setting on the left and the FFT data captured to a CSV file.

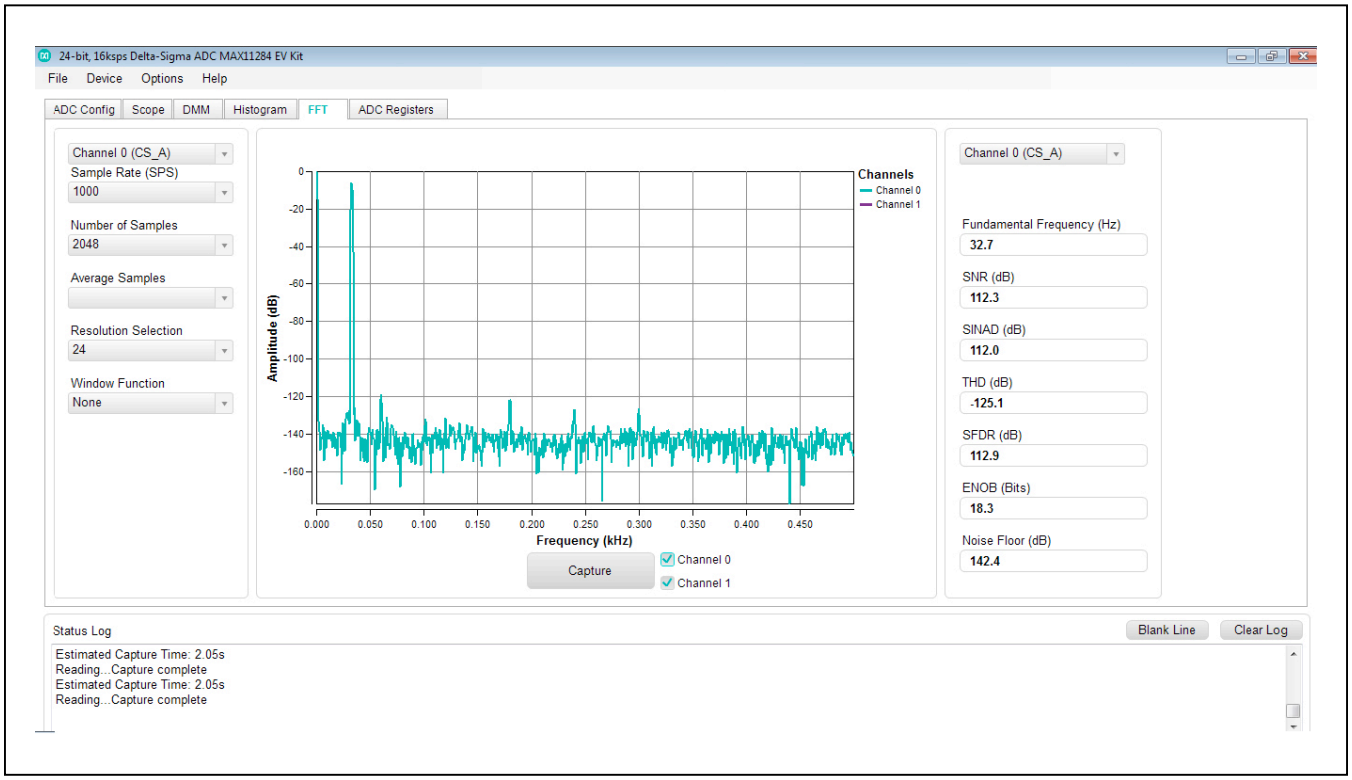


Figure 6. MAX11284 EV Kit Software (FFT Tab)

ADC Registers Tab

The **ADC Registers** tab sheet shows the IC registers on the left. The middle section shows the bits and bit descriptions of the selected register. Click **Read All** to read all registers and refresh the window with the register settings. To write a register first select the hex value in the Value column, type the desired hex value and press **Enter** on the keyboard.

The command byte is on the right side of the tab sheet. This byte precedes all SPI transactions and is described in the IC datasheet. To send a command byte enter a hex value in the numeric box and click the **Send** button. The command byte has two different formats including Conversion Mode and Register Access Mode. Select the radio button for the desired mode to see the bit description in the table.

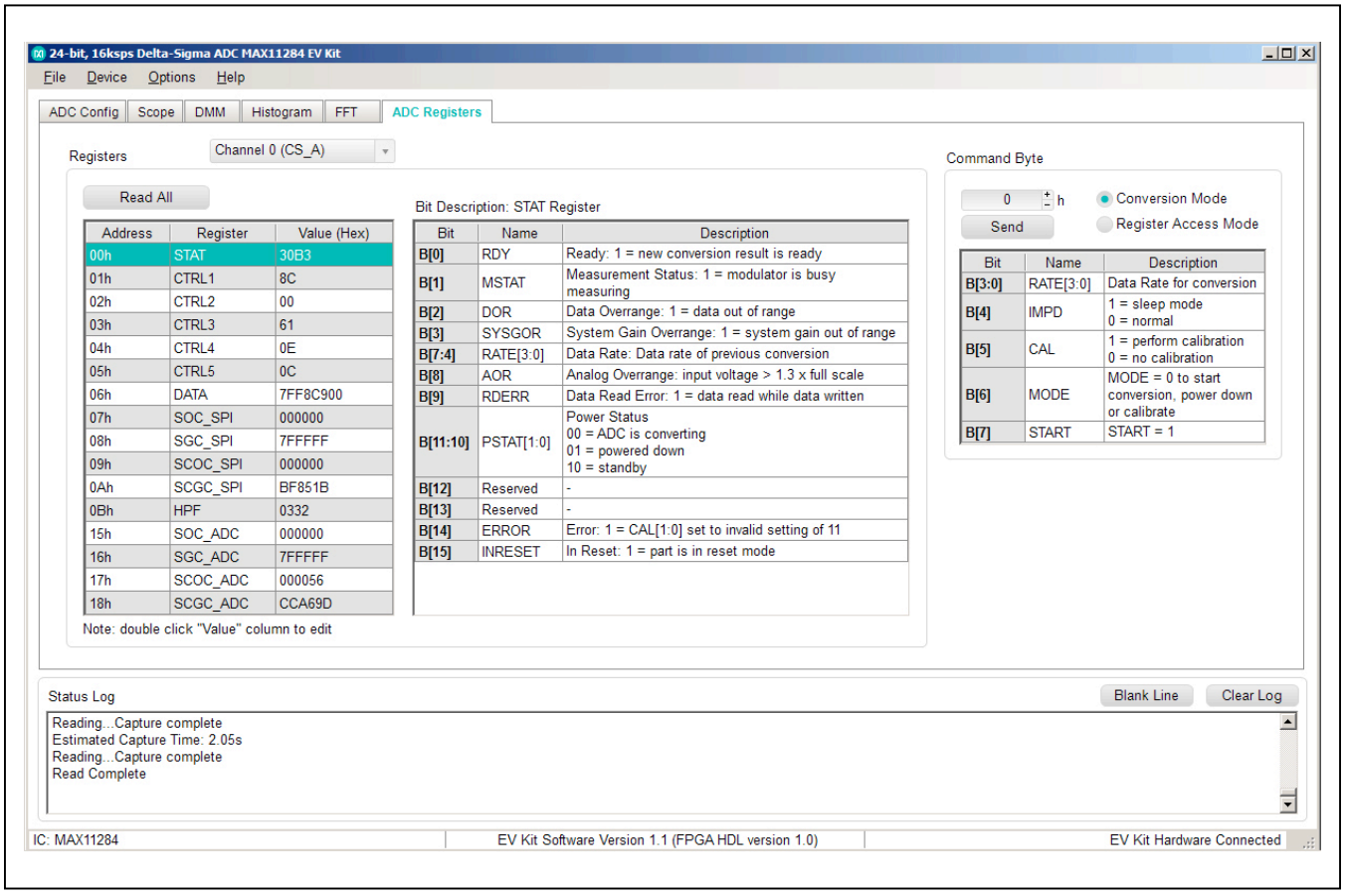


Figure 7. MAX11284 EV Kit Software (ADC Registers Tab)

System Offset and Gain

Control 5 (CTRL5) register is used to calibrate the system offset and gain. NOSYSO bit and NOSYSG bit are “1” only if no system offset and gain calibrations are needed. Change these bit to “0” allows for system offset and gain calibrations. The system offset and gain calibrations are required for each specific gain setting.

Before proceeding with the register writes to CTRL5, set the gain (PGA = xx) to required value.

For System Offset Calculation:

- System offset requires connecting zero volt differentially across the ADC inputs. Once connected, Write 0x48 to CTRL5 register to perform the system offset calibration.

For System Gain Calculation:

- System gain requires connecting an external ADC input pins (at measurement point) to full-scale reference voltage. Make sure to scale down V_{REF} by the gain factor. For gain of 2, the input applied is $V_{REF}/2$, and gain of 4, input applied is $V_{REF}/4$, etc. Once connected, write 0x84 to CTRL5 register to perform a system full-scale calibration.

  After calibration, an analog signal may be applied at the ADC inputs and start conversion.

Detailed Description of Hardware

This EV kit provides a proven layout to demonstrate the performance of the MAX11284 24-bit dual-channel Delta-Sigma ADC. Included in the EV kit are digital isolators (MAX14934), ultra-low-noise LDOs (MAX8842) to all supply pins of the IC, and on-board references (MAX6126).

An onboard controller is provided to allow for evaluation in standalone mode, which has limitations on maximum sample size and it can perform coherent sampling at lower frequencies with a precision analog generator. The EV Kit can be used with ZedBoard to achieve larger sample depth and coherent sampling.

The ADC has several input options which are selectable through J5_A and J6_A for channel A, and J5_B and J6_B for channel B. The external option allows for wires attached to the screw terminals at J7_A and J7_B.

User-Supplied SPI and IO

To evaluate the EV kit with a user-supplied SPI bus, disconnect from the FMC bus and remove jumper J17. Apply the user-supplied SPI and IO signals to SCLK, CS, DIN, DOUT, RDYB, and SYNC at the PMOD_A (J26) and PMOD_B (J27) headers. Make sure the return ground is connected to the system ground. When using PMOD_A and PMOD_B headers, ensure that DIN, DOUT, and SCLK are only driven by one port. The onboard FTDI chip used for standalone mode does not conflict with the user-supplied SPI if it is powered off by removing jumper J17.

Caution: Do not plug this header into a standard peripheral module interface found on other FPGA or microcontroller products. The signal definition is unique to this EV kit.

User-Supplied Reference

For user-supplied reference voltage, place the shunts to the 2-3 position at J1_A and J3_A for channel A, and J1_B and J3_B for channel B, and apply external reference to the terminal connector (J1).

User-Supplied AVSS

The AVSS supply is set to GND or -1.8V by jumper J2_A for channel A and J2_B for channel B. For user-supplied AVSS, remove shunts from J2_A and J2_B and apply AVSS to pin 2 of those jumpers. Make sure that this external supply has the correct relation to system ground.

User-Supplied AVDD

The AVDD supply is set to 3.6V or 1.8V by jumper J23_A for channel A and jumper J23_B for channel B. For user-supplied AVDD, remove the shunts from J23_A and J23_B and apply AVDD to pin 2 of those jumpers. Make sure that this external supply has the correct relation to system ground.

Bipolar Powered vs Unipolar Powered

The IC supports both unipolar and bipolar ranges. For unipolar mode jumper J23_A pins 1-2 to power AVDD with 3.6V and jumper J2_A pins 1-2 to set AVSS to GND. For bipolar mode jumper J23_A pins 2-3 to power AVDD with 1.8V and jumper J2_A pins 2-3 to set AVSS to -1.8V. Same principle applies to channel using jumpers J23_B and J2_B.

External Clock

When the IC is configured to use an external clock, jumper J40 provides the option to select the source. Pins 2-3 selects the onboard oscillator as the clock source and jumper J2 must be installed to power the oscillator. The on-board oscillator is designed for a 3.3V digital DUT supply. If a 2.0V digital DUT supply is used, use an external 2V clock. Jumper J40 pins 1-2 selects the SMA connector (and user-provided clock) as the clock source and jumper J2 must be removed to disable the on-board oscillator.

GPIO1_A and GPIO1_B

Test points are provided for GPIO1_A and GPIO1_B. The ADC Config tab can configure these as input/output and read/drive the GPIO pins.

ADC Inputs

Table 4 provides input options to both ADC channels.

Sync Input and Sync Output

Sync Input and Sync Output is applicable to the ZedBoard and is not used in standalone mode.

The SYNC_CLK_IN SMA accepts an approximate 100MHz waveform signal to generate the system clock of the ZedBoard. For maximum performance, use a low-jitter clock that syncs to the user's analog function generator. See Figure 8.

The SYNC_OUT SMA outputs a 10MHz square wave can be used as reference for signal source. See Figure 9. Both options are used for coherent sampling of the IC. Only one option should be used at a time. The relationship between f_{IN}, f_S, N_{CYCLES}, and $M_{SAMPLES}$ is given as follows:

$$\frac{f_{IN}}{f_S} = \frac{N_{CYCLES}}{M_{SAMPLES}}$$

where:

f_{IN} = Input frequency

f_S = Sampling frequency

N_{CYCLES} = Prime number of cycles in the sampled set

$M_{SAMPLES}$ = Total number of samples

Table 4. Analog Input Configurations

CONFIGURATION		SIGNAL PATH INPUT CONFIGURATION	INPUT CONNECTORS	JUMPER POSITIONS
No.	DESCRIPTION			
1	External Inputs	User-supplied signals	IN+ and IN- (both channels and A and B)	J5_A: 1-2 J6_A: 1-2 J5_B: 1-2 J6_B: 1-2
2	ADC Voltage Reference	Voltage Reference Input to ADC from MAX6126 or external source (see J1_A and J3_A for channel A, and J1_B and J3_B for channel B)	ADC_REFP and ADC_REFN (both channels and A and B)	J5_A: 3-4 J6_A: 3-4 J5_B: 3-4 J6_B: 3-4

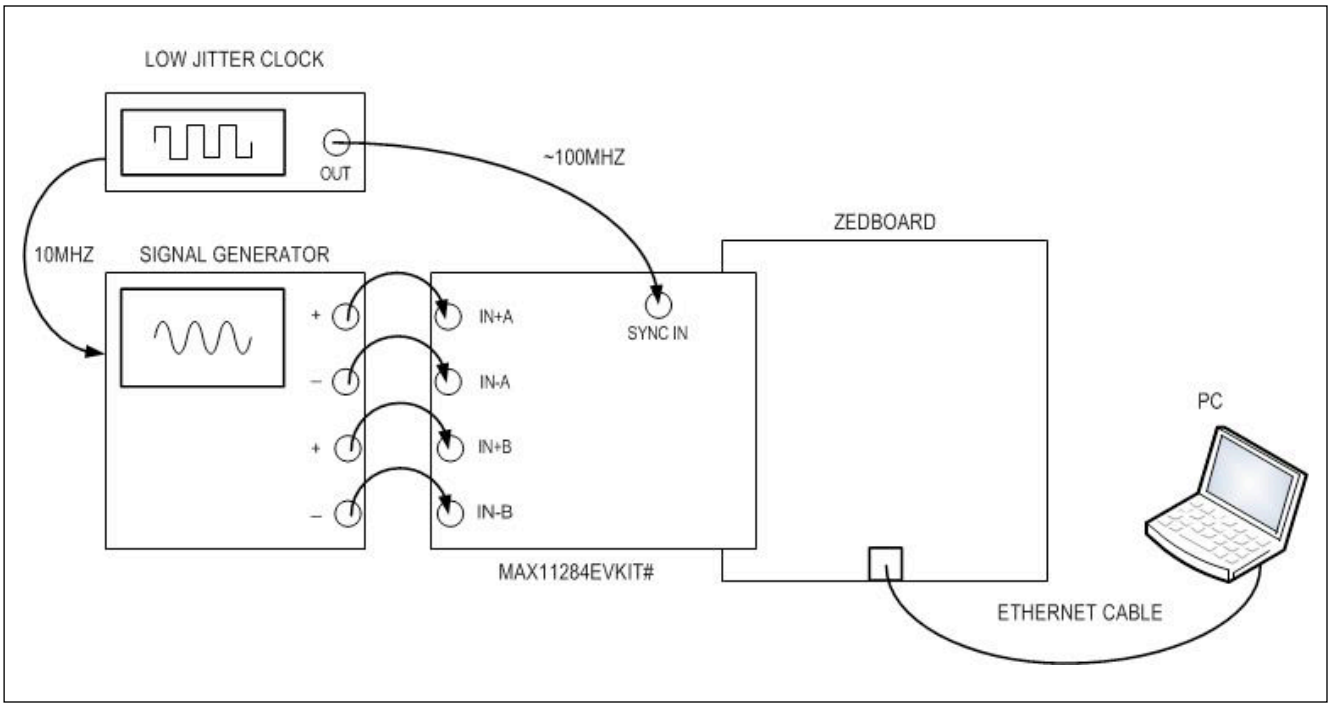


Figure 8. MAX11284 EV Kit Coherent Sampling Setup Using SYNC IN

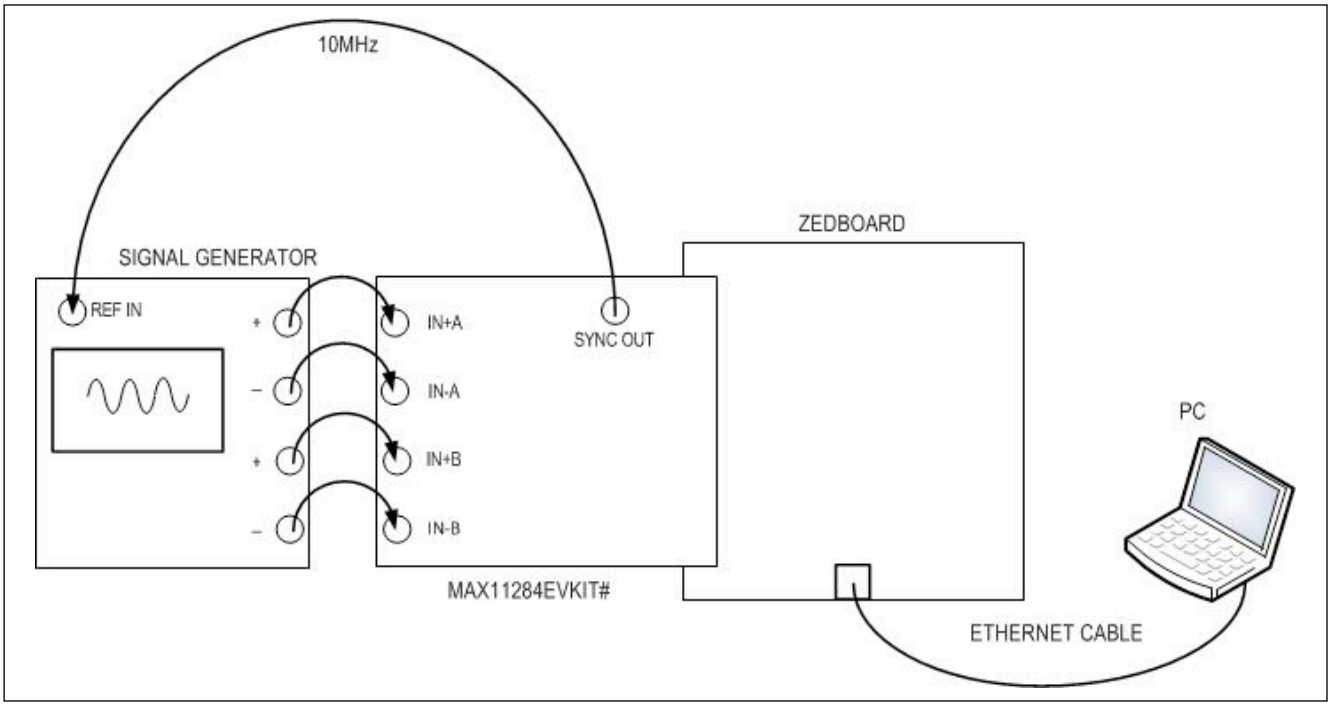


Figure 9. MAX11284 EV kit Coherent Sampling Setup Using SYNC OUT

Component List, PCB Layout, and Schematics

See the following links for component information, PCB layout diagrams, and schematics.

- **MAX11284 EV BOM**
- **MAX11284 EV PCB Layout**
- **MAX11284 EV Schematics**

Ordering Information

PART	TYPE
MAX11284EVKIT#	EVKIT

#Denotes RoHS compliant.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/16	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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TITLE: Bill of Materials
DATE: 09/11/2015
DESIGN: max11284_evkit_b

ITEM	REF_DES	DNI/ DNP	QTY	MFG PART #	MNFCTR	VALUE	DESCRIPTION
1	+5V, +10V, +12V, +1.8V, +2.0V, +3.3V, -1.8V, A3.6V, D3.6V, +10VEXT, +15VEXT, -	-	12	5005	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.35IN; BOARD HOLE=0.063IN; RED; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
2	G1, G3, -10V, G4_A, IN+_A, IN+_B, IN-_A, IN-_B, -10VEXT, GPIO1_A, GPIO1_B, ADC_INN_A, ADC_INN_B, ADC_INP_A, ADC_INP_B, ADC_CAPR_A, ADC_CAPR_B,	-	21	5006	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.35IN; BOARD HOLE=0.063IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
3	C2_A, C2_B, C3_A, C3_B, C5_A, C5_B	-	6	GRM188R71C103KA01; ECJ-1VB1C10; CL10B103KO8NNN	MURATA; PANASONIC; SAMSUNG	0.01UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.01UF; 16V; TOL=10%; TG=-55 DEGC TO +125 DEG; TC=X7R
4	C28, C32, C34, C38, C41-C47, C51, C52, C56, C66, C67, C79, C84, C88, C93, C94, C106, C107, C110, C117, C118, C120, C170, C4_A, C4_B, C6_A,	-	38	C0603C104K3RAC; GRM188R71E104KA01; C1608X7R1E104K	KEMET/MURATA/TDK	0.1UF	CAPACITOR; SMT; 0603; CERAMIC; 0.1uF; 25V; 10%; X7R; -55degC to + 125degC; +/-15% from -55degC to +125degC;
5	C11_A, C11_B, C12_A, C12_B	-	4	GRM1885C1H102FA01	MURATA	1000PF	CAPACITOR; SMT (0603); CERAMIC CHIP; 1000PF; 50V; TOL=1%; MODEL=GRM SERIES; TG=-55 DEGC TO +125 DEGC; TC=C0G
6	C60, C69, C78, C90, C91, C103, C104, C115, C116, C13_A, C13_B	-	11	C0603C105K4RAC; GRM188R71C105KA12; C1608X7R1C105K; EMK107B7105KA	KEMET/MURATA/TDK/TAIYO YUDEN	1UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 1UF; 16V; TOL=10%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=X7R
7	C14_A, C14_B, C15_A, C15_B	-	4	C1608C0G1E103J	TDK	0.01UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.01UF; 25V; TOL=5%; MODEL=; TG=-55 DEGC TO +125 DEGC;
8	C29, C39	-	2	C0603C181K5GAC	KEMET	180PF	CAPACITOR; SMT (0603); CERAMIC CHIP; 180PF; 50V; TOL=10%; MODEL=C0G; TG=-55 DEGC TO +125 DEGC; TC=+/

9	C33	-	1	GRM188R71E474KA12	MURATA	0.47UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.47UF; 25V; TOL=10%; MODEL=GRM SERIES; TG=-55 DEGC TO +125 DEGC; TC=X7R
10	C86_A, C86_B, C109_A, C109_B	-	4	C0603C102J5GAC; 06035A102JAT2A	KEMET/AVX/ MURATA	1000PF	CAPACITOR; SMT; 0603; CERAMIC; 1000pF; 50V; 5%; C0G; -55degC to +125degC, USE 20-1000p-E4 FOR NEW DESIGN
11	C111, C121	-	2	C0603C102K5RAC; GRM188R71H102KA01; C0603X7R500-102KNE	KEMET/MURATA/VENKEL	1000PF	CAPACITOR; SMT; 0603; CERAMIC; 1000pF; 50V; 10%; X7R; -55degC to + 125degC; +/-15% from -55degC to +125degC, USE 20-1000p-E4 FOR NEW
12	C126, C127	-	2	C0603C0G500-180JNE; C1608C0G1H180J; GRM1885C1H180J	VENKEL LTD./TDK/MURATA	18PF	CAPACITOR; SMT (0603); CERAMIC CHIP; 18PF; 50V; TOL=5%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=C0G
13	CE1, CE2, CE4, CE5, CE10-CE12, CE14-CE17, CE19, CE20, CE22, CE24	-	15	C0805X7R250-105KNE; TMK212BJ10;TMK212B7105KG-T;GRM21BR71E105KA9	VENKEL LTD./TAIYO YUDEN/MURATA	1UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 1UF; 25V; TOL=10%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=X7R-
14	CE3, CE6, CE13, CE18, CE21, CE26	-	6	TMK212BBJ106KG-T; CL21A106KAFN3N	TAIYO YUDEN	10UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 10UF; 25V; TOL=10%; MODEL=; TG=-55 DEGC TO +85 DEGC;
15	CE7-CE9	-	3	GRM21BR61E475KA	MURATA	4.7UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 4.7UF; 25V; TOL=10%; MODEL=X5R; TG=-55 DEGC TO +125 DEGC; TC=+/
16	CE23B, CE23_A	-	2	C2012X7R1E475K125AB	TDK	4.7UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 4.7UF; 25V; TOL=10%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=X7R
17	D1_A, D1_B, D2_A, D2_B	-	4	BAT54S	FAIRCHILD SEMICONDUCTOR	BAT54S	DIODE; SCH; SCHOTTKY DIODE; SMT (SOT-23); PIV=30V; IF=0.2A
18	D3, D4, DB1	-	3	MBR0520L	FAIRCHILD SEMICONDUCTOR	MBR0520L	DIODE, SCHOTTKY, SOD-123, PIV=20V, Vf=0.385V@If=0.5A, If(ave)=0.5A
19	DS1, DSB1	-	2	LG L29K-G2J1-24	OSRAM	LG L29K-G2J1-24	DIODE; LED; SMT (0603); Vf=1.7V; If(test)=0.002A; -40 DEGC TO +100 DEGC
20	DS2	-	1	LS L29K-G1J2-1-Z	OSRAM	LS L29K-G1J2-1-	DIODE; LED; SMART; RED; SMT (0603); PIV=1.8V; IF=0.02A; -40 DEGC TO +100 DEGC

21	G2	-	1	5001	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
22	J1, J10, J7_A, J7_B	-	4	OSTTA020161	ON-SHORE TECHNOLOGY INC.	OSTTA020161	CONNECTOR; FEMALE; THROUGH HOLE; 5MM TERMINAL BLOCK CONNECTOR; STRAIGHT; 2PINS
23	J32, J40, J1_A-J3_A, J1_B-J3_B, J23_A, J23_B, RST_A, RST_B	-	12	PBC03SAAN	SULLINS	PBC03SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 3PINS; -65 DEGC TO +125 DEGC
24	J2, J11, J17, J18, J4_A, J4_B	-	6	PCC02SAAN	SULLINS	PCC02SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT THROUGH; 2PINS; -65 DEGC TO +125
25	J14, J15, J5_A, J5_B, J6_A, J6_B	-	6	PBC03DAAN	SULLINS ELECTRONICS CORP.	PBC03DAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 6PINS; -65 DEGC TO +125 DEGC
26	J8	-	1	10118192-0001LF	FCI CONNECT	10118192-	CONNECTOR; FEMALE; SMT; MICRO USB B TYPE RECEPTACLE; RIGHT ANGLE; 5PINS
27	J9, J12	-	2	PBC03SABN	SULLINS	PBC03SABN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 3PINS
28	J13	-	1	KLDX-0202-B	KYCON	KLDX-0202-B	CONNECTOR; FEMALE; THROUGH HOLE; DC POWER JACK; RIGHT ANGLE; 3PINS
29	J16	-	1	PBC06SAAN	SULLINS ELECTRONICS CORP.	PBC06SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 6PINS; -65 DEGC TO +125 DEGC
30	J19, J21	-	2	PBC10SAAN	SULLINS ELECTRONICS CORP.	PBC10SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 10PINS; -65 DEGC TO +125 DEGC
31	J20, J24, J28, J29, J35	-	5	73391-0060	MOLEX	73391-0060	CONNECTOR; FEMALE; THROUGH HOLE; SMA JACK CONNECTOR; STRAIGHT; 5PINS
32	J26, J27	-	2	TSW-106-08-S-D-RA	SAMTEC	TSW-106-08-S-D-RA	CONNECTOR; THROUGH HOLE; DOUBLE ROW; RIGHT ANGLE; 12PINS;
33	J30	-	1	ASP-134604-01	SAMTEC	ASP-134604-01	CONNECTOR; MALE; SMT; HIGH SPEED/HIGH DENSITY OPEN PIN FIELD TERMINAL ARRAY; STRAIGHT; 160PINS

34	J37_A	-	1	PEC02DAAN	SULLINS ELECTRONIC CORP.	PEC02DAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 4PINS
35	L1-L5	-	5	MPZ1608S601A	TDK	600	INDUCTOR; SMT (0603); FERRITE-BEAD; 600; TOL=+/-25%; 1A; -55 DEGC TO +125 DEGC
36	MECH1-MECH4	-	4	24427	GENERIC PART	24427	STANDOFF; FEMALE-THREADED; HEX; M2.5; 20MM; ALUMINUM
37	R16_A, R16_B, R17_A, R17_B	-	4	CR0603-16W-000T; CR0603-16W-000RJT	VENKEL LTD.	0	RESISTOR; 0603; 0 OHM; 5%; JUMPER; 0.063W; THICK FILM
38	R18_A, R18_B, R19_A, R19_B	-	4	CRCW060310R0FK; MCR03EZPFX10R0	VISHAY DALE/ROHM	10	RESISTOR; 0603; 10 OHM; 1%; 100PPM; 0.10W; THICK FILM
39	R20_A, R20_B	-	2	CRCW0603100RFK; ERJ-3EKF1000	VISHAY DALE/PANASONIC	100	RESISTOR; 0603; 100 OHM; 1%; 100PPM; 0.10W; THICK FILM
40	R30, R35, R61, R82, R21_A, R21_B	-	6	CRCW06031003FK; ERJ-3EKF1003	VISHAY DALE/PANASONIC	100K	RESISTOR; 0603; 100K; 1%; 100PPM; 0.10W; THICK FILM
41	R130, R131, R133, R136, R138, R140, R145, R146, R148, R22_A, R22_B, R23_A, R23_B	-	13	CRCW060310K0FK; 9C06031A1002FK; ERJ-3EKF1002	VISHAY DALE/YAGEO PHICOMP/PANASONIC	10K	RESISTOR; 0603; 10K; 1%; 100PPM; 0.10W; THICK FILM
42	R24_A, R24_B, R25_A, R25_B	-	4	CRCW06034R99FK	VISHAY DALE	4.99	RESISTOR; 0603; 4.99 OHM; 1%; 100PPM; 0.1W; THICK FILM
43	R26, R27, R62, R64, R65, R68, R70, R71, R73, R76, R80, R81, R87, R89, R92, R95-R98, R100-R102, R105, R108, R132, R134, R137, R139, R141, R143, R144, R147, R149, R150, R152-R154,	-	45	ERJ-3EKF28R0V	PANASONIC	28	RESISTOR; 0603; 28 OHM; 1%; 100PPM; 0.10W; THICK FILM
44	R31, R40	-	2	CRCW0603715KFK	VISHAY DALE	715K	RESISTOR; 0603; 715K OHM; 1%; 100PPM; 0.10W; METAL FILM
45	R36, R37, R124, R125	-	4	CRCW06031001FK; ERJ-3EKF1001V	VISHAY DALE; PANASONIC	1K	RESISTOR; 0603; 1K; 1%; 100PPM; 0.10W; THICK FILM

46	R48, R77, R151	-	3	CRCW06030000ZS; MCR03EZPJ000; ERJ-3GEY0R00	VISHAY DALE/ROHM/ PANASONIC	0	RESISTOR; 0603; 0 OHM; 0%; JUMPER; 0.10W; THICK FILM
47	R49, R50	-	2	CRCW06036K04FK	VISHAY DALE	6.04K	RESISTOR; 0603; 6.04K; 1%; 100PPM; 0.10W; THICK FILM
48	R53	-	1	CRCW0603150KFK	VISHAY DALE	150K	RESISTOR, 0603, 150K OHM,1%, 100PPM, 0.10W, THICK FILM
49	R54, R55	-	2	ERJ-3EKF4533V	PANASONIC	453K	RESISTOR; 0603; 453K OHM; 1%; 100PPM; 0.10W; THICK FILM
50	R57-R59, R72	-	4	CRCW0603237KFK; ERJ3EKF2373V	VISHAY DALE/PANASONIC	237K	RESISTOR; 0603; 237K OHM; 1%; 100PPM; 0.10W; THICK FILM
51	R63	-	1	ERJ-3EKF1693V	PANASONIC	169K	RESISTOR; 0603; 169K OHM; 1%; 100PPM; 0.10W; THICK FILM
52	R74	-	1	CRCW0603105KFK	VISHAY DALE	105K	RESISTOR; 0603; 105K OHM; 1%; 100PPM; 0.10W; THICK FILM
53	R83	-	1	CRCW0603100RJN	VISHAY DALE	100	RESISTOR; 0603; 100 OHM; 5%; 200PPM; 0.10W; THICK FILM
54	R85	-	1	CRCW060339K0FK	VISHAY DALE	39K	RESISTOR, 0603, 39K OHM, 1%, 100PPM, 0.10W, THICK FILM
55	R112-R114, R119, R122, R123, R166, R161_A, R167_A	-	9	CRCW060349R9FK	VISHAY DALE	49.9	RESISTOR; 0603; 49.9 OHM; 1%; 100PPM; 0.10W; THICK FILM
56	R128	-	1	CRCW060312K0FK	VISHAY DALE	12K	RESISTOR, 0603, 12K OHM, 1%, 100PPM, 0.10W, THICK FILM
57	R129	-	1	CRCW060315K0FK	VISHAY DALE	15K	RESISTOR, 0603, 15K OHM,1%, 100PPM, 0.10W, THICK FILM
58	R135	-	1	CRCW06032K20FK	VISHAY DALE	2.2K	RESISTOR, 0603, 2.2K OHM, 1%, 100PPM, 0.10W, THICK FILM
59	R142	-	1	CRCW06034K70FK	VISHAY DALE	4.7K	RESISTOR; 0603; 4.7K; 1%; 100PPM; 0.10W; THICK
60	SCREW1-SCREW4	-	4	29301	KEYSTONE	29301	MACHINE SCREW; SLOTTED; PAN; M2.5; 6MM; STEEL; ZINC PLATE
61	SU1-SU27	-	27	STC02SYAN	SULLINS ELECTRONICS CORP.	STC02SYAN	TEST POINT; JUMPER; STR; TOTAL LENGTH=0.256IN; BLACK; INSULATION=PBT CONTACT=PHOSPHOR BRONZE; COPPER PLATED TIN OVERALL

62	SYNC_CLK_IN, SYNC_CLK_OUT	-	2	5123	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.35IN; BOARD HOLE=0.063IN; GRAY; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
63	T1	-	1	TGM-H240V8LF	HALO ELECTRONICS, INC	TGM-H240V8LF	TRANSFORMER; SMT; 1:1:1.3:1.3; DC/DC CONVERTER
64	U1	-	1	MAX11284EUG+	MAXIM	MAX11284EUG	EVKIT PART; IC; PACKAGE CODE T4066-5; TQFN40-EP
65	U2_A,U2_B	-	2	MAX6126AASA25+	MAXIM	MAX6126AASA25	IC; SERIES VOLTAGE REFERENCE; ULTRA HIGH PRECISION; ULTRA LOW NOISE VOLTAGE REFERENCE; SOIC8 150MIL; Vout=2.5V, 3ppm/degC max TEMPCO
66	U3, U6	-	2	BAS4002A-RPP	INFINEON	BAS4002A-RPP	DIODE; SCH; LOW VF SCHOTTKY DIODE ARRAY; SMT (SOT-143); PIV=40V; IF=0.2A
67	U4,U7,U23	-	3	MAX15006CATT+	MAXIM	MAX15006CAT	IC; VREG; ULTRA-LOW QUIESCENT-CURRENT LINEAR REGULATOR; TDFN6-EP 3X3
68	U5	-	1	MAX13256ATB+	MAXIM	MAX13256ATB	IC; DRV; 36V H-BRIDGE TRANSFORMER DRIVER FOR ISOLATED SUPPLIES; TDFN10-EP 3X3
69	U8	-	1	MAX15006BATT+	MAXIM	MAX15006BAT	IC; VREG; ULTRA-LOW QUIESCENT-CURRENT LINEAR REGULATOR; TDFN6-EP 3X3
70	U9-U11,U13	-	4	MAX8842ELT+	MAXIM INTEGRATED	MAX8842ELT+	IC; VREG; ULTRA-LOW-NOISE; HIGH PSRR; LOW-DROPOUT; LINEAR REGULATOR; UDFN6 1.5MM X 1.0MM
71	U12, UB1	-	2	93LC66BT-I/OT	MICROCHIP	93LC66BT-I/OT	IC; EPROM; 4K MICROWIRE SERIAL EEPROM; SOT23-6
72	U14	-	1	MAX15006AATT+	MAXIM	MAX15006AAT	IC; VREG; ULTRA-LOW QUIESCENT-CURRENT LINEAR REGULATOR; TDFN6-EP 3X3
73	U15	-	1	MAX664ESA	MAXIM	MAX664ESA	IC, NEGATIVE VOLTAGE REGULATOR, DUAL MODE, 5V/PROGRAMMABLE, 2V TO 16.5V INPUT VOLTAGE RANGE,VS(MAX)=-18V, SOIC8-150MIL, -40degC TO +85degC
74	U16,U17,U19	-	3	MAX14934FAWE+	MAXIM	MAX14934FA	IC; DISO; 4/0 CHANNEL; 150MBPS; DEFAULT LOW; 5KVRMS DIGITAL ISOLATOR; WSOIC16 300MIL
75	U18, U20	-	2	74LVC2G125DP	NXP	74LVC2G125DP	IC; DRV; DUAL BUS BUFFER/LINE DRIVER; 3-STATE; TSSOP8

76	U21	-	1	FXO-HC730-2.048	FOX	FXO-HC730-2.048	OSCILLATOR; SMT 7X5; 15PF; 2.048MHZ; +/-100PPM
77	UB2	-	1	FT2232HL	FUTURE TECHNOLOGY DEVICES INTL LTD.	FT2232HL	IC; MMRY; DUAL HIGH SPEED USB TO MULTIPURPOSE UART/FIFO; LQFP64
78	YB1	-	1	ABM7-12.000MHZ-D2Y-T	ABRACON	12MHZ	CRYSTAL; SMT ; 18PF; 12MHZ; +/-20PPM; +/-30PPM
79	C8_A-C10_A, C8_B-C10_B	DNP	6	N/A	N/A	?	CAPACITOR; 0603 PACKAGE; GENERIC
80	R186-R188	DNP	3	CR0603-16W-000T; CR0603-16W-000RJT	VENKEL LTD.	0	RESISTOR; 0603; 0 OHM; 5%; JUMPER; 0.063W; THICK FILM
81	-	-	1	AK67421-1-R	ASSMANN	CONNECTOR; MALE; USB; USB2.0 MICRO CONNECTION CABLE;	
82	-	-	1	B00ET4KHJ2	CABLE MATTERS	USB 2.0 TO 10/100	
83	-	-	1	SDC4/4GB	KINGSTON TECHNOLOGY	ACCESSORY; MEMORY CARD;	
TOTA			382				

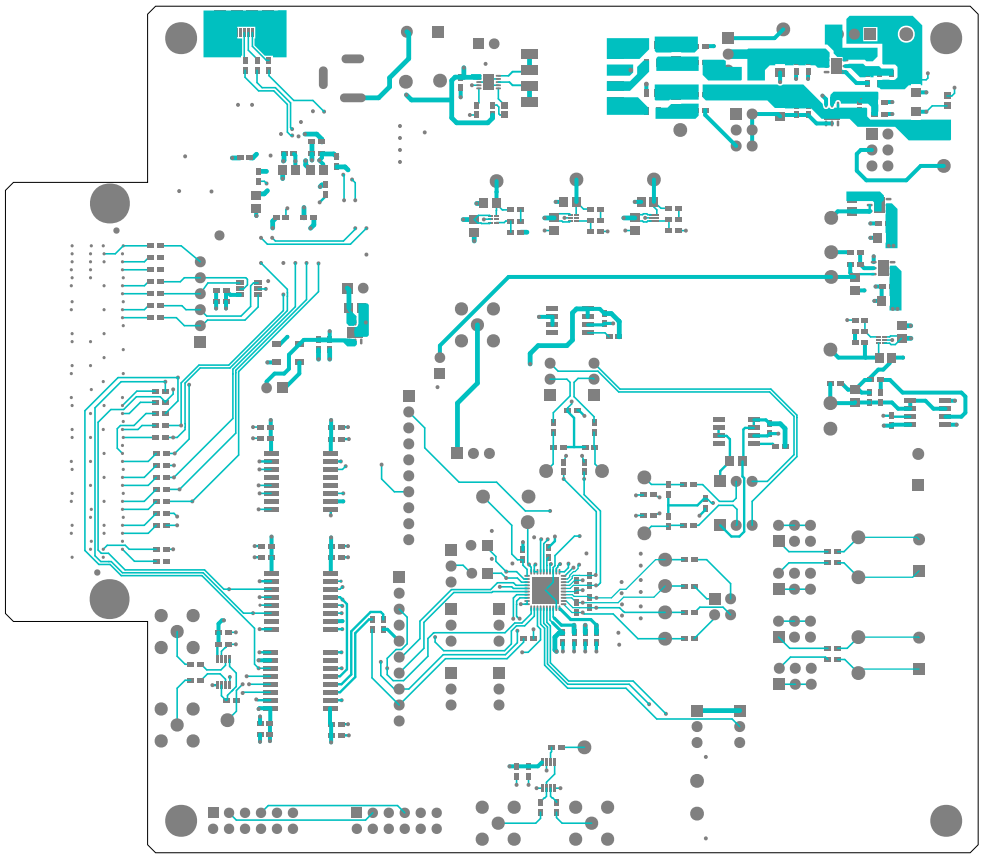
maxim integrated

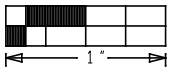
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: TOP





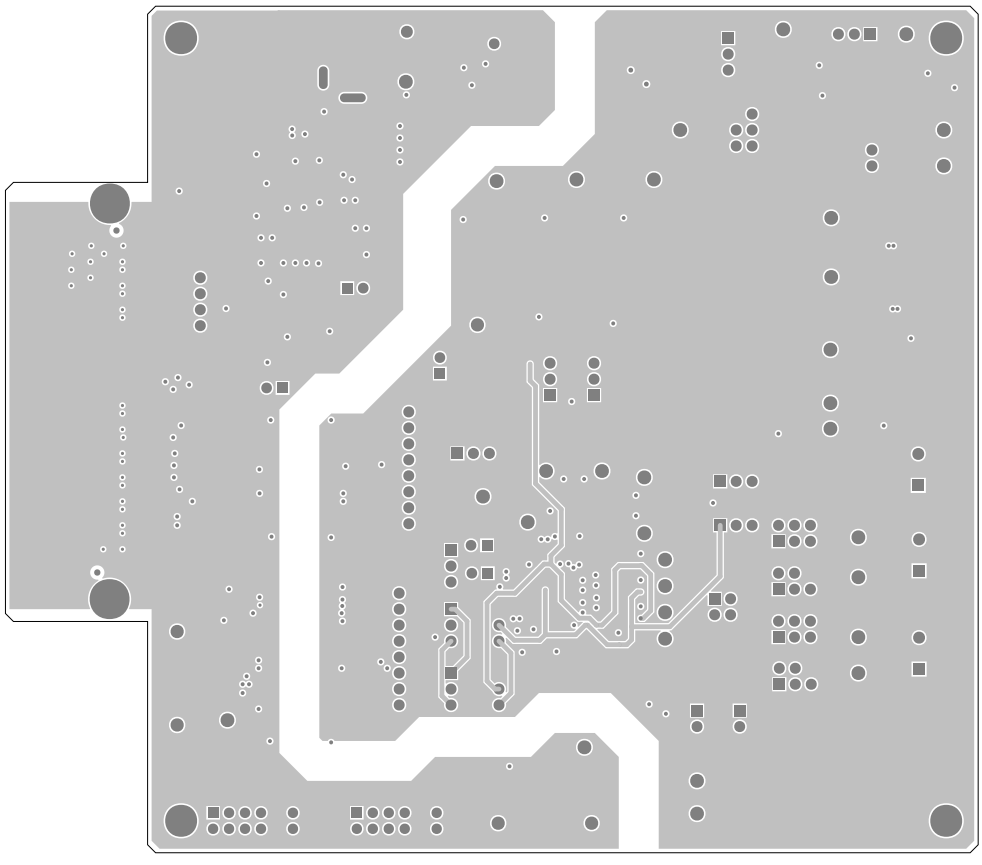
maxim integrated

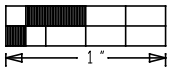
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: INTERNAL2





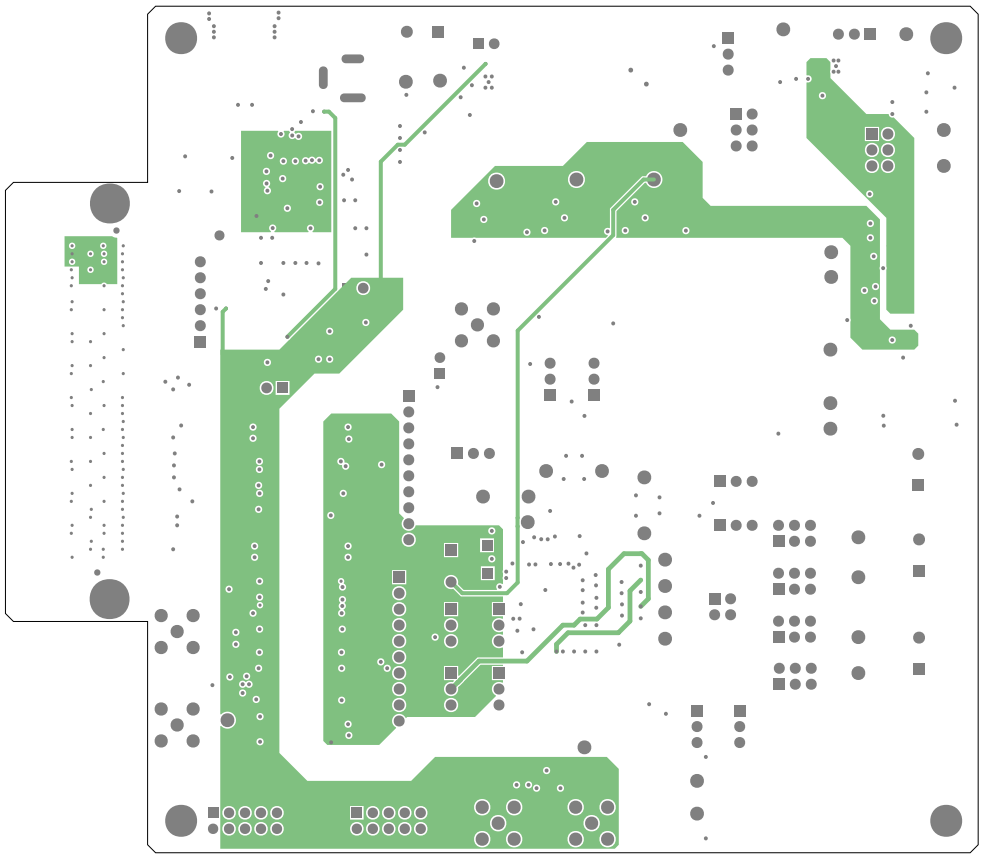
maxim integrated

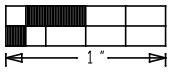
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: INTERNAL3





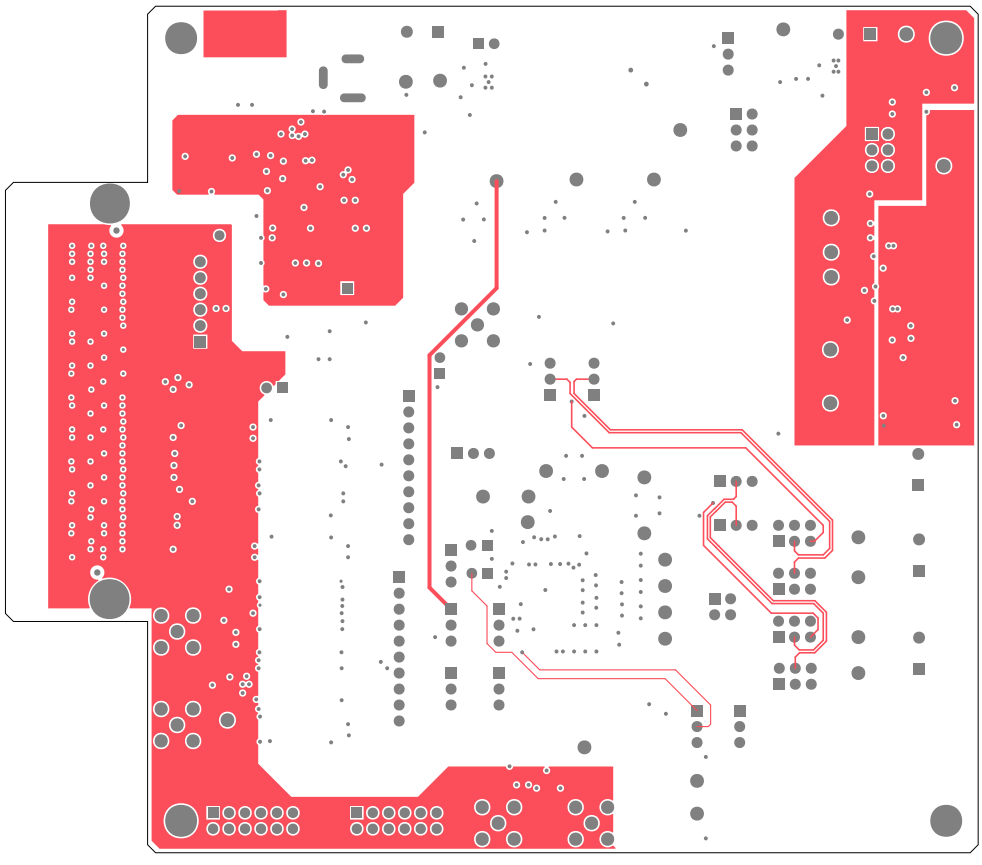
maxim integrated

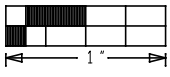
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: INTERNAL4





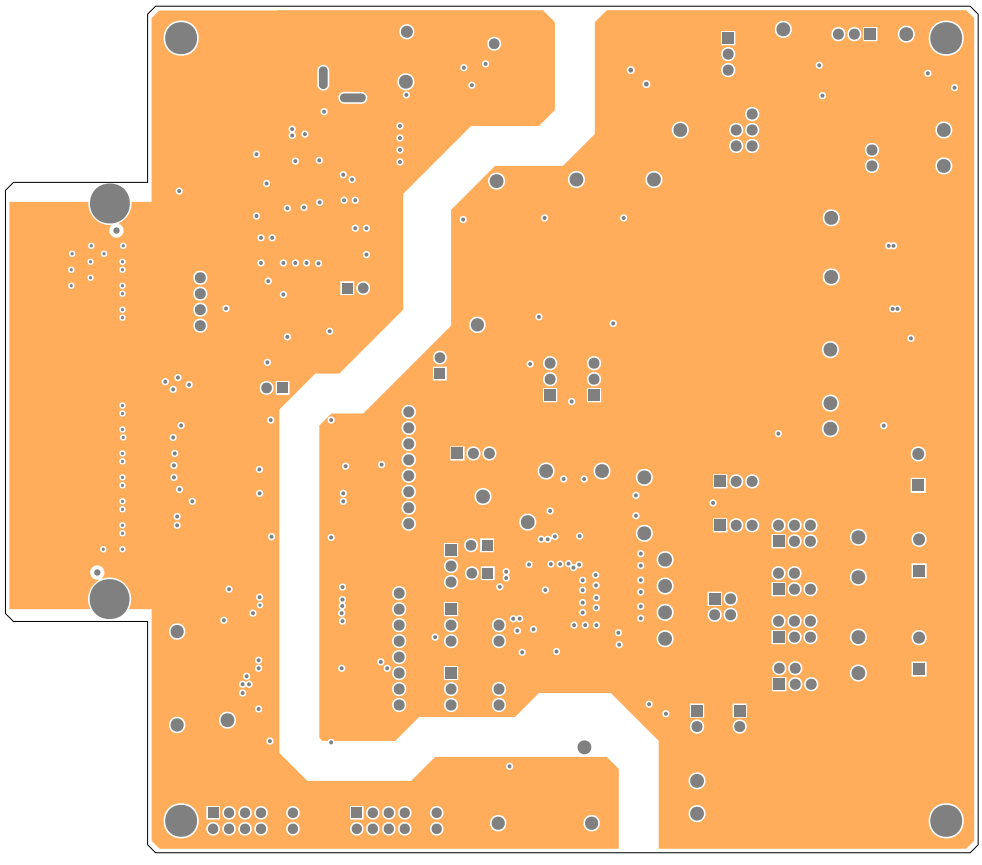
maxim integrated

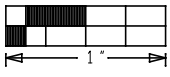
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: INTERNAL5





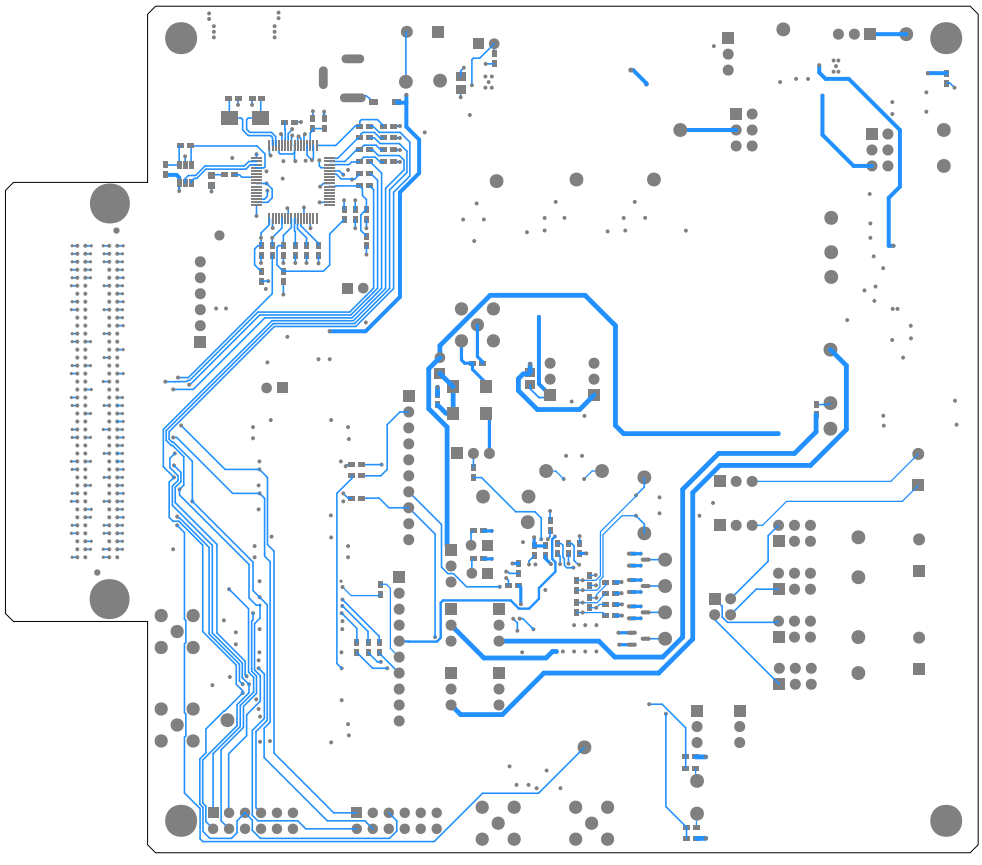
maxim integrated

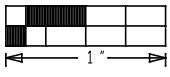
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: BOTTOM



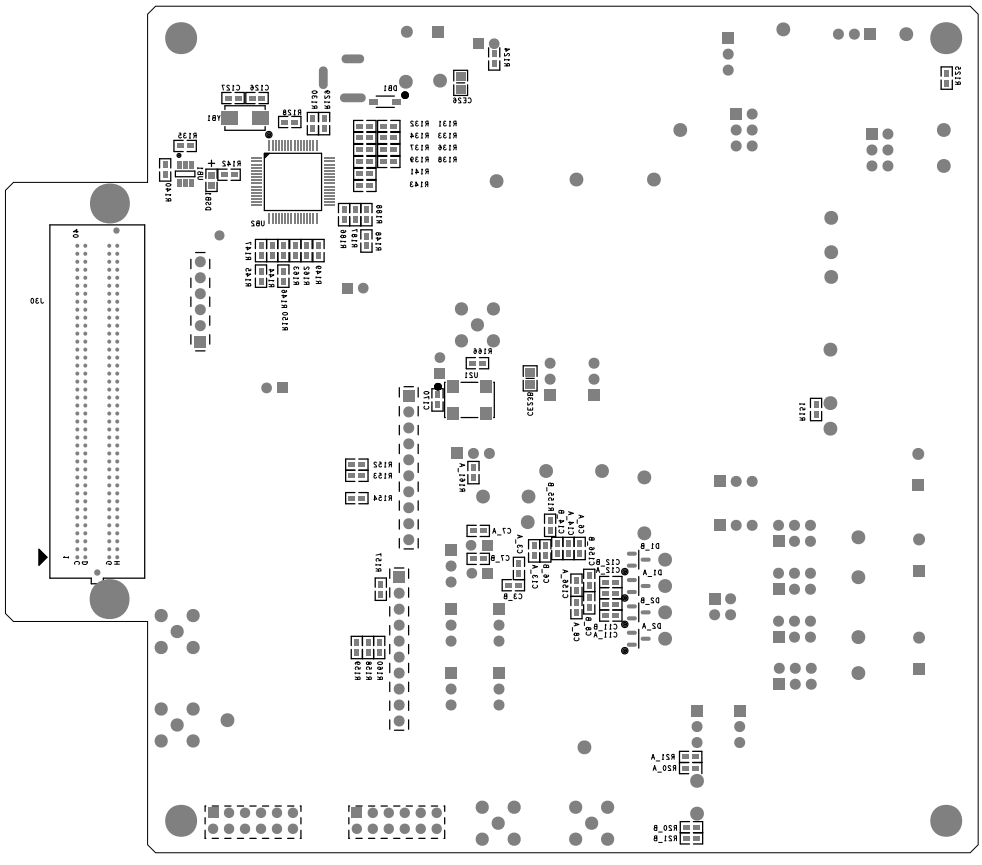


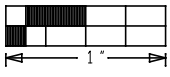
HARDWARE NAME:MAX11284_EVKIT_B

HARDWARE NUMBER:

ENGINEER: DESIGNER:

DATE: 09/05/2015 ODB++/GERBER: SILK_BOT





11214_16_evkit_p1_power

+3.3V
+2.0V
+1.8V
-1.8V
A3.6V
D3.6V
AGND
USB+5V
5V_FPGA
+3V3_USB
VDDIO
+12V_FPGA
GND

ROUTE CSB AND B PINS

11214_16_evkit_p1_adc_module

SYNC_ADC_B — SYNC_ADC_B
CS_ADC_B — CS_ADC_B
RDYB_ADC_B — RDYB_ADC_B

SYNC_ADC_A
DOUT_ADC
DIN_ADC
SCLK_ADC
CS_ADC_A
RDYB_ADC_A

DVDD_ADC

+1.8V
-1.8V
+2.0V
A3.6V
+3.3V

AGND

INTERFACE

11214_16_evkit_p1_interface_module

SYNC_ADC_A
DOUT_ADC
DIN_ADC
SCLK_ADC
CS_ADC_A
RDYB_ADC_A

SYNC_ADC_B — SYNC_ADC_B
CS_ADC_B — CS_ADC_B

RDYB_ADC_B — RDYB_ADC_B
GND
5V_FPGA
VDDIO
+3.3V
AGND
+12V_FPGA
D3.6V
DVDD_ADC

CS_ADC_A_FPGA
SYNC_ADC_A_FPGA
SCLK_ADC_FPGA
DIN_ADC_FPGA
DOUT_ADC_FPGA
SCLK_ADC_OUT_FPGA
RDYB_ADC_A_FPGA
SYNC_ADC_B_FPGA
RDYB_ADC_B_FPGA
CS_ADC_B_FPGA

USB_FTDI_CHIP

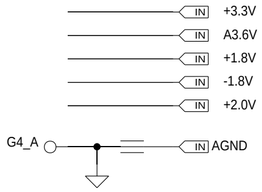
CS_ADC_B_FPGA
RDYB_ADC_B_FPGA
SYNC_ADC_B_FPGA
RDYB_ADC_A_FPGA

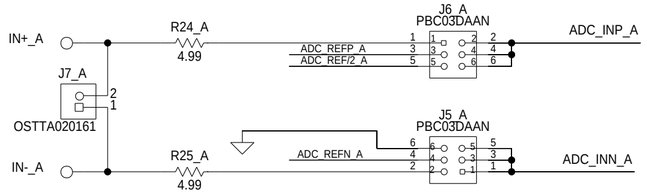
DOUT_ADC_FPGA
DIN_ADC_FPGA
SCLK_ADC_FPGA
SYNC_ADC_A_FPGA
CS_ADC_A_FPGA

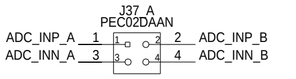
USB+5V
+3.3V_USB

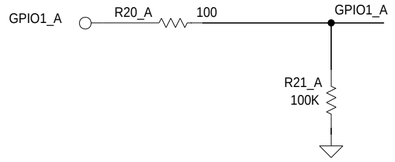
GND

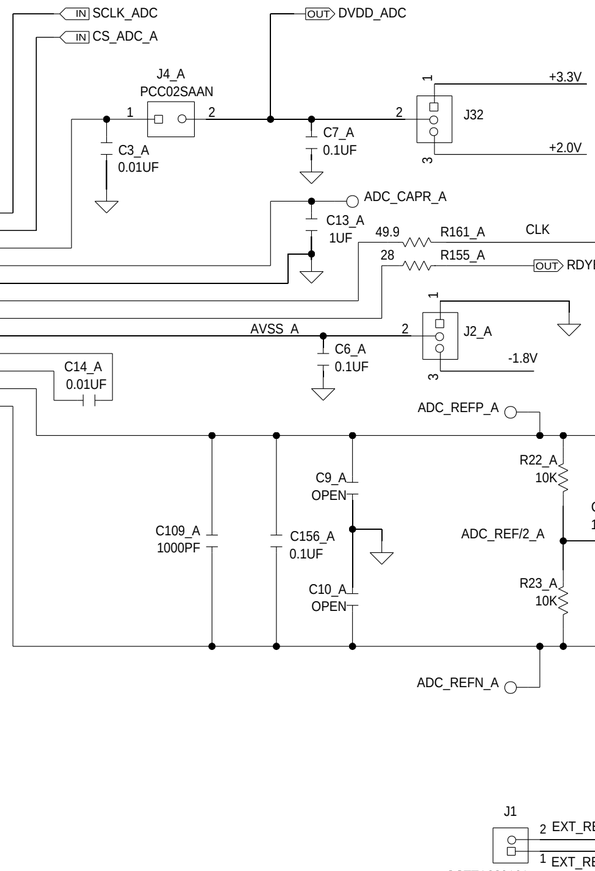
PROJECT TITLE: MAX11284 EVKIT		
DRAWING TITLE:		
SIZE: C	HARDWARE NUMBER: .	DATE: SEPT 2015
ENGINEER: –	DRAWN BY: –	REV.: B
	TEMPLATE REV.: 1.4	SHEET 1 OF 6





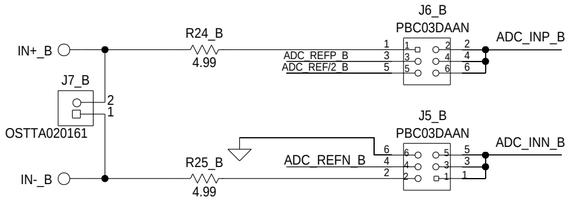


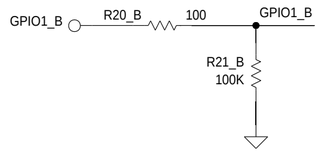


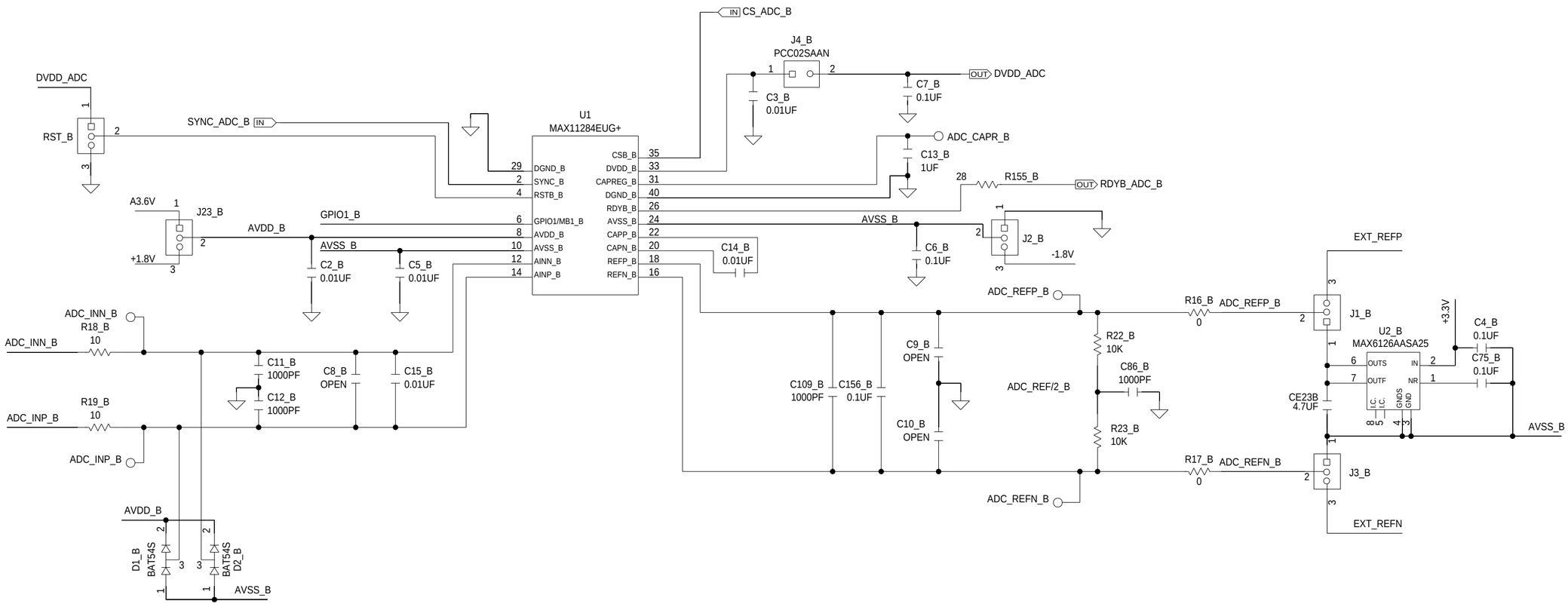


THE ON BOARD OSCILLATOR IS DESIGNED
FOR 3.3V DIGITAL DUT SUPPLY.
IF +2.0V DIGITAL DUT SUPPLY IS USED,
USE EXTERNAL 2V CLOCK.

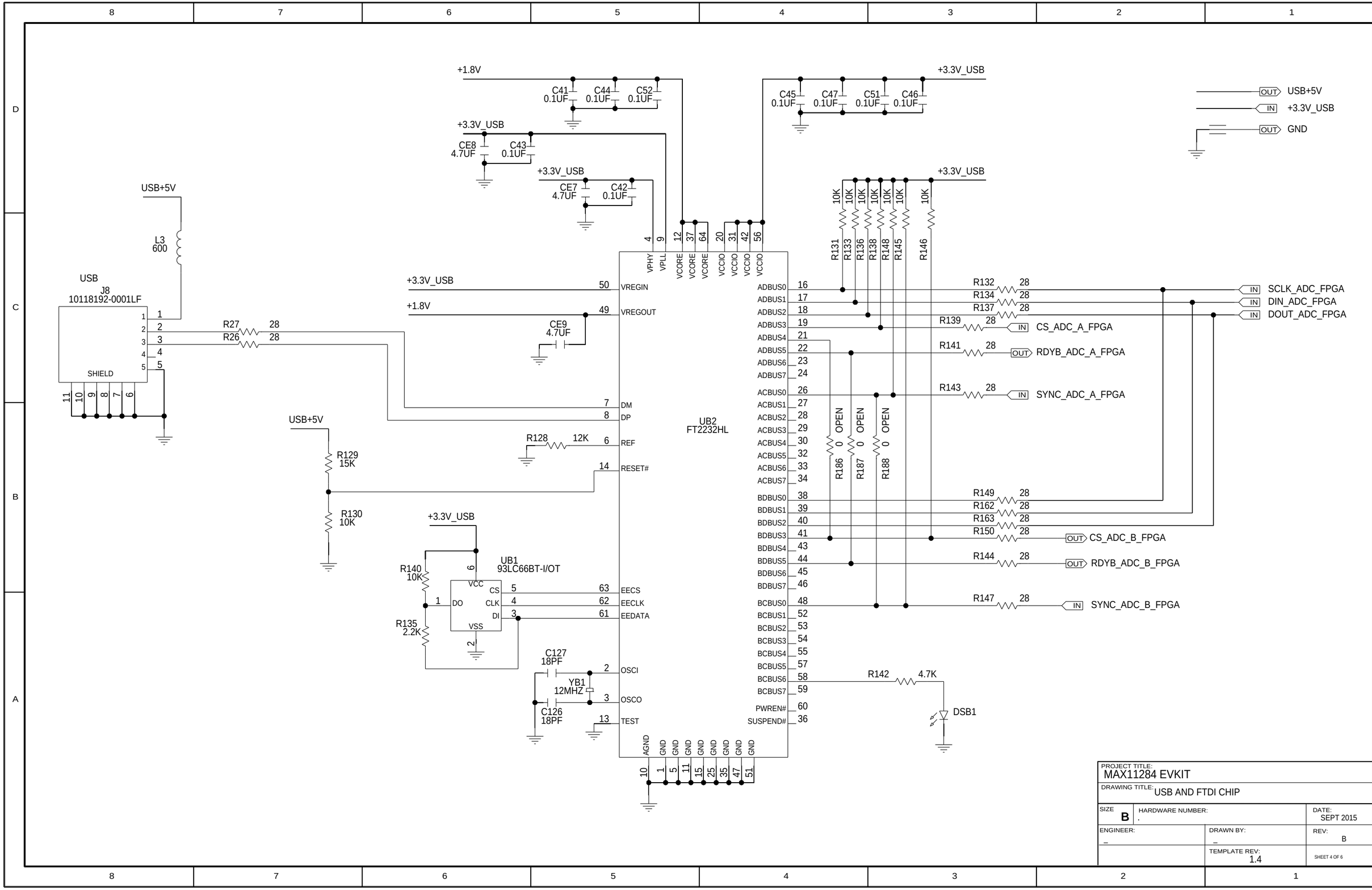
PROJECT TITLE: MAX11284 EVKIT		
DRAWING TITLE: ADC MODULE		
SIZE: C	HARDWARE NUMBER: .	DATE: SEPT 2015
ENGINEER: _	DRAWN BY: _	REV.: B
	TEMPLATE REV.: 1.4	SHEET 2 OF 6







PROJECT TITLE: MAX11284 EVKIT		
DRAWING TITLE: ADC MODULE		
SIZE: C	HARDWARE NUMBER: .	DATE: SEPT 2015
ENGINEER: _	DRAWN BY: _	REV.: B
	TEMPLATE REV.: 1.4	SHEET 3 OF 6



PROJECT TITLE:	MAX11284 EVKIT
DRAWING TITLE:	USB AND FTDI CHIP
SIZE: B	HARDWARE NUMBER: .
DATE:	SEPT 2015
ENGINEER:	_
DRAWN BY:	_
REV:	B
TEMPLATE REV:	1.4
SHEET 4 OF 6	

ISOLATED

IN D3.6V
IN DVDD_ADC
IN +3.3V
IN 5V_FPGA
IN VDDIO
IN GND
NI AGND

DVDD_ADC
C104 1UF
C107 0.1UF
VDDIO
C106 0.1UF
C103 1UF

U17
MAX14934FAWE+

CS_ADC_A OUT R157 28
SCLK_ADC OUT R160 28
DIN_ADC OUT R158 28
SYNC_ADC_A OUT R159 28
DOUT_ADC IN R76 28
RDYB_ADC_A IN R102 28

16 VDDB
15 GNDB
14 OUTB1
13 OUTB2
12 OUTB3
11 OUTB4
10 ENB
9 GNDB
1 VDDA
2 GNDA
3 INA1
4 INA2
5 INA3
6 INA4
7 I.C.
8 GNDA

CS_ADC_A_FPGA
SCLK_ADC_FPGA
DIN_ADC_FPGA
SYNC_ADC_A_FPGA

DVDD_ADC
C116 1UF
C118 0.1UF
VDDIO
C117 0.1UF
C115 1UF

U19
MAX14934FAWE+

RDYB_ADC_B IN R153 28

1 VDDA
2 GNDA
3 INA1
4 INA2
5 INA3
6 INA4
7 I.C.
8 GNDA
16 VDDB
15 GNDB
14 OUTB1
13 OUTB2
12 OUTB3
11 OUTB4
10 ENB
9 GNDB

DOUT_ADC_FPGA
RDYB_ADC_A_FPGA
SCLK_ADC_OUT_FPGA
RDYB_ADC_B_FPGA

DVDD_ADC
C91 1UF
C94 0.1UF
VDDIO
C93 0.1UF
C90 1UF

U16
MAX14934FAWE+

CS_ADC_B OUT R152 28
SYNC_ADC_B OUT R154 28

16 VDDB
15 GNDB
14 OUTB1
13 OUTB2
12 OUTB3
11 OUTB4
10 ENB
9 GNDB
1 VDDA
2 GNDA
3 INA1
4 INA2
5 INA3
6 INA4
7 I.C.
8 GNDA

CS_ADC_B_FPGA
SYNC_ADC_B_FPGA

FMC CONNECTOR

J30
ASP-134604-01

R105 28
VADJ

G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 G27 G28 G29 G30 G31 G32 G33 G34 G35 G36 G37 G38 G39 G40

J30
ASP-134604-01

R108 28
R101 28
R100 28
R98 28
R97 28
R96 28
R95 28
R73 28
R87 28
R92 28
R89 28
R81 28
R80 28
R71 28
R70 28
R68 28
R65 28
R64 28
R62 28
C60 1UF
VADJ

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H20 H21 H22 H23 H24 H25 H26 H27 H28 H29 H30 H31 H32 H33 H34 H35 H36 H37 H38 H39 H40

SYNC_CLK_IN
SYNC_CLK_OUT
OUT SCLK_ADC_FPGA
OUT DIN_ADC_FPGA
IN DOUT_ADC_FPGA
IN SCLK_ADC_OUT_FPGA
IN RDYB_ADC_A_FPGA
OUT RDYB_ADC_B_FPGA
OUT SYNC_ADC_B_FPGA
OUT CS_ADC_B_FPGA
OUT CS_ADC_A_FPGA
OUT SYNC_ADC_A_FPGA
SO_EEPROM_FPGA
SI_EEPROM_FPGA
SCK_EEPROM_FPGA
CS_EEPROM_FPGA

J16
SO_EEPROM_FPGA
SI_EEPROM_FPGA
SCK_EEPROM_FPGA
CS_EEPROM_FPGA
1 2 3 4 5 6
PBC06SAAN

FPGA INI

VDDIO
C69 1UF
C67 0.1UF
U12
93LC66BT-I/OT
5 CS
4 CLK
3 DI
1 DO
6 VCC
2 VSS
SO_EEPROM_FPGA

J30
ASP-134604-01

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40

+12V_FPGA IN

J30
ASP-134604-01

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 D38 D39 D40

3V3_FPGA

VDDIO
C121 1000PF
C120 0.1UF
GND
U20
74LVC2G125DP
SYNC CLK IN
J28
73391-0060
R122 49.9
R119 49.9
SYNC_CLK_IN
SYNC_CLK_IN
SYNC CLK IN SPLIT
J29
73391-0060
R123 49.9

VDDIO
C111 1000PF
C110 0.1UF
GND
U18
74LVC2G125DP
SYNC CLK OUT
SYNC_CLK_OUT
SYNC_CLK_OUT
R114 49.9
SYNC CLK OUT
J20
73391-0060
R112 49.9
J24
73391-0060
R113 49.9

PMOD PORT B

J27
TSW-106-08-S-D-RA

CS_ADC_B_FPGA
DIN_ADC_FPGA
DOUT_ADC_FPGA
SCLK_ADC_FPGA
RDYB_ADC_B_FPGA
SYNC_ADC_B_FPGA
VDDIO

PMOD PORT A

J26
TSW-106-08-S-D-RA

CS_ADC_A_FPGA
DIN_ADC_FPGA
DOUT_ADC_FPGA
SCLK_ADC_FPGA
RDYB_ADC_A_FPGA
SYNC_ADC_A_FPGA
VDDIO

WHEN USING PMOD A AND PMOD B
ENSURE THAT DIN DOUT SCLK ARE ONLY DRIVEN BY ONE OF THE PORTS

TEST

J19
PBC10SAAN
RDYB_ADC_B
CS_ADC_B
SYNC_ADC_B

J21
PBC10SAAN
SYNC_ADC_A
RDYB_ADC_A
CS_ADC_A
SCLK_ADC
DIN_ADC
DOUT_ADC

PROJECT TITLE: MAX11284 EVKIT		
DRAWING TITLE: FMC AND ISOLATION		
SIZE: C	HARDWARE NUMBER: .	DATE: SEPT 2015
ENGINEER: _	DRAWN BY: _	REV.: B
	TEMPLATE REV.: 1.4	SHEET 5 OF 6