MAX11300

PIXI, 20-Port Programmable Mixed-Signal I/O with 12-Bit ADC, 12-Bit DAC, Analog Switches, and GPIO

General Description

The MAX11300 integrates a PIXI™, 12-bit, multichannel, analog-to-digital converter (ADC) and a 12-bit, multichannel, buffered digital-to-analog converter (DAC) in a single integrated circuit. This device offers 20 mixed-signal high-voltage, bipolar ports, which are configurable as an ADC analog input, a DAC analog output, a general-purpose input (GPI), a general-purpose output (GPO), or an analog switch terminal. One internal and two external temperature sensors track junction and environmental temperature. Adjacent pairs of ports are configurable as a logic-level translator for open-drain devices or an analog switch.

PIXI ports provide highly flexible hardware configuration for 12-bit mixed-signal applications. The MAX11300 is best suited for applications that demand a mixture of analog and digital functions. Each port is individually configurable with up to four selectable voltage ranges within -10V to +10V.

The MAX11300 allows for the averaging of 2, 4, 8, 16, 32, 64, or 128 ADC samples from each ADC-configured port to improve noise performance. A DAC-configured output port can drive up to 25mA. The GPIO ports can be programmed to user-defined logic levels, and a GPI coupled with a GPO forms a logic-level translator.

Internal and external temperature measurements monitor programmable conditions of minimum and maximum temperature limits, using the interrupt to notify the host if one or more conditions occur. The temperature measurement results are made available through the serial interface.

The device features an internal, low-noise 2.5V voltage reference and provides the option to use external voltage references with separate inputs for the DAC and ADC. The device uses a 4-wire, 20MHz, SPI-compatible serial interface, operating from a 5V analog supply and a 1.8V to 5.0V digital supply. The PIXI port supply voltages operate from a wide range of -12.0V to +12.0V.

The MAX11300 is available in a 40-pin TQFN, 6mm x 6mm package or a 48-pin TQFP, 7mm x 7mm package specified over the -40°C to +105°C temperature range.

Applications

- Base Station RF Power Device Bias Controllers
- System Supervision and Control
- Power-Supply Monitoring
- Industrial Control and Automation
- Control for Optical Components

Benefits and Features

- 20 Configurable Mixed-Signal Ports Maximize Design Flexibility Across Platforms
  - Up to 20 12-Bit ADC Inputs
    - Single-Ended, Differential, or Pseudo-Differential
    - Range Options: 0 to 2.5V, ±5V, 0 to +10V, -10V to 0V
    - Programmable Sample Averaging Per ADC Port
    - Unique Voltage Reference for Each ADC PIXI Port
  - Up to 20 12-Bit DAC Outputs
    - Range Options: ±5V, 0 to +10V, -10V to 0V
    - 25mA Current Drive Capability with Overcurrent Protection
  - Up to 20 General-Purpose Digital I/Os
    - 0 to +5V GPI Input Range
    - 0 to +2.5V GPI Programmable Threshold Range
    - 0 to +10V GPO Programmable Output Range
    - Logic-Level Shifting Between Any Two Pins
  - 60Ω Analog Switch Between Adjacent PIXI Ports
  - Internal/External Temperature Sensors, ±1°C Accuracy
- Adapts to Specific Application Requirements and Allows for Easy Reconfiguration as System Needs Change
- Configurability of Functions Enables Optimized PCB Layout
- Reduces BOM Cost with Fewer Components in Small Footprint
  - 36mm2 40-Pin TQFN
  - 49mm2 48-Pin TQFP

Ordering Information ***appears at end of data sheet.***

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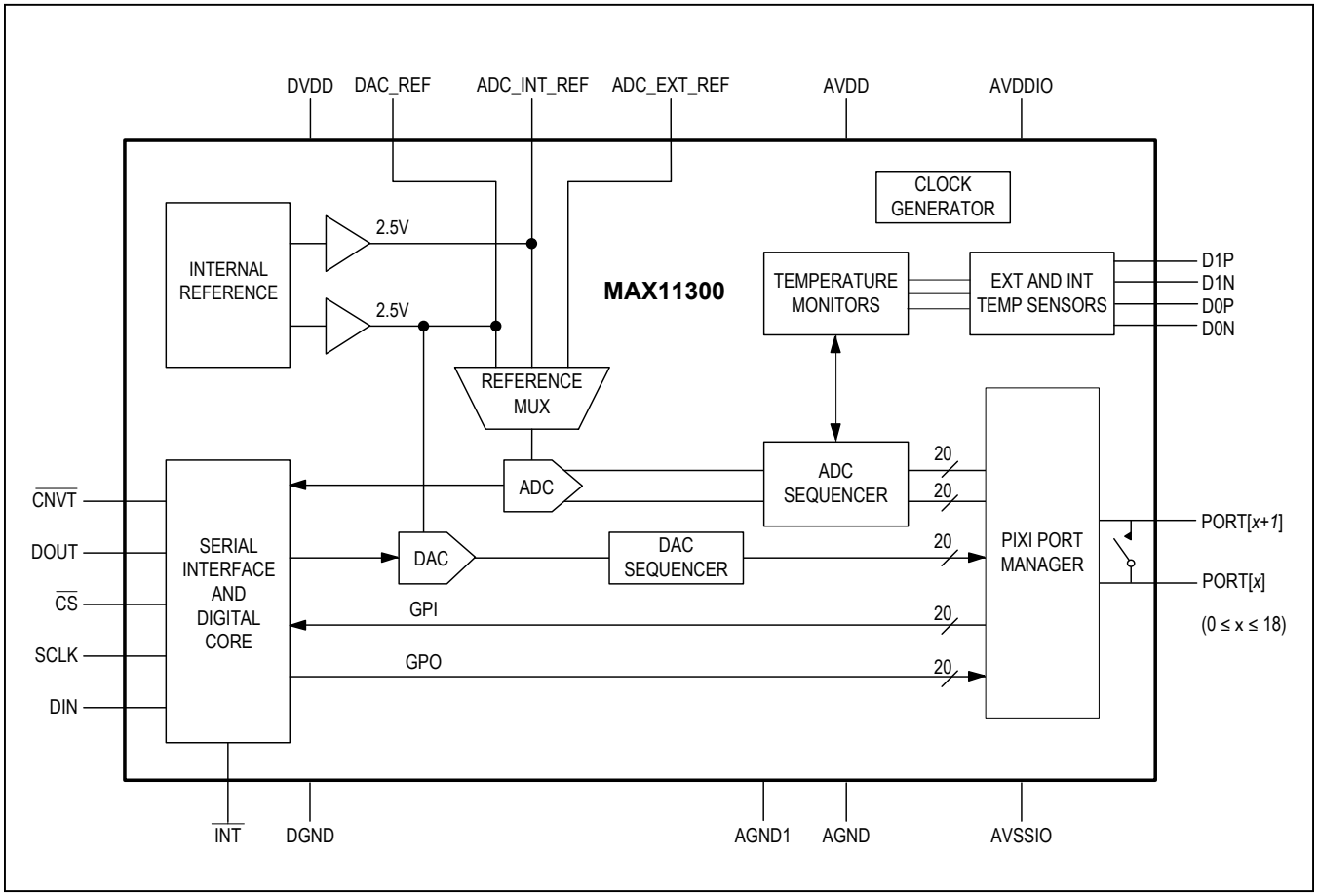
Functional Diagram



Absolute Maximum Ratings

DVDD to DGND.....-0.3V to +6V
AVDD to AGND .....-0.3V to +6V
AVDDIO to AVSSIO.....-0.3V to +25V
AVDDIO to AGND.....-0.3V to +17V
AVSSIO to AGND.....-14V to +0.3V
AGND to AGND1.....-0.3V to +0.3V
AGND to DGND .....-0.3V to +0.3V
AGND1 to DGND .....-0.3V to +0.3V
(PORT0 to PORT19) to AGND.....max of (V_{AVSSIO} - 0.3V) or -14V to min of (V_{AVDDIO} + 0.3V) or +17V
(PORT0 to PORT19) to AGND (GPI and Bidirectional Level Translator Modes).....-0.3V to the min of (V_{AVDD} + 0.3V) or +6V
($\overline{CNVT}$, DOUT) to DGND... -0.3V to the min of (V_{DVDD} + 0.3V) or +6V
($\overline{CS}$, SCLK, DIN, $\overline{INT}$) to DGND.....-0.3V to +6V
DAC and ADC Reference Pins to AGND (DAC_REF, ADC_INT_REF, ADC_EXT_REF)..... -0.3V to the min of (V_{AVDD} + 0.3V) or +4V
Temperature Sensor Pins (D0N, D0P, D1N, D1P) to AGND..... -0.3V to the min of (V_{AVDD} + 0.3V) or +6V
Current into Any PORT Pin 100mA
Current into Any Other Pin Except Supplies and Ground.....50mA
Continuous Power Dissipation (T_A = +70°C) (Multilayer board)
TQFN (derate 37mW/°C above +70°C) 2963mW
TQFP (derate 36.2mW/°C above +70°C).....2898.6mW
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}) .....1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27°C/W

TQFP
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

ADC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 3)						
Resolution			12			Bits
Integral Nonlinearity	INL				±2.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.5	±8	LSB
Offset Error Drift				±0.002		LSB/ºC
Gain Error					±11	LSB
Gain Error Drift				±0.01		LSB/ºC
Channel-to-Channel Offset Matching				1		LSB
Channel-to-Channel Gain Matching				2		LSB

Electrical Characteristics (continued)

ADC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Single-Ended Inputs)						
Signal-to-Noise Plus Distortion	SINAD	f_S = 400ksps, f_{IN} = 10kHz		70		dB
Signal to Noise	SNR	f_S = 400ksps, f_{IN} = 10kHz		71		dB
Total Harmonic Distortion	THD	f_S = 400ksps, f_{IN} = 10kHz		-75		dB
Spurious-Free Dynamic Range	SFDR	f_S = 400ksps, f_{IN} = 10kHz		75		dB
Crosstalk		f_S = 100ksps, f_{IN} = 10kHz		-85		dB
DYNAMIC PERFORMANCE (Differential Inputs)						
Signal-to-Noise Plus Distortion	SINAD	f_S = 400ksps, f_{IN} = 10kHz		71		dB
Signal to Noise	SNR	f_S = 400ksps, f_{IN} = 10kHz		72		dB
Total Harmonic Distortion	THD	f_S = 400ksps, f_{IN} = 10kHz		-82		dB
Spurious-Free Dynamic Range	SFDR	f_S = 400ksps, f_{IN} = 10kHz		82		dB
Crosstalk		f_S = 100ksps, f_{IN} = 10kHz		-85		dB
CONVERSION RATE						
Throughput (Note 4)		ADCCONV[1:0] = 00		200		ksps
		ADCCONV[1:0] = 01		250		
		ADCCONV[1:0] = 10		333		
		ADCCONV[1:0] = 11		400		
Acquisition Time	t_{ACQ}	ADCCONV[1:0] = 00		3.5		µs
		ADCCONV[1:0] = 01		2.5		
		ADCCONV[1:0] = 10		1.5		
		ADCCONV[1:0] = 11		1.0		
ANALOG INPUT (All Ports)						
Absolute Input Voltage (Note 5)	V_{PORT}	Range 1	0		10	V
		Range 2	-5		+5	
		Range 3	-10		0	
		Range 4	0		2.5	
Input Resistance		Range 1, 2, 3	70	100	130	kΩ
		Range 4	50	75	100	kΩ

REF Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC INTERNAL REFERENCE						
Reference Output Voltage		Internal references at T_A = +25°C	2.494	2.5	2.506	V
REF Output Tempco (Note 6)	T_{C-VREF}			±10	±25	ppm/°C
Capacitor Bypass at ADC_INT_REF			4.7		10	µF
DAC INTERNAL REFERENCE						
Reference Output Voltage		Internal references at T_A = +25°C	2.494	2.5	2.506	V
REF Output Tempco (Note 6)	T_{C-VREF}			±10	±25	ppm/°C
Capacitor Bypass at DAC_REF			4.7		10	µF
ADC EXTERNAL REFERENCE						
Reference Input Range			2		2.75	V
DAC EXTERNAL REFERENCE						
Reference Input Range			1.25		2.5	V

GPIO Electrical Specifications

(V_{AVDD} = 5.0V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPIO EXCEPT IN BIDIRECTIONAL LEVEL TRANSLATION MODE						
Programmable Input Logic Threshold	V_{ITH}		0.3		V_{DACREF}	V
Input High Voltage	V_{IH}		V_{ITH} + 0.3			V
Input Low Voltage	V_{IL}				V_{ITH} - 0.3	V
Hysteresis				±30		mV
Programmable Output Logic Level	V_{OLVL}		0		4 x V_{DACREF}	V
Propagation Delay from GPI Input to GPO Output in Unidirectional Level Translating Mode		Midscale threshold, 5V logic swing		2		µs
BIDIRECTIONAL LEVEL TRANSLATION PATH AND ANALOG SWITCH						
Input High Voltage	V_{IH}		1			V
Input Low Voltage	V_{IL}				0.2	V
On-Resistance		From V_{AVSSIO} +2.50V to V_{AVDDIO} - 2.50V			60	Ω

GPIO Electrical Specifications (continued)

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay		10kΩ pullup resistors to rail in each side. Midvoltage to midvoltage when driving side goes from high to low			1	µs
ANALOG SWITCH						
Turn-On Delay		(Note 7)			400	ns
Turn-Off Delay		(Note 7)			400	ns
On-Time Duration		(Note 7)	1			µs
Off-Time Duration		(Note 7)	1			µs
On-Resistance		From V_{AVSSIO} +2.50V to V_{AVDDIO} - 2.50V			60	Ω

DAC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N		12			Bits
Output Range (Note 5)	V_{PORT}	Range 1	0		+10	V
		Range 2	-5		+5	
		Range 3	-10		0	
Integral Linearity Error	INL	From code 100 to code 3996		±0.5	±1.5	LSB
Differential Linearity Error	DNL			±0.5	±1	LSB
Offset Voltage		At code 100			±20	LSB
Offset Voltage Tempco				15		ppm/°C
Gain Error		From code 100 to code 3996	-0.6		+0.6	% of FS
Gain Error Tempco		From code 100 to code 3996		4		ppm of FS/°C
Power-Supply Rejection Ratio	PSRR			0.4		mV/V
DYNAMIC CHARACTERISTICS						
Output Voltage Slew Rate	SR			1.6		V/µs
Output Settling Time		To ±1 LSB, from 0 to full scale, output load capacitance of 250pF (Note 7)		40		µs
Settling Time After Current-Limit Condition				6		µs
Noise		f = 0.1Hz to 300kHz		3.8		mV_{P-P}

DAC Electrical Specifications (continued)

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRACK-AND-HOLD						
Digital Feedthrough				5		nV·s
Hold Step				1	6	mV
Droop Rate (note 6)				0.3	15	mV/s

Interface Digital IO Electrical Specifications

(V_{AVDD} = 5.0V, V_{DVDD} = 1.62V to 5.50V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI IO DC SPECIFICATION						
Input High Voltage (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)		V_{DVDD} = 2.50V to 5.50V	0.7 x V_{DVDD}			V
		V_{DVDD} = 1.62V to 2.50V	0.85 x V_{DVDD}			V
Input Low Voltage (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)		V_{DVDD} = 2.50V to 5.50V			0.3 x V_{DVDD}	V
		V_{DVDD} = 1.62V to 2.50V			0.15 x V_{DVDD}	V
Input Leakage Current (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$, $\overline{INT}$)		Input voltage at DVDD	-10		+10	µA
Input Capacitance (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)				10		pF
Output High Voltage (DOUT)		I_{SRC} = 5mA, V_{DVDD} = 2.50V to 5.50V	V_{DVDD} - 0.5			V
		I_{SRC} = 2mA, V_{DVDD} = 1.62V to 2.50V	V_{DVDD} - 0.3			V
Output Low Voltage (DOUT, $\overline{INT}$)		I_{SNK} = 5mA, V_{DVDD} = 2.50V to 5.50V			0.4	V
		I_{SNK} = 2mA, V_{DVDD} = 1.62V to 2.50V			0.2	V
Output Leakage Current (DOUT)			-10		+10	µA

Interface Digital IO Electrical Specifications (continued)

(V_{AVDD} = 5.0V, V_{DVDD} = 1.62V to 5.50V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING REQUIREMENTS (See Figures 1 and 2)						
SCLK Frequency	f_{SCLK}	V_{DVDD} = 2.50V to 5.50V			20	MHz
		V_{DVDD} = 1.62V to 2.50V			10	MHz
SCLK Clock Period	t_{CP}	V_{DVDD} = 2.50V to 5.50V	50			ns
		V_{DVDD} = 1.62V to 2.50V	100			ns
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}	V_{DVDD} = 2.50V to 5.50V	25			ns
		V_{DVDD} = 1.62V to 2.50V	65			ns
$\overline{CS}$ Low to First SCLK Rise Setup	t_{CSS0}		5			ns
24th SCLK Rising Edge to $\overline{CS}$ Rising Edge	t_{CSS1}		5			ns
SCLK Rise to $\overline{CS}$ Low	t_{CSH0}		5			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		50			ns
DIN to SCLK Setup	t_{DS}		5			ns
DIN Hold After SCLK	t_{DH}		5			ns
DOUT Transition Valid After SCLK Fall	t_{DOT}	V_{DVDD} = 2.50V to 5.50V			23	ns
		V_{DVDD} = 1.62V to 2.50V			55	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 20pF			50	ns

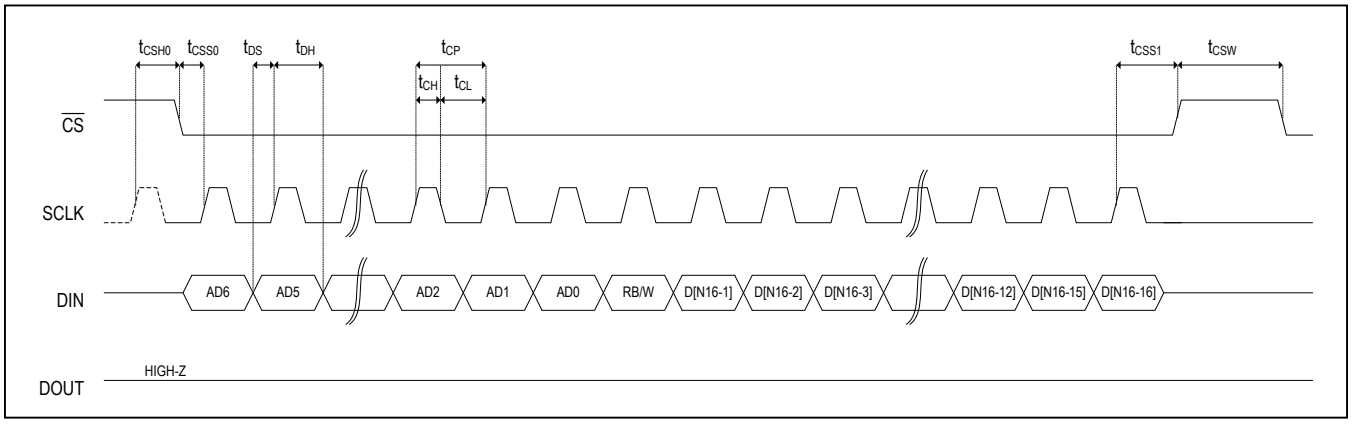


Figure 1. SPI Write Timing (N = Number of Words Written; N > 1 for Burst Mode)

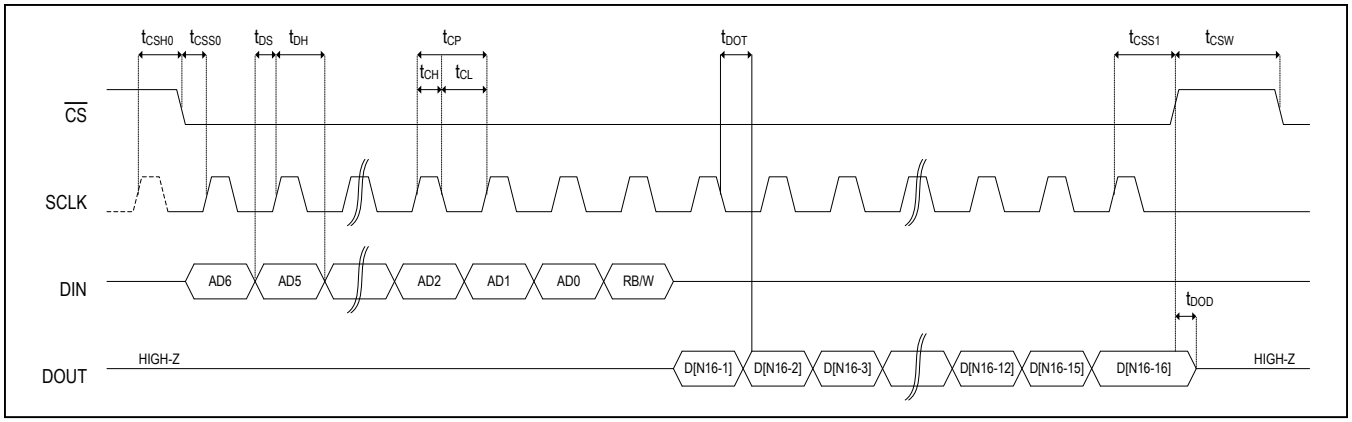


Figure 2. SPI Read Timing (N = Number of Words Written; N > 1 for Burst Mode)

Internal and External Temperature Sensor Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Accuracy of Internal Sensor (Note 6,8)		0°C ≤ T_J ≤ +80°C		±0.3	±2.0	°C
		-40°C ≤ T_J ≤ +125°C		±0.7	±5	°C
Accuracy of External Sensor (Note 6,8)		0°C ≤ T_{RJ} ≤ +80°C		±0.3	±2.0	°C
		-40°C ≤ T_{RJ} ≤ +150°C		±1.0	±5	°C
Temperature Measurement Resolution				0.125		°C
External Sensor Junction Current	High			68		µA
	Low			4		µA
External Sensor Junction Current	High	Series resistance cancellation mode		136		µA
	Low	Series resistance cancellation mode		8		µA
D0N/D1N Voltage		Internally generated		0.5		V

Power Supply Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{AVDD}			4.75		5.25	V
V_{DVDD}			1.62		5.50	V
V_{AVDDIO}			V_{AVDD}		15.75	V
V_{AVSSIO}			- 12.0		0	V
V_{AVDDIO} to V_{AVSSIO}			V_{AVDD}		24	V
I_{AVDD}		All ports in high-impedance mode		14	18	mA
		LPEN = 1		11		mA
		All ports in ADC-related modes		17		mA
		All ports in DAC-related modes		18		mA
I_{DVDD}		Serial interface in idle mode			2	µA
I_{AVDDIO}		All ports in mode 0			150	µA
I_{AVSSIO}		All ports in mode 0	-400			µA

Recommended VDDIO/VSSIO Supply Selection

		ADC RANGE			
		-10V TO 0V	**-5V TO +5V**	**0V TO +10V**	**0 TO 2.5V**
DAC RANGE	**-10V TO 0V**	V_{AVDDIO} = +5V V_{AVSSIO} = -12V	V_{AVDDIO} = +5V V_{AVSSIO} = -12V	V_{AVDDIO} = +10V V_{AVSSIO} = -12V	V_{AVDDIO} = +5V V_{AVSSIO} = -12V
	-5V TO +5V	V_{AVDDIO} = +7V V_{AVSSIO} = -10V	V_{AVDDIO} = +7V V_{AVSSIO} = -7V	V_{AVDDIO} = +10V V_{AVSSIO} = -7V	V_{AVDDIO} = +7V V_{AVSSIO} = -7V
	0V TO +10V	V_{AVDDIO} = +12V V_{AVSSIO} = -10V	V_{AVDDIO} = +12V V_{AVSSIO} = -5V	V_{AVDDIO} = +12V V_{AVSSIO} = -2V	V_{AVDDIO} = +12V V_{AVSSIO} = -2V

The values of V_{AVDDIO} and V_{AVSSIO} supply voltages depend on the application circuit and the device configuration.

V_{AVDDIO} needs to be the maximum of those four values:

- If one or more ports are in mode 3, 4, 5, 6, or 10 (DAC-related modes), V_{AVDDIO} must be set, at minimum, to the value of the largest voltage driven by any of the ports set in those modes. For improved linearity, it is recommended to set V_{AVDDIO} 2.0V above the largest voltage value.
- If one or more ports are in mode 7, 8, or 9 (ADC-related modes), V_{AVDDIO} must be set, at minimum, to the value of the largest voltage applied to any of the ports set in those modes.
- If one or more ports are in mode 11 or 12 (Analog switch-related modes), V_{AVDDIO} must be set, at minimum, to 2.0V above the value of the largest voltage applied to any of the ports functioning as analog switch terminals.
- V_{AVDDIO} cannot be set lower than V_{AVDD}.

V_{AVSSIO} needs to be the minimum of those four values:

- If one or more ports are in mode 3, 4, 5, 6, or 10 (DAC-related modes), V_{AVSSIO} must be set, at maximum, to the value of the lowest voltage driven by any of the ports set in those modes. For improved linearity, it is recommended to set V_{AVSSIO} 2.0V below the lowest voltage value.
- If one or more ports are in mode 7, 8, or 9 (ADC-related modes), V_{AVSSIO} must be set, at maximum, to the value of the lowest voltage applied to any of the ports set in those modes.

Recommended VDDIO/VSSIO Supply Selection (continued)

- If one or more ports are in mode 11 or 12 (Analog Switch-related modes), V_{AVSSIO} must be set, at maximum, to 2.0V below the value of the lowest voltage applied to any of the ports functioning as analog switch terminals.
- V_{AVSSIO} cannot be set higher than V_{AGND}.

For example, the MAX11300 can operate with only one voltage supply of 5V (±5%) connected to AVDD, AVDDIO, and DVDD, and one ground of 0V connected to AGND, DGND, and AVSSIO. However, the level of performance presented in the electrical specifications requires the setting of the supplies connected to AVDDIO and AVSSIO as previously described.

Common PIXI Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PIXI PORTS						
Input Capacitance		All PIXI ports		20		pF
Input Resistance		All PIXI input ports except ADC mode	50	75	100	kΩ
Startup Time		Between stable supplies and accessing registers			100	ms
HIGH-VOLTAGE OUTPUT DRIVER CHARACTERISTICS						
Maximum Output Capacitance					250	pF
Output Low Voltage, DAC Mode		Sinking 25mA, V_{AVSSIO} = 0V, AVDDIO = 10V			V_{AVSSIO} + 1.0	V
Output High Voltage, DAC Mode		Sourcing 25mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V	V_{AVDDIO} - 1.5			V
Output Low Voltage, GPO Mode		Sinking 2mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V			V_{AVSSIO} + 0.4	V
Output High Voltage, GPO Mode		Sourcing 2mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V	V_{AVDDIO} – 0.4			V
Current Limit		Short to AVDDIO		75		mA
		Short to AVSSIO		75		mA

Note 2: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at T_A = +25°C.

Note 3: DC accuracy specifications are tested for single-ended ADC inputs only.

Note 4: The effective ADC sample rate for port X configured in mode 6, 7, or 8 is:

[ADC sample rate per ADCCONV]/(([number of ports in modes 6,7,8] + [1 if TMPSEL ≠ 000]) x [$2^{\#\ OF\ SAMPLES\ for\ port\ X}$])

Note 5: See the *Recommended VDDIO/VSSIO Supply Selection* table for each range. For ports in modes 6, 7, 8, or 9, the voltage applied to those ports must be within the limits of their selected input range, whether in single-ended or differential mode.

Note 6: Specification is guaranteed by design and characterization.

Note 7: Switch controlled by GPI-configured port. One switch terminal connected to 0V, the other terminal connected to 5V through a 5mA current source. Timing is measured at the 2.5V transition point. Turn-on and turn-off delays are measured from the edge of the control signal to the 2.5V transition point. Turn-on and turn-off durations are measured between control signal transitions.

Note 8: In DAC-related modes, the rate, at which PIXI ports configured in mode 1, 3, 4, 5, 6, or 10 are refreshed, is as follows:

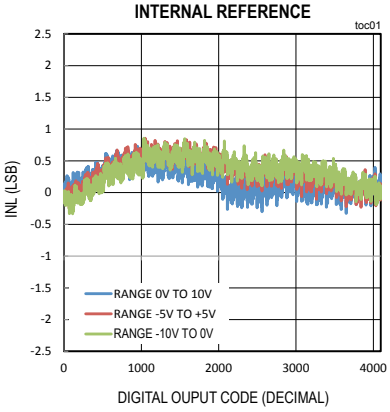
1/(40µs x [number of ports in modes 1, 3, 4, 5, 6, 10])

Note 9: Typical (TYP) values represent the errors at the extremes of the given temperature range.

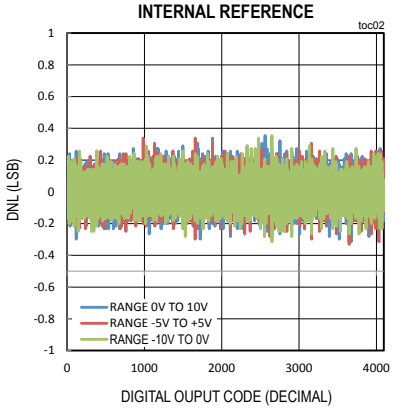
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

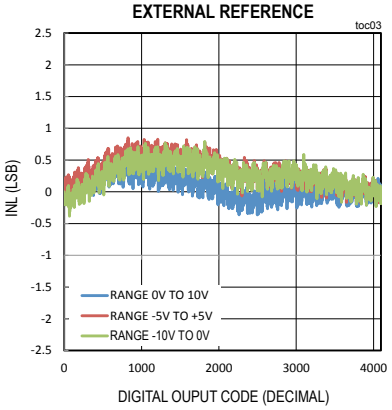
ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE INTERNAL REFERENCE



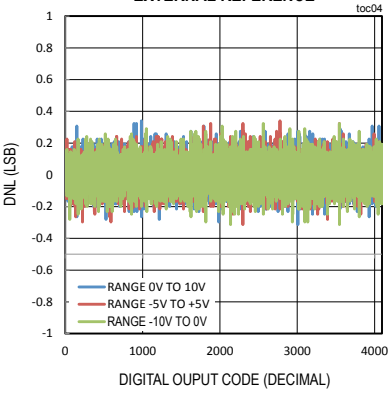
ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE INTERNAL REFERENCE



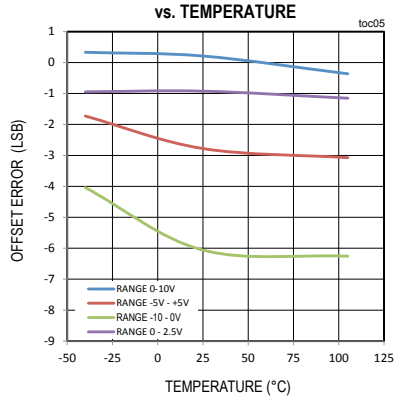
ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE EXTERNAL REFERENCE



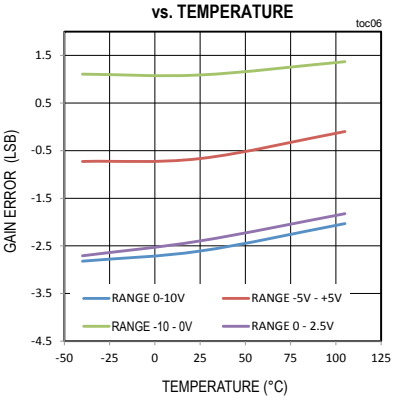
ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE EXTERNAL REFERENCE



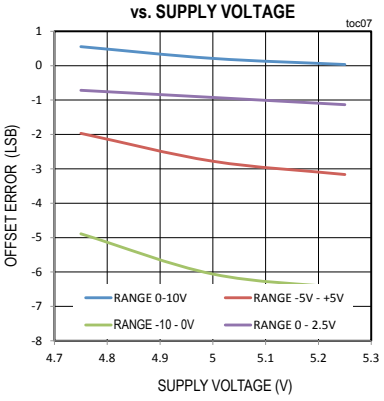
ADC OFFSET ERROR vs. TEMPERATURE



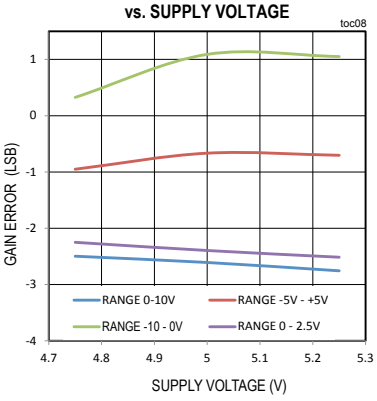
ADC GAIN ERROR vs. TEMPERATURE



ADC OFFSET ERROR vs. SUPPLY VOLTAGE



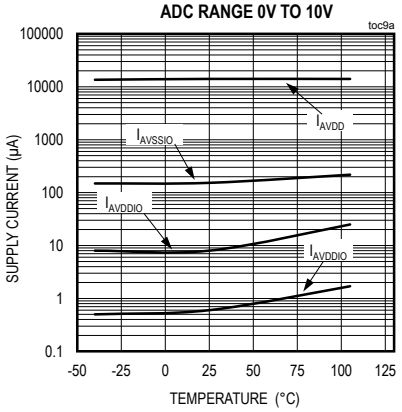
ADC GAIN ERROR vs. SUPPLY VOLTAGE



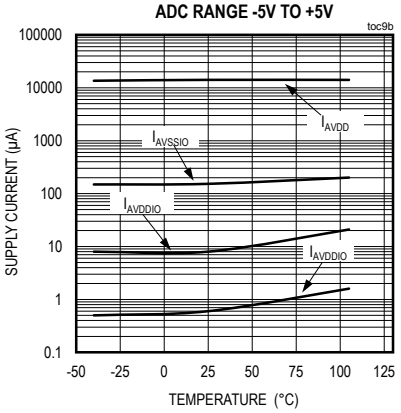
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

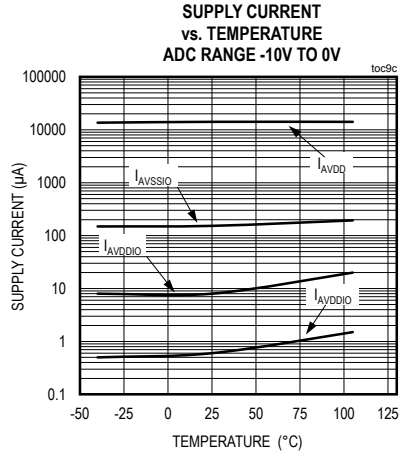
SUPPLY CURRENT vs. TEMPERATURE ADC RANGE 0V TO 10V



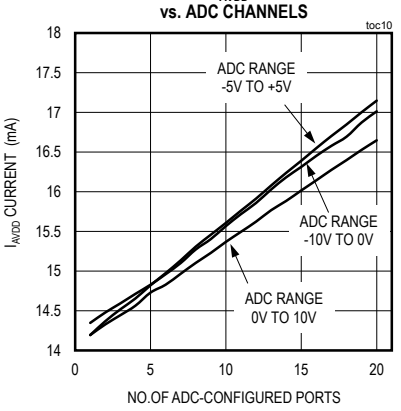
SUPPLY CURRENT vs. TEMPERATURE ADC RANGE -5V TO +5V



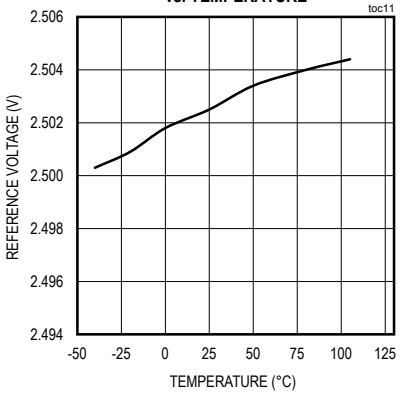
SUPPLY CURRENT vs. TEMPERATURE ADC RANGE -10V TO 0V



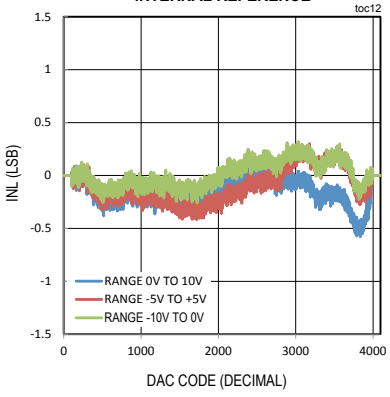
I_{AVDD} vs. ADC CHANNELS



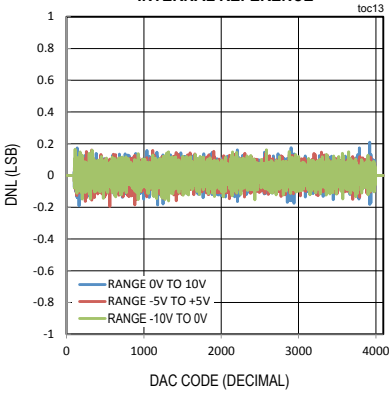
ADC INTERNAL REFERENCE vs. TEMPERATURE



DAC INTEGRAL NONLINEARITY vs. DIGITAL CODE INTERNAL REFERENCE



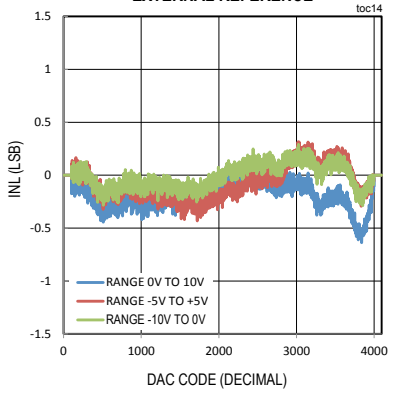
DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE INTERNAL REFERENCE



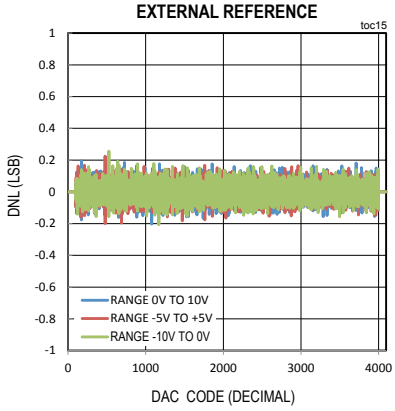
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

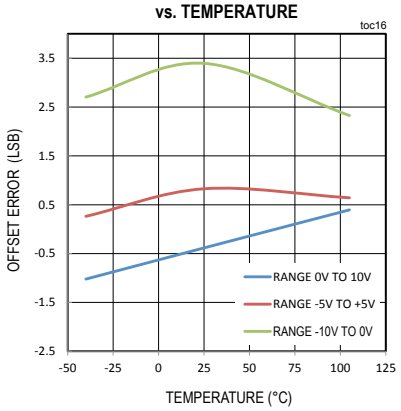
DAC INTEGRAL NONLINEARITY vs. DIGITAL CODE EXTERNAL REFERENCE



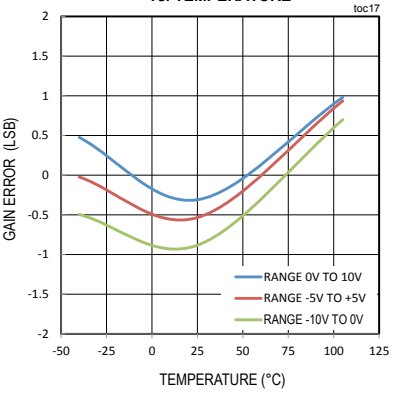
DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE EXTERNAL REFERENCE



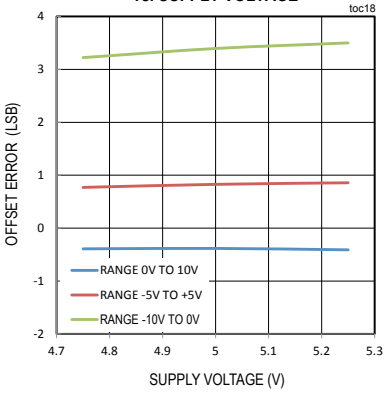
DAC OFFSET ERROR vs. TEMPERATURE



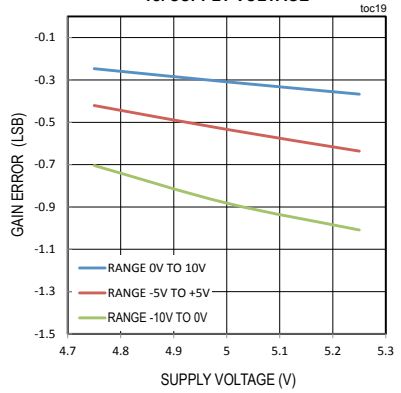
DAC GAIN ERROR vs. TEMPERATURE



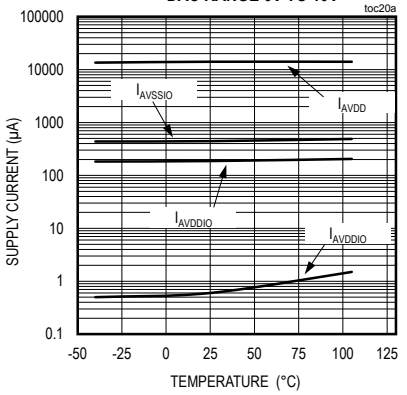
DAC OFFSET ERROR vs. SUPPLY VOLTAGE



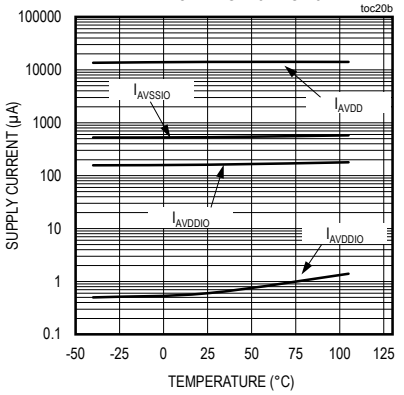
DAC GAIN ERROR vs. SUPPLY VOLTAGE



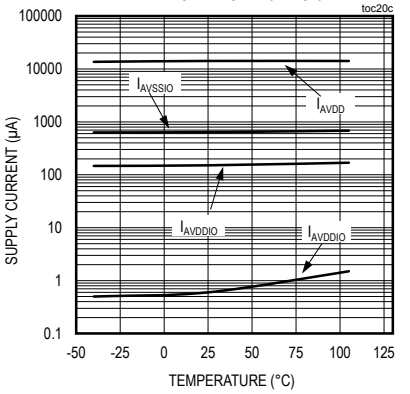
SUPPLY CURRENT vs. TEMPERATURE DAC RANGE 0V TO 10V



SUPPLY CURRENT vs. TEMPERATURE DAC RANGE -5V TO +5V



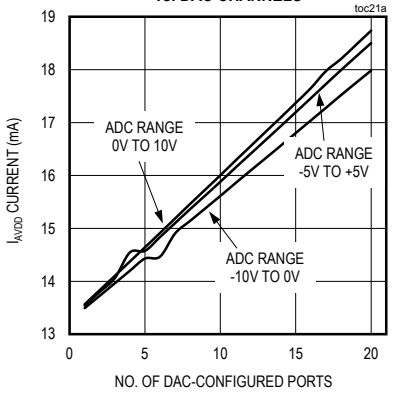
SUPPLY CURRENT vs. TEMPERATURE DAC RANGE -10V TO 0V



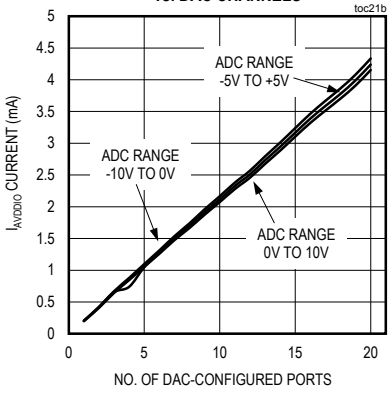
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

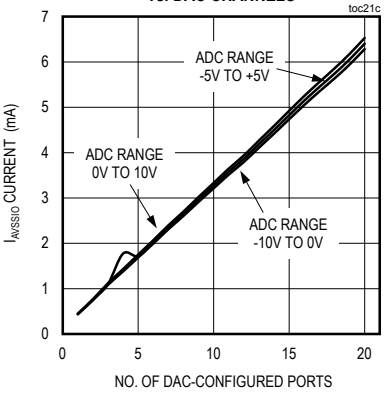
I_{AVDD} vs. DAC CHANNELS



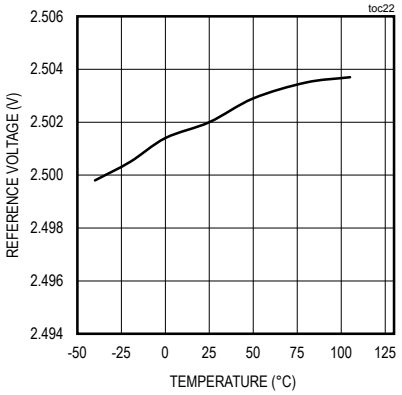
I_{AVDDIO} vs. DAC CHANNELS



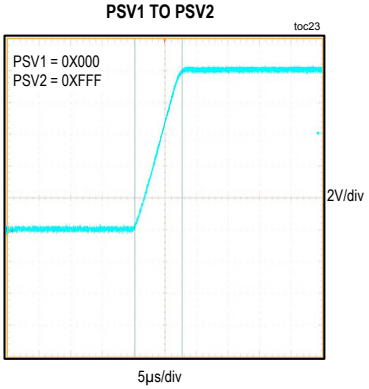
I_{AVSSIO} vs. DAC CHANNELS



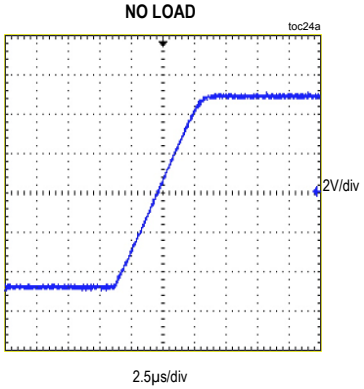
DAC INTERNAL REFERENCE vs. TEMPERATURE



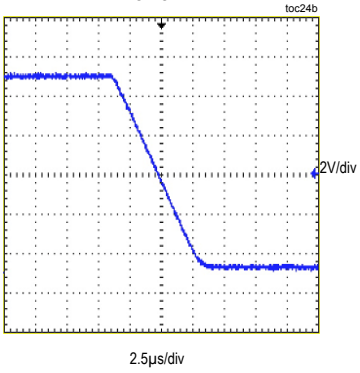
DAC SETTLING TIME CHANGE FROM PSV1 TO PSV2



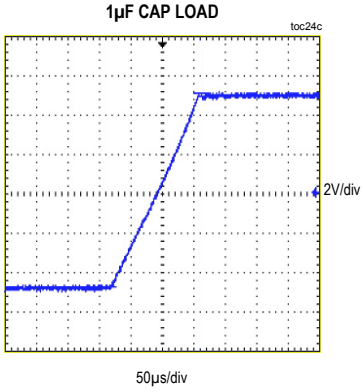
DAC SETTLING TIME CHANGE FROM MIN TO MAX NO LOAD



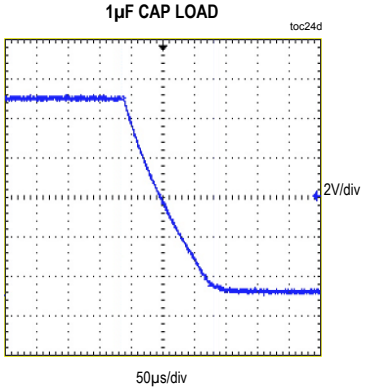
DAC SETTLING TIME CHANGE FROM MAX TO MIN NO LOAD



DAC SETTLING TIME CHANGE FROM MIN TO MAX 1µF CAP LOAD



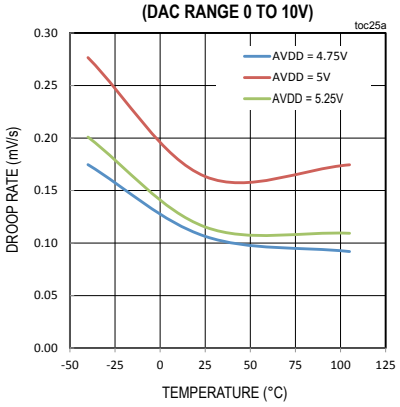
DAC SETTLING TIME CHANGE FROM MAX TO MIN 1µF CAP LOAD



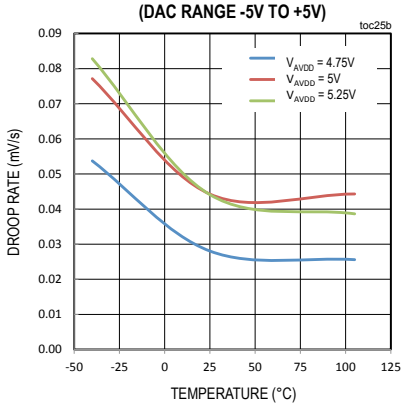
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

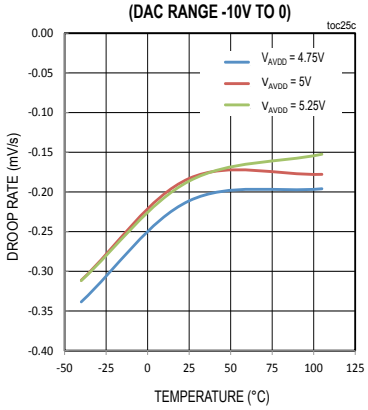
DAC DROOP RATE vs. TEMPERATURE (DAC RANGE 0 TO 10V)



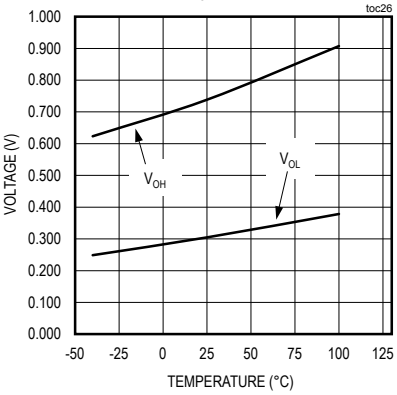
DAC DROOP RATE vs. TEMPERATURE (DAC RANGE -5V TO +5V)



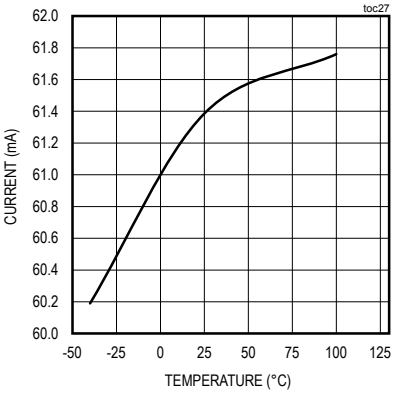
DAC DROOP RATE vs. TEMPERATURE (DAC RANGE -10V TO 0)



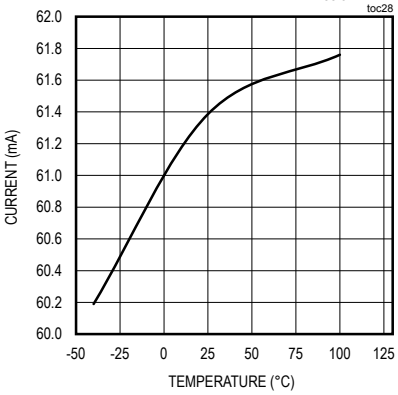
DAC V_{OH} AND V_{OL} vs. TEMPERATURE (I_{LOAD} = 25mA)



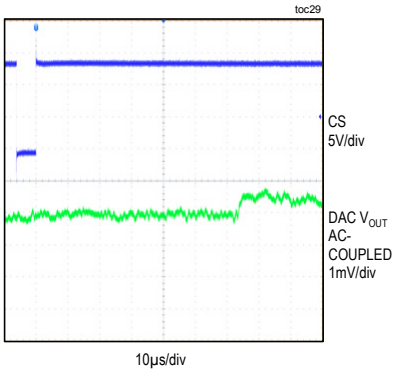
DAC DRIVE CURRENT LIMIT vs. TEMPERATURE DAC = 0V, SHORTED TO V_{DDIO}



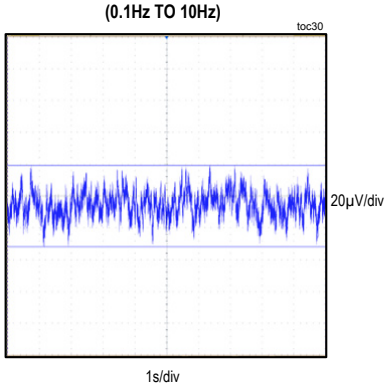
DAC DRIVE CURRENT LIMIT vs. TEMPERATURE DAC = 10V, SHORTED TO V_{SSIO}



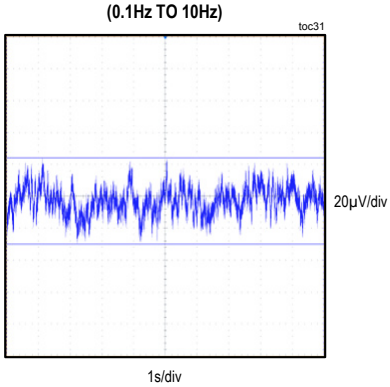
MAJOR-CODE TRANSITION GLITCH DAC CODE FROM 0x7FF TO 0x800



DAC OUTPUT NOISE INTERNAL REFERENCE (0.1Hz TO 10Hz)



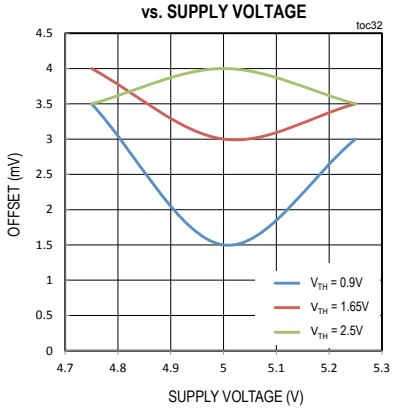
DAC OUTPUT NOISE EXTERNAL REFERENCE (0.1Hz TO 10Hz)



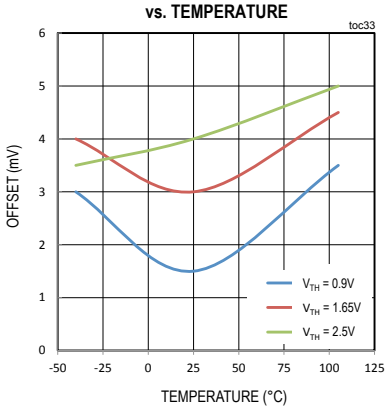
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

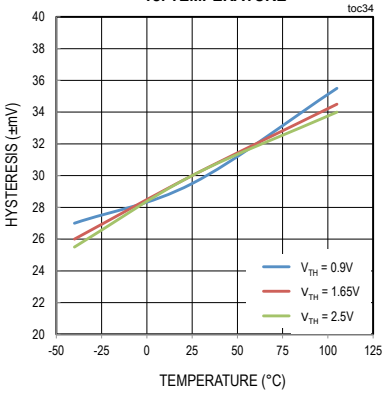
GPI OFFSET vs. SUPPLY VOLTAGE



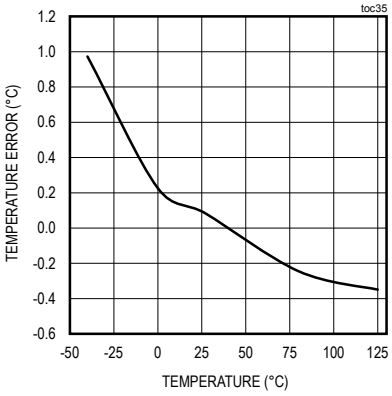
GPI OFFSET vs. TEMPERATURE



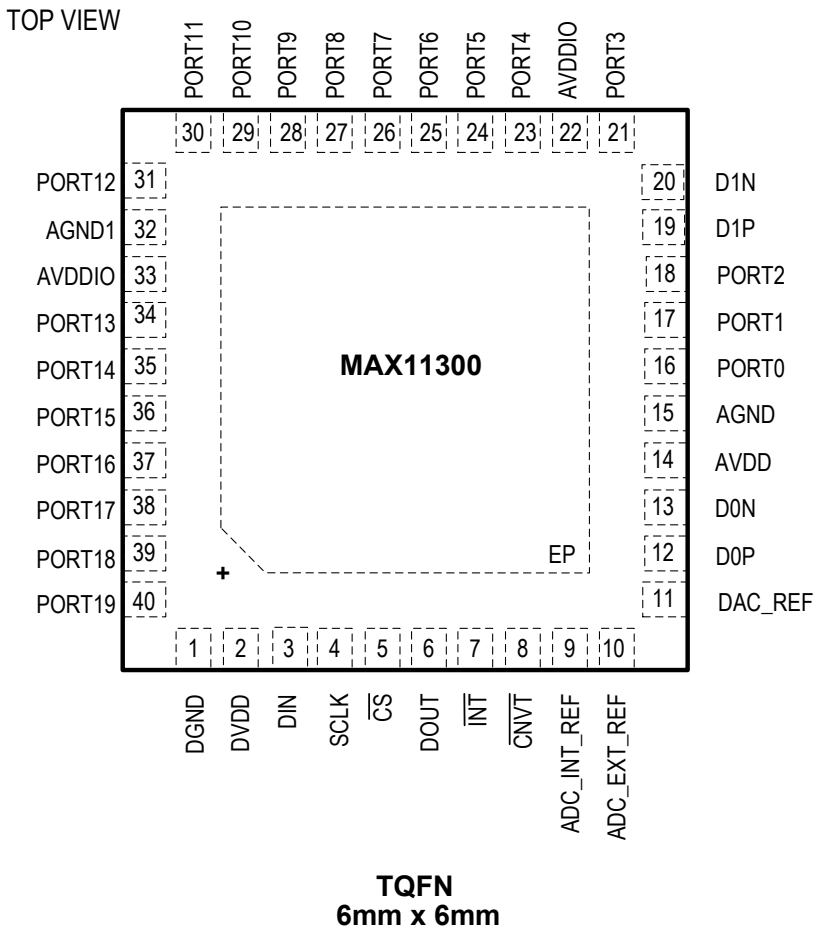
GPI HYSTERESIS vs. TEMPERATURE



EXTERNAL TEMPERATURE SENSOR ERROR vs. TEMPERATURE

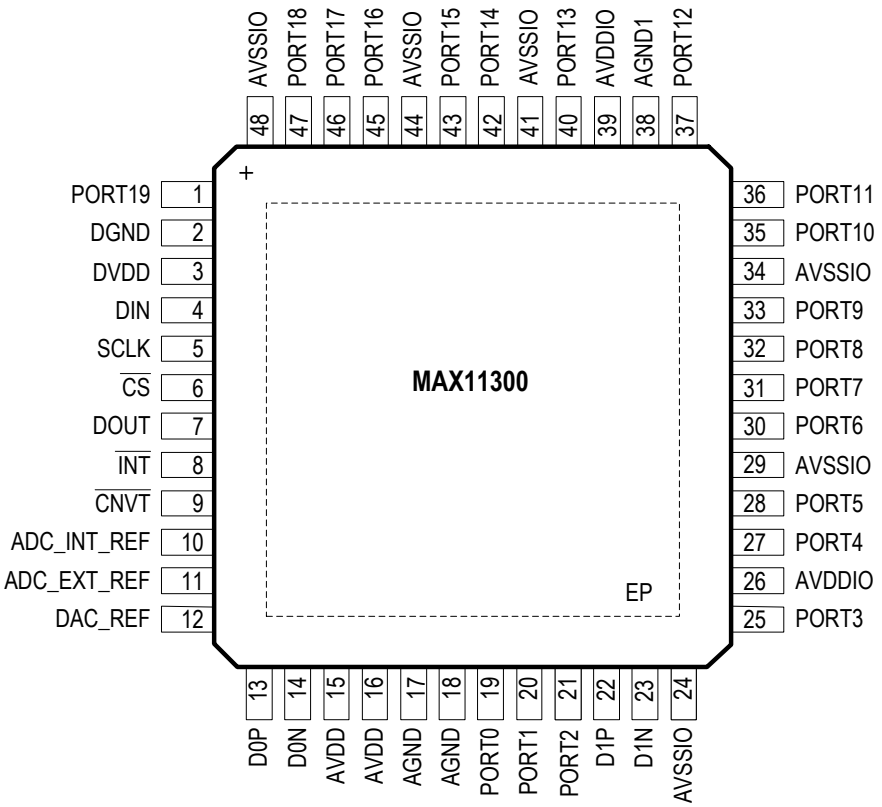


Pin Configurations



TQFN
6mm x 6mm

Pin Configurations (continued)



TQFP
7mm x 7mm
81mm^2 total area

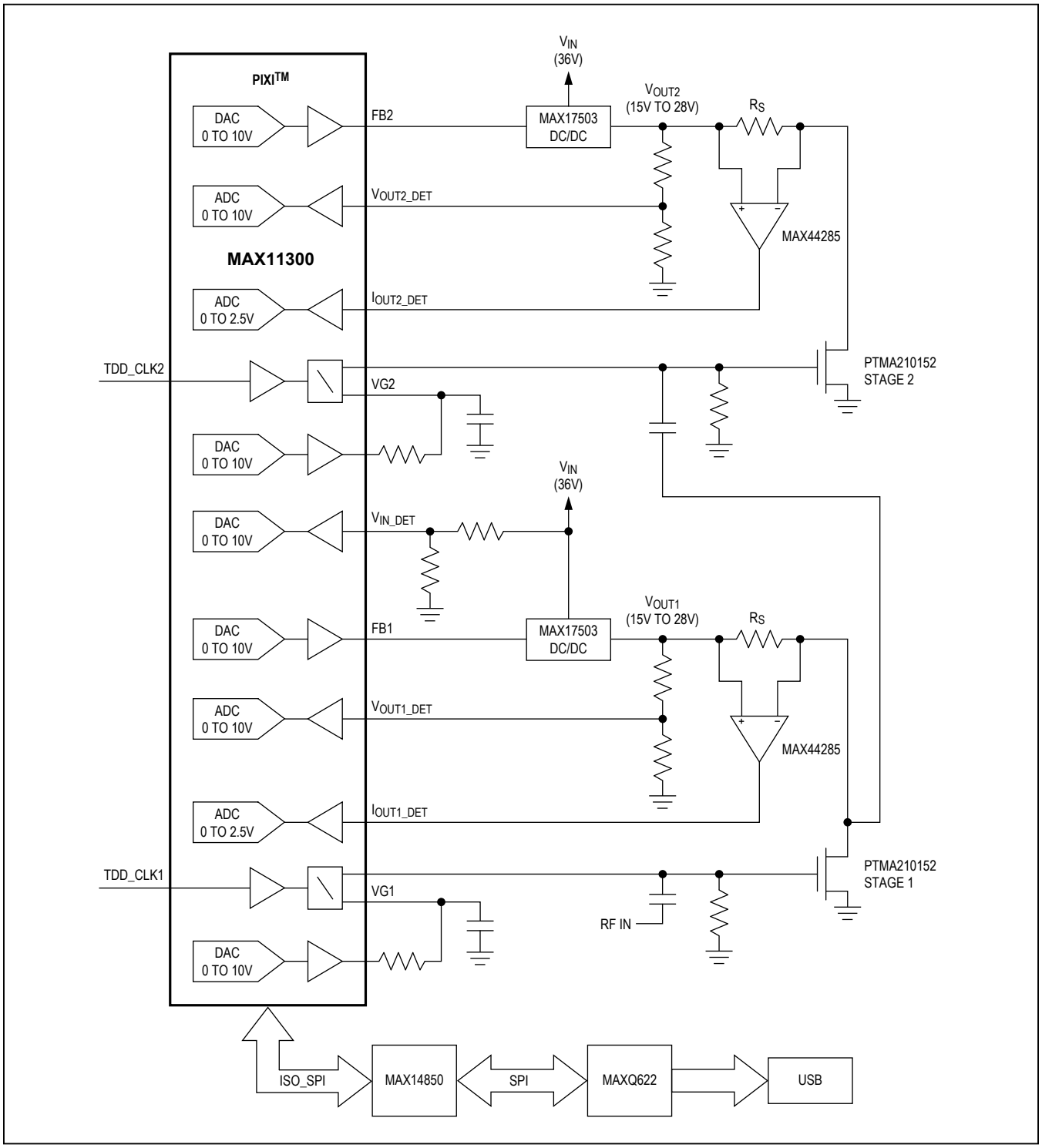
Pin Description

PIN		NAME	FUNCTION
TQFN	TQFP		
1	2	DGND	Digital Ground
2	3	DVDD	Positive Digital Supply
3	4	DIN	Serial Interface Data Input
4	5	SCLK	Serial Interface Clock Input
5	6	$\overline{CS}$	Serial Interface Chip-Select–Active Low
6	7	DOUT	Serial Interface Data Output
7	8	$\overline{INT}$	Interrupt Open-Drain Output. Active low.
8	9	$\overline{CNVT}$	ADC Trigger Control Input. Active low.
9	10	ADC_INT_REF	ADC Internal Voltage Reference Output. Connect a bypass capacitor at this pin (4.7µF to 10µF).
10	11	ADC_EXT_REF	ADC External Voltage Reference Input. Connect a bypass capacitor at this pin (4.7µF recommended).
11	12	DAC_REF	DAC External/Internal Voltage Reference Input. Connect a bypass capacitor at this pin (4.7µF to 10µF).
12	13	D0P	1st External Temperature Sensor Positive Input
13	14	D0N	1st External Temperature Sensor Negative Input
14	15, 16	AVDD	Positive Analog Supply. For TQFP, connect both pins to AVDD.
15	17, 18	AGND	Analog Ground. For TQFP, connect both pins to AGND.
16	19	PORT0	Configurable Mixed-Signal Port 0
17	20	PORT1	Configurable Mixed-Signal Port 1
18	21	PORT2	Configurable Mixed-Signal Port 2
19	22	D1P	2nd External Temperature Sensor Positive Input
20	23	D1N	2nd External Temperature Sensor Negative Input
21	25	PORT3	Configurable Mixed-Signal Port 3
22, 33	26, 39	AVDDIO	Analog Positive Supply For Mixed-Signal Ports. Connect both pins to AVDDIO.
23	27	PORT4	Configurable Mixed-Signal Port 4
24	28	PORT5	Configurable Mixed-Signal Port 5
25	30	PORT6	Configurable Mixed-Signal Port 6
26	31	PORT7	Configurable Mixed-Signal Port 7
27	32	PORT8	Configurable Mixed-Signal Port 8
28	33	PORT9	Configurable Mixed-Signal Port 9
29	35	PORT10	Configurable Mixed-Signal Port 10
30	36	PORT11	Configurable Mixed-Signal Port 11
31	37	PORT12	Configurable Mixed-Signal Port 12
32	38	AGND1	Analog Ground.

Pin Description (continued)

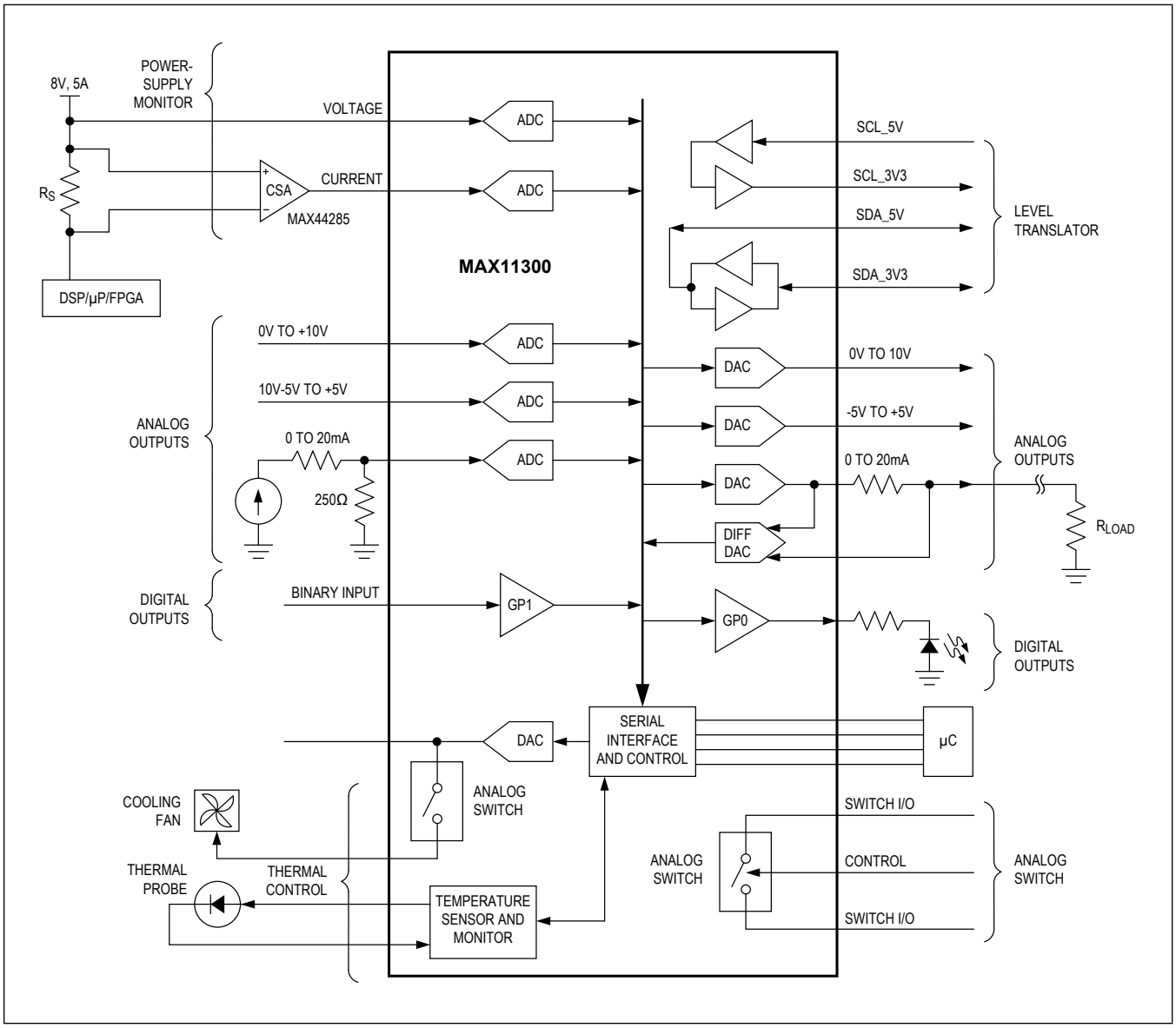
PIN		NAME	FUNCTION
TQFN	TQFP		
34	40	PORT13	Configurable Mixed-Signal Port 13
35	42	PORT14	Configurable Mixed-Signal Port 14
36	43	PORT15	Configurable Mixed-Signal Port 15
37	45	PORT16	Configurable Mixed-Signal Port 16
38	46	PORT17	Configurable Mixed-Signal Port 17
39	47	PORT18	Configurable Mixed-Signal Port 18
40	1	PORT19	Configurable Mixed-Signal Port 19
—	24, 29, 34, 41, 44, 48	AVSSIO	Analog Negative Supply for Mixed-Signal Ports. For TQFP, connect all pins to AVSSIO..
—	—	EP	Exposed Pad. For TQFN, connect EP to AVSSIO. For TQFP, connect EP to AGND.

Typical Application Circuits



PA Biasing Solution

Typical Application Circuits (continued)



Control and Monitoring Solution

Detailed Description

Functional Overview

The MAX11300 has 20 configurable mixed-signal I/O ports. Each port is independently configured as a DAC output, an ADC input, a GPI, a GPO, or an analog switch terminal. User-controllable parameters are available for each of those configurations. The device offers one internal and two external temperature sensors. The serial interface operates as a SPI Mode 0 interface.

The DAC is used to drive out a voltage defined by the DAC data register of the DAC-configured ports. The DAC uses either an internal or external voltage reference. The selection of the voltage reference is set for all the ports and cannot be configured on a port-by-port basis.

The ADC converts voltages applied to the ADC-configured ports. The ADC can operate in single-ended mode or in differential mode, by which any two ports can form a differential pair. The port configured as the negative input of the ADC can be used by more than one differential ADC input pairs. The ADC uses either an internal or external voltage reference. In some configurations, the ADC uses the DAC voltage reference. The ADC voltage reference selection can be configured on a port-by-port basis.

Interrupts provide the host with the occurrence of user-selected events through the configuration of an interrupt mask register.

ADC Operations

The ADC is a 12-bit, low-power, successive approximation analog-to-digital converter, capable of sampling a single input at up to 400ksps. The ADC's conversion rate can be programmed to 400ksps, 333ksps, 250ksps, or 200ksps. The default conversion rate setting is 200ksps. Each ADC-configured port can be programmed for one of four input voltage ranges: 0V to +10V, -5V to +5V, -10V to 0V, and 0V to +2.5V. The ADC uses the internal ADC 2.5V voltage reference, the external ADC voltage reference, or, in some cases, the DAC voltage reference. The voltage reference can be selected on a port-by-port basis.

ADC Control

The ADC can be triggered using an external signal $\overline{CNVT}$ or from a control bit. $\overline{CNVT}$ is active-low and must remain low for a minimal duration of 0.5 µs to trigger a conversion. Four configurations are available:

- Idle mode (default setting).
- Single sweep mode. The ADC sweeps sequentially the ADC-configured ports, from the lowest index port to the highest index port, once $\overline{CNVT}$ is asserted.
- Single conversion mode. The ADC performs a single conversion at the current port in the series of ADC-configured ports when $\overline{CNVT}$ is asserted.
- Continuous sweep mode. The ADC continuously sweeps the ADC-configured ports. The $\overline{CNVT}$ port has no effect in this mode.

ADC Averaging Function

ADC-configured ports can be configured to average blocks of 2, 4, 8, 16, 32, 64, or 128 conversion results. The corresponding ADC data register is updated only when the averaging is completed, thus decreasing the throughput proportionally. If the number of samples to average is modified for a given port, the content of the ADC data register for that port is cleared before starting to average the new block of samples.

ADC Mode Change

When users change the ADC active mode (continuous sweep, single sweep, or single conversion), the ADC data registers are reset. However, ADC data registers retain content when the ADC is changed to idle mode.

ADC Configurations

The ADC can operate in single-ended, differential, or pseudo-differential mode. In single-ended mode, the PIXI port is the positive input to the ADC while the negative input is grounded internally (Figure 3). In differential mode (Figure 4), any pair of PIXI ports can be configured as inputs to the differential ADC. In pseudo-differential mode (Figure 5), one PIXI port produces the voltage applied to the negative input of the ADC while another PIXI port forms the positive input.

The ADC data format is straight binary in single-ended mode, and two's complement in differential and pseudo-differential modes.

DAC Operations

The MAX11300 uses a 12-bit DAC, which operates at the rate of 40µs per port. Since up to 20 ports can be configured in DAC-related modes, the minimum refresh rate per port is 1.25kHz.

No external component is required to set the offset and gain of the DAC drivers. The PIXI port driver features a wide output voltage range of ±10V and high current capability with dedicated power supplies (AVDDIO, AVSSIO).

The DAC uses either the internal or external voltage reference. Unlike the ADC, the DAC voltage reference cannot be configured on a port-by-port basis. DAC mode configuration is illustrated in Figure 6.

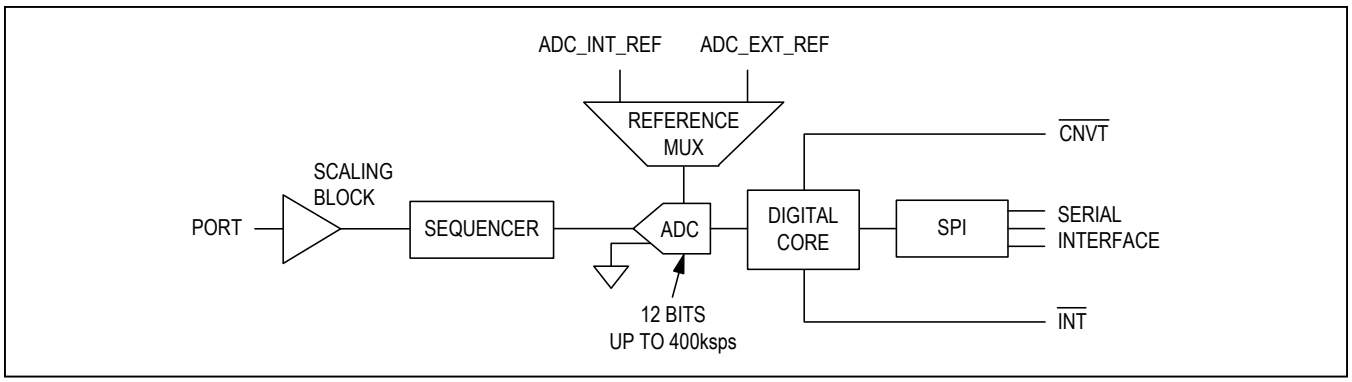


Figure 3. ADC with Single-Ended Input

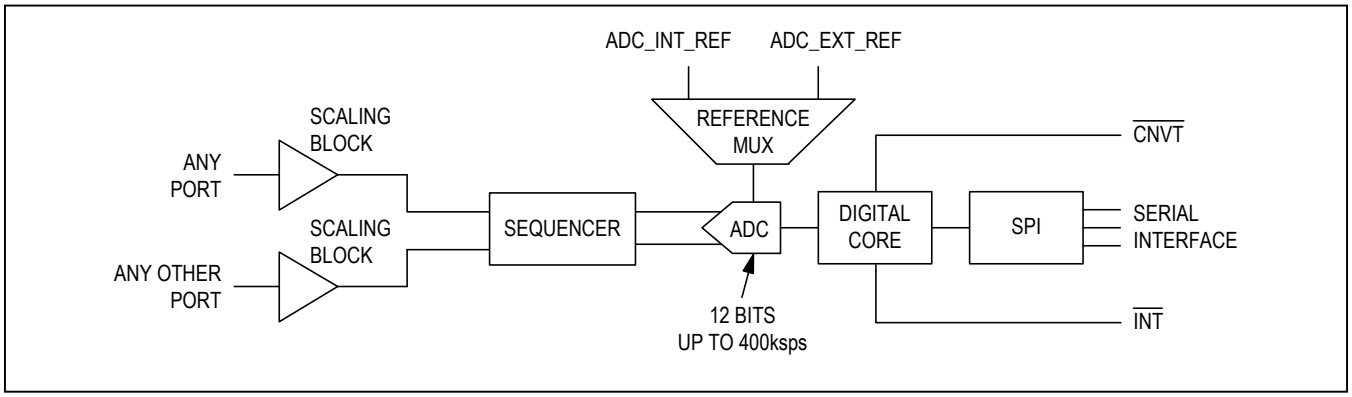


Figure 4. ADC with Differential Inputs

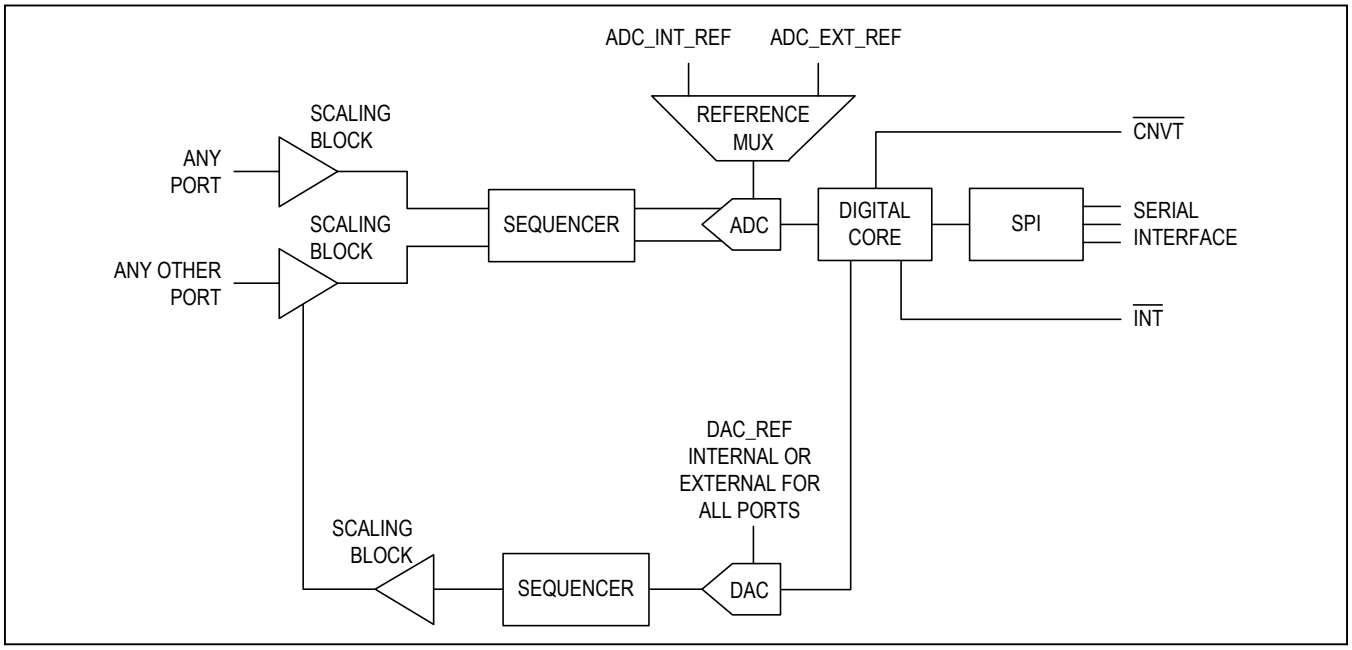


Figure 5. ADC with Pseudo-Differential Input Set by DAC

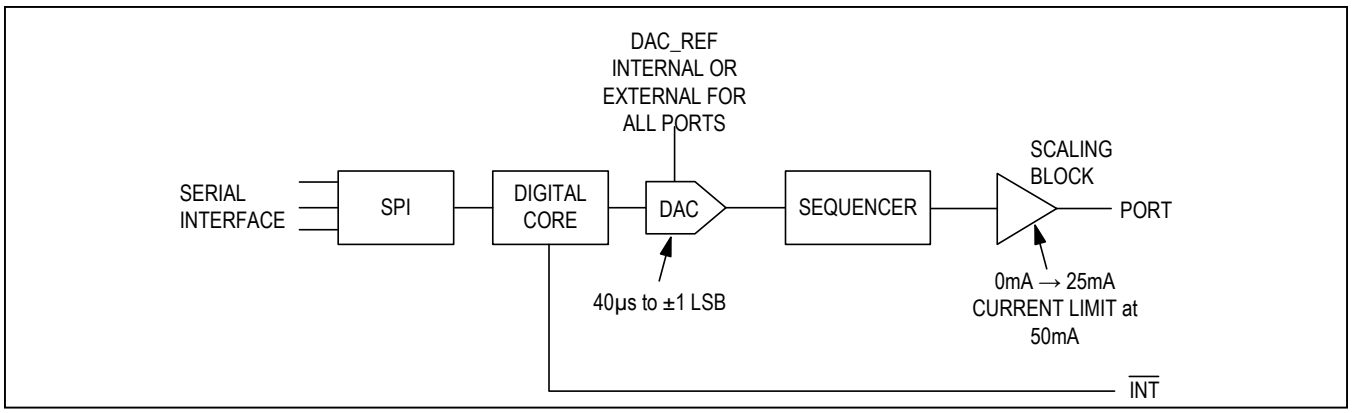


Figure 6. DAC Configuration

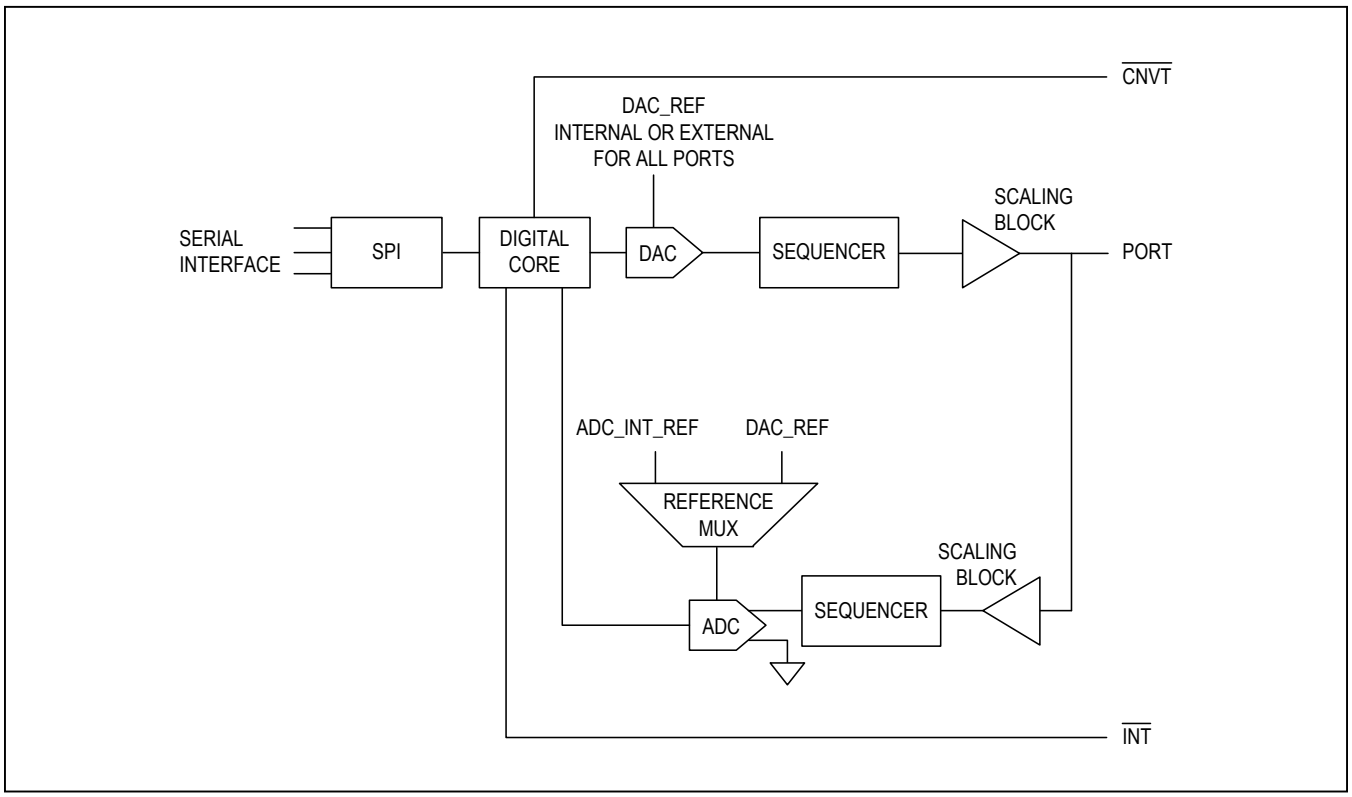


Figure 7. DAC Configuration with ADC Monitoring

DAC operations can be monitored by the ADC. In such a mode, the ADC samples the DAC-configured port to allow the host to monitor that the voltage at the port is within expectations given the accuracy of the ADC and DAC. This ADC monitoring mode is shown in Figure 7.

By default, the DAC updates the DAC-configured ports sequentially. However, users can configure the DAC so that its sequence can jump to update the port that just received new data to convert. After having updated this port, the DAC continues its default sequence from that port. In that mode, users should allow a minimum of 80µs between DAC data register updates for subsequent jump operations.

In addition to port-specific DAC data registers, the host can also use the same data for all DAC-related ports using one of two preset DAC data registers.

All DAC output drivers are protected by overcurrent limit circuitry. In case of overcurrent, the MAX11300 generates an interrupt. Detailed status registers are offered to the host to determine which ports are current limited.

General-Purpose Input and Output

Each PIXI port can be configured as a GPI or a GPO. The GPI threshold (Figure 8) is adjusted by setting the DAC data register of that GPI port to the corresponding voltage. If the DAC data register is set at 0x0FFF, the GPI threshold is the DAC reference voltage. The amplitude of the input signal must be contained within 0V to V_{AVDD}. The GPI-configured port can be set to detect rising edges, falling edges, either rising or falling edges, or none.

When a port is configured as GPO (Figure 9), the amplitude of its logic-one level is set by its DAC data register. If the DAC data register is set at 0x0FFF, the GPO logic-one level is four times the DAC reference voltage. The logic-zero level is always 0V. The host can set the logic state of GPO-configured ports through the corresponding GPO data registers.

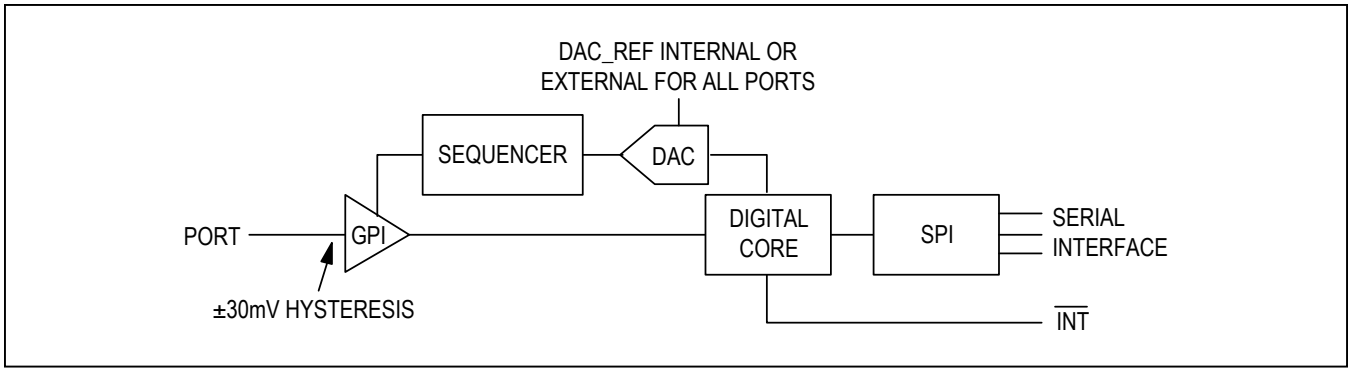


Figure 8. GPI Mode

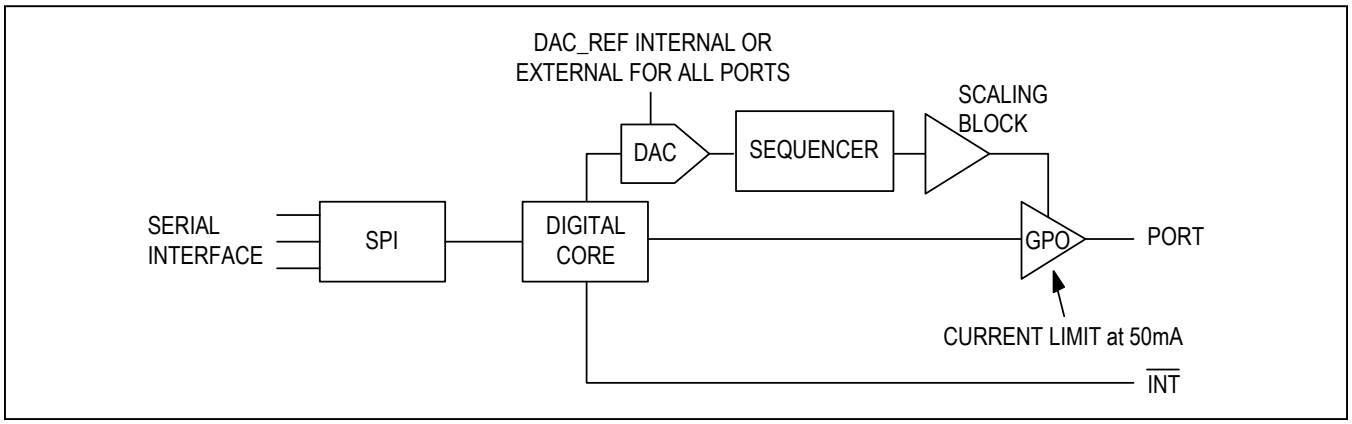


Figure 9. GPO Mode

Unidirectional and Bidirectional Level Translator Operations

By combining GPI- and GPO-configured ports, unidirectional level translator paths can be formed. The signaling at the input of the path can be different from the signaling at the end (Figure 10). For example, a unidirectional path could convert a signal from 1.8V logic level to 3.3V logic level.

The unidirectional path configuration allows for the transmission of signals received on a GPI-configured port to one or more GPO-configured ports.

Pairs of adjacent PIXI ports can also form bidirectional level translator paths that are targeted to operate with open-drain drivers (Figure 11). When used as a bidirectional level translator, the pair of PIXI ports must be accompanied with external pullup resistors to meet proper logic levels.

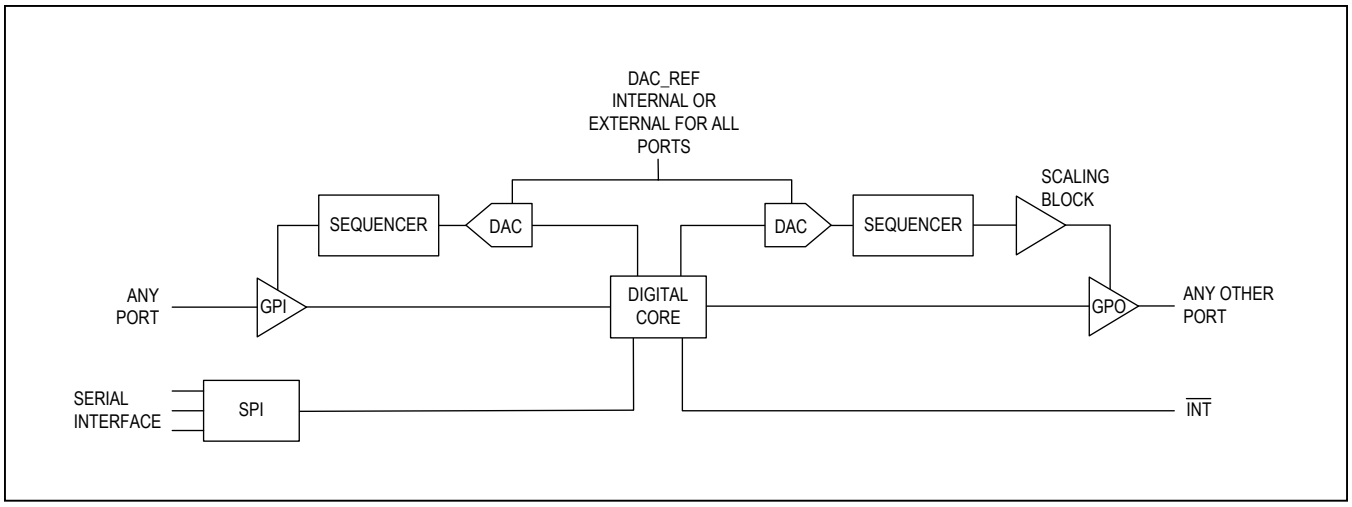


Figure 10. Unidirectional Level Translator Path Mode

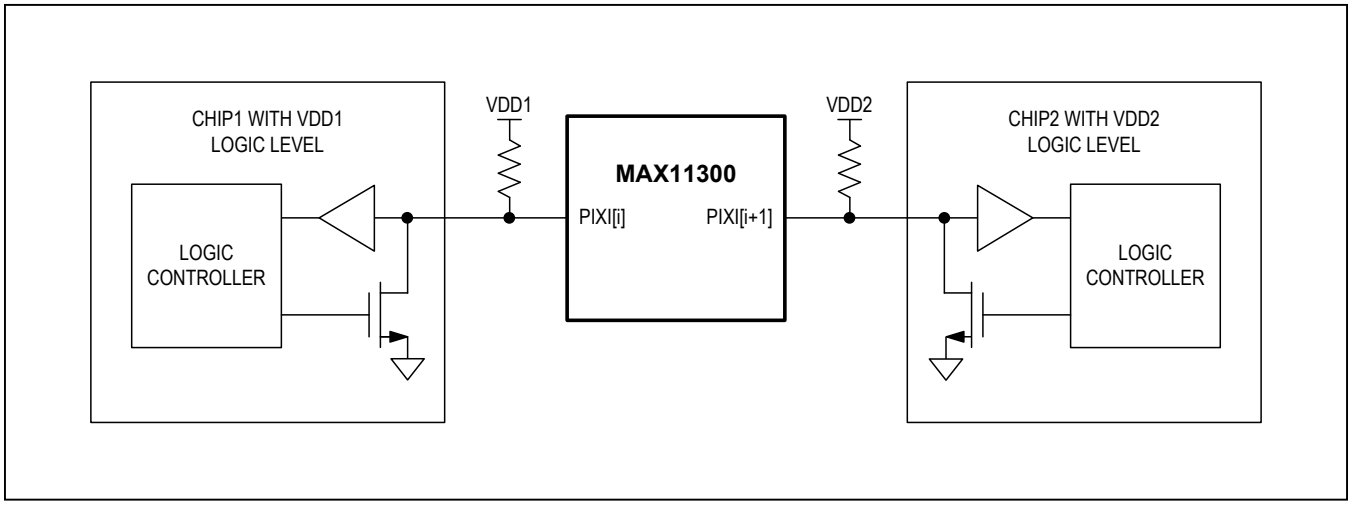


Figure 11. Bidirectional Level Translation Application Diagram

Internally or Externally Controlled Analog Switch Operation

Two adjacent PIXI ports can form a 60Ω analog switch that is controlled by two different configurations. In one configuration, the switch is dynamically controlled by any other GPI-configured PIXI port, as illustrated in Figure 12. The signal applied to that GPI-configured port can be inverted.

In the other configuration, the switch is programmed to be permanently “ON” by configuring the corresponding PIXI port. To turn the switch “OFF”, the host must set that PIXI port in high-impedance configuration.

Power-Supply Brownout Detection

The MAX11300 features a brownout detection circuit that monitors AVDDIO and AVDD pins. When AVDDIO goes below approximately 4.0V, an interrupt is registered, and the interrupt port is asserted if not masked. When AVDD goes below approximately 4.0V, the device resets.

SPI Operations

The MAX11300 SPI interface complies with the timing of Mode 0, as illustrated in Figure 13. The MAX11300 samples incoming data on the rising edge of SCLK and releases outgoing data on the falling edge of SCLK.

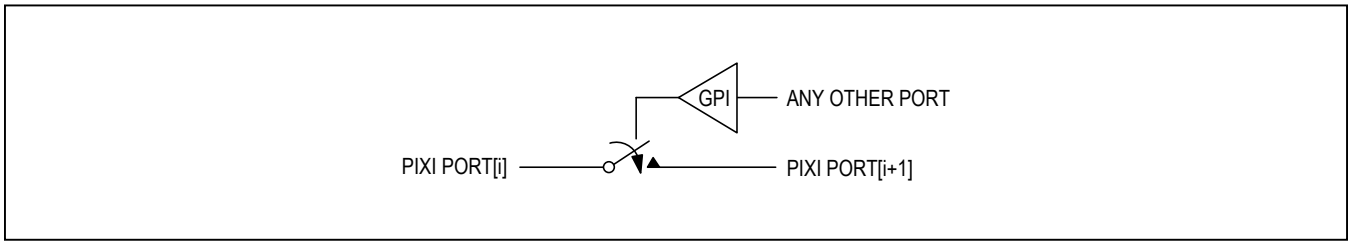


Figure 12. PIXI Ports as a Controllable Analog Switch

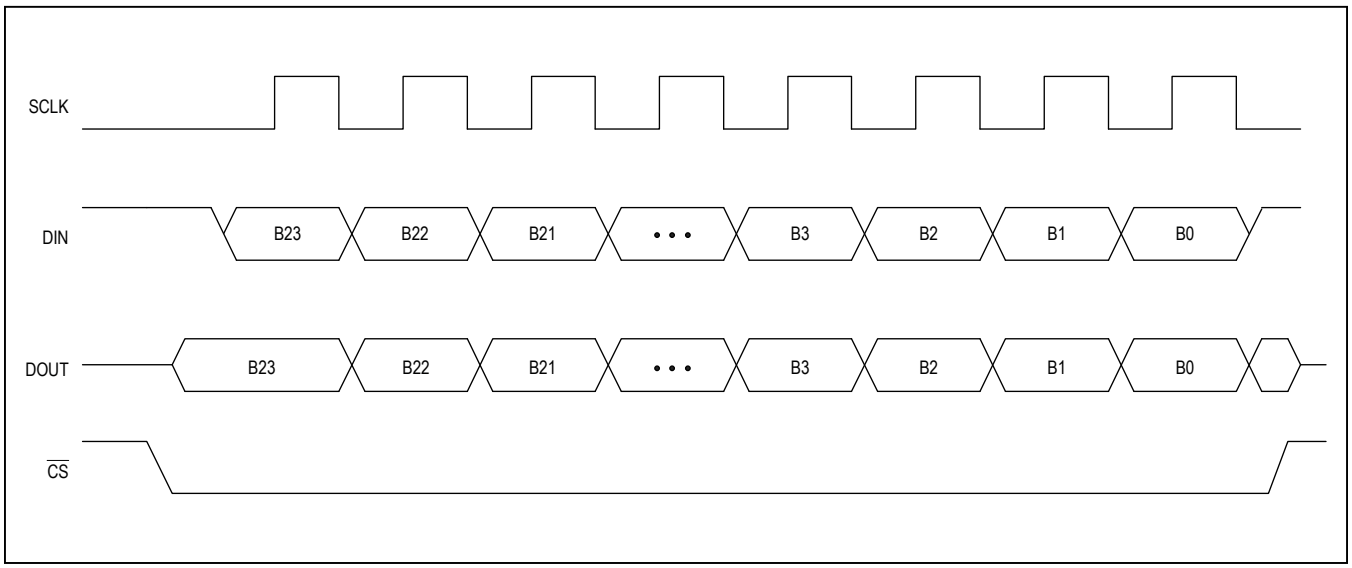


Figure 13. SPI Timing (Mode 0)

SPI transactions are made of a minimum of three bytes. Each transaction is defined by the assertion of $\overline{CS}$. The first byte contains the address and the read/write bit. The second byte carries the most significant byte of the data to either write or read. The third byte contains the least significant byte of the data to either write or read. Such a transaction is shown in Table 1. For write transactions, the targeted register content is modified only after the third byte has been fully received. The bits come out of DOUT (or come in DIN), most significant bit first.

Note that the duration of the transaction is determined by the assertion of $\overline{CS}$. If $\overline{CS}$ remains asserted past the third byte, and if SCLK remains active past the third byte, the MAX11300 assumes that a second data sample is received (or transmitted) corresponding to the next register address. The address keeps on incrementing as $\overline{CS}$ remains asserted and SCLK remains active. Table 2 shows an example of such a burst transaction.

Each time a new data sample is read or written, the register address is incremented by one until it reaches the last register address.

If a transaction targets an unused address, nothing is written within the MAX11300 for write transactions, and all zeros are read back for read transactions. Similarly, if a write transaction targets a read-only register, nothing is written to the device.

Table 1. Single Register SPI Transaction Format

	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	Address[6:0]							R/WB
2nd Byte	Data[15:8]							
3rd Byte	Data[7:0]							

Burst Transaction Address Incrementing Modes

With a burst transaction, the address of the initial register is entered once. The data of the targeted register can then be written or read. If the serial clock keeps running, and if $\overline{CS}$ remains asserted, the device increments the address pointer and writes or reads the next data after the next 16 serial clock periods. This scheme goes on until $\overline{CS}$ is deasserted.

There are two address incrementing modes. In one mode, the address is simply incremented by one (default mode), while in the other, the address is incremented contextually. When writing DAC data registers in a burst fashion using contextual addressing, the host would write the address of the first port that is DAC-configured (starting from the lowest port index). As $\overline{CS}$ remains asserted and another set of 16 serial clock cycles are received, the next DAC-configured port is written. This scheme continues until the last DAC-configured port is reached. At that point, any additional serial clock cycle results in looping back to the first DAC-configured port.

The contextual addressing scheme is only valid for writing DAC data registers, as described above, and reading ADC data registers.

Interrupt Operations

The MAX11300 issues interrupts to alert the host of various events. All events are recorded by the interrupt register. The assertion of an interrupt register bit results in the assertion of the interrupt port ($\overline{INT}$) if that interrupt bit

Table 2. Multiple Register SPI Transaction Format

	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	Address_N[6:0]							R/WB
2nd Byte	Data_N[15:8]							
3rd Byte	Data_N[7:0]							
4th Byte	Data_N+1[15:8]							
5th Byte	Data_N+1[7:0]							
6th Byte	Data_N+2[15:8]							
7th Byte	Data_N+2[7:0]							
8th Byte	Data_N+3[15:8]							
9th Byte	Data_N+3[7:0]							
10th Byte	Data_N+4[15:8]							
11th Byte	Data_N+4[7:0]							

is not masked. By default, all interrupts are masked upon power-up or reset. The interrupts are listed hereafter.

The ADCFLAG (ADC Flag) interrupt indicates that the ADC just completed a conversion or set of conversions. It is asserted either at the end of a conversion when the ADC is in single-conversion mode or at the end of a sweep when the ADC is either in single-sweep mode or continuous-sweep mode. ADCFLAG is cleared when the interrupt register is read.

The ADCDR (ADC Data Ready) interrupt is asserted when at least one ADC data register is refreshed. Since one conversion per ADC-configured port is performed per sweep, many sweeps may be required before refreshing the data register of a given ADC-configured port that utilizes the averaging function. See the *ADC Averaging Function* section. To determine which ADC-configured port received a new data sample, the host must read the ADC status registers. ADCDR is cleared after the interrupt register and both ADC status registers are read subsequently.

The ADCDM (ADC Data Missed) interrupt is asserted when any ADC data register is not read by the host before new data is stored in that ADC data register. ADCDM is cleared after the interrupt register is read.

The GPIER (GPI Event Received) interrupt indicates that an event has been received on one of the GPI-configured ports. Each GPI port can be configured to generate an interrupt for an event such as detecting a rising edge, a falling edge, or either edge at the corresponding port. If the GPI port is configured to detect no edge, it is equivalent to masking the interrupt related to that port. A GPI status register allows the host to identify which port detected the event. GPIER is cleared after the interrupt register and both GPI status registers are read subsequently.

The GPIEM (GPI Event Missed) interrupt informs the host that it did not service the GPI interrupt caused by the occurrence of an event recorded by GPI status registers before another event was received on the same port. The host must read the interrupt register and the GPI status registers whenever a GPI event received interrupt occurs; otherwise, the GPIEM register is asserted upon receiving the next event. This interrupt must be used in conjunction with the GPIER interrupt bit to operate properly. GPIEM is cleared after the interrupt register and both GPI status registers are read subsequently.

The DACOI (DAC Overcurrent) interrupt indicates that a DAC-configured port current exceeded approximately 50mA. This limit is not configurable. A DAC overcurrent status register allows the host to identify which DAC-configured port exceeded the 50mA current limit. DACOI is cleared after the interrupt register is read, and both DAC overcurrent status registers are read subsequently.

The TMPINT[2:0] (Internal Temperature Monitor) interrupt has three sources of interrupt, each independently controllable: a new internal temperature value is ready, the internal temperature value exceeds the maximum limit, or the internal temperature value is below the minimum limit. TMPINT is cleared after the interrupt register is read.

The TMPEXT1[2:0] (1st External Temperature Monitor) interrupt has three sources of interrupt, each independently controllable: a new first external temperature value is ready, the first external temperature value exceeds the maximum limit, or the first external temperature value is below the minimum limit. TMPEXT1 is cleared after the interrupt register is read.

The TMPEXT2[2:0] (2nd External Temperature Monitor) interrupt has three sources of interrupt, each independently controllable: a new second external temperature value is ready, the second external temperature value exceeds the maximum limit, or the second external temperature value is below the minimum limit. TMPEXT2 is cleared after the interrupt register is read.

The VMON (High-Voltage Supply Monitor) interrupt is triggered when AVDDIO supply voltage falls below approximately 4V. VMON is cleared after the interrupt register is read.

Temperature Sensors Overview

The MAX11300 integrates one internal and two external temperature sensors. The external sensors are diode-connected transistors, typically a low-cost, easily mounted 2N3904 NPN type, that replace conventional thermistors or thermocouples. The external sensors' accuracy is typically ±1°C over the -40°C to +150°C temperature range with no calibration necessary. Use of a transistor with a different ideality factor produces a proportionate difference in the absolute measured temperature. Parasitic series resistance results in a temperature reading error of about 0.25°C per Ohm of resistance. The MAX11300 features a series resistance cancellation mode (RS_CANCEL) that eliminates this error for resistances up to 10 Ohms. The external sensors can also measure the die temperature of other ICs, such as microprocessors, that contain a substrate-connected diode available for temperature-sensing purposes. Temperature data can be read from the temperature data registers. The temperature data format is in two's complement, with one LSB representing 0.125°C.

Register Description

Register bits that are shown unused do not impact device functionality and read out as “0”.

Table 3. Register Table (Read/Write)

ADDRESS	DESCRIPTION	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0x00 (R)	Device ID	DEVID[15:0]																0x0424
0x01 (R)	Interrupt	VMON	TMPEXT2[2:0]			TMPEXT1[2:0]			TMPINT[2:0]			DACOI	GPIDM	GPIDR	ADCDM	ADCDR	ADCFLAG	0x0000
0x02 (R)	ADC data status; ports 0-15	ADCST[15:0]																0x0000
0x03 (R)	ADC data status; ports 16-19	UNUSED												ADCST[19:16]				0x0000
0x04 (R)	Overcurrent status; ports 0-15	DACOIST[15:0]																0x0000
0x05 (R)	Overcurrent status; ports 16-19	UNUSED												DACOIST[19:16]				0x0000
0x06 (R)	GPI status; ports 0-15	GPIST[15:0]																0x0000
0x07 (R)	GPI status; ports 16-19	UNUSED												GPIST[19:16]				0x0000
0x08 (R)	Internal temperature data	UNUSED				TMPINTDAT[11:0]												0x0000
0x09 (R)	1st external temperature data	UNUSED				TMPEXT1DAT[11:0]												0x0000
0x0A (R)	2nd external temperature data	UNUSED				TMPEXT2DAT[11:0]												0x0000
0x0B (R)	GPI data; ports 15-0	GPIDAT[15:0]																0x0000
0x0C (R)	GPI data; ports 19-16	UNUSED												GPIDAT[19:16]				0x0000
0x0D (R/W)	GPO data; ports 15-0	GPODAT[15:0]																0x0000
0x0E (R/W)	GPO data; ports 19-16	UNUSED												GPODAT[19:16]				0x0000
0x10 (R/W)	Device control	Reset	BRST	LPEN	RS_CANCEL	TMPPER	TmPCTL[2:0]			THSHDN	DACREF	ADCconv[1:0]		DACCtL[1:0]		ADCCTL[1:0]		0x0000
0x11 (R/W)	Interrupt mask	VMON MSK	TMPEXT2 MSK[2:0]			TMPEXT1 MSK[2:0]			TMPINT MSK[2:0]			DACOI MSK	GPID MMSK	GPIDR MSK	ADCDM MSK	ADCDR MSK	ADCFLAG MSK	0xFFFF
0x12 (R/W)	GPI IRQ mode; ports 0–7	GPIMD_7[1:0]		GPIMD_6[1:0]		GPIMD_5[1:0]		GPIMD_4[1:0]		GPIMD_3[1:0]		GPIMD_2[1:0]		GPIMD_1[1:0]		GPIMD_0[1:0]		0x0000
0x13 (R/W)	GPI IRQ mode; ports 8–15	GPIMD_15[1:0]		GPIMD_14[1:0]		GPIMD_13[1:0]		GPIMD_12[1:0]		GPIMD_11[1:0]		GPIMD_10[1:0]		GPIMD_9[1:0]		GPIMD_8[1:0]		0x0000
0x14 (R/W)	GPI IRQ mode; ports 16–19	UNUSED								GPIMD_19[1:0]		GPIMD_18[1:0]		GPIMD_17[1:0]		GPIMD_16[1:0]		0x0000
0x16 (R/W)	DAC preset data #1	UNUSED				DACPRSTDAT1[11:0]												0x0000
0x17 (R/W)	DAC preset data #2	UNUSED				DACPRSTDAT2[11:0]												0x0000
0x18 (R/W)	Temperature monitor Configuration	UNUSED										TMPEXT2MONCFG [1:0]		TMPEXT1MONCFG [1:0]		TMPINTMONCFG [1:0]		0x0000

Table 3. Register Table (Read/Write) (continued)

ADDRESS	DESCRIPTION	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0x19 (R/W)	Internal temperature high threshold	UNUSED				TMPINTHI[11:0]												0x07FF
0x1A (R/W)	Internal temperature low threshold	UNUSED				TMPINTLO[11:0]												0x0800
0x1B (R/W)	1st external temperature high threshold	UNUSED				TMPEXT1HI[11:0]												0x07FF
0x1C (R/W)	1st external temperature low threshold	UNUSED				TMPEXT1LO[11:0]												0x0800
0x1D (R/W)	2nd external temperature high threshold	UNUSED				TMPEXT2HI[11:0]												0x07FF
0x1E (R/W)	2nd external temperature low threshold	UNUSED				TMPEXT2LO[11:0]												0x0800
0x20 (R/W)	Port 0 configuration	FUNCID_0[3:0]				FUNCPRM_0[11:0]												0x0000
0x21 (R/W)	Port 1 configuration	FUNCID_1[3:0]				FUNCPRM_1[11:0]												0x0000
0x22 (R/W)	Port 2 configuration	FUNCID_2[3:0]				FUNCPRM_2[11:0]												0x0000
0x23 (R/W)	Port 3 configuration	FUNCID_3[3:0]				FUNCPRM_3[11:0]												0x0000
0x24 (R/W)	Port 4 configuration	FUNCID_4[3:0]				FUNCPRM_4[11:0]												0x0000
0x25 (R/W)	Port 5 configuration	FUNCID_5[3:0]				FUNCPRM_5[11:0]												0x0000
0x26 (R/W)	Port 6 configuration	FUNCID_6[3:0]				FUNCPRM_6[11:0]												0x0000
0x27 (R/W)	Port 7 configuration	FUNCID_7[3:0]				FUNCPRM_7[11:0]												0x0000
0x28 (R/W)	Port 8 configuration	FUNCID_8[3:0]				FUNCPRM_8[11:0]												0x0000
0x29 (R/W)	Port 9 configuration	FUNCID_9[3:0]				FUNCPRM_9[11:0]												0x0000
0x2A (R/W)	Port 10 configuration	FUNCID_10[3:0]				FUNCPRM_10[11:0]												0x0000
0x2B (R/W)	Port 11 configuration	FUNCID_11[3:0]				FUNCPRM_11[11:0]												0x0000
0x2C (R/W)	Port 12 configuration	FUNCID_12[3:0]				FUNCPRM_12[11:0]												0x0000
0x2D (R/W)	Port 13 configuration	FUNCID_13[3:0]				FUNCPRM_13[11:0]												0x0000
0x2E (R/W)	Port 14 configuration	FUNCID_14[3:0]				FUNCPRM_14[11:0]												0x0000
0x2F (R/W)	Port 15 configuration	FUNCID_15[3:0]				FUNCPRM_15[11:0]												0x0000
0x30 (R/W)	Port 16 configuration	FUNCID_16[3:0]				FUNCPRM_16[11:0]												0x0000
0x31 (R/W)	Port 17 configuration	FUNCID_17[3:0]				FUNCPRM_17[11:0]												0x0000

Table 3. Register Table (Read/Write) (continued)

ADDRESS	DESCRIPTION	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0x32 (R/W)	Port 18 configuration	FUNCID_18[3:0]				FUNCPRM_18[11:0]												0x0000
0x33 (R/W)	Port 19 configuration	FUNCID_19[3:0]				FUNCPRM_19[11:0]												0x0000
0x40 (R)	Port 0 ADC data	UNUSED				ADCDAT_0[11:0]												0x0000
0x41 (R)	Port 1 ADC data	UNUSED				ADCDAT_1[11:0]												0x0000
0x42 (R)	Port 2 ADC data	UNUSED				ADCDAT_2[11:0]												0x0000
0x43 (R)	Port 3 ADC data	UNUSED				ADCDAT_3[11:0]												0x0000
0x44 (R)	Port 4 ADC data	UNUSED				ADCDAT_4[11:0]												0x0000
0x45 (R)	Port 5 ADC data	UNUSED				ADCDAT_5[11:0]												0x0000
0x46 (R)	Port 6 ADC data	UNUSED				ADCDAT_6[11:0]												0x0000
0x47 (R)	Port 7 ADC data	UNUSED				ADCDAT_7[11:0]												0x0000
0x48 (R)	Port 8 ADC data	UNUSED				ADCDAT_8[11:0]												0x0000
0x49 (R)	Port 9 ADC data	UNUSED				ADCDAT_9[11:0]												0x0000
0x4A (R)	Port 10 ADC data	UNUSED				ADCDAT_10[11:0]												0x0000
0x4B (R)	Port 11 ADC data	UNUSED				ADCDAT_11[11:0]												0x0000
0x4C (R)	Port 12 ADC data	UNUSED				ADCDAT_12[11:0]												0x0000
0x4D (R)	Port 13 ADC data	UNUSED				ADCDAT_13[11:0]												0x0000
0x4E (R)	Port 14 ADC data	UNUSED				ADCDAT_14[11:0]												0x0000
0x4F (R)	Port 15 ADC data	UNUSED				ADCDAT_15[11:0]												0x0000
0x50 (R)	Port 16 ADC data	UNUSED				ADCDAT_16[11:0]												0x0000
0x51 (R)	Port 17 ADC data	UNUSED				ADCDAT_17[11:0]												0x0000
0x52 (R)	Port 18 ADC data	UNUSED				ADCDAT_18[11:0]												0x0000
0x53 (R)	Port 19 ADC data	UNUSED				ADCDAT_19[11:0]												0x0000
0x60 (R/W)	Port 0 DAC data	UNUSED				DACDAT_0[11:0]												0x0000
0x61 (R/W)	Port 1 DAC data	UNUSED				DACDAT_1[11:0]												0x0000
0x62 (R/W)	Port 2 DAC data	UNUSED				DACDAT_2[11:0]												0x0000
0x63 (R/W)	Port 3 DAC data	UNUSED				DACDAT_3[11:0]												0x0000
0x64 (R/W)	Port 4 DAC data	UNUSED				DACDAT_4[11:0]												0x0000
0x65 (R/W)	Port 5 DAC data	UNUSED				DACDAT_5[11:0]												0x0000
0x66 (R/W)	Port 6 DAC data	UNUSED				DACDAT_6[11:0]												0x0000
0x67 (R/W)	Port 7 DAC data	UNUSED				DACDAT_7[11:0]												0x0000
0x68 (R/W)	Port 8 DAC data	UNUSED				DACDAT_8[11:0]												0x0000
0x69 (R/W)	Port 9 DAC data	UNUSED				DACDAT_9[11:0]												0x0000
0x6A (R/W)	Port 10 DAC data	UNUSED				DACDAT_10[11:0]												0x0000
0x6B (R/W)	Port 11 DAC data	UNUSED				DACDAT_11[11:0]												0x0000
0x6C (R/W)	Port 12 DAC data	UNUSED				DACDAT_12[11:0]												0x0000
0x6D (R/W)	Port 13 DAC data	UNUSED				DACDAT_13[11:0]												0x0000
0x6E (R/W)	Port 14 DAC data	UNUSED				DACDAT_14[11:0]												0x0000
0x6F (R/W)	Port 15 DAC data	UNUSED				DACDAT_15[11:0]												0x0000
0x70 (R/W)	Port 16 DAC data	UNUSED				DACDAT_16[11:0]												0x0000
0x71 (R/W)	Port 17 DAC data	UNUSED				DACDAT_17[11:0]												0x0000
0x72 (R/W)	Port 18 DAC data	UNUSED				DACDAT_18[11:0]												0x0000
0x73 (R/W)	Port 19 DAC data	UNUSED				DACDAT_19[11:0]												0x0000

Register Detailed Description

Device ID Register (Read)

BIT	FIELD NAME	DESCRIPTION
15:0	DEVID[15:0]	**Device ID** • 0000_0100_0010_0100

Interrupt Register (Read)

BIT	FIELD NAME	DESCRIPTION
0	ADCFLAG	**ADC flag interrupt** • Asserted when the ADC completes a conversion (ADC set in single-conversion mode) or when the ADC completes a sweep (ADC set in single-sweep or continuous-sweep mode). • No interrupt is generated when the ADC is in idle mode. • Cleared after the interrupt register is read.
1	ADCDR	**ADC data ready interrupt** • Asserted when any ADC data register receives a new data sample. If a port is configured to average 2^N samples, it takes 2^N sweeps for that port data register to be refreshed and assert ADCDR. • Data registers are refreshed either at the end of a conversion (ADC set in single-conversion mode) or at the end of a sweep (ADC set in single-sweep or continuous-sweep mode). • Cleared after the interrupt register is read, and after both ADCST[15:0] and ADCST[19:16] registers are read subsequently.
2	ADCDM	**ADC data missed interrupt** • Asserted when the host missed reading a port's ADC data register by the time that port's ADC data register is overwritten by new data. • Cleared after the interrupt register is read.
3	GPIDR	**GPI event ready interrupt** • Asserted when a new event is captured by GPI-configured ports. The type of event is set by the corresponding GPI IRQ mode register. The host can then consult GPIST[15:0] and GPIST[19:16] registers to identify the port that caused the interrupt. • Cleared after the interrupt register is read, and after both GPIST[15:0] and GPIST[19:16] are read subsequently.
4	GPIDM	**GPI event missed interrupt** • Asserted when the host missed reading the GPI status register by the time that register is overwritten. • Must be used in conjunction with GPIDR for proper operation. • Cleared after the interrupt register is read, and after both GPIST[15:0] and GPIST[19:16] are read subsequently.
5	DACOI	**DAC driver overcurrent interrupt** • Asserted when the DAC driver current exceeds approximately 50mA. The host can then read DACOIST[15:0] and DACOIST[19:16] to identify the port that caused the interrupt. • Cleared after the interrupt register is read, and after both DACOIST[15:0] and DACOIST[19:16] registers are read subsequently.

Interrupt Register (Read) (continued)

BIT	FIELD NAME	DESCRIPTION
8:6	TMPINT[2:0]	**Internal temperature interrupts** • TMPINT[2]: Asserted when the internal temperature value is larger than the value stored in TMPINTHI[11:0]. Cleared after the interrupt register is read. • TMPINT[1]: Asserted when the internal temperature value is lower than the value stored in TMPINTLO[11:0]. Cleared after the interrupt register is read. • TMPINT[0]: Asserted when a new temperature value is available. Cleared after the interrupt register is read.
11:9	TMPEXT1[2:0]	**1st external temperature interrupts** • TMPEXT1[2]: Asserted when the 1st external temperature value is larger than the value stored in TMPEXT1HI[11:0]. Cleared after the interrupt register is read. • TMPEXT1[1]: Asserted when the 1st external temperature value is lower than the value stored in TMPEXT1LO[11:0]. Cleared after the interrupt register is read. • TMPEXT1[0]: Asserted when a new temperature value is available. Cleared after the interrupt register is read.
14:12	TMPEXT2[2:0]	**2nd external temperature interrupts** • TMPEXT2[2]: Asserted when the 2nd external temperature value is larger than the value stored in TMPEXT2HI[11:0]. Cleared after the interrupt register is read. • TMPEXT2[1]: Asserted when the 2nd external temperature value is lower than the value stored in TMPEXT2LO[11:0]. Cleared after the interrupt register is read. • TMPEXT2[0]: Asserted when a new temperature value is available. Cleared after the interrupt register is read.
15	VMON	**High-voltage supply monitor interrupt** • Asserted when the high voltage supply (AVDDIO) falls below approximately 4V. • Cleared after the interrupt register is read.

ADC Status Registers (Read)

BIT	FIELD NAME	DESCRIPTION
15:0 3:0	ADCST[15:0] ADCST[19:16]	**Status of ADC data received for ports 0 to 19** • Once new data is written in an ADC data register, the corresponding ADCST bit is asserted. The new data is written only after the set of samples to average is collected when the averaging function is enabled. • This register content is not affected by any related interrupt mask. Activity on ADC-configured ports is recorded by this register regardless of the mask interrupt register setting. • Cleared after the interrupt register is read, and after both ADCST[15:0] and ADCST[19:16] registers are read, subsequently.

Overcurrent Status Registers (Read)

BIT	FIELD NAME	DESCRIPTION
15:0 3:0	DACOIST[15:0] DACOIST[19:16]	**Status of DAC drivers overcurrent for ports 0 to 19** • Once a port driver exceeds approximately 50mA, the host can identify which driver caused the interrupt by reading DACOIST[15:0] and DACOIST[19:16]. • This register content is not affected by any related interrupt mask. Activity on overcurrent detection is recorded by these registers regardless of the mask interrupt register setting. • Cleared after the interrupt register is read, and after both DACOIST[15:0] and DACOIST[19:16] registers are read, subsequently..

Internal Temperature Data Register (Read)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPINTDAT[11:0]	**Internal temperature measurement data** • Temperature measurement produced by the internal temperature sensor. • The data sample is represented in two's complement, and one LSB represents 0.125°C.

1st External Temperature Data Register (Read)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT1DAT[11:0]	**1st external temperature measurement data** • Temperature measurement produced by the first external temperature sensor. • The data sample is represented in two's complement, and one LSB represents 0.125°C.

2nd External Temperature Data Register (Read)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT2DAT[11:0]	**2nd external temperature measurement data** • Temperature measurement produced by the second external temperature sensor. • The data sample is represented in two's complement, and one LSB represents 0.125°C.

GPI Status Registers (Read)

BIT	FIELD NAME	DESCRIPTION
15:0 3:0	GPIST[15:0] GPIST[19:16]	**Status of GPI event detection for ports 0 to 19** • Asserted when an event is detected on a GPI-configured port. The type of event to detect is set by the corresponding GPI IRQ register. • Once a GPIDT interrupt is generated, the host can identify which GPI port(s) caused the interrupt by reading GPIST[15:0] and GPIST[19:16] registers. • GPIST content is not affected by any related interrupt mask. Activity on GPI-configured ports is recorded by GPIST regardless of the mask interrupt register setting. • Cleared after the interrupt register is read, and after both GPIST[15:0] and GPIST[19:16] registers are read, subsequently.

Interrupt Mask Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
0	ADCFLAGMSK	**ADC flag interrupt mask** • Masks ADCFLAG interrupt bit when asserted. • In ADC continuous-sweep mode, $\overline{INT}$ is asserted for 100nS at the end of each sweep whether ADCFLAG interrupt is cleared or not. • 1: Prevents the assertion of ADCFLAG interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of ADCFLAG interrupt bit to pull $\overline{INT}$ low.
1	ADCDRMSK	**ADC data ready interrupt mask** • Masks ADCDR interrupt bit when asserted. • 1: Prevents the assertion of ADCDR interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of ADCDR interrupt bit to pull $\overline{INT}$ low.
2	ADCDMMSK	**ADC data missed interrupt mask** • Masks ADCDM interrupt bit when asserted. • 1: Prevents the assertion of ADCDM interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of ADCDM interrupt bit to pull $\overline{INT}$ low.
3	GPIDRMSK	**GPI event ready interrupt mask** • Masks GPIDR interrupt bit when asserted. • Supersedes the settings in the GPI IRQ Mode registers. • 1: Prevents the assertion of GPIDR interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of GPIDR interrupt bit to pull $\overline{INT}$ low.
4	GPIDMMSK	**GPI event missed interrupt mask** • Masks GPIDM interrupt bit when asserted. • Can be deasserted only if GPIDRMSK is deasserted. • 1: Prevents the assertion of GPIDM interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of GPIDM interrupt bit to pull $\overline{INT}$ low.
5	DACOIMSK	**DAC driver overcurrent interrupt mask** • Masks DACOI interrupt bit when asserted. • 1: Prevents the assertion of DACOI interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of DACOI interrupt bit to pull $\overline{INT}$ low.
8:6	TMPINTMSK[2:0]	**Internal temperature interrupt mask** • Masks TMPINT[2:0] interrupt bits when asserted on a bit-by-bit basis. • 1: Prevents the assertion of TMPINT[i] interrupt bit from pulling $\overline{INT}$ low ($0 \le i \le 2$). • 0: Allows the assertion of TMPINT[i] interrupt bit to pull $\overline{INT}$ low ($0 \le i \le 2$).
11:9	TMPEXT1MSK[2:0]	**1st external temperature interrupt mask** • Masks TMPEXT1[2:0] interrupt bits when asserted on a bit-by-bit basis. • 1: Prevents the assertion of TMPEXT1[i] interrupt bit from pulling $\overline{INT}$ low ($0 \le i \le 2$). • 0: Allows the assertion of TMPEXT1[i] interrupt bit to pull $\overline{INT}$ low ($0 \le i \le 2$).
14:12	TMPEXT2MSK[2:0]	**2nd external temperature interrupt mask** • Masks TMPEXT2[2:0] interrupt bits when asserted on a bit-by-bit basis. • 1: Prevents the assertion of TMPEXT2[i] interrupt bit from pulling $\overline{INT}$ low ($0 \le i \le 2$). • 0: Allows the assertion of TMPEXT2[i] interrupt bit to pull $\overline{INT}$ low ($0 \le i \le 2$).
15	VMONMSK	**High-voltage supply monitor mask** • Masks VMON interrupt bit when asserted. • 1: Prevents the assertion of VMON interrupt bit from pulling $\overline{INT}$ low. • 0: Allows the assertion of VMON interrupt bit to pull $\overline{INT}$ low.

GPI IRQ Mode Registers (Read/Write)

BIT	FIELD NAME	DESCRIPTION

1:0	GPIMD_0[1:0]	**GPI interrupt request mode for ports 0 to 19**
		• Each input port is controlled by GPIMD, a 2-bit code.
		• For a given port i (0≤i≤19):
		  • GPIMD_i[1:0] = 00: GPIST[i] is never asserted
		  • GPIMD_i[1:0] = 01: GPIST[i] is asserted upon detection of a positive edge
		  • GPIMD_i[1:0] = 10: GPIST[i] is asserted upon detection of a negative edge
		  • GPIMD_i[1:0] = 11: GPIST[i] is asserted upon detection of a positive or a negative edge

3:2	GPIMD_1[1:0]	
5:4	GPIMD_2[1:0]	
7:6	GPIMD_3[1:0]	
9:8	GPIMD_4[1:0]	
11:10	GPIMD_5[1:0]	
13:12	GPIMD_6[1:0]	
15:14	GPIMD_7[1:0]	
1:0	GPIMD_8[1:0]	
3:2	GPIMD_9[1:0]	
5:4	GPIMD_10[1:0]	
7:6	GPIMD_11[1:0]	
9:8	GPIMD_12[1:0]	
11:10	GPIMD_13[1:0]	
13:12	GPIMD_14[1:0]	
15:14	GPIMD_15[1:0]	
1:0	GPIMD_16[1:0]	
3:2	GPIMD_17[1:0]	
5:4	GPIMD_18[1:0]	
7:6	GPIMD_19[1:0]	

Device Control Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
1:0	ADCCTL[1:0]	**ADC conversion mode selection** • 00: Idle mode – The ADC does not perform any conversion. • 01: Single sweep – The ADC performs one conversion for each of the ADC-configured ports sequentially. The assertion of $\overline{CNVT}$ triggers the single sweep. The sweep starts with the ADC-configured port of lowest index and stops with the ADC-configured port of highest index. • 10: Single conversion – The ADC performs one conversion for the current port. It starts with the lowest index port that is ADC-configured, and it progresses to higher index ports as $\overline{CNVT}$ is asserted. • 11: Continuous sweep – This mode is not controlled by $\overline{CNVT}$. The ADC continuously sweeps the ADC-configured ports.
3:2	DACCTL[1:0]	**DAC mode selection** • 00: Sequential update mode for DAC-configured ports. • 01: Immediate update mode for DAC-configured ports. The DAC-configured port that received new data is the next port to be updated. After updating that port, the DAC-configured port update sequence continues from that port onward. A minimum of 80µs must be observed before requesting another immediate update. • 10: All DAC-configured ports use the same data stored in DACPRSTDAT1[11:0]. • 11: All DAC-configured ports use the same data stored in DACPRSTDAT2[11:0].
5:4	ADCCONV[1:0]	**ADC conversion rate selection** • 00: ADC conversion rate of 200ksps (default) • 01: ADC conversion rate of 250ksps • 10: ADC conversion rate of 333ksps • 11: ADC conversion rate of 400ksps

Device Control Register (Read/Write) (continued)

BIT	FIELD NAME	DESCRIPTION
6	DACREF	**DAC voltage reference selection** • 0: External reference voltage • 1: Internal reference voltage
7	THSHDN	**Thermal shutdown enable** • 0: Thermal shutdown function disabled. • 1: Thermal shutdown function enabled. If the internal temperature monitor is enabled, and if the internal temperature is measured to be larger than 145°C, the device is reset, thus bringing all channels to high-impedance mode and setting all registers to their default value.
10:8	TMPCTL[2:0]	**Temperature monitor selection** • TMPCTL[0]: Internal temperature monitor (0: disabled; 1: enabled) • TMPCTL[1]: 1st external temperature monitor (0: disabled; 1: enabled) • TMPCTL[2]: 2nd external temperature monitor (0: disabled; 1: enabled)
11	TMPPER	**Temperature conversion time control** • 0: Default conversion time setting. Selected for junction capacitance filter < 100pF. • 1: Extended conversion time setting. Selected for junction capacitance filter from 100pF to 390pF
12	RS_CANCEL	**Temperature sensor series resistor cancellation mode** • 0: Temperature sensor series resistance cancellation disabled. • 1: Temperature sensor series resistance cancellation enabled.
13	LPEN	**Power mode selection** • 0: Default power mode for normal operations • 1: Lower power mode. The analog ports are in high-impedance mode. The device can be brought out of the lower power mode by deasserting this bit. The device would then undergo the regular power-on sequence.
14	BRST	**Serial interface burst-mode selection** • 0: Default address incrementing mode. The address is automatically incremented by “1” in burst mode. • 1: Contextual address incrementing mode. In burst mode, the address automatically points to the next ADC- or DAC-configured port data register. Specifically, when reading ADC data (writing DAC data), the serial interface reads (writes to) only the data registers of those ports that are ADC-configured (DAC-configured). This mode applies to ADC data read and DAC data write, not DAC data read.
15	RESET	**Soft reset control** • Self-clearing soft reset register, equivalent to power-on reset.

GPI Data Registers (Read)

BIT	FIELD NAME	DESCRIPTION

15:0
3:0
	GPIDAT[15:0]
	GPIDAT[19:16]
		Data received on GPI ports 0 to 19
		• The data received on GPI-configured ports can be read by the host.
		• For a given port i (0≤i≤19):
		  • GPIDAT[i] = 0: A logic zero level is received at GPI port i
		  • GPIDAT[i] = 1: A logic one level is received at GPI port i

GPO Data Registers (Read/Write)

BIT	FIELD NAME	DESCRIPTION

15:0
3:0
	GPODAT[15:0]
	GPODAT[19:16]
		Data transmitted through GPO ports 0 to 19
		• Data written by the host to be transmitted through the GPO-configured ports
		• For a given port i (0≤i≤19):
		  • GPIDAT[i] = 0: A logic zero level is transmitted through GPO port i
		  • GPIDAT[i] = 1: A logic one level is transmitted through GPO port i

DAC Preset Data Registers (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0 11:0	DACPRSTDAT1[11:0] DACPRSTDAT2[11:0]	**DAC preset data register 1 and 2** • DAC data used by all ports configured in a DAC-related mode (1, 3, 4, 5, 6, and 10) • Writing to these registers does not alter the contents of the DAC data registers

Temperature Monitor Configuration Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
1:0	TMPINTMONCFG[1:0]	**Number of samples averaged for calculating the internal temperature** • 00: 4 samples • 01: 8 samples • 10: 16 samples • 11: 32 samples
3:2	TMPEXT1MONCFG[1:0]	**Number of samples averaged for calculating the 1st external temperature** • 00: 4 samples • 01: 8 samples • 10: 16 samples • 11: 32 samples
5:4	TMPEXT2MONCFG[1:0]	**Number of samples averaged for calculating the 2nd external temperature** • 00: 4 samples • 01: 8 samples • 10: 16 samples • 11: 32 samples

Internal Temperature Monitor High Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPINTHI[11:0]	**Internal temperature monitor high threshold** • Maximum temperature value beyond which TMPINT[2] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

Internal Temperature Monitor Low Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPINTLO[11:0]	**Internal temperature monitor low threshold** • Minimum temperature value below which TMPINT[1] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

1st External Temperature Monitor High Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT1HI[11:0]	**1st external temperature monitor high threshold** • Maximum temperature value beyond which TMPEXT1[2] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

1st External Temperature Monitor Low Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT1LO[11:0]	**1st external temperature monitor low threshold** • Minimum temperature value below which TMPEXT1[1] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

2nd External Temperature Monitor High Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT2HI[11:0]	**2nd external temperature monitor high threshold** • Maximum temperature value beyond which TMPEXT2[2] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

2nd External Temperature Monitor Low Threshold Register (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	TMPEXT2LO[11:0]	**2nd external temperature monitor low threshold** • Minimum temperature value below which TMPEXT2[1] is asserted. • This value is represented in two's complement; one LSB represents 0.125°C.

Port Configuration Registers (Read/Write)

<table>
<tr><th>BIT</th><th>FIELD NAME</th><th>DESCRIPTION</th></tr>
<tr><td>11:0</td><td>FUNCPRM_0[11:0]
FUNCPRM_1[11:0]
FUNCPRM_2[11:0]
FUNCPRM_3[11:0]
FUNCPRM_4[11:0]
FUNCPRM_5[11:0]
FUNCPRM_6[11:0]
FUNCPRM_7[11:0]
FUNCPRM_8[11:0]
FUNCPRM_9[11:0]
FUNCPRM_10[11:0]
FUNCPRM_11[11:0]
FUNCPRM_12[11:0]
FUNCPRM_13[11:0]
FUNCPRM_14[11:0]
FUNCPRM_15[11:0]
FUNCPRM_16[11:0]
FUNCPRM_17[11:0]
FUNCPRM_18[11:0]
FUNCPRM_19[11:0]</td><td>
FUNCPRM_i[4:0]: ASSOCIATED PORT
• Defines the port to use in conjunction with a port configured in mode 4, 8, or 11.

FUNCPRM_i[7:5]: # OF SAMPLES (for ADC-related functional modes only)
• Defines the number of samples to be captured and averaged before loading the result in the port’s ADC data register. The coding of the number of samples is $2^{\#\ OF\ SAMPLES}$. The number of samples to average can be 1, 2, 4, 8, 16, 32, 64, or 128.

FUNCPRM_i[10:8]: RANGE
• Determines the input voltage range of ports configured in input modes, or the output voltage range of ports configured in output modes.
• In ADC- or DAC-related modes, RANGE cannot be set to 000.

<table>
<tr><th>VOLTAGE RANGE CODES</th><th>ADC VOLTAGE RANGE (V)</th><th>DAC VOLTAGE RANGE (V)</th></tr>
<tr><td>000</td><td>No Range Selected</td><td>No Range Selected</td></tr>
<tr><td>001</td><td>0 to +10</td><td>0 to +10</td></tr>
<tr><td>010</td><td>-5 to +5</td><td>-5 to +5</td></tr>
<tr><td>011</td><td>-10 to 0</td><td>-10 to 0</td></tr>
<tr><td>100</td><td>0 to +2.5</td><td>-5 to +5</td></tr>
<tr><td>101</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>110</td><td>0 to +2.5</td><td>0 to +10</td></tr>
<tr><td>111</td><td>Reserved</td><td>Reserved</td></tr>
</table>
FUNCPRM_i[11]: AVR (for ADC-related functional modes only)
• ADC voltage reference selection
  • 0: ADC internal voltage reference
  • 1: ADC external voltage reference (all modes except mode 6) or DAC voltage reference determined by DACREF (mode 6 only)

FUNCPRM_i[11]: INV (for GPI-controlled functional modes only)
• Asserted to invert the data received by the GPI-configured port.
  • 0: Data received from GPI-configured port is not inverted
  • 1: Data received from GPI-configured port is inverted
</td></tr>
</table>

Port Configuration Registers (Read/Write)(continued)

BIT	FIELD NAME	DESCRIPTION

15:12	FUNCID_0[3:0]
	FUNCID_1[3:0]
	FUNCID_2[3:0]
	FUNCID_3[3:0]
	FUNCID_4[3:0]
	FUNCID_5[3:0]
	FUNCID_6[3:0]
	FUNCID_7[3:0]
	FUNCID_8[3:0]
	FUNCID_9[3:0]
	FUNCID_10[3:0]
	FUNCID_11[3:0]
	FUNCID_12[3:0]
	FUNCID_13[3:0]
	FUNCID_14[3:0]
	FUNCID_15[3:0]
	FUNCID_16[3:0]
	FUNCID_17[3:0]
	FUNCID_18[3:0]
	FUNCID_19[3:0]
		Functional mode for port i (0≤i≤19)
		• When switching from one mode to another, it is recommended to first switch to the high-impedance mode. The duration for which the device may need to stay in the transitional high-impedance mode depends on the application and hardware configuration.
		• 0000: **Mode 0 - High impedance**
		  • The port is configured in high-impedance mode.
		• 0001: **Mode 1 - Digital input with programmable threshold, GPI** (Figure 8)
		  • The port is configured as a GPI whose threshold is set through the DAC data register. The DAC data register for that port needs to be set to the value corresponding to the intended input threshold voltage. Any input voltage above that programmed threshold is reported as a logic one. The input voltage must be between 0V and 5V.
		  • To avoid false interrupts, the port's GPIERMSK register bit must be asserted. The DAC data register can then be set for the desired threshold voltage. It may take up to 1ms for the threshold voltage to be effective. The port's GPIMD register bit is set next. At that point, GPIERMSK can be deasserted for the port to start detecting events. The data resulting from the comparison between the threshold voltage and the voltage at the port can be read from the corresponding GPIDAT register bit.
		• 0010: **Mode 2 - Bidirectional level translator terminal** (Figure 11)
		  • Any pair of adjacent ports can form a bidirectional level translator path. Only the lower index port of the pair needs to be configured to enable this mode. The other port (index + 1) must be set in high-impedance mode.
		  • Port 19 cannot be set in mode 2.
		  • The activity on this port is observable through its GPI path. The GPI-related registers are configured as described for mode 1.

Port Configuration Registers (Read/Write)(continued)

BIT	FIELD NAME	DESCRIPTION

		• 0011: **Mode 3 - Register-driven digital output with DAC-controlled level, GPO** (Figure 9)
		  • The port is configured as a GPO driven by the corresponding GPODAT register bit. The logic one level is set by the DAC data register of that port.
		  • The port's DAC data register needs to be set first. It may require up to 1ms for the port to be ready to produce the desired logic one level. At that point, the port can be set in mode 3. The logic level at the port is then controlled by the corresponding GPODAT register bit.
		• 0100: **Mode 4 - Unidirectional path output with DAC-controlled level, GPO** (Figure 10)
		  • The port is configured as a GPO forming the output of a unidirectional level translator path. The input port of that path is specified by the functional parameter, ASSOCIATED PORT, and that port must be separately configured in GPI mode. The port's DAC data register defines the logic one level. The data received by the GPI-configured port is transmitted by this port configured in mode 4.
		  • The data from the associated GPI-configured port can be inverted by asserting the functional parameter INV.
		  • Multiple ports configured in mode 4 can refer to the same GPI-configured port through the functional parameter, ASSOCIATED PORT. Therefore, one GPI-configured port can transmit its data to multiple ports configured in mode 4.
		  • To avoid false interrupts and unexpected activity at the port configured in mode 4, the GPI port must be configured before this port is configured in mode 4.
		  • Functional parameters to be set: INV, ASSOCIATED PORT
		• 0101: **Mode 5 - Analog output for DAC** (Figure 6)
		  • The port's DAC data register must be set for the desired voltage at the port. It may take up to 1ms for the port to reflect the data written in the DAC data register.
		  • Functional parameters to be set: RANGE (codes 001, 010, and 011 apply to this mode).
		• 0110: **Mode 6 - Analog output for DAC with ADC monitoring** (Figure 7)
		  • In addition to the functionality of mode 5, the port is sampled by the ADC. The result of the ADC conversion is stored in the port's ADC data register. The host can access that register to monitor the voltage at the port.
		  • When the ADC input voltage range is set from 0V to 2.5V, (RANGE = 100 or 110), the DAC data register value must be limited to the range of values corresponding to 0V to 2.5V at the port. Internally, the DAC data register value is clipped, so that the PIXI port voltage is contained within a range from 0V to 5V to prevent device damage.
		  • Functional parameters to be set: AVR, RANGE
		• 0111: **Mode 7 - Positive analog input to single-ended ADC** (Figure 3)
		  • The port is configured as a single-ended ADC input.
		  • Functional parameters to be set: AVR, RANGE, # OF SAMPLES
		• 1000: **Mode 8 - Positive analog input to differential ADC** (Figure 4)
		  • The port is configured as a differential ADC positive input.
		  • Functional parameters to be set: AVR, RANGE, # OF SAMPLES, ASSOCIATED PORT

Port Configuration Registers (Read/Write)(continued)

BIT	FIELD NAME	DESCRIPTION

		• 1001: **Mode 9 - Negative analog input to differential ADC**
		  • The port is configured as a differential ADC negative input.
		  • The number of samples to average is defined by the associated positive port. The functional parameters AVR and RANGE must be identical to those used by the corresponding positive port.
		  • A port configured in mode 9 can be associated to more than one port configured in mode 8.
		  • Functional parameters to be set: AVR, RANGE
		
		• 1010: **Mode 10 - Analog output for DAC and negative analog input to differential ADC** (Figure 5)
		  • While this port drives the voltage corresponding to its DAC data register, it also operates as the negative input for the ADC.
		  • The number of samples to average is defined by the associated positive port. The functional parameters AVR and RANGE must be identical to those used by the corresponding positive port.
		  • A port configured in mode 10 can be associated to more than one port configured in mode 8.
		  • When the ADC input voltage range is set from 0V to 2.5V (RANGE = 100 or 110), the DAC data register value must be limited to the range of values corresponding to 0V to 2.5V at the port. Internally, the DAC data register value is clipped, so that the PIXI port voltage is contained within a range from 0V to 5V to prevent device damage.
		  • Functional parameters to be set: AVR, RANGE
		
		• 1011: **Mode 11 - Terminal to GPI-controlled analog switch** (Figure 12)
		  • In this mode, two adjacent ports can be connected together through an analog switch controlled by a GPI-configured port (designated by the functional parameter ASSOCIATED PORT). This function involves three ports. The switch controlling port needs to be separately configured in GPI mode. Only the port with the lower index needs to be configured in mode 11. The port with the higher index can be configured in any other mode, except mode 2. If the port of higher index operates in an ADC-related mode (mode 6, 7, 8, or 9), the signals applied to the port in mode 11 must comply with the input voltage range for which the port of higher index is configured.
		  • Port 19 cannot be configured in mode 11, as there is no switch between ports 0 and 19.
		  • Functional parameters to be set: INV, ASSOCIATED PORT
		
		• 1100: **Mode 12 - Terminal to register-controlled analog switch**
		  • This mode is identical to Mode 11, except that the switch remains closed as long as this port is configured in mode 12.

Table 4. Port Functional Modes

		FUNCID[3:0]				FUNCPRM[11:0]											
MODE	**DESCRIPTION**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	High impedance	0	0	0	0												
1	Digital input with programmable threshold, GPI	0	0	0	1												
2	Bidirectional level translator terminal	0	0	1	0												
3	Register-driven digital output with DAC-controlled level, GPO	0	0	1	1												
4	Unidirectional path output with DAC-controlled level, GPO	0	1	0	0	INV							ASSOCIATED PORT*				
5	Analog output for DAC	0	1	0	1		RANGE										
6	Analog output for DAC with ADC monitoring	0	1	1	0	AVR	RANGE										
7	Positive analog input to single-ended ADC	0	1	1	1	AVR	RANGE			# OF SAMPLES							
8	Positive analog input to differential ADC	1	0	0	0	AVR	RANGE			# OF SAMPLES			ASSOCIATED PORT*				
9	Negative analog input to differential ADC	1	0	0	1	AVR	RANGE										
10	Analog output for DAC and negative analog input to differential ADC (pseudo-differential mode)	1	0	1	0	AVR	RANGE										
11	Terminal to GPI-controlled analog switch	1	0	1	1	INV							ASSOCIATED PORT*				
12	Terminal to register-controlled analog switch	1	1	0	0												

*Port must be configured separately to a compatible mode.

ADC Data Registers (Read)

BIT	FIELD NAME	DESCRIPTION
11:0	ADCDAT_0[11:0] ADCDAT_1[11:0] ADCDAT_2[11:0] ADCDAT_3[11:0] ADCDAT_4[11:0] ADCDAT_5[11:0] ADCDAT_6[11:0] ADCDAT_7[11:0] ADCDAT_8[11:0] ADCDAT_9[11:0] ADCDAT_10[11:0] ADCDAT_11[11:0] ADCDAT_12[11:0] ADCDAT_13[11:0] ADCDAT_14[11:0] ADCDAT_15[11:0] ADCDAT_16[11:0] ADCDAT_17[11:0] ADCDAT_18[11:0] ADCDAT_19[11:0]	**ADC data for port i (0≤i≤19)** • 12-bit data produced by the ADC when converting the analog input signal on port i. • The conversion result is represented in straight binary for ports configured in single-ended mode (modes 6, 7), and in two's complement for ports configured as an ADC positive input (mode 8) in differential or pseudo-differential mode (mode 9). The ADC data register of the port configured as an ADC negative input in differential (mode 9) or pseudo-differential mode (mode 10) contains 0x0000.

DAC Data Registers (Read/Write)

BIT	FIELD NAME	DESCRIPTION
11:0	DACDAT_0[11:0] DACDAT_1[11:0] DACDAT_2[11:0] DACDAT_3[11:0] DACDAT_4[11:0] DACDAT_5[11:0] DACDAT_6[11:0] DACDAT_7[11:0] DACDAT_8[11:0] DACDAT_9[11:0] DACDAT_10[11:0] DACDAT_11[11:0] DACDAT_12[11:0] DACDAT_13[11:0] DACDAT_14[11:0] DACDAT_15[11:0] DACDAT_16[11:0] DACDAT_17[11:0] DACDAT_18[11:0] DACDAT_19[11:0]	**DAC data for port i (0≤i≤19)** • 12-bit DAC data for port i. • The data is represented in straight binary.

Applications Information

Configuration Flow Chart

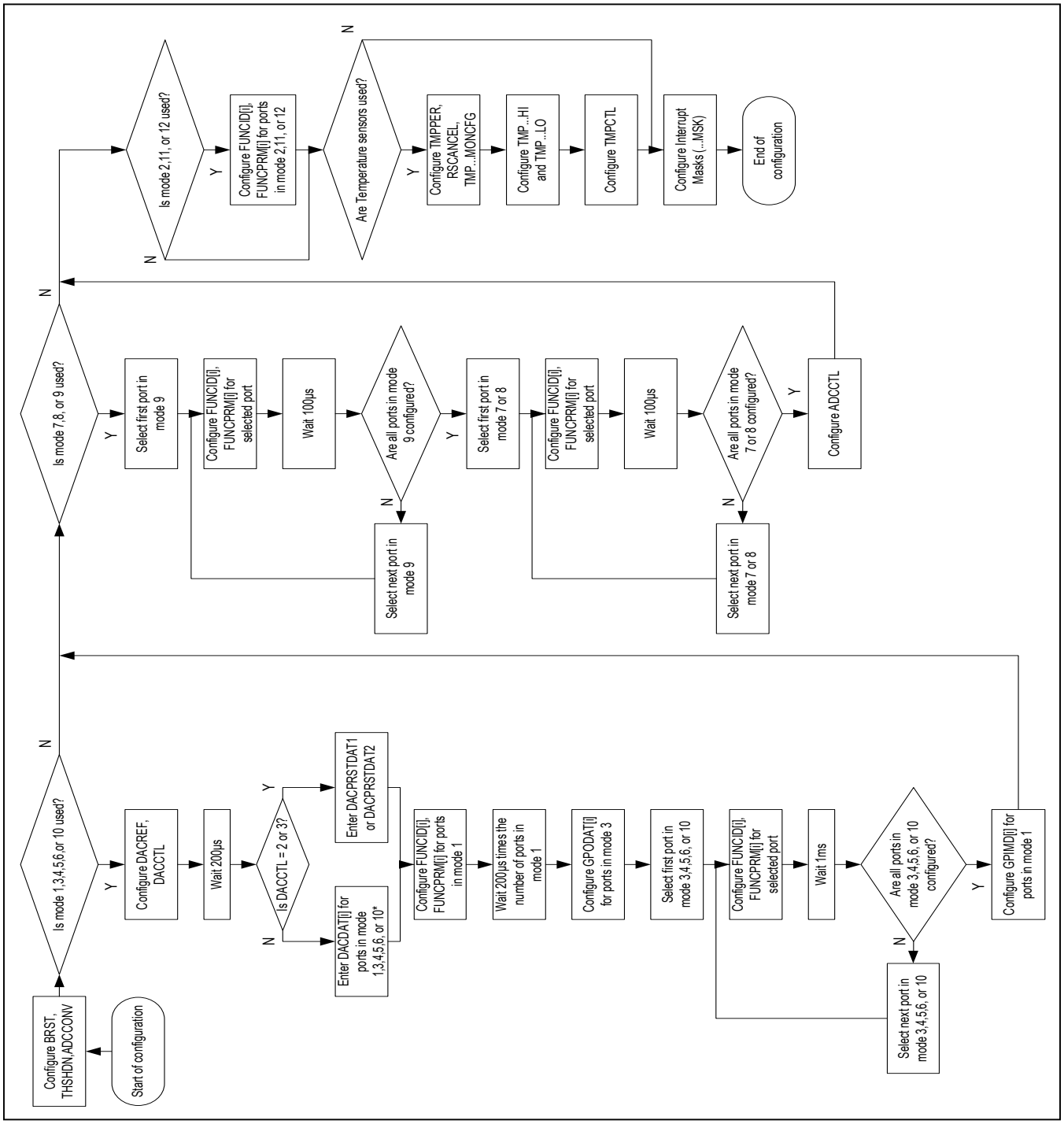


Figure 14. PIXI Port Configuration Flow Chart

Configuration Software (GUI)

To simplify use of the MAX11300, Maxim has created a GUI for users to easily configure the device for unique application needs with a simple drag and drop. The software generates register addresses and corresponding register values. Figure 15 shows an example of this software with a few functional connections.

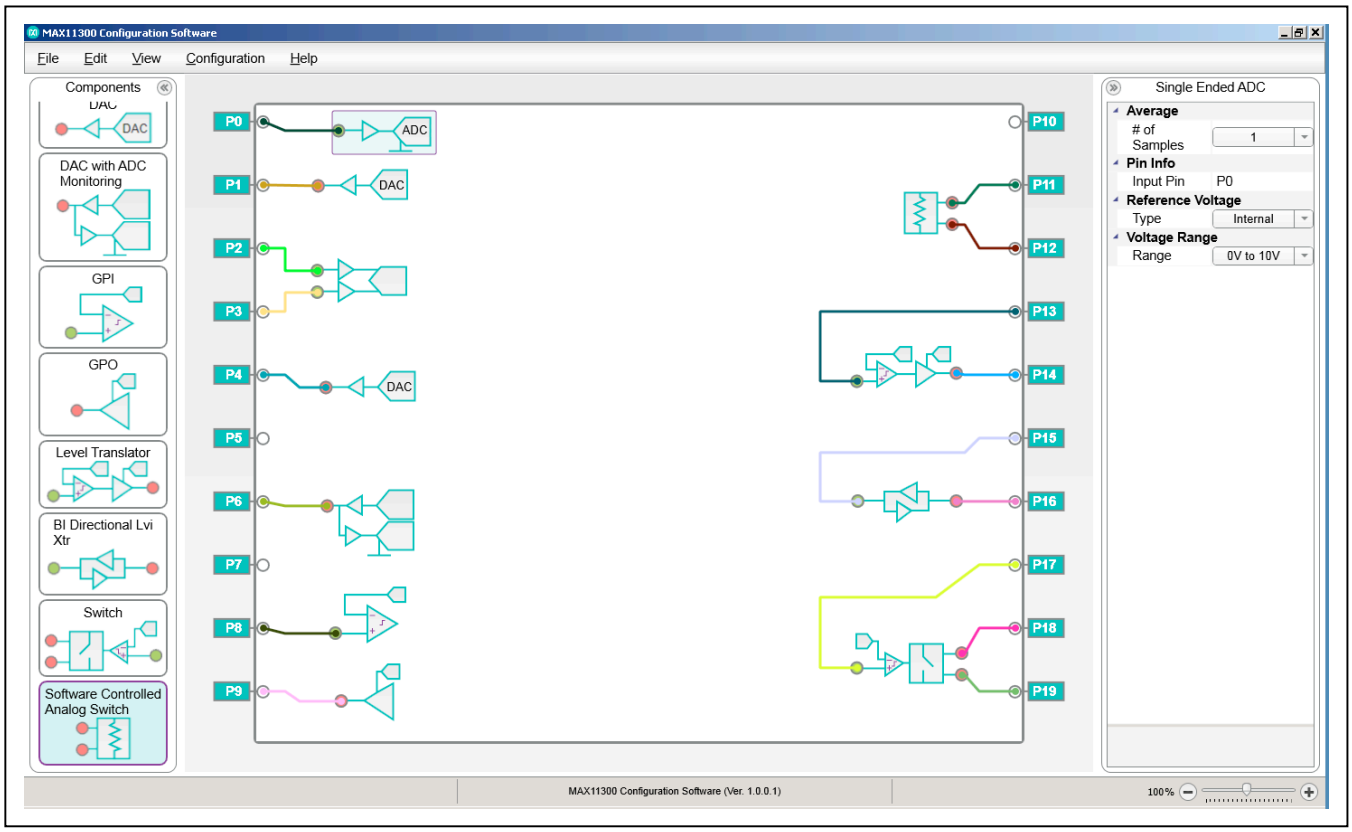


Figure 15. Example of GUI to Develop Configuration File

Configuration Software Output File

Generated on	dd/mm/yyyy hr:min		
SUPPLY	**VOLTAGE**		
VDDIO	12.5		
VSSIO	-2.5		
AVDD	5		
DVDD	3.3		
ADC_EXT_REF	2.5		
DAC_REF	2.5		
NAME	**ADDRESS**	**VALUE**	**DESCRIPTION**
gpo_data_15_to_0	0x0D	0x0000	GPO data for PIXI ports 15 to 0
gpo_data_19_to_16	0x0E	0x0000	GPO data for PIXI ports 19 to 16
device_control	0x10	0x00c0	Device main control register
interrupt_mask	0x11	0xffff	Interrupt mask register
gpi_irqmode_7_to_0	0x12	0x0000	GPI port 0 to 7 mode register
gpi_irqmode_15_to_8	0x13	0x0000	GPI port 8 to 15 mode register
gpi_irqmode_19_to_16	0x14	0x0000	GPI port 16 to 19 mode register
dac_preset_data_1	0x16	0x0000	DAC preset data #1
dac_preset_data_2	0x17	0x0000	DAC preset data #2
tmp_mon_cfg	0x18	0x0000	Temperature monitor configuration
tmp_mon_int_hi_thresh	0x19	0x07ff	Internal temperature monitor high threshold
tmp_mon_int_lo_thresh	0x1A	0x0800	Internal temperature monitor low threshold
tmp_mon_ext1_hi_thresh	0x1B	0x07ff	1st external temperature monitor high threshold
tmp_mon_ext1_lo_thresh	0x1C	0x0800	1st external temperature monitor low threshold
tmp_mon_ext2_hi_thresh	0x1D	0x07ff	2nd external temperature monitor high threshold
tmp_mon_ext2_lo_thresh	0x1E	0x0800	2nd external temperature monitor low threshold
port_cfg_00	0x20	0x7100	Configuration register for PIXI port 0
port_cfg_01	0x21	0x5100	Configuration register for PIXI port 1
port_cfg_02	0x22	0x8103	Configuration register for PIXI port 2
port_cfg_03	0x23	0x9100	Configuration register for PIXI port 3
port_cfg_04	0x24	0x5100	Configuration register for PIXI port 4
port_cfg_05	0x25	0x0000	Configuration register for PIXI port 5
port_cfg_06	0x26	0x6100	Configuration register for PIXI port 6
port_cfg_07	0x27	0x0000	Configuration register for PIXI port 7
port_cfg_08	0x28	0x1000	Configuration register for PIXI port 8
port_cfg_09	0x29	0x3000	Configuration register for PIXI port 9
port_cfg_10	0x2A	0x0000	Configuration register for PIXI port 10

Configuration Software Output File (continued)

NAME	ADDRESS	VALUE	DESCRIPTION
port_cfg_11	0x2B	0xc000	Configuration register for PIXI port 11
port_cfg_12	0x2C	0x0000	Configuration register for PIXI port 12
port_cfg_13	0x2D	0x1000	Configuration register for PIXI port 13
port_cfg_14	0x2E	0x400d	Configuration register for PIXI port 14
port_cfg_15	0x2F	0x2000	Configuration register for PIXI port 15
port_cfg_16	0x30	0x0000	Configuration register for PIXI port 16
port_cfg_17	0x31	0x1000	Configuration register for PIXI port 17
port_cfg_18	0x32	0xb011	Configuration register for PIXI port 18
port_cfg_19	0x33	0x0000	Configuration register for PIXI port 19
dac_data_port_00	0x60	0x0000	DAC data register for PIXI port 0
dac_data_port_01	0x61	0x0000	DAC data register for PIXI port 1
dac_data_port_02	0x62	0x0000	DAC data register for PIXI port 2
dac_data_port_03	0x63	0x0000	DAC data register for PIXI port 3
dac_data_port_04	0x64	0x0000	DAC data register for PIXI port 4
dac_data_port_05	0x65	0x0000	DAC data register for PIXI port 5
dac_data_port_06	0x66	0x0000	DAC data register for PIXI port 6
dac_data_port_07	0x67	0x0000	DAC data register for PIXI port 7
dac_data_port_08	0x68	0x0666	DAC data register for PIXI port 8
dac_data_port_09	0x69	0x0666	DAC data register for PIXI port 9
dac_data_port_10	0x6A	0x0000	DAC data register for PIXI port 10
dac_data_port_11	0x6B	0x0000	DAC data register for PIXI port 11
dac_data_port_12	0x6C	0x0000	DAC data register for PIXI port 12
dac_data_port_13	0x6D	0x0666	DAC data register for PIXI port 13
dac_data_port_14	0x6E	0x0666	DAC data register for PIXI port 14
dac_data_port_15	0x6F	0x0000	DAC data register for PIXI port 15
dac_data_port_16	0x70	0x0000	DAC data register for PIXI port 16
dac_data_port_17	0x71	0x0666	DAC data register for PIXI port 17
dac_data_port_18	0x72	0x0000	DAC data register for PIXI port 18
dac_data_port_19	0x73	0x0000	DAC data register for PIXI port 19

Layout, Grounding, Bypassing

For best performance, use PCBs with a solid ground plane. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the MAX11300 package. Noise in AVDD, AGND, AVDDIO, AVSSIO, ADC_REF_INT, ADC_EXT_INT, and DAC_REF affects the device performance. Bypass AVDD, DVDD, AVDDIO, and AVSSIO to ground with 0.1µF and 10µF bypass capacitors. Bypass ADC_INT_REF and DAC_REF to ground with capacitors whose values are shown in the *REF Electrical Specifications* table. Bypass ADC_EXT_REF to ground with a 4.7µF capacitor. Place the bypass capacitors as close as possible to the respective pins and minimize capacitor lead and trace lengths for best supply-noise rejection. For optimum heat dissipation, connect the exposed pad (EP) to a large copper area, such as a ground plane.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11300GCM+	-40°C to +105°C	48 TQFP-EP*
MAX11300GCM+T	-40°C to +105°C	48 TQFP-EP*
MAX11300GTL+	-40°C to +105°C	40 TQFN-EP*
MAX11300GTL+T	-40°C to +105°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4066+3	**21-0141**	**90-0054**
48 TQFP-EP	C48E+8	**21-0065**	**90-0138**