*Click **here** for production status of specific part numbers.*

MAX14576/MAX14636/ MAX14637

USB Charger Detectors

General Description

The MAX14576/MAX14636/MAX14637 are USB charger detectors. The MAX14576/MAX14636/MAX14637 will pass USB Battery Charger Specification Revision 1.2 (USB BC 1.2) compliance tests. The MAX14636/MAX14637 can also detect Apple chargers, and other nonstandard types. These devices are capable of detecting multiple USB battery charging methods, including standard downstream ports (SDP), charging downstream ports (CDP), and dedicated charger ports (DCP). The devices also feature USB BC 1.2 defined dead-battery option support.

The MAX14576/MAX14636/MAX14637 feature analog switches that are capable of passing USB Hi-Speed, full-speed, and low-speed signals. The switches have low on-resistance (3I, typ) and low on-capacitance (4.5pF, typ). The CDN and CDP are high ESD protected up to Q15kV Human Body Model (HBM), Q15kV IEC61000-4-2 Air Gap Discharge, and Q 8kV IEC61000-4-2 Contact Discharge.

The MAX14576/MAX14636/MAX14637 are available in a 10-pin (1.6mm x 2.1mm) UTQFN package and operate over the 0°C to +70°C extended temperature range.

Applications

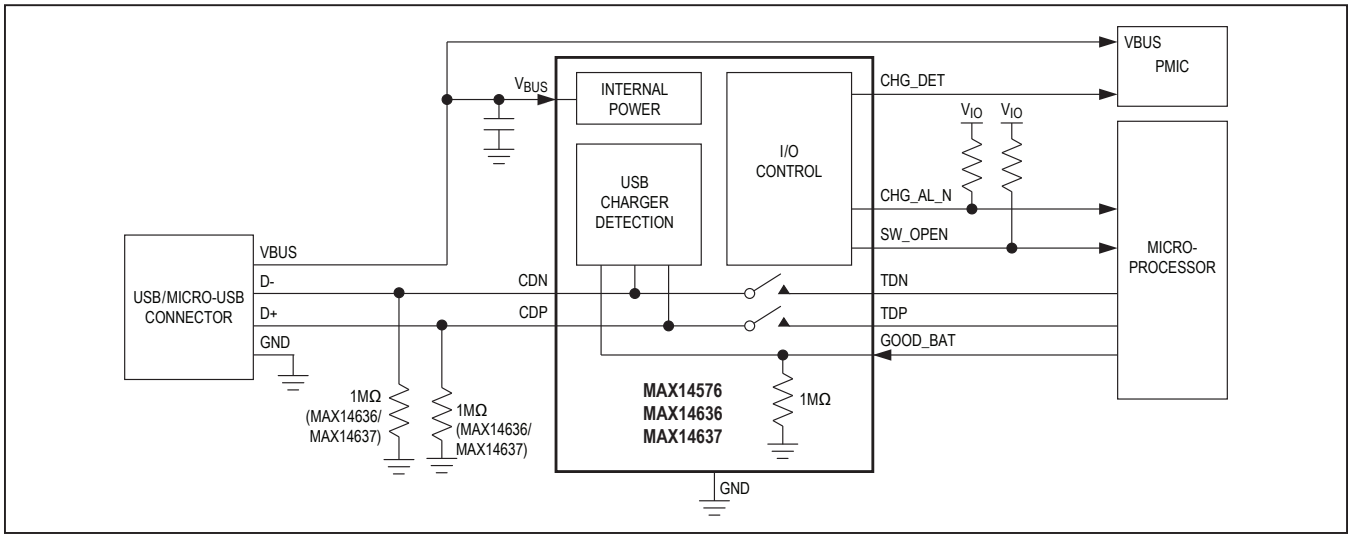
- Cell Phones
- Digital Cameras
- eReaders
- Tablets
- Portable Industrial Products

Benefits and Features

- High Level of Integration
  - Capability to Withstand -6V to +30V (Absolute Maximum) on VBUS Line
  - USB Battery Charger Detection
    - Will Pass USB Battery Charger Specification Rev 1.2 Compliance Tests
    - USB DCP, SDP, and CDP Detection
    - Proprietary Charger Detection Capability (MAX14636/MAX14637)
  - USB 2.0 Hi-Speed Switch with 3Ω (typ) On-Resistance and 4.5pF (typ) On-Capacitance
  - High ESD Protection on CDP and CDN
    - ±15kV—HBM
    - ±15kV—IEC 61000-4-2 Air-Gap Discharge
    - ±8kV—IEC 61000-4-2 Contact Discharge
  - ±15kV HBM ESD Protection VBUS When Bypassed with 0.1µF or Greater Ceramic Capacitor
- Save Power in Portable Applications
  - Low Supply Current (150µA, typ)
- Space Saving
  - 10-Pin, 1.6mm x 2.1mm, UTQFN Package

***Ordering Information/Selector guide* appears at end of data sheet.**

Functional Diagram/Typical Application Circuit



Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{VBUS} .....-6V to +30V
CHG_AL_N.....-0.3V to +30V
SW_OPEN, GOOD_BAT.....-0.3V to +6V
CHG_DET (Note 1) ..... -0.3V to (V_{CCINT} + 0.3V)
TDP, TDN ..... -0.3V to (V_{CCINT} + 0.3V)
CDP, CDN..... -0.3V to +6V
Continuous Current into All Terminals .....±50mA

Continuous Power Dissipation (T_A = +70°C)
UTQFN (derate 9mW/°C above +70°C).....722mW
Operating Temperature Range.....0°C to +70°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: V_{CCINT} = min (V_{VBUS}, +4.2V).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10 ULTRA QFN	
Package Code	V101A2CN+1
Outline Number	**21-0610**
Land Pattern Number	**90-0386**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	110.8°C/W
Junction to Case (θ_{JC})	62.1°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{VBUS} = 3.5V to 5.5V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{VBUS} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{VBUS}		0		28	V
VBUS POR	$V_{VBUSUVLO}$		1.4	2.2	3.15	V
VBUS Supply Current	I_{VBUS}	V_{VBUS} = 5.5V, GOOD_BAT = 1, charger detection not running		150	300	µA
VBUS Supply Current	I_{VBUS12}	V_{VBUS} = 12V, GOOD_BAT = 1, charger detection not running		10	16	mA
CHARGER DETECTION						
V_{DP_SRC} Voltage	V_{DP_SRC}	I_{DP_SRC} = 0 to 250µA	0.5		0.7	V
V_{DAT_REF} Voltage	V_{DAT_REF}		0.25		0.4	V
V_{LGC} Voltage	V_{LGC}		0.8		2.0	V
I_{DP_SRC} Current	I_{DP_SRC}		7		10	µA
CDN Pulldown Resistor	R_{DM_DWN}		14.25		24.8	kΩ
CDP Pulldown Resistor	R_{DP_DWN}		14.25		24.8	kΩ
CDP and CDN Sink Current	I_{DP_SINK} I_{DM_SINK}		50		150	µA
CDP and CDN Weak Sink	I_{WEAK}	V_{CDN} = 3.6V			0.3	µA
VBUS Detection Ratio	VBUS_LOW	V_{VBUS} = 5V	22.5	25	27.5	%
	VBUS_MID		42.3	47	51.7	
	VBUS_HIGH		76	80	89	
CDP and CDN Overvoltage Comparator		V_{VBUS} = 5V, no load on CHG_DET		4.2		V
Primary Detection Voltage Source Time	$t_{VDP\_SRC\_ON}$			46		ms
VBUS Attach to CHG_DET	t_{VBUS_CHG}	From V_{VBUS} > V_{VBDET} to CHG_DET change, assuming DCD delay = 0ms; Figure 1, Figure 2, Figure 3			250	ms
GOOD_BAT to SW_OPEN	tG_{OOD_SW}	Figure 2, Figure 3		15	20	ms
DCD Time Out	t_{DCD_TMO}		0.7	0.8	0.89	s
VBUS Detect Threshold Rising	V_{VBDET}		3.3	3.5	4	V
VBUS Detect Threshold Hysteresis	V_{VBDET_HYST}			50		mV
USB ANALOG SWITCHES						
Analog Signal Range		(Note 3, Note 4)	0		V_{CCINT}	V
On-Resistance	R_{ONUSB}	I_{CDP}, I_{CDN} = 10mA, V_{CDP}, V_{CDN} = 0 to 3V		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	I_{CDP}, I_{CDN} = 10mA, V_{CDP}, V_{CDN} = 0.4V (Note 4)			0.5	Ω

Electrical Characteristics (continued)

(V_{VBUS} = 3.5V to 5.5V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{VBUS} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance Flatness	$R_{FLATUSB}$	I_{CDP}, I_{CDN} = 10mA, V_{CDP}, V_{CDN} = 0 to 3.3V (Note 4)		0.06	0.2	Ω
Off-Leakage Current	$I_{LUSB(OFF)}$	Switch open, V_{TDN} or V_{TDP} = 0.3V, 2.5V; V_{CDN} or V_{CDP} = 2.5V, 0.3V	-360		360	nA
On-Leakage Current	$I_{LUSB(ON)}$	Switch closed, V_{CDN} or V_{CDP} = 0.3V, 2.5V	-360		360	nA
DIGITAL SIGNALS (GOOD_BAT, CHG_DET, SW_OPEN, CHG_AL_N)						
GOOD_BAT Input Logic High	V_{IH}		1.1			V
GOOD_BAT Input Logic Low	V_{IL}				0.5	V
GOOD_BAT Pulldown	R_{PD}			1		MΩ
CHG_DET Output Logic High	V_{OH}	I_{SOURCE} = -3mA	2		4.36	V
CHG_DET Output Logic Low	V_{OL}	I_{SINK} = 3mA			0.4	V
SW_OPEN, CHG_AL_N Output Leakage	$I_{OUTLEAK}$	V_{IO} = 5V, output is in high-impedance	-1		+1	µA
SW_OPEN, CHG_AL_N Output Logic Low	V_{OL_OD}	I_{SINK} = 5mA			0.4	V
DYNAMIC PERFORMANCE						
GOOD_BAT Debounce Time	t_{GBDEB}			4		ms
VBUS Debounce Time	t_{CDEB}			5		ms
Off-Capacitance	COFF	TDN, TDP applied voltage = $0.5V_{P-P}$, DC bias = 0V, f = 240MHz		2		pF
On-Capacitance	CONCOM	CDN, CDP connected to TDN, TDP; applied voltage = $0.5V_{P-P}$, DC bias = 0V, f = 240MHz		4.5		pF
Off-Isolation		R_L = 50Ω, f = 20kHz, V_{CDN}, V_{CDP} = $0.5V_{P-P}$		-60		dB
ESD PROTECTION						
CDN, CDP		Human Body Model		±15		kV
		IEC61000-4-2 Air-Gap Discharge		±15		
		IEC61000-4-2 Contact		±8		
All Other Pins		Human Body Model		±2		kV

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design.
Note 3: V_{CCINT} = min (V_{VBUS}, +4.2V).
Note 4: Not production tested. Guaranteed by design.

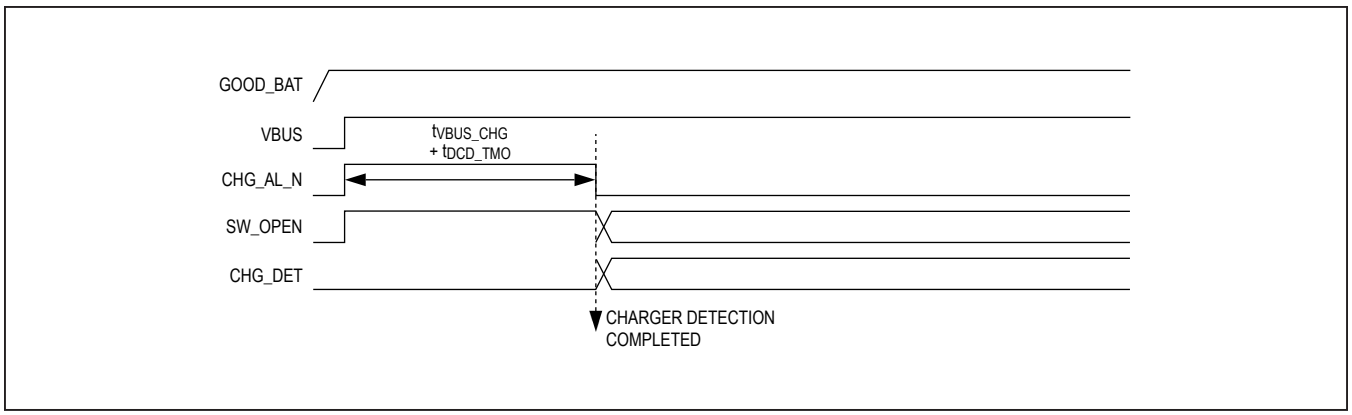


Figure 1. Normal Charger Detection (No Dead Battery)

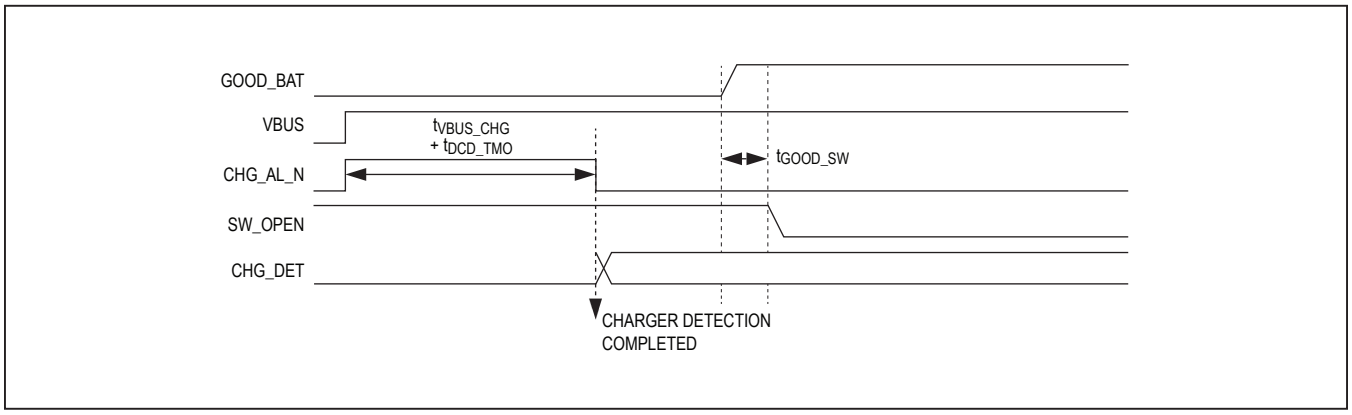


Figure 2. Charger Detection with Dead Battery

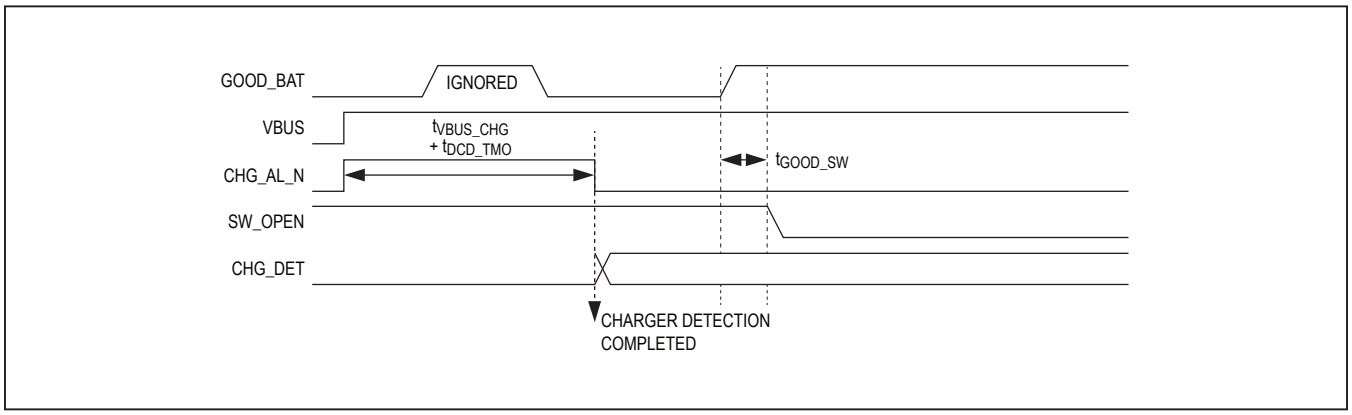
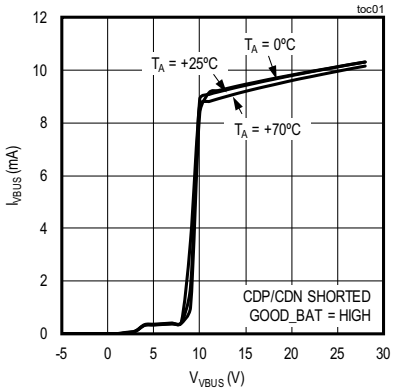


Figure 3. Charger Detection and Phone Flashing

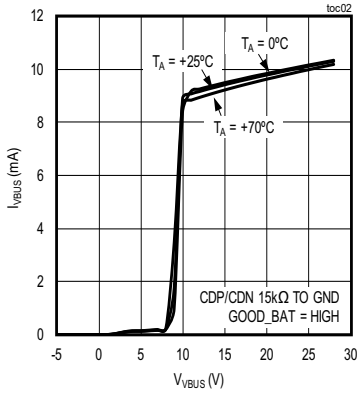
Typical Operating Characteristics

(V_{VBUS} = 5.0V, T_A = +25°C, unless otherwise noted)

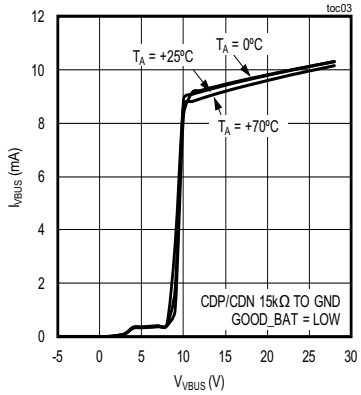
V_{BUS} SUPPLY CURRENT vs. SUPPLY VOLTAGE



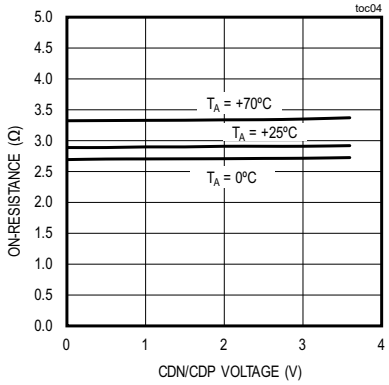
V_{BUS} SUPPLY CURRENT vs. SUPPLY VOLTAGE



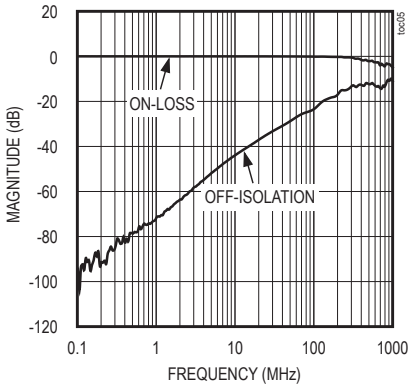
V_{BUS} SUPPLY CURRENT vs. SUPPLY VOLTAGE



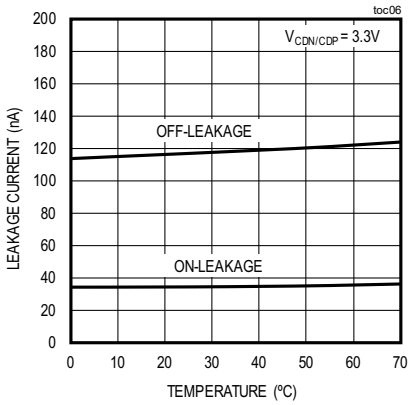
ANALOG SWITCH ON-RESISTANCE vs. CDN/CDP VOLTAGE



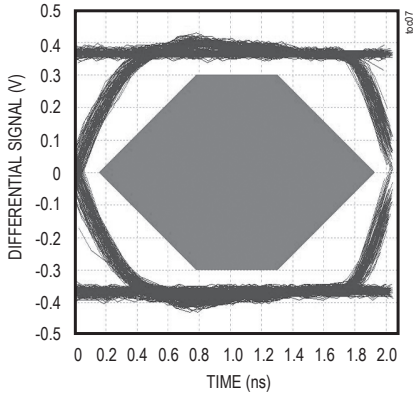
ANALOG SWITCH FREQUENCY RESPONSE



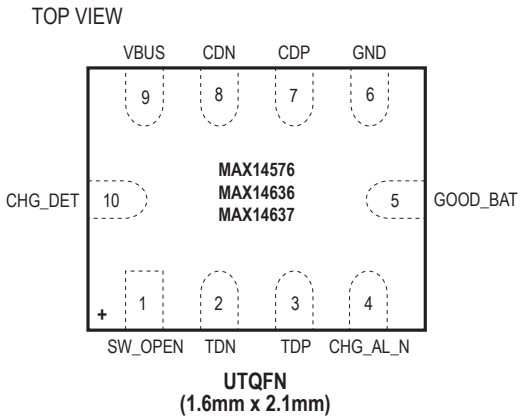
CDN.CDP LEAKAGE CURRENT vs. TEMPERATURE



USB EYE TRANSMIT DIAGRAM (MEASURE AT TEST POINT TP3 AS DEFINED IN USB 2.0 SPECIFICATION)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SW_OPEN	Data Switches Open Indicator. SW_OPEN is low when switches are closed. SW_OPEN is high impedance when switches are open. SW_OPEN is an open-drain output. Connect SW_OPEN to a pullup resistor externally.
2	TDN	USB Transceiver D- Connection
3	TDP	USB Transceiver D+ Connection
4	CHG_AL_N	Charging Allow Indicator. CHG_AL_N is low when VBUS is valid and charging is allowed. CHG_AL_N is an open-drain output. Connect CHG_AL_N to a pullup resistor externally.
5	GOOD_BAT	Good Battery Digital Input. Set GOOD_BAT low for a dead battery and enable USB BC 1.2 compliant dead battery charging. Set GOOD_BAT high for a good battery.
6	GND	Ground
7	CDP	USB Connector D+ Connection
8	CDN	USB Connector D- Connection
9	V_{BUS}	USB VBUS Input. Bypass VBUS to ground with a 0.1µF ceramic capacitor as close to the device as possible to achieve high ±15kV HBM ESD protection.
10	CHG_DET	Charger Detection Push-Pull Output. CHG_DET indicates the capability of the connected charger type (see Tables 1, 2, 3).

Detailed Description

The MAX14576/MAX14636/MAX14637 detect battery charging sources as defined in USB Battery Charging Specification Rev 1.2 (USB BC 1.2). These devices are capable of detecting multiple USB battery charging methods including SDP, CDP, and DCP. The MAX14636/MAX14637 are also capable of detecting Apple chargers, and other nonstandard types (e.g., TomTom charger, and PC PS2 adapter). The devices also feature USB BC1.2 defined dead battery option support.

USB Charger Detection

The charger detection starts when VBUS rises above the threshold. After the type of charger is determined, the MAX14576/MAX14636/MAX14637 set SW_OPEN, CHG_AL_N, and CHG_DET according to the charger type found (Table 1, Table 2, Table 3).

In case of SDP and CDP detection, dead battery mode (DB mode) is entered if GOOD_BAT is low at the end of charger detection. After entering in DB mode, a 45 minute timer starts, V_{DP_SRC} is set on CDP and the device is allowed to charge at a 100mA rate. During DB mode, if GOOD_BAT goes high, then DB mode ends, V_{DP_SRC} is removed and USB switches are closed. If GOOD_BAT goes low again before the 45 minute timer expires, DB mode is entered again. If GOOD_BAT is low when the 45 minute timer expires, DB mode ends and the device is not allowed to charge until VBUS is removed and reconnected. For GOOD_BAT sensitivity in DB mode, the MAX14576/MAX14636 treat CDP as SDP and the MAX14637 treats CDP as DCP.

USB Switches

The switches between CDP/CDN and TDP/TDN are low capacitance and low resistance, and capable of passing Hi-Speed USB signals. The switches are normally open when no valid VBUS is present. When valid VBUS is applied, the switches act according to the charger found (Table 1, Table 2, Table 3).

Table 1. Charger Detection and Events (MAX14576)

ATTACHED CHARGING SOURCE	INPUT	OUTPUTS			USB SWITCHES	SYSTEM
	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET		
DCP	X	Hi-Z	Low	High	Open	Charge with full current
CDP	High	Low	Low	High	Closed	Charge with full current
	Low	Hi-Z	Low	High	Open	Charge with full current
SDP/Apple® Charger/ TomTom® Charger*	High	Low	Low	Low	Closed	Charge with 100mA
	Low	Hi-Z	Low	Low	Open	Charge with 100mA
PS2	X	Hi-Z	Low	Low	Open	Charge with 100mA
No Valid VBUS	X	Hi-Z	Hi-Z	Low	Open	X

X = Don't care.
**Detected as SDP after DCD timeout*

Apple is a registered trademark of Apple, Inc.

TomTom is a registered trademark of TomTom International.

Table 2. Charger Detection and Events (MAX14636)

ATTACHED CHARGING SOURCE	INPUT	OUTPUTS			USB SWITCHES	SYSTEM
	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET		
DCP/Apple Charger/ TomTom Charger**	X	Hi-Z	Low	High	Open	Charge with full current
CDP	High	Low	Low	High	Closed	Charge with full current
	Low	Hi-Z	Low	High	Open	Charge with full current
SDP	High	Low	Low	Low	Closed	Charge with 100mA
	Low	Hi-Z	Low	Low	Open	Charge with 100mA
PS2	X	Hi-Z	Low	Low	Open	Charge with 100mA
No Valid VBUS	X	Hi-Z	Hi-Z	Low	Open	X

X = Don't care.
***TomTom charger detected as DCP after DCD timeout.*

Table 3. Charger Detection and Events (MAX14637)

ATTACHED CHARGING SOURCE	INPUT	OUTPUTS			USB SWITCHES	SYSTEM
	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET		
DCP/Apple Charger	X	Hi-Z	Low	High	Open	Charge with full current
CDP	X	Low	Low	High	Closed	Charge with full current
SDP	High	Low	Low	Low	Closed	Charge with 100mA
	Low	Hi-Z	Low	Low	Open	Charge with 100mA
PS2	X	Hi-Z	Low	Low	Open	Charge with 100mA
No Valid VBUS	X	Hi-Z	Hi-Z	Low	Open	X

X = Don't care.

Applications Information

Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended/90Ω differential controlled-impedance matched traces of equal lengths.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. CDN and CDP are further protected against ESD up to ±15kV (HBM), ±15kV (Air-Gap Discharge method described in IEC 61000-4-2) and ±8kV (Contact Discharge Method described in IEC 61000-4-2) without damage. The VBUS input withstands up to ±15kV (HBM) if bypassed with a 0.1µF ceramic capacitor close to the pin.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14576/MAX14636/MAX14637 continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 6 shows the IEC 61000-4-2 model, and Figure 7 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

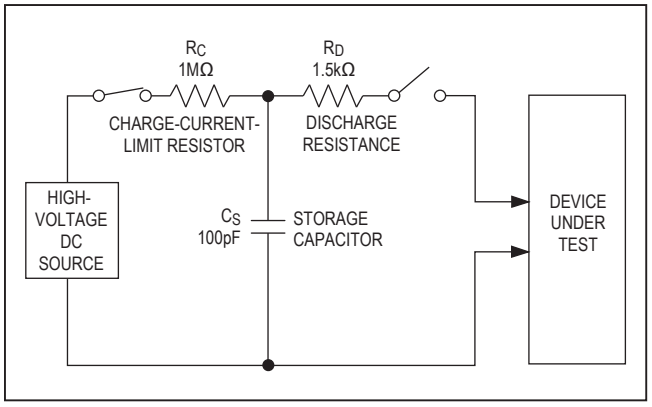


Figure 4. Human Body ESD Test Model

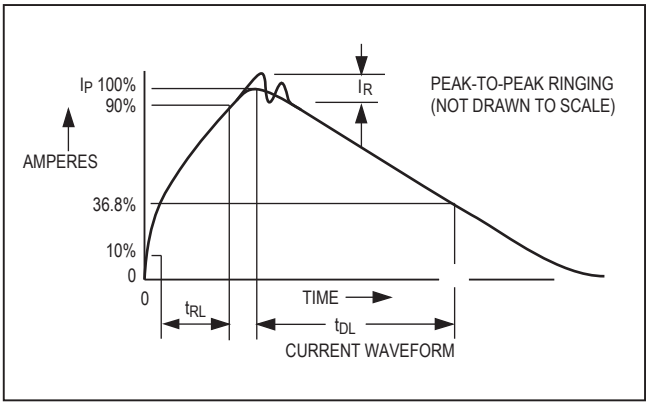


Figure 5. Human Body Current Waveform

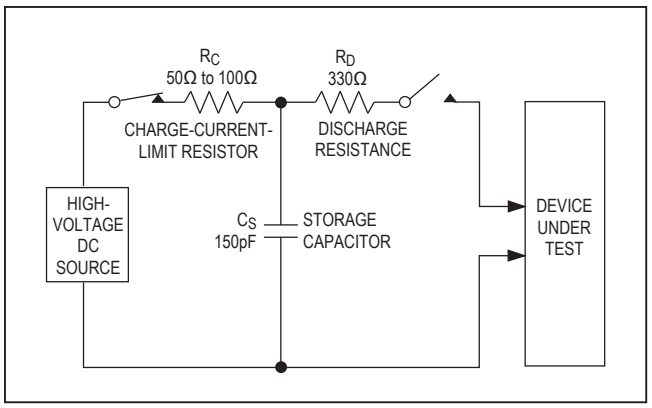


Figure 6. IEC 61000-4-2 ESD Test Model

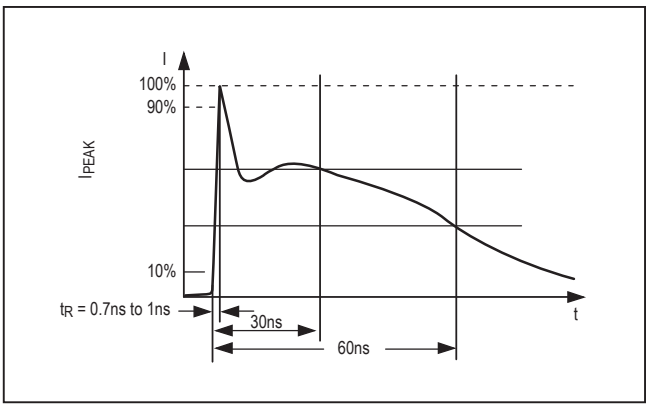


Figure 7. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information/Selector Guide

PART	TEMP RANGE	APPLE CHARGE CURRENT	TomTom CHARGE CURRENT	TOP MARK	PIN-PACKAGE
MAX14576CVB+T	0°C to +70°C	100mA	100mA	ABD	10 UTQFN
MAX14636CVB+T	0°C to +70°C	Full Current	Full Current	ABE	10 UTQFN
MAX14637CVB+T	0°C to +70°C	Full Current	Not Supported	ABG	10 UTQFN

+ Denotes a lead(Pb)-free package/RoHS-compliant package.
T = Tape and reel

Chip Information

PROCESS: BiCMOS