Click here to ask about the production status of specific part numbers.

MAX14689

Ultra-Small, Low-R_{ON}, Beyond-the-Rails™ DPDT Analog Switches

General Description

The MAX14689 ultra-small, low-on-resistance (R_{ON}) double-pole/double-throw (DPDT) analog switches feature Beyond-the-Rails™ capability that allows signals from -5.5V to +5.5V to pass without distortion, even when the power supply is below the signal range. The low on-resistance (0.25Ω) also makes the device ideal for low-distortion switching applications, such as audio or video.

The MAX14689 is fully specified to operate from a single +1.6V to +5.5V power supply. Because of the low supply current requirement, V_{CC} can be provided by a GPIO. When power is not applied, the switches go to a high-impedance mode and all analog signal ports can withstand signals from -5.5V to +5.5V. The switch is controlled with a single control bit, CB.

The MAX14689 is available in a 1.2mm x 1.2mm, 0.4mm pitch, 9-bump wafer-level package (WLP) and 10-pin, 2.5mm x 2.0mm TDFN package. It operates over the -40°C to +85°C extended temperature range.

Applications

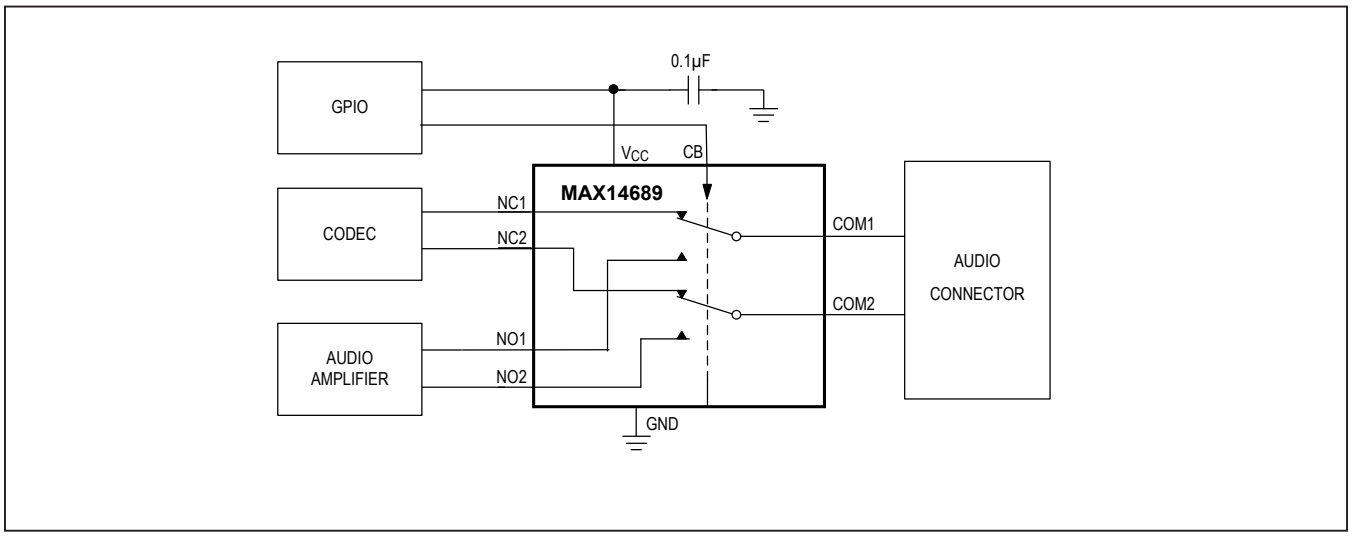
- Smartphones
- Tablets
- Portable Audio/Video Equipment
- Low-Distortion Signal Switches

Benefits and Features

- Distortion-Free Beyond-the-Rails Signaling
  - Negative Voltage Audio and Video Signal Capable
  - -5.5V to +5.5V Analog Signal Range Independent from V_{CC}
  - On-Resistance 0.25Ω (typ)
  - +1.6V to +5.5V Single-Supply Range
  - Total Harmonic Distortion Plus Noise 0.001% (typ)
  - On-Resistance Flatness 0.001Ω (typ)
- Low Supply Current 40µA (typ) at 1.6V
  - Can be Powered by GPIO
  - High-Impedance Mode when V_{CC} Not Applied
- ESD Protection on COM_
  - ±15kV Human Body Model
  - ±10kV IEC 61000-4-2 Air Gap
  - ±8kV IEC 61000-4-2 Contact
- ESD Protection on NC_ and NO_
  - ±15kV Human Body Model
- Design Flexibility
  - Break-Before-Make Operation
  - 9-Bump WLP (1.2mm x 1.2mm) Package
  - 10-Pin TDFN (2.5mm x 2.0mm) Package
  - -40°C to +85°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit/Functional Diagram



Beyond-the-Rails™ is a trademark of Maxim Integrated Products, Inc.

19-6784; Rev 5; 6/20

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{CC}, CB.....-0.3V to +6V
NC_, NO_, COM_.....-6V to +6V
Continuous Current NC_, NO_, COM_.....±500mA
Peak Current NC_, NO_, COM_ (50% duty cycle).....±850mA

Continuous Power Dissipation (T_A = +70°C)
9-Bump WLP (derate 12mW/°C above +70°C).....963.8mW
10-Pin TDFN (derate 9.8mW/°C above +70°C) 784mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 9 WLP	
Package Code	W91J1+1
Outline Number	**21-0459**
Land Pattern Number	**Refer to Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	83°C/W

PACKAGE TYPE: 10 TDFN	
Package Code	T102A2+2C
Outline Number	**21-100013**
Land Pattern Number	**90-100007**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	102°C/W
Junction to Case (θ_{JC})	2.9°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
Power-Supply Range	V_{CC}			1.6		5.5	V
Power-Supply Rejection Ratio	PSRR	$R_{COM\_}$ = 32Ω, f = 20kHz			80		dB
Supply Current	I_{CC}	V_{CC} = +1.6V, V_{CB} = 0V or V_{CC}			40	65	µA
		V_{CC} = +4.2V, V_{CB} = 0V or V_{CC}			70	125	
ANALOG SWITCH							
Analog Signal Range	$V_{NC\_}$, $V_{NO\_}$, $V_{COM\_}$			-5.5		+5.5	V
On-Resistance	R_{ON}	$V_{COM\_}$ = 0V, $I_{COM\_}$ = 100mA (Note 3)	V_{CC} = 2.5V		0.25	0.45	Ω
			V_{CC} = 1.8V		0.325	0.55	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.5V, $V_{NC\_}$ = 0V, $I_{COM\_}$ = 100mA, between same NC_ and NO_ channel (Note 4)			0.005	0.05	Ω
On-Resistance Flatness	R_{FLAT}	V_{CC} = 2.5V, $I_{COM\_}$ = 100mA, $V_{COM\_}$ = -5.5V to 5.5V (Notes 5,6)			0.001	0.01	Ω
NC_ or NO_ Off-Leakage Current	$I_{NC\_(OFF)}$, $I_{NO\_(OFF)}$,	V_{CC} = 2.5V, switch open, $V_{NO\_}$ or $V_{NC\_}$ = -5.5 or +5.5V $V_{COM\_}$ = +5.5V, -5.5V, unconnected		-100		+100	nA
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V_{CC} = 0V $V_{COM\_}$ = -5.5V, 0V, +5.5 $V_{NO\_}$ or $V_{NC\_}$ = -5.5V, +5.5V, unconnected		-100		+100	nA
COM_ On Leakage-Current	$I_{COM\_(ON)}$	V_{CC} = 2.5V, switch closed, $V_{COM\_}$ = +5.5V, -5.5V $V_{NO\_}$ or $V_{NC\_}$ = +5.5V, -5.5V, unconnected		-100		+100	nA
DYNAMIC TIMING							
Turn-Off Time	t_{OFF}	V_{NO} or $V_{NC\_}$ = 0V, R_L = 50Ω, Figure 1 (Note 6)			5	30	µs
Break-Before-Make Time	t_{BBM}	R_L = 50Ω. Time that both NC_/NO_ switches are open during transition, Figure 2 (Note 6)	V_{CC} = 2.5V	0	80	150	µs
			V_{CC} = 1.8V	0		250	
Turn-On Time	t_{ON}	V_{NO} or $V_{NC\_}$ = 0V, Figure 1 (Note 6)	V_{CC} = 2.5V		85	200	µs
			V_{CC} = 1.8V			250	

Electrical Characteristics (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	f = 20Hz to 20kHz, $V_{COM\_}$ = 0.5V_{P-P}, R_S = R_L = 50Ω; DC bias = 0V		0.001		%
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω; $V_{COM\_}$ = 0.5V_{P-P}, f = 100kHz, V_{CC} = 0V, DC bias = 0.25V, Figure 3		-60		dB
Crosstalk	V_{CT}	R_S = R_L = 50Ω; $V_{COM\_}$ = 0.5V_{P-P}, f = 100kHz (Note 7), Figure 3		-100		dB
-3dB Bandwidth	BW	R_S = R_L = 50Ω		110		MHz
NC_ or NO_ Off-Capacitance	$C_{NC\_(OFF)}$ $C_{NO\_(OFF)}$	V_{NC} / $V_{NO\_}$ = 0.5V_{P-P}, f = 1MHz		25		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	V_{NC}/$V_{NO\_}$ = 0.5V_{P-P}, f = 1MHz		50		pF
DIGITAL I/O						
Input Logic High Voltage	V_{IH}		1.4			V
Input Logic Low Voltage	V_{IN}				0.325	V
Input Leakage Current	I_{IN}	V_{CB} = 0V or V_{CC}	-1		+1	µA
THERMAL PROTECTION						
Thermal Shutdown				+150		°C
Thermal Shutdown Hysteresis				25		°C
ESD PROTECTION						
COM_		Human Body Model		±15		kV
		IEC 61000-4-2 Air-Gap		±10		
		IEC 61000-4-2 Contact Discharge		±8		
NC_, NO_		Human Body Model		±15		kV
All Other Pins		Human Body Model		±2		kV

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications over T_A = -40°C to +85°C are guaranteed by design.
Note 2: The same limits apply for $V_{COM\_}$ = -5.5V to +5.5V and are guaranteed by design.
Note 3: $\Delta R_{ON} = |R_{ON(CH1)} - R_{ON(CH2)}|$.
Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.
Note 5: Guaranteed by design; not production tested.
Note 6: Between two switches.

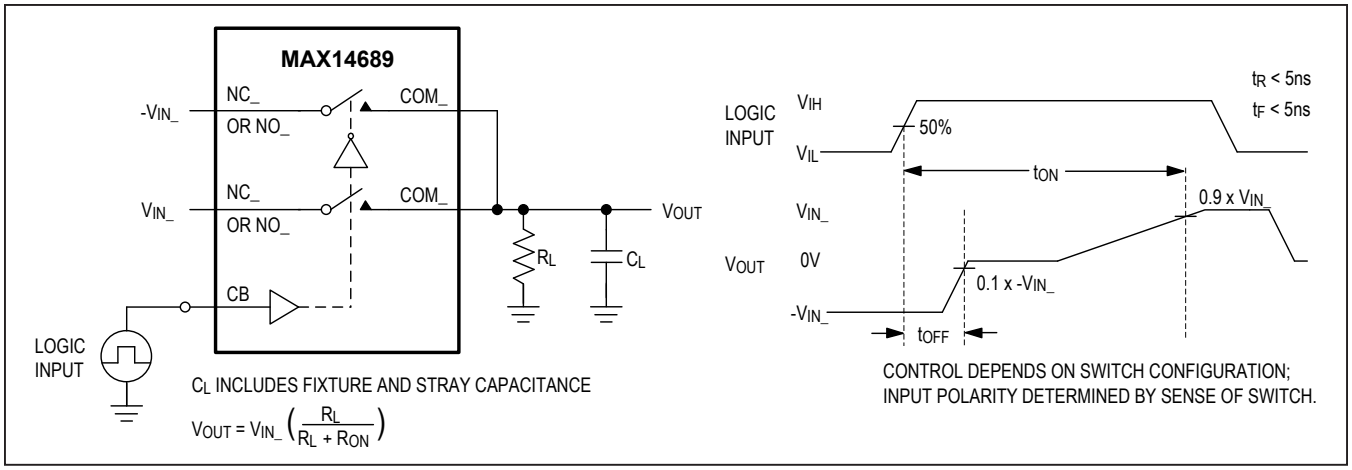


Figure 1. Switching Time

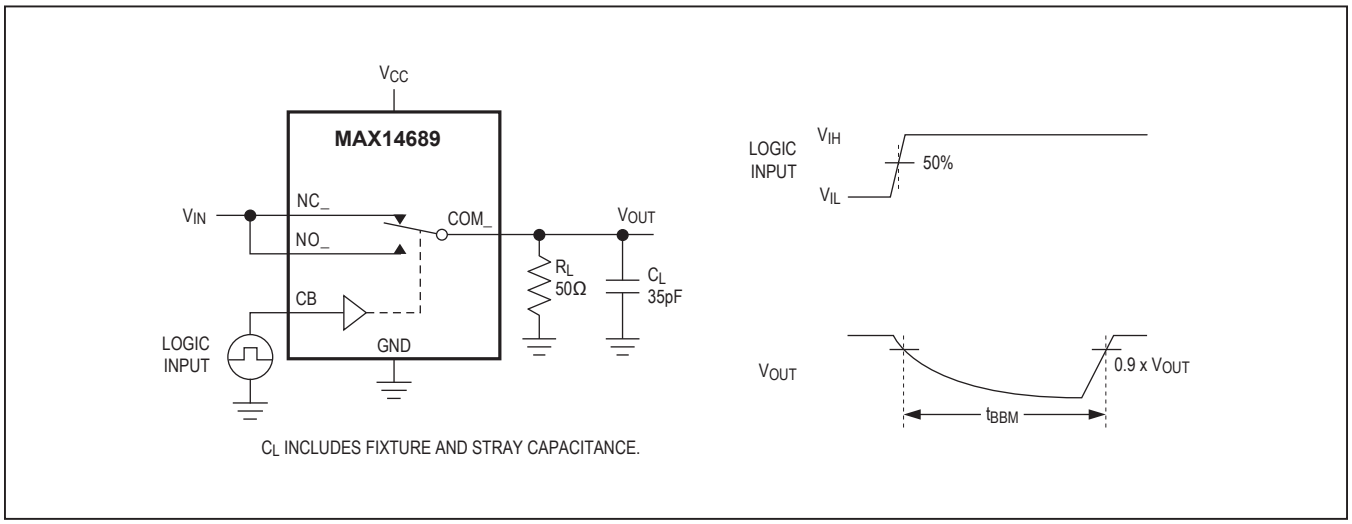


Figure 2. Break-Before-Make Interval

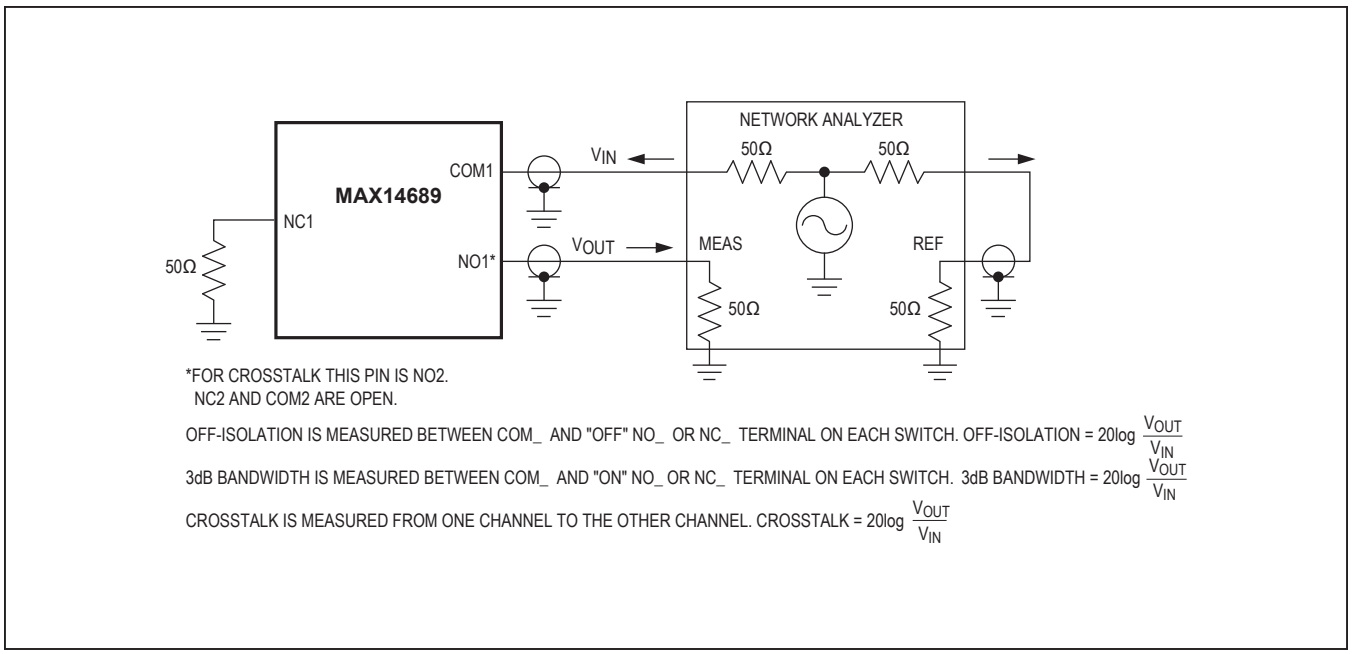


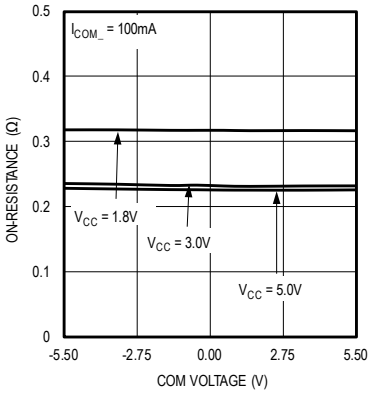
Figure 3. 3dB Bandwidth, Off-Isolation, and Crosstalk

Typical Operating Characteristics

(V_{CC} = 2.5V, T_A = +25°C, unless otherwise noted.)

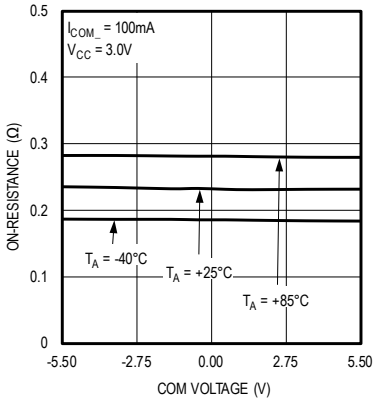
TOC1

ON-RESISTANCE vs. COM VOLTAGE



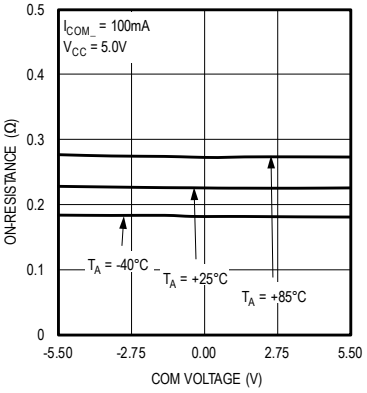
TOC2

ON-RESISTANCE vs. COM VOLTAGE



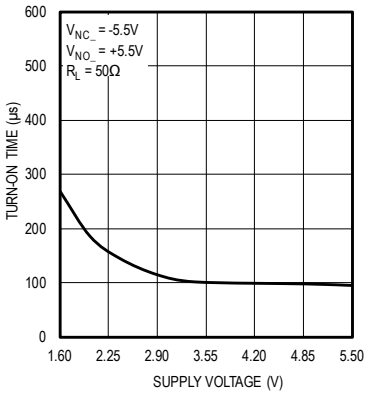
TOC3

ON-RESISTANCE vs. COM VOLTAGE



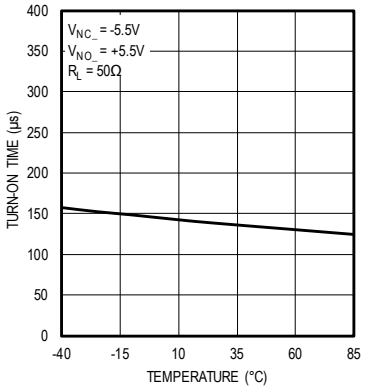
TOC4

TURN-ON TIME vs. SUPPLY VOLTAGE



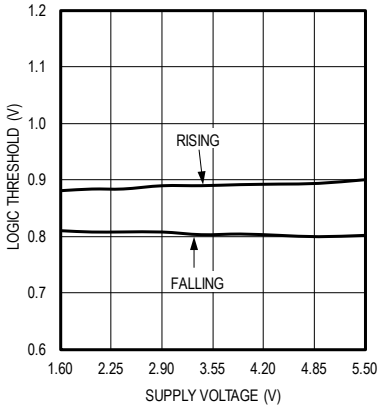
TOC5

TURN-ON TIME vs. TEMPERATURE



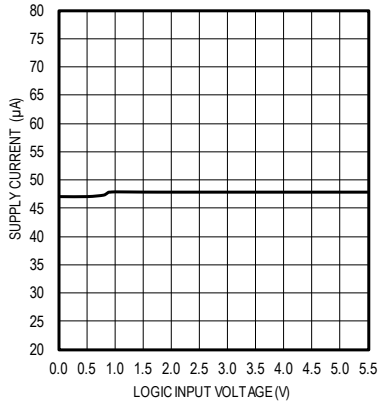
TOC6

LOGIC THRESHOLD vs. SUPPLY VOLTAGE



TOC7

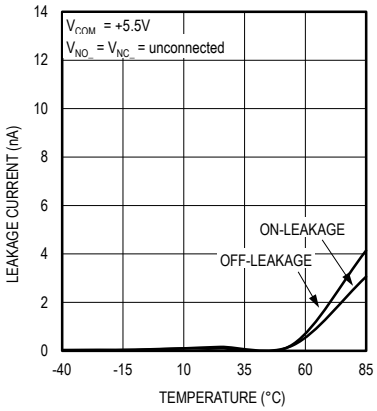
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



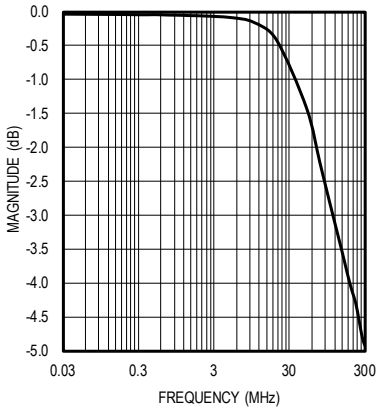
Typical Operating Characteristics (continued)

(V_{CC} = 2.5V, T_A = +25°C, unless otherwise noted.)

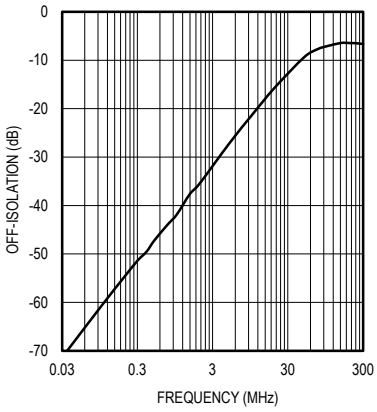
COM_ LEAKAGE CURRENT vs. TEMPERATURE TOC8



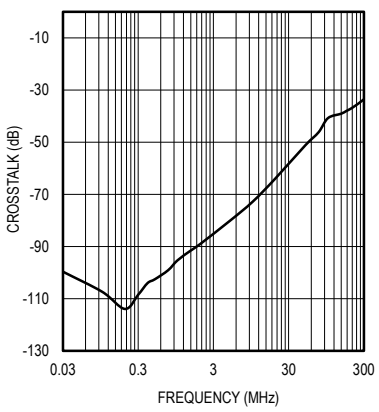
FREQUENCY RESPONSE TOC9



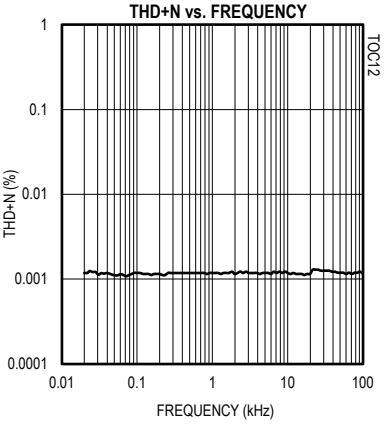
OFF-ISOLATION vs. FREQUENCY TOC10



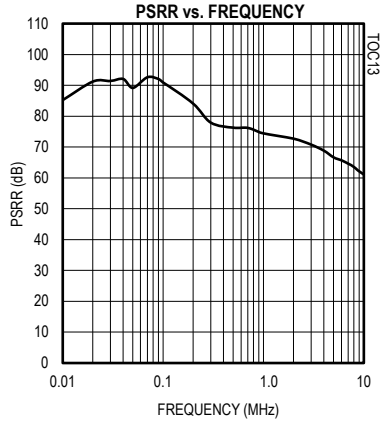
CROSSTALK vs FREQUENCY TOC11



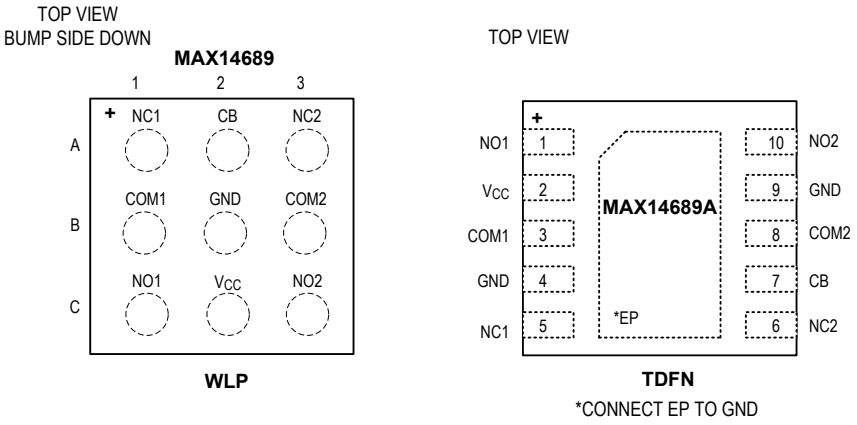
THD+N vs. FREQUENCY TOC12



PSRR vs. FREQUENCY TOC13



Pin Configuration



Pin Description

WLP BUMP	TDFN PIN	NAME	FUNCTION
A1	5	NC1	Normally Closed Terminal for Switch 1
A2	7	CB	Digital Control Input. Drive CB low to connect COM_ to NC_. Drive CB high to connect COM_ to NO_.
A3	6	NC2	Normally Closed Terminal for Switch 2
B1	3	COM1	Common Terminal for Switch 1
B2	4, 9	GND	Ground
B3	8	COM2	Common Terminal for Switch 2
C1	1	NO1	Normally Open Terminal for Switch 1
C2	2	V_{CC}	Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close to the device as possible.
C3	10	NO2	Normally Open Terminal for Switch 2
—	—	EP	Exposed Pad. Connect EP to ground. (TDFN only)

Detailed Description

The MAX14689 is an ultra-small, low on-resistance, high ESD-protected DPDT switch that operates from a +1.6V to +5.5V supply, and is designed to pass analog signals such as AC-biased or DC-biased audio and video signals. These switches feature the low on-resistance (R_{ON}) necessary for high-performance switching applications. The Beyond-the-Rails signal capability of the MAX14689 allows signals below ground and above V_{CC} to pass without distortion.

Analog Signal Levels

The MAX14689 is bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs. The topology of the switches allows the signal to drop below ground without the need of an external negative voltage supply. Note: The devices can also withstand analog signal levels of -5.5V to +5.5V when the device is not powered.

Digital Control Input

The MAX14689 provides a single-bit control logic input, CB. CB controls the switch position, as shown in the *Typical Application Circuit/Functional Diagram*.

Applications Information

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. COM1 and COM2 are further protected against ESD up to ±15kV (HBM), ±10kV (Air-Gap Discharge), and ±8kV (Contact Discharge) without damage. NO_ and NC_ are protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the devices continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test methodology and test results.

Human Body Model

Figure 4 shows the Human Body Model. Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. Figure 6 shows the IEC 61000-4-2 model and Figure 7 shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD Contact-Discharge Method.

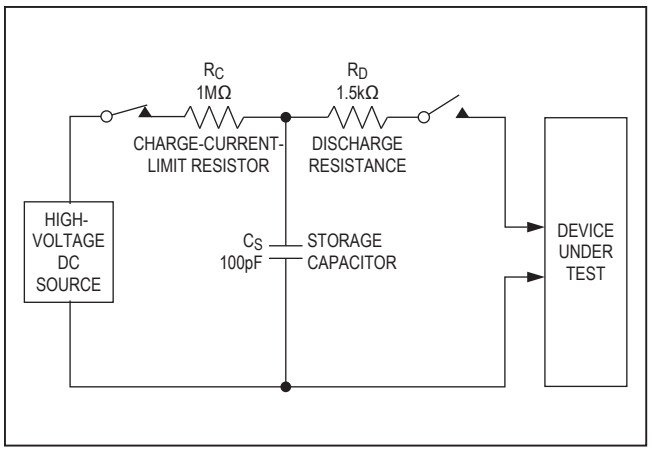


Figure 4. Human Body ESD Test Model

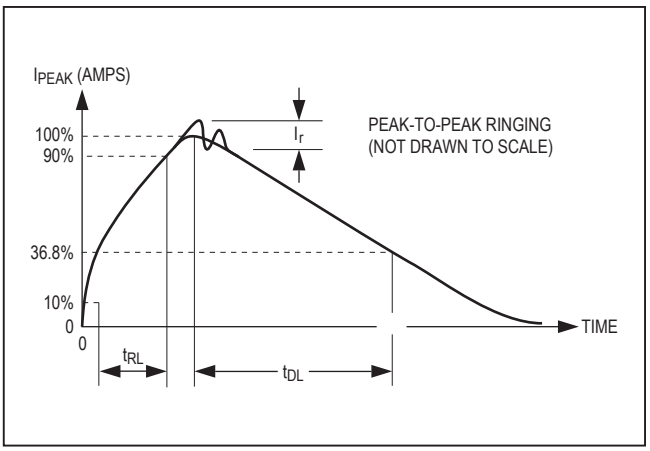


Figure 5. Human Body Current Waveform

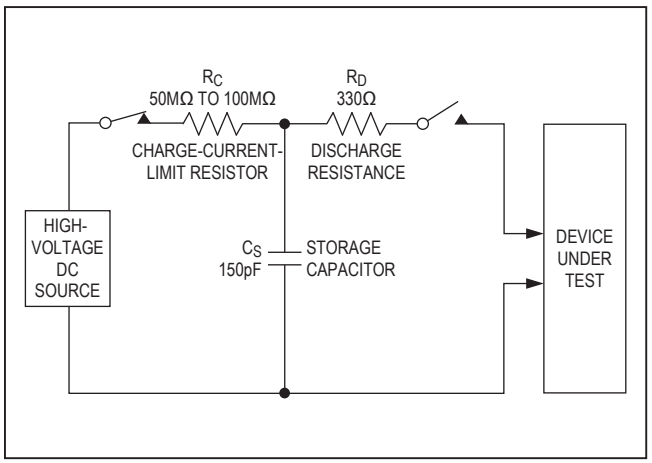


Figure 6. IEC 61000-4-2 ESD Test Model

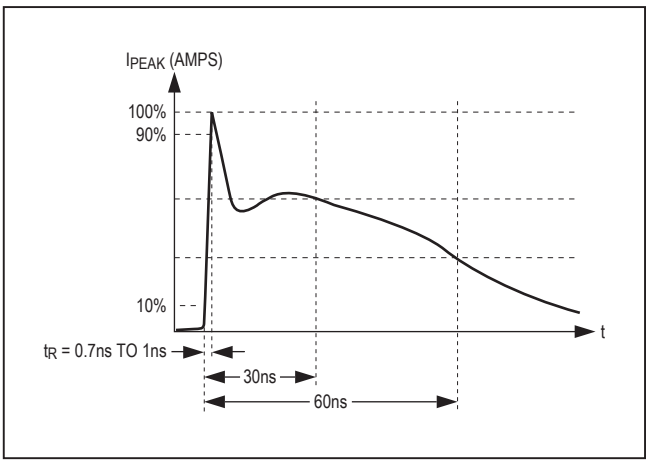


Figure 7. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX14689EWL+T	9 WLP	AKL
MAX14689AETB+T	10 TDFN-EP*	AAF

**EP = Exposed pad*
+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS