General Description

The MAX14691–MAX14693 adjustable overvoltage, undervoltage, and overcurrent protection devices guard systems against overcurrent faults in addition to positive overvoltage and reverse-voltage faults. When used with an optional external pMOSFET, the devices also protect downstream circuitry from voltage faults up to +58V, -60V (for -60V external pFET rating). The devices feature a low, 31mΩ, on-resistance integrated FET.

During startup, the devices are designed to charge large capacitances on the output in a continuous mode for applications where large reservoir capacitors are used on the inputs to downstream devices. Additionally, the devices feature a dual-stage, current-limit mode in which the current is continuously limited to 1x, 1.5x, and 2x the programmed limit, respectively, for a short time after startup. This enables faster charging of large loads during startup.

The MAX14691–MAX14693 also feature reverse-current and overtemperature protection. The devices are available in a 20-pin (5mm x 5mm) TQFN package and operate over the -40°C to 125°C temperature range.

Applications

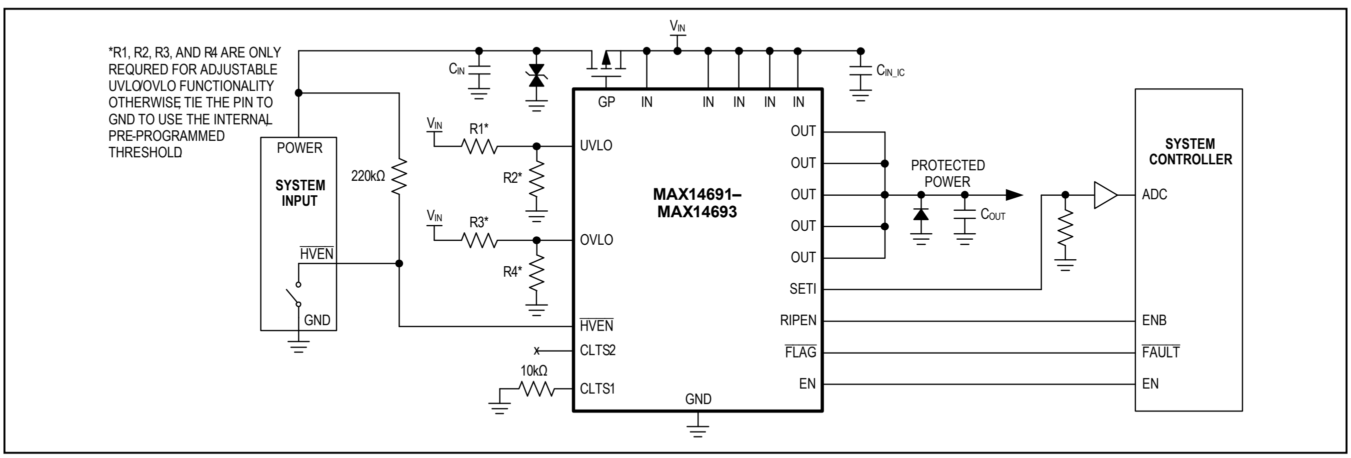
- Industrial Power Systems
- Control and Automation
- Motion System Drives
- Human Machine Interfaces
- High-Power Applications

Benefits and Features

- Robust, High-Power Protection Reduces System Downtime
  - Wide Operating Input Range: +5.5V to +58V
  - -60V Negative Input Tolerance (for -60V External pFET Rating
  - Low 31mΩ (typ) R_{ON}
  - Reverse Current-Blocking Protection with External pFET
- Enables Fast Startup and Brownout Recovery
  - Thermal Foldback Current-Limit Protection
  - Dual-Stage Current Limiting
    - 1.0x Startup Current (MAX14691)
    - 1.5x Startup Current (MAX14692)
    - 2.0x Startup Current (MAX14693)
- Flexible Design Enables Reuse and Less Requalification
  - Adjustable OVLO and UVLO Thresholds
  - Programmable Forward Current Limit From 0.6A to 6A with ±15% Accuracy Over Full Temperature Range
  - Normal and High-Voltage Enable Inputs (EN and $\overline{\text{HVEN}}$)
  - Protected External pFET Gate Drive
- Saves Board Space and Reduces External BOM Count
  - 20-Pin 5mm x 5mm TQFN Package
  - Integrated nFET

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



Absolute Maximum Ratings

(All voltages referenced to GND.)
IN (Note 1)...-0.3V to +58V
OUT ....-0.3V to V_{IN} + 0.3V
HVEN (Note 1) ....-0.3V to V_{IN} + 0.3V
GP ....max (-0.3V, V_{IN} - 20V) to V_{IN} + 0.3V
UVLO, OVLO..............................-0.3V to min (V_{IN} + 0.3V, 20V)
FLAG, EN, RIPEN, CLTS1, CLTS2........................-0.3V to +6V
Maximum Current into IN (DC) (Note 2) 6A
SETI...-0.3V to min (V_{IN} + 0.3V, 6V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C).................2758mW
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range............................-65ºC to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: An external pFET or diode is required to achieve negative input protection.
Note 2: DC current-limited by R_{SETI}, as well as by thermal design.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 3)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})..........29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................2°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 5.5V to 58V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V, T_A = +25°C) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
IN Voltage Range	V_{IN}		5.5		58	V
Shutdown IN Current	I_{SHDN}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{IN} < 24V		4	7	µA
		V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{IN} < 40V		4	10	
Supply Current	I_{IN}	V_{IN} = V_{OUT} = 24V, $V_{\overline{HVEN}}$ = 0V		1.4	1.9	mA
Shutdown OUT Current	I_{OFF}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V		50	100	µA
UVLO, OVLO						
Internal UVLO Trip Level	V_{UVLO}	V_{IN} falling, UVLO trip point	11.5	12	12.5	V
		V_{IN} rising	11.9	12.4	13	
UVLO Hysteresis		% of typical UVLO		3		%
Internal OVLO Trip Level	V_{OVLO}	V_{IN} falling	32.2	34.1	35.8	V
		V_{IN} rising, OVLO trip point	34.7	36.2	37.6	
OVLO Hysteresis		% of typical OVLO		6		%
External UVLO Adjustment Range (Note 5)			5.5		24	V
External UVLO Select Voltage	V_{UVLO_SEL}		0.15	0.38	0.5	V
External UVLO Leakage Current	I_{UVLO_LEAK}		-250		+250	nA
External OVLO Adjustment Range (Note 5)			6		40	V
External OVLO Select Voltage	V_{OVLO_SEL}		0.15	0.38	0.5	V

Electrical Characteristics (continued)

(V_{IN} = 5.5V to 58V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V, T_A = +25°C) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External OVLO Leakage Current	I_{OVLO_LEAK}		-250		+250	nA
External UVLO/OVLO Set Voltage	V_{SET}		1.18	1.22	1.27	V
Undervoltage Trip Level on OUT	V_{UVLO_OUT}	V_{OUT} falling, UVLO trip point	11.5	12	12.5	V
		V_{OUT} rising	11.9	12.4	13	
GP						
Gate Clamp Voltage	V_{GP}		10	16.1	20	V
Gate Active Pullup				25	50	Ω
Gate Active Pulldown		V_{EN} = 5V	47	100		µA
Shutdown Gate Active Pullup		VEN = 0V, $V_{\overline{HVEN}}$ = 5V		2.4		MΩ
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} ≥ 10V, T_A = +25°C		31	42	mΩ
Current Limit Adjustment Range	I_{LIM}		0.6		6	A
Current Limit Accuracy	I_{LIM_ACC}	1A ≤ I_{LIM} ≤ 6A (T_A = +25°C)	-10		+10	%
		0.6A ≤ I_{LIM} ≤ 6A	-15		+15	
$\overline{FLAG}$ Assertion Drop Voltage Threshold	V_{FA}	Increase in (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V		490		mV
Reverse Current-Blocking Threshold	V_{RIB}	V_{IN} – V_{OUT}	0	-10	-16	mV
Reverse Current-Blocking Response Time	t_{RIB}	(V_{IN} – V_{OUT}) changes from 0.2V to -0.3V in 100nsec, t_{RIB} is the interval between V_{IN} = V_{OUT} and V_{IN} - GP = 0.5V without capacitive load on GP		1	1.5	µs
Reverse-Blocking Supply Current	I_{RBS}	V_{OUT} = 24V		2460	4060	µA
LOGIC INPUT ($\overline{HVEN}$, CLTS1, CLTS2, EN, RIPEN)						
$\overline{HVEN}$ Threshold Voltage	$V_{\overline{HVEN}\_TH}$		1	2	3.1	V
$\overline{HVEN}$ Threshold Hysteresis				5		%
$\overline{HVEN}$ Input Leakage Current	$I_{\overline{HVEN}\_LEAK}$	$V_{\overline{HVEN}}$ = 58V		42	66	µA
EN, RIPEN, CLTS1, CLTS2 Input Logic-High	V_{IH}		1.4			V
EN, RIPEN, CLTS1, CLTS2 Input Logic-Low	V_{IL}				0.4	V
EN, RIPEN Input Leakage Current	I_{EN_LEAK}, I_{RIPEN_LEAK}	V_{EN}, V_{RIPEN} = 0V, 5V	-1		+1	µA
CLTS_ Leakage Current		CLTS_ = GND		25		µA
LOGIC OUTPUT ($\overline{FLAG}$)						
Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
Input Leakage Current		V_{IN} = 5.5V, $\overline{FLAG}$ deasserted			1	µA

Electrical Characteristics (continued)

(V_{IN} = 5.5V to 58V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V, T_A = +25°C) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SETI						
R_{SETI} x I_{LIM}	V_{RI}	See *Setting the Current-Limit Threshold* section		1.5		V
Current Mirror Output Ratio	C_{IRATIO}			25000		
DYNAMIC PERFORMANCE (NOTE 6)						
Switch Turn-On Time	t_{ON}	V_{IN} = 24V, switch OFF to ON, R_{LOAD} = 240Ω, I_{LIM} = 1A, C_{OUT} = 4.7µF, V_{OUT} from 20% to 80% of V_{IN}		68		µs
Fault Recovery NFET Turn-On Time	t_{ON_NFET}	V_{OUT} > V_{UVLO_OUT}, turn-on delay after fault timers expired		420	770	µs
Reverse-Current Fault Recovery Time	t_{REV_REC}		2.18	2.4	2.64	ms
OVP Switch Response Time	t_{OVP_RES}			3		µs
Overcurrent Switch Response time	t_{OCP_RES}	I_{LIM} = 4A		3		µs
Startup Timeout	t_{STO}	Initial start current-limit foldback timeout (Figure 1)	1090	1200	1320	ms
Startup Initial Time	t_{STI}	Current is continuously limited to 1x/1.5x/2x in this interval (Figure 1)	21.8	24	26.4	ms
IN Debounce Time	t_{DEB}	Interval between V_{IN} > V_{UVLO} and V_{OUT} = 10% of V_{IN} (Figure 2)	1	1.5	2.1	ms
Blanking Time	t_{BLANK}	(Figures 3 and 4)	21.8	24	26.4	ms
Autoretry Time	t_{RETRY}	(Figure 3, Note 7)	554	720	792	ms
THERMAL PROTECTION						
Thermal Foldback	T_{J_FB}			150		°C
Thermal Shutdown	T_{J_MAX}			165		°C
Thermal Shutdown Hysteresis				10		°C

Note 4: All devices are 100% production-tested at T_A = +25ºC. Specifications over the operating temperature range are guaranteed by design.
Note 5: Not production-tested, user-adjustable. See the *Overvoltage Lockout (OVLO)* and *Undervoltage Lockout (UVLO)* sections.
Note 6: All timing is measured using 20% and 80% levels, unless otherwise specified.
Note 7: The autoretry time-to-blanking time ratio is fixed and is equal to 30.

Timing Diagrams

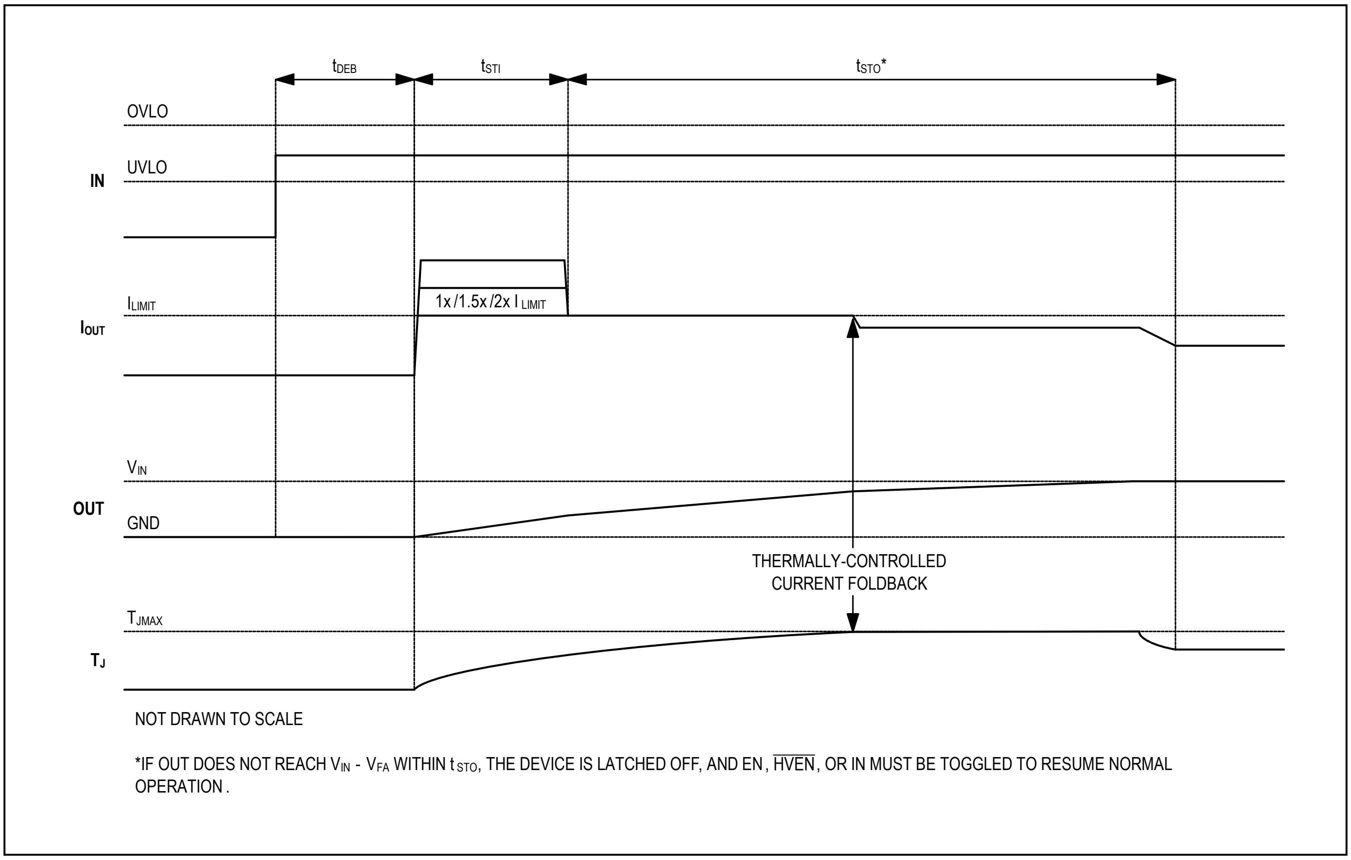


Figure 1. Startup Timing

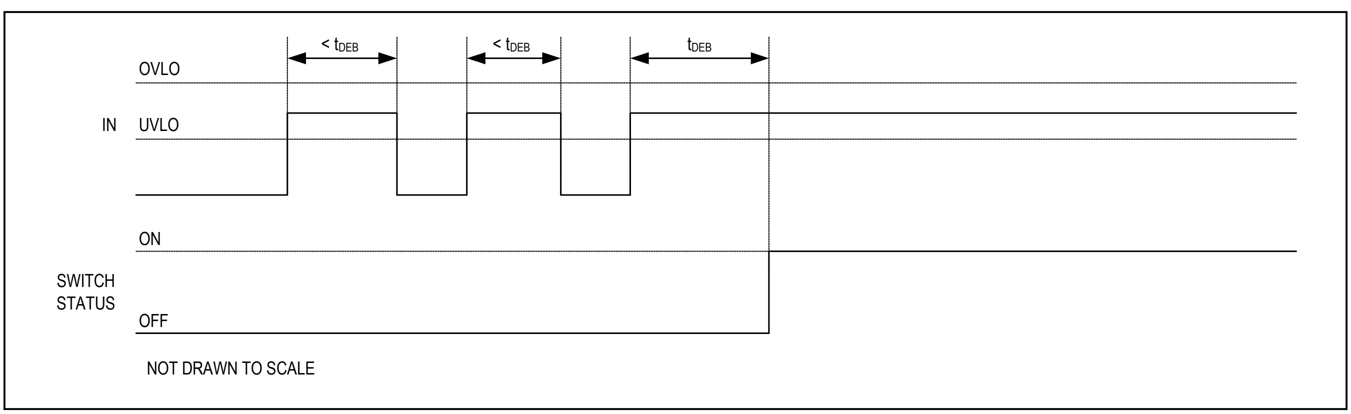
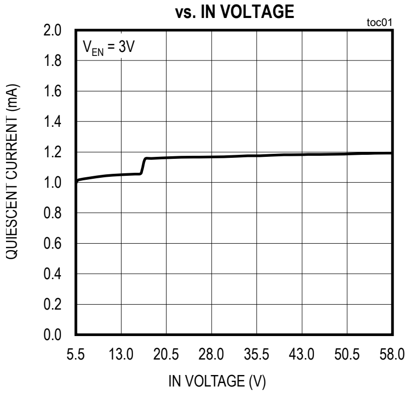


Figure 2. Debounce Timing

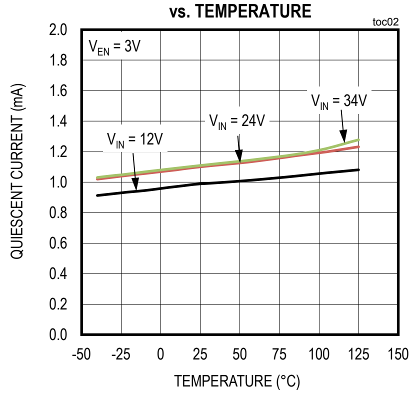
Typical Operating Characteristics

(V_{IN} = 12V, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

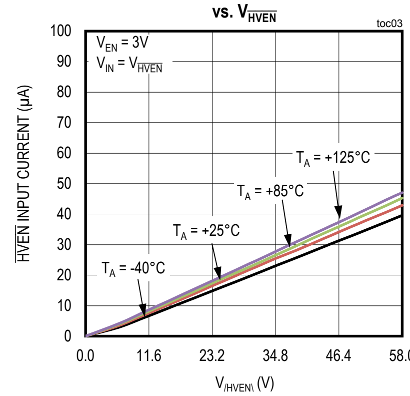
QUIESCENT IN CURRENT vs. IN VOLTAGE



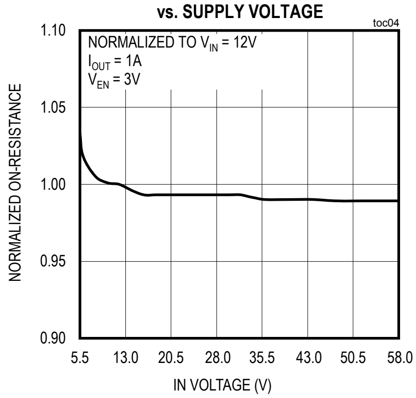
QUIESCENT IN CURRENT vs. TEMPERATURE



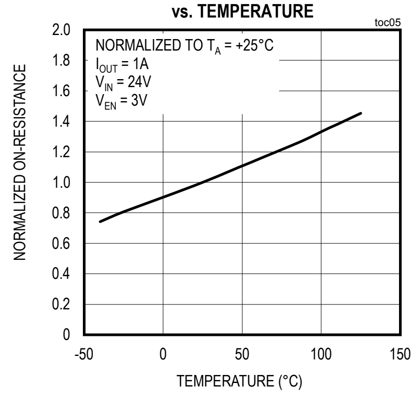
HVEN INPUT CURRENT vs. $V_{\overline{HVEN}}$



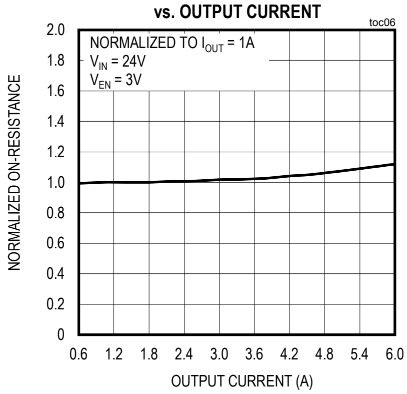
NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



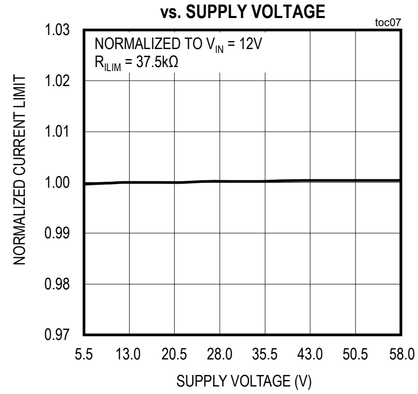
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



NORMALIZED ON-RESISTANCE vs. OUTPUT CURRENT



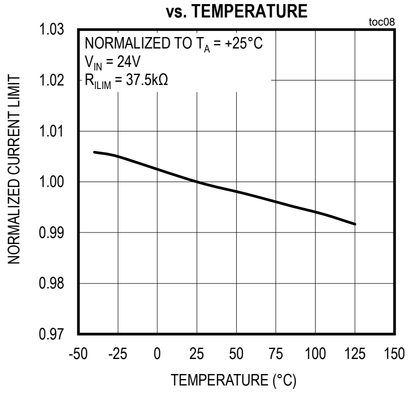
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



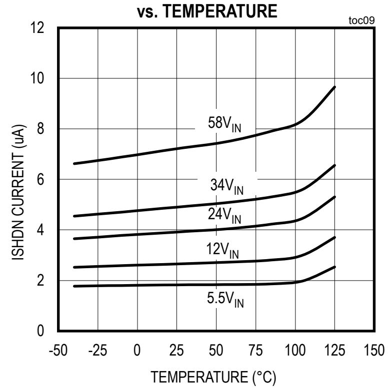
Typical Operating Characteristics (continued)

(V_{IN} = 12V, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

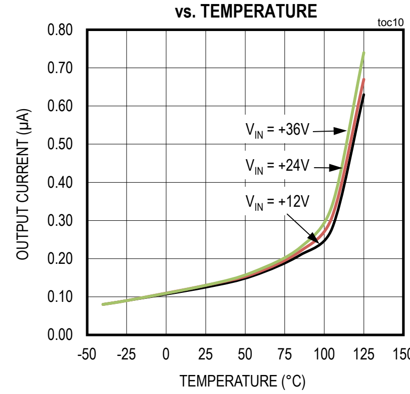
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



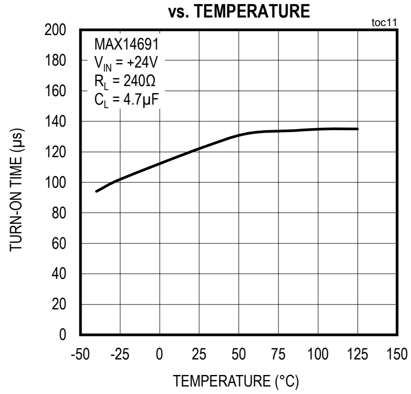
SHUTDOWN IN CURRENT vs. TEMPERATURE



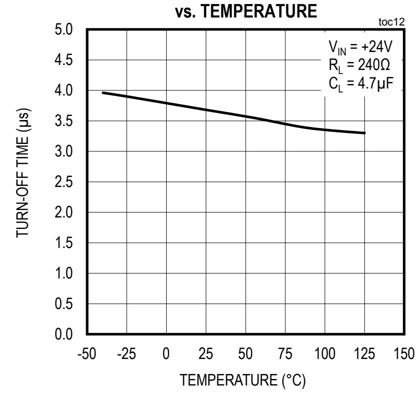
SHUTDOWN OUTPUT CURRENT vs. TEMPERATURE



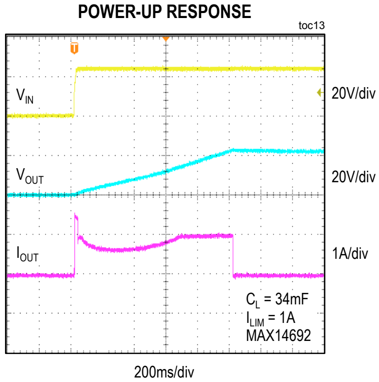
SWITCH TURN-ON TIME vs. TEMPERATURE



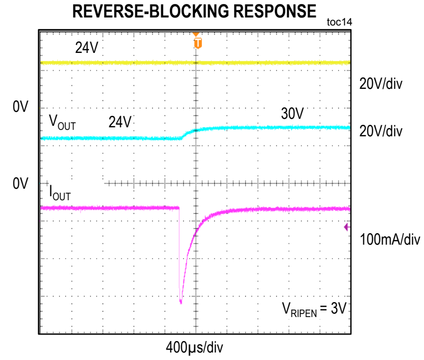
SWITCH TURN-OFF TIME vs. TEMPERATURE



POWER-UP RESPONSE

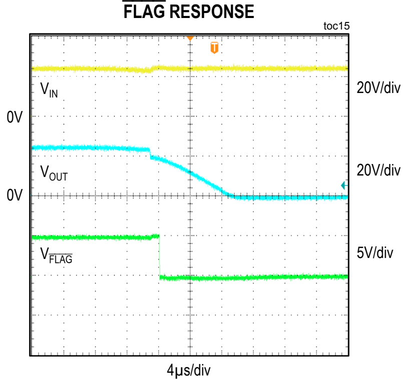


REVERSE-BLOCKING RESPONSE

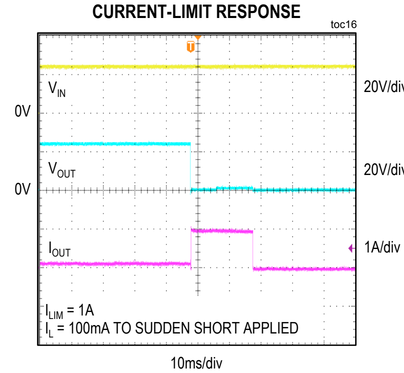


Typical Operating Characteristics

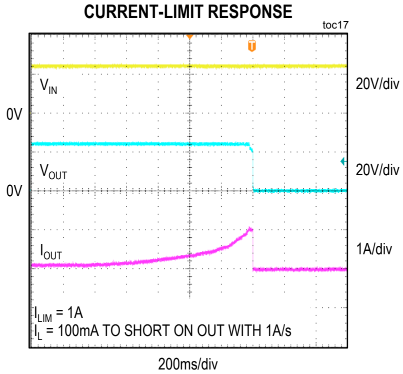
(V_{IN} = 12V, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)



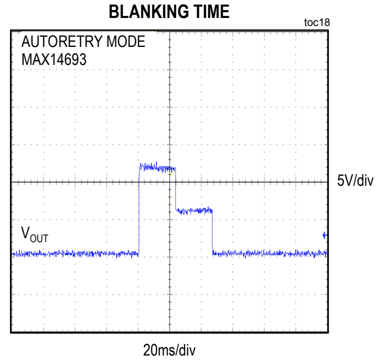
$\overline{\text{FLAG}}$ RESPONSE



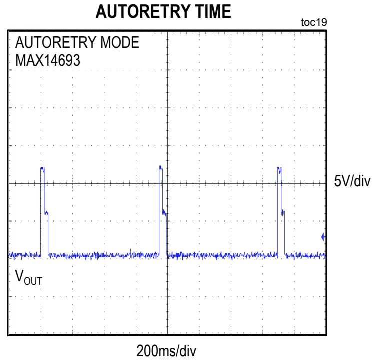
CURRENT-LIMIT RESPONSE



CURRENT-LIMIT RESPONSE

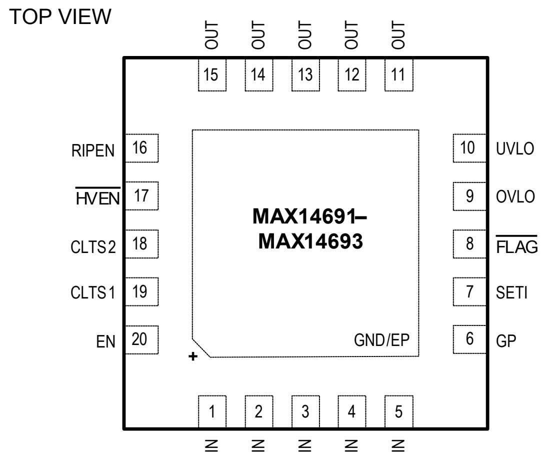


BLANKING TIME



AUTORETRY TIME

Pin Configurations

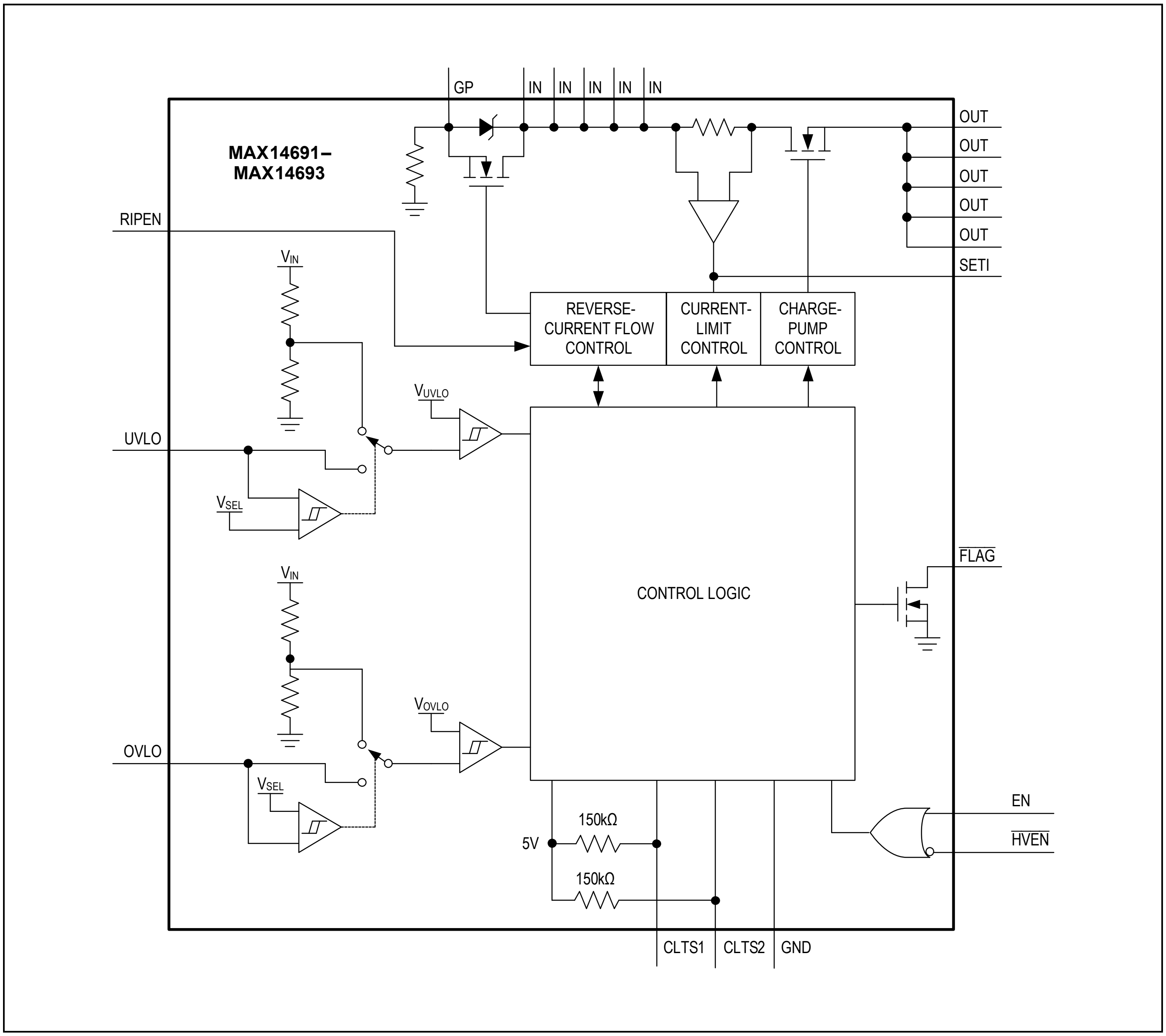


TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	FUNCTION
1–5	IN	Switch Input. Bypass IN to ground with a 1µF ceramic capacitor for ±15kV Human Body Model ESD protection on IN. In applications in which an external pFET is used, a 4.7µF capacitor should be placed at the drain of the pFET and a reduced capacitor of 10nF to 100nF should be placed at IN. The maximum slew rate allowed at IN is 30V/µs. IN serves as the under/overvoltage sensed input when preprogrammed UVLO/OVLO is used.
6	GP	Gate Driver Output for External pFET.
7	SETI	Overload Current-Limit Adjust. Connect a resistor from SETI to GND to program the overcurrent limit. SETI must be connected to a resistor. If SETI is connected to GND during startup, then the switch does not turn on. Do not connect more than 30pF to SETI.
8	$\overline{FLAG}$	Open Drain Fault Indicator Output. $\overline{FLAG}$ asserts low when the V_{IN} - V_{OUT} voltage exceeds V_{FA}, reverse current is detected, thermal shutdown mode is active, OVLO or UVLO threshold is reached, or SETI is connected to GND.
9	OVLO	Externally-Programmable Overvoltage-Lockout Threshold. Connect OVLO to GND to use the default internal OVLO threshold. Connect OVLO to an external resistor-divider to define a threshold externally and override the preset internal OVLO threshold.
10	UVLO	Externally Programmable Undervoltage-Lockout Threshold. Connect UVLO to GND to use the default internal UVLO threshold. Connect UVLO to an external resistor-divider to define a threshold externally and override the preset internal UVLO threshold.
11–15	OUT	Switch Output. Bypass OUT to GND with a 4.7µF ceramic capacitor placed as close as possible to the device.
16	RIPEN	Reverse-Current Protection Enable. Connect RIPEN to GND to disable the reverse-current flow protection. Connect RIPEN to logic-high to activate the reverse-current flow protection.
17	$\overline{HVEN}$	58V Capable Active-Low Enable Input. See Table 1.
18	CLTS2	Current-Limit Type Select 2. See Table 2.
19	CLTS1	Current-Limit Type Select 1. See Table 2.
20	EN	Active-High Enable Input. See Table 1.
—	GND/EP	Ground/Exposed Pad. Connect to a large copper ground plane to maximize thermal performance.

Functional Diagram



Detailed Description

The MAX14691—MAX14693 adjustable overvoltage, undervoltage, and overcurrent protection devices guard systems against overcurrent faults in addition to positive overvoltage and reverse-voltage faults. When used with an optional external pMOSFET, the devices also protect downstream circuitry from voltage faults up to +58V, -60V (for -60V external pFET rating). The devices feature a low, 31mΩ, on-resistance integrated FET. During startup, the devices are designed to charge large capacitances on the output in a continuous mode for applications where large reservoir capacitors are used on the inputs to downstream devices. Additionally, the devices feature a dual-stage current-limit mode in which the current is continuously limited to 1x, 1.5x, and 2x the programmed limit, respectively, for a short time after startup. This enables faster charging of large loads during startup.

The devices feature the option to set the overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds manually using external voltage-dividers or to use the factory-preset internal thresholds by connecting the OVLO and/or UVLO pin(s) to GND. The permitted overvoltage setting range of the devices is 6V to 40V. Therefore, the pFET and internal nFET must be kept off in the 40V to 58V range by appropriate OVLO resistor-divider.

The adjustable overvoltage range of the devices is 6V to 40V, while the adjustable undervoltage range is 5.5V to 24V. The factory-preset internal threshold for the devices is 36V (typ), with the preset internal UVLO threshold being 12V (typ).

The devices' programmable current-limit threshold can be set for currents up to 6A in autoretry, latchoff, or continuous-fault-response mode. When the device is set to autoretry mode and the current exceeds the threshold for more than 24ms (typ), both FETs are turned off for 720ms (typ), then turned back on. If the fault is still present, the cycle repeats. In latchoff mode, if a fault is present for more than 24ms (typ), both FETs are turned off until enable is toggled or the power is cycled. In continuous mode, the current is limited continuously to the programmed current-limit value. In all modes, $\overline{FLAG}$ asserts if V_{IN} - V_{OUT} is greater than the $\overline{FLAG}$ assertion drop voltage threshold (V_{FA}).

Startup Control

The devices feature a dual-stage startup sequence that continuously limits the current to 1x/1.5x/2x the set current limit during the startup initial time (t_{STI}), allowing large capacitors present on the output of the switch to be rapidly charged. The MAX14691 limits the current to 1x the set limit during this period, while the MAX14692 and MAX14693 limit the current to 1.5x and 2x the set limit, respectively. If the temperature of any device rises to the thermal-foldback threshold (T_{J_FB}), the device enters power-limiting mode (Figure 1). In this mode, the device thermally regulates the current through the switch to protect itself while still delivering as much current as possible to the output regardless of the current-limit type selected. If the output is not charged within the startup timeout period (t_{STO}), the switch turns off and IN, EN, or $\overline{HVEN}$ must be toggled to resume normal operation. The devices have a 16ms (typ) time delay at the end of startup, during which the reverse threshold is set at -180mV (typ.) to prevent false reverse faults due to oscillation. After this delay, the reverse-current blocking threshold is reduced to -10mV (V_{RIB}, typ).

Overvoltage Lockout (OVLO)

The devices feature two methods for determining the OVLO threshold. By connecting the OVLO pin to GND, the preset internal OVLO threshold of 36V (typ) is selected. If the voltage at OVLO rises above the OVLO select threshold (V_{OVLO_SEL}), the device enters adjustable OVLO mode. Connect an external voltage-divider to the OVLO pin, as shown in the *Typical Application Circuit* to adjust the OVLO threshold. R3 = 2.2MΩ is a good starting value for minimum current consumption. Since V_{SET} is known, R3 has been chosen, and V_{OVLO} is the target OVLO value, R4 can then be calculated by the following equation:

$$R4 = \frac{R3 \times V_{SET}}{V_{OVLO} - V_{SET}}$$

Undervoltage Lockout (UVLO)

The devices feature two methods for determining the UVLO threshold. By connecting the UVLO pin to GND, the preset, internal UVLO threshold of 12V (typ) is selected. If the voltage at UVLO rises above the UVLO select threshold (V_{UVLO_SEL}), the device enters adjustable UVLO mode. Connect an external voltage-divider to the UVLO pin, as shown in the *Typical Application Circuit* to adjust the UVLO threshold. R1 = 2.2MΩ is a good starting value for minimum current consumption. Since V_{SET} is known, R1 has been chosen, and V_{UVLO} is the target value, R2 can then be calculated by the following equation:

$$R2 = \frac{R1 \times V_{SET}}{V_{UVLO} - V_{SET}}$$

Table 1. Enable Inputs

$\overline{HVEN}$	EN	SWITCH STATUS
0	0	ON
0	1	ON
1	0	OFF
1	1	ON

Switch Control

There are two independent enable inputs on the devices: $\overline{HVEN}$ and EN. $\overline{HVEN}$ is a high-voltage-capable input, accepting signals up to 58V. EN is a low-voltage input, accepting a maximum voltage of 5V. In case of a fault condition, toggling $\overline{HVEN}$ or EN resets the fault. The enable inputs control the state of the switch based on the truth table (Table 1).

Input Debounce

The devices feature a built-in input debounce time (t_{DEB}). The debounce time is a delay between a POR event and the switch being turned on. If the input voltage rises above the UVLO threshold voltage or if, with a voltage greater than V_{UVLO} present on IN, the enable pins toggle to the on state, the switch turns on after t_{DEB}. In cases where the voltage at IN falls below V_{UVLO} before t_{DEB} has passed, the switch remains off (Figure 2). If the voltage at OUT is already above V_{UVLO_OUT} when the device is turned on through either enable pin or coming out of OVLO, there is no debounce interval. This is due to the device already being out of the POR condition with OUT above V_{UVLO_OUT}.

Current-Limit Type Select

The devices feature three selectable current-limiting modes. During power-up, all devices default to continuous mode and follow the procedure defined in the *Startup Control* section. Once the part has been successfully powered on and t_{STO} has expired, the device senses the condition of CLTS1 and CLTS2. The condition of CLTS1 and CLTS2 sets the current-limit mode type according to Table 2. CLTS1,2 are internally pulled up to an internal 5V supply. Therefore, the device is in continuous current-limit mode when CLTS1 and 2 are open. To set CLTS_ state to low, connect a 10kΩ resistor or below to ground.

In addition to the selectable current-limiting modes, the device has a protection feature against a severe overload condition. If the output current exceeds 2 times the set current limit, the device will turn off the internal nFET and external pFET immediately and will attempt to restart to allow the overcurrent to last for t_{BLANK} time. The off duration depends on fault condition occurred after the FETs turn off, with the shortest duration of 420µs (t_{ON_FET}) if there is no fault. In latchoff mode, the device will latch off if the overcurrent fault last longer than t_{BLANK}.

Table 2. Current-Limit Type Select

CLTS2	CLTS1	CURRENT-LIMIT TYPE
0	0	LATCHOFF MODE
0	1	AUTORETRY MODE
1	0	CONTINUOUS MODE
1	1	CONTINUOUS MODE

Autoretry Mode (Figure 3)

In autoretry current-limit mode, when current through the device reaches the threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ output asserts low when the voltage drop across the switch rises above V_{FA}. If the overcurrent condition is present for t_{BLANK}, the switch is turned off. The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. A retry time delay (t_{RETRY}) starts immediately once t_{BLANK} has elapsed. During the retry time, the switch remains off and, once t_{RETRY} has elapsed, the switch is turned back on. If the fault still exists, the cycle is repeated and $\overline{FLAG}$ remains low. If the fault has been removed, the switch stays on.

The autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is on during t_{BLANK} time, the supply current is held at the current limit. When the switch is off during t_{RETRY} time, there is no current through the switch. Thus, the output current is much less than the programmed current limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK} + t_{STI} \times K}{t_{BLANK} + t_{RETRY} + t_{STI}}\right]$$

where K is the multiplication factor of the initial current limit (1x, 1.5x or 2x). With a 24ms (typ) t_{BLANK}, 24ms t_{STI}, K = 1 and 720ms (typ) t_{RETRY}, the duty cycle is 3.1%, resulting in 97% power saving when compared to the switch being on the entire time.

Latchoff Mode (Figure 4)

In latchoff current-limit mode, when current through the device reaches the threshold, the t_{BLANK} timer begins counting. $\overline{FLAG}$ asserts when the voltage drop across the switch rises above V_{FA}. The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off if the overcurrent condition remains for the blanking time. The switch remains off until the control logic (EN or $\overline{HVEN}$) is toggled or the input voltage is cycled.

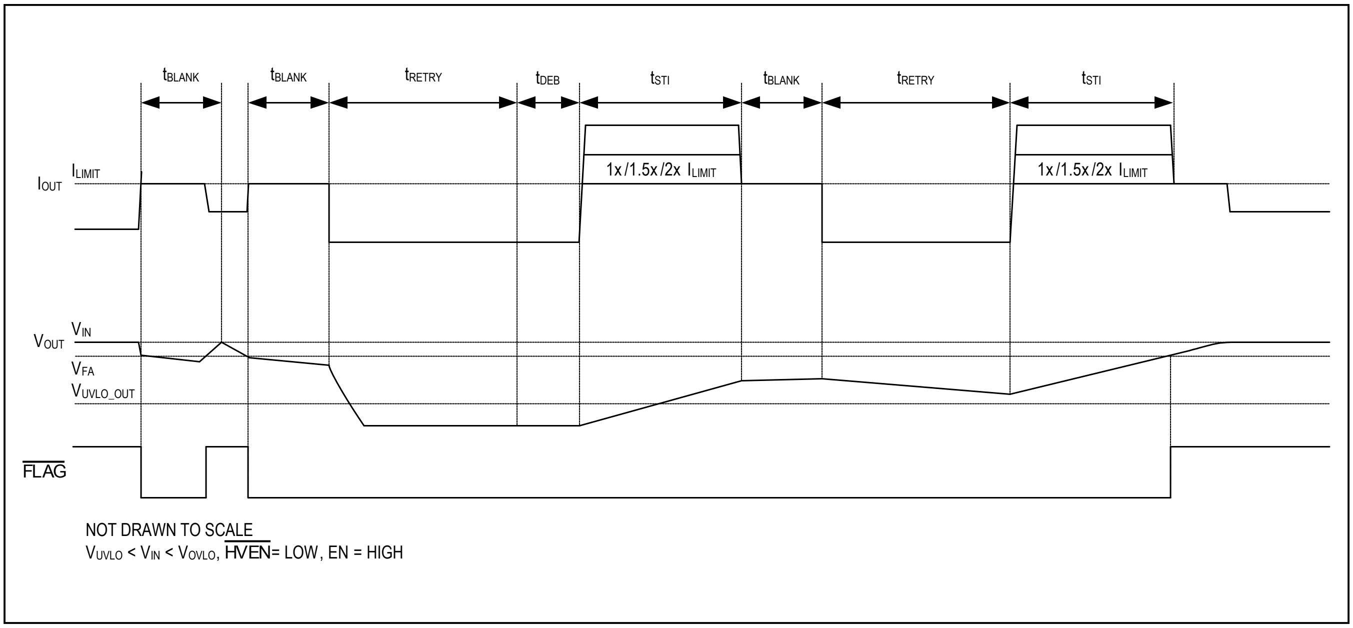


Figure 3. Autoretry Fault Diagram

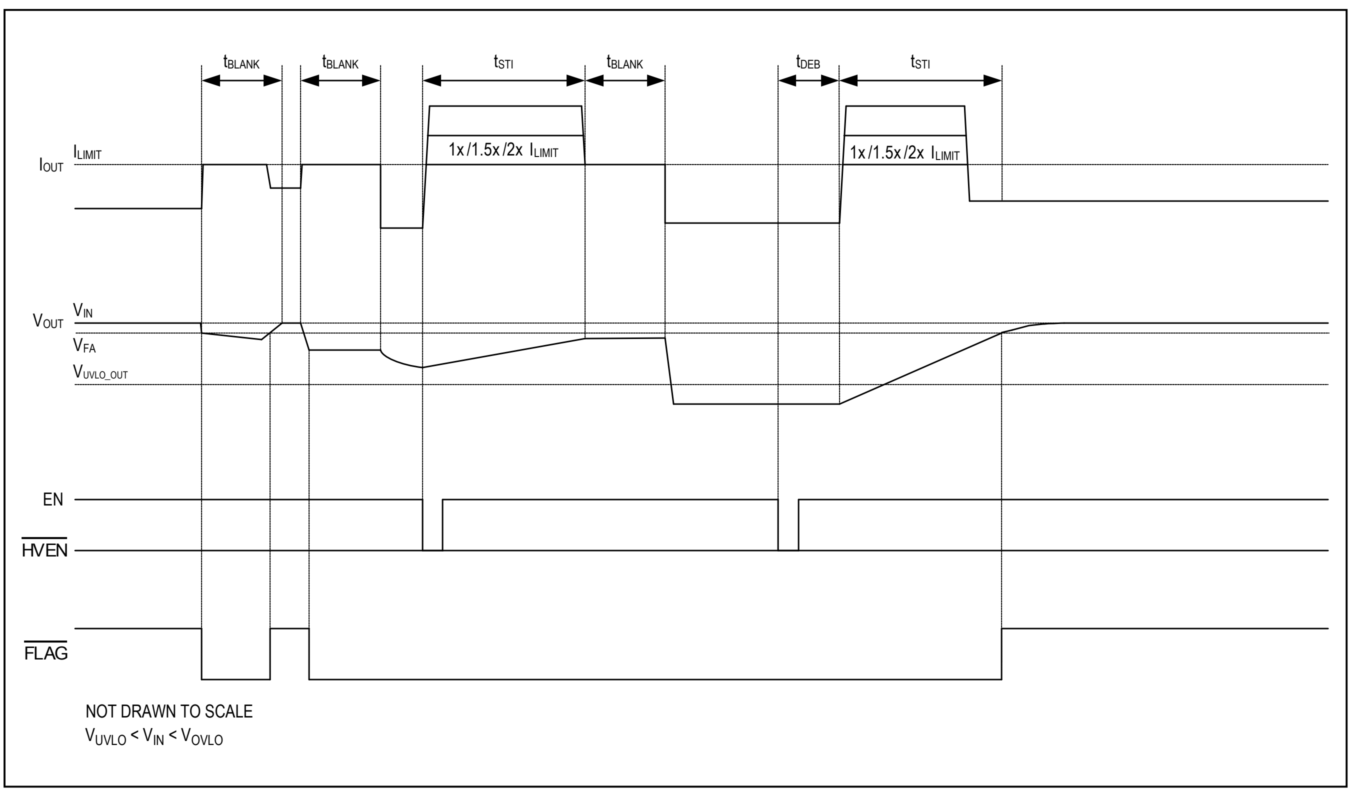


Figure 4. Latchoff Fault Diagram

Continuous Mode (Figure 5)

In continuous current-limit mode, when current through the device reaches the threshold, the device limits the current to the programmed limit. $\overline{FLAG}$ asserts when the voltage drop across the switch rises above V_{FA}, and deasserts when it falls below V_{FA}.

Reverse-Current Blocking (Figure 6)

The devices feature a current-blocking functionality to be used with an external pFET. To enable the reverse-current blocking feature, pull RIPEN high. With RIPEN high, if a reverse-current condition is detected (V_{IN} - V_{OUT} < V_{RIB}), the internal nFET and the external pFET are turned off for 2.4ms (t_{REV_REC}). During and after this time, the device monitors the voltage difference between OUT and IN pins to determine whether the reverse current is still present. Once t_{REV_REC} expired and the reverse-current condition has been removed, the nFET and pFET are turned back on after an additional time delay follows by the dual-stage startup control mechanism as defined in the Startup Control section.

The additional time delay will be 420µs (t_{ON_NFET}) if voltage at OUT is more than or equal to VUVLO_OUT falling at the end of t_{REV_REC} delay, otherwise the delay will be 1.5ms (t_{DEB}). After a reverse-current event, the device will attempt a restart regardless of the current-type select.

Fault Indicator ($\overline{FLAG}$) Output

$\overline{FLAG}$ is an open-drain fault-indicator output. It requires an external pullup resistor to a DC supply. $\overline{FLAG}$ asserts when any of the following conditions occur:

- V_{IN} - V_{OUT} > V_{FA}
- Reverse-current protection is tripped
- Die temperature exceeds +165°C
- SETI is connected to ground
- UVLO threshold has not been reached
- OVLO threshold is reached

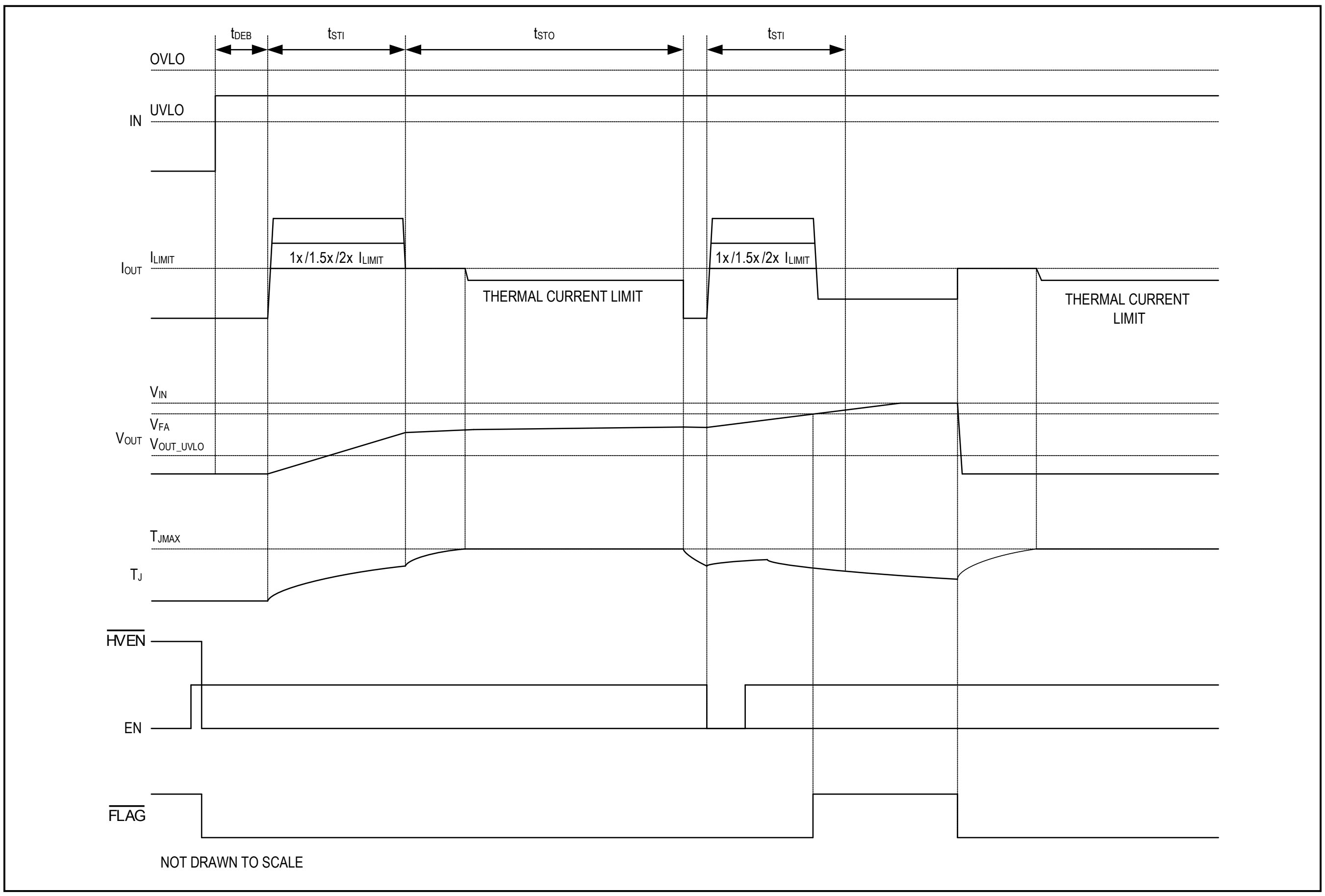


Figure 5. Continuous Fault Diagram

Thermal Shutdown Protection

Thermal-shutdown circuitry protects the devices from overheating. The switch turns off and $\overline{FLAG}$ asserts when the junction temperature exceeds +165°C (typ). The devices exit thermal shutdown and resume normal operation once the junction temperature cools by 10°C (typ) when the device is in autoretry or continuous current-limiting mode. When in latchoff mode, the device remains latched off until the input voltage is cycled or one of the enable pins is toggled.

The thermal shutdown technology built into the devices behave in accordance with the selected current-limit mode. While the devices are in autoretry mode, the thermal limit uses the autoretry timing when coming out of a fault condition. When the devices detect an overtemperature fault, the switch turns off. Once the temperature of the junction falls below the falling thermal threshold, the device turns on after the time interval t_{RETRY}. In latchoff mode, the device latches off until the input is cycled or one of the enable pins is toggled. In continuous current-limiting mode, the device turns off while the temperature is over the limit, then turns back on after t_{DEB} when the temperature reaches the falling threshold. There is no retry time for thermal protection.

Applications Information

Setting the Current-Limit Threshold

Connect a resistor between SETI and ground to program the current-limit threshold for the devices. Leaving SETI unconnected sets the current-limit threshold to 0A and, since connecting SETI to ground is a fault condition, this causes the switch to remain off and $\overline{FLAG}$ to assert. Use the following formula to calculate the current-limit threshold:

$$R_{SETI}(k\Omega) = \frac{V_{RI}(\Omega \times A)}{I_{LIM}(mA)} \times C_{IRATIO}$$

Do not use a R_{SETI} smaller than 6kΩ. Table 3 shows current-limit thresholds for different resistor values at SETI.

A current mirror with a ratio of C_{IRATIO} is implemented with a current-sense auto-zero operational amplifier. The mirrored current of the IN-OUT FET is provided on the SETI pin. Therefore, the voltage (V_{SETI}) read on the SETI pin should be interpreted as the current through the IN-OUT FET, as shown below:

$$I_{IN-OUT} = I_{SETI} \times C_{IRATIO} = \frac{V_{SETI}(V)}{R_{SETI}(k\Omega)} \times C_{IRATIO} = \frac{V_{SETI}(V)}{V_{RI}(V)} \times I_{LIM}$$

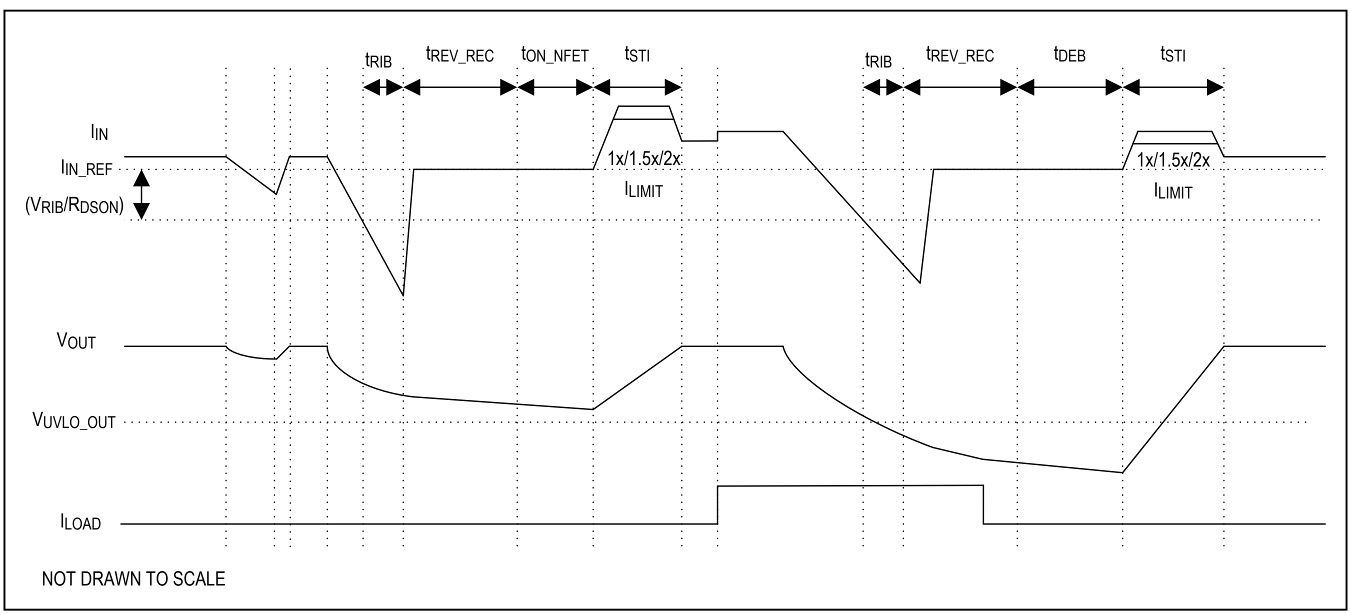


Figure 6. Reverse-Current Timing Diagram

IN Bypass Capacitor

In applications in which an external pFET is not used, connect a minimum of 1µF capacitor from IN to GND to limit the input voltage drop during momentary output short-circuit conditions. Larger capacitor values further reduce the voltage droop at the input caused by load transients. In applications in which an external pFET is used, a 4.7µF capacitor is placed at the drain of the pFET, and the capacitor at IN is reduced to 10nF (100nF max).

Hot Plug-In

In many power applications, an input filtering capacitor is required to lower the radiated emission and enhance the ESD capability, etc. In hot-plug applications, parasitic cable inductance, along with the input capacitor, causes overshoot and ringing when a powered cable is suddenly connected to the input terminal. This effect causes the protection device to see almost twice the applied voltage. An input voltage of 24V can easily exceed 40V due to ringing. The devices contain internal protection against hot-plug input transients on the IN pins, with slew rate up to 30V/µs. However, in the case where the harsh industrial EMC test is required, use a transient voltage suppressor (TVS) placed close to the input terminal that is capable of limiting the input surge to 58V.

OUT Capacitance

For stable operation over the full temperature range and over the entire programmable current-limit range, connect a 4.7µF ceramic capacitor from OUT to ground. Other circuits connected to the output of the device may introduce additional capacitance, but it should be noted that excessive output capacitance on the devices can cause faults. If the capacitance is too high, the devices may not be able to charge the capacitor before the startup timeout. Calculate the maximum capacitive load (C_{MAX}) value that can be connected to OUT using the following formula:

$$C_{MAX}(mF) = I_{LIM}(A)\left[\frac{M \times t_{STI}(ms) + t_{STO}(ms)}{V_{IN\_MAX}(V)}\right]$$

where M is the multiplier (1x/1.5x/2x) applied to the current limit during startup. For example, when using MAX14691, if V_{IN_MAX} = 30V, t_{STO} (min) = 1090ms, t_{STI} (min) = 22ms, and I_{LIM} = 3A, C_{MAX} results in the theoretical maximum of 111mF. In this case, any capacitance larger than 111mF will cause a fault condition because the capacitor cannot be charged to a sufficient voltage before t_{STO} has expired. In practical applications, the output capacitor size is limited by the thermal performance of the PCB. Poor thermal design can cause the thermal-foldback current-limiting function of the device to kick in too early, which may further limit the maximum capacitance that can be charged. Therefore, good thermal PCB design is imperative to charge large capacitor banks.

Table 3. Current-Limit Threshold vs. Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT (A)
62.5	0.6
37.5	1.0
25.0	1.5
18.75	2.0
15.0	2.5
12.5	3.0
10.7	3.5
9.375	4.0
8.3	4.5
7.5	5.0
6.82	5.5
6.25	6.0

OUT Freewheeling Diode for Inductive Hard Short to Ground

In applications with a highly inductive load, a freewheeling diode is required between the OUT terminal and GND. This protects the device from inductive kickback that occurs during short-to-ground events.

PCB Layout Recommendations

To optimize the switch response to output short-circuit conditions, it is important to reduce the effect of undesirable parasitic inductance by keeping all traces as short as possible. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During steady-state operation, the power dissipation is typically low and the package temperature change is usually minimal.

PCB layout designs need to meet two challenges: high-current input and output paths and important heat dissipation.

Heat Dissipation

Maxim recommends the use of 2oz copper on FR4 isolator in a four-layer configuration.

The layer stack needs to be top (routing), GND (plane), power (plane, connected to V_{OUT}), and bottom (routing), in this order, from top to bottom.

Install the IC on an exposed pad landing of minimum 100 x 100 mils, with at least five through vias to the GND plane. The vias should be 32mils in diameter, with a 16mils plated hole. The hole plating needs to be at least 0.5oz copper.

Provide a minimum of 1in x 1in area of copper plane on all four layers. It is important to remember that the inner planes do not contribute much to heat dissipation, due to FR4 isolation, but are important from an electrical point of view.

If possible, keep the top and bottom copper areas clear of solder mask, as this will greatly improve heat dissipation.

Use a similarly large copper area connected directly to the OUT pins. A dimension of 1in x 1in is also recommended. This might look oversized for current path requirements, but is essential for heat dissipation. Keep in mind that heat is generated at the drain junction of the internal nMOS pass FET, which is then eliminated through the five OUT pins and needs to be dissipated on this same copper area.

Current Path Requirements

Connect all five IN pins to a copper area that is at least 150mils wide. Using 2oz copper may reduce this requirement to 100mils. Remember to provide the same copper trace width on the source connection, when using the external pMOS pass FET (with the drain connected to the IN pins).

Use extreme caution when placing the decoupling capacitors to the IN and OUT pins. The tendency to go as close as possible to the IC pins might interfere with the minimum requirement of the trace width above.

It is important to note that the return load current does not flow through the IC. Therefore, it is important to provide an external ground trace of at least the same width as the input/output one.

Maxim recommends the use of a GND plane. Connect the input and output grounds to this plane using at least four plated vias each. The vias should be 84mils in diameter (or 60mils x 60mils, if square), with a 35mils plated hole.

Additional Information

For more information on heat dissipation, see the *IC Application Section* on **http://www.maximintegrated.com**.

ESD Test Conditions

The devices are specified for ±15kV (HBM) ESD on IN when IN is bypassed to ground with a 1μF, low ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) (typ) ESD on IN. All pins have ±2kV (HBM) ESD protection. In applications in which an external pFET is used, see the *IN Bypass Capacitor* section.

HBM ESD Protection

Figure 7 shows the Human Body Model and Figure 8 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

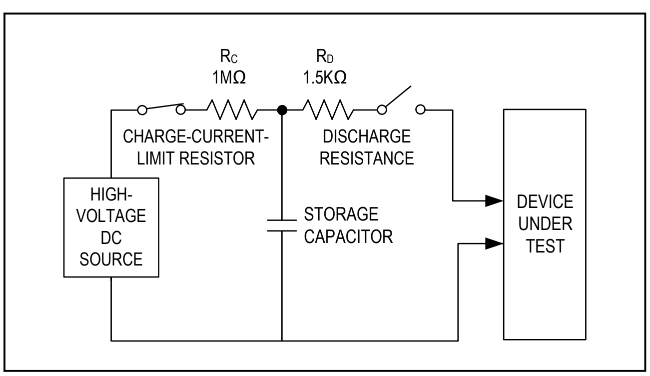


Figure 7. Human Body ESD Test Model

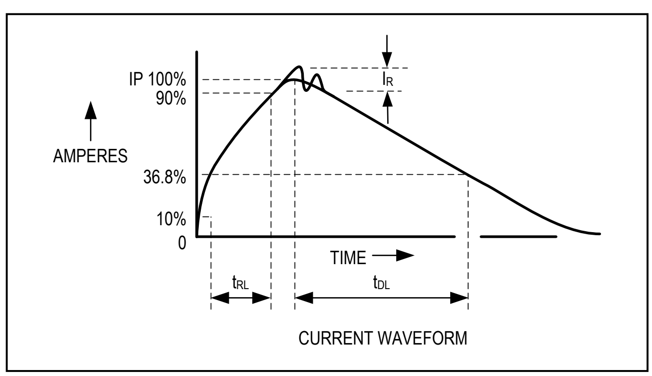
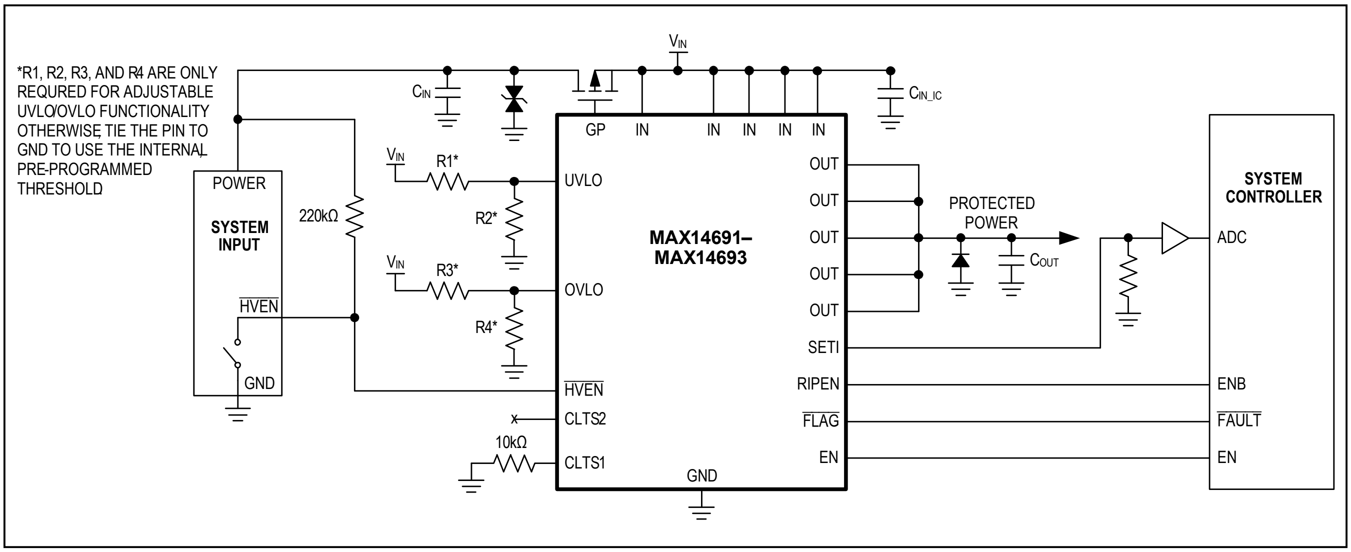


Figure 8. Human Body Current Waveform

Typical Application Circuit



Ordering Information

PART	INITIAL CURRENT LIMIT	TEMP RANGE	PIN-PACKAGE
MAX14691ATP+T	1.0x	-40°C to +125°C	20 TQFN-EP*
MAX14692ATP+T	1.5x	-40°C to +125°C	20 TQFN-EP*
MAX14693ATP+T	2.0x	-40°C to +125°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+5C	21-0140	90-0010