High-Accuracy, Surge-Protected Overvoltage Protectors

General Description

The MAX14699 overvoltage protection (OVP) device features a low 38mΩ (typ) on-resistance (R_{ON}) internal FET and protects low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the device from surges up to +100V. The MAX14699 features a 100ns (typ) overvoltage response time to minimize voltage rise on OUT during an overvoltage event. When the input voltage exceeds the overvoltage threshold, the internal FET is quickly turned off to prevent damage to the protected downstream components.

The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the MAX14699 automatically selects the accurate internal trip threshold. The internal overvoltage threshold (OVLO) is preset to 13.75V (typ). The device features an open-drain $\overline{ACOK}$ output, indicating a stable supply between minimum supply voltage and V_{OVLO}. The MAX14699 is protected against overcurrent events by an internal thermal shutdown.

The MAX14699 is offered in a small, 12-bump WLP package and operates over the -40°C to +85°C extended temperature range.

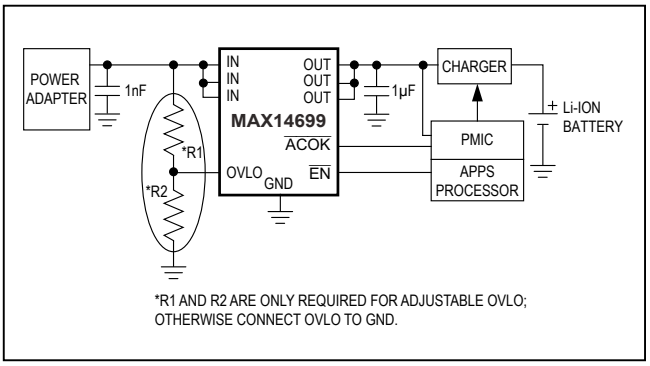
Applications

- Smartphones
- Tablet PCs
- Portable Media Players

Benefits and Features

- Protects High-Power Portable Devices
  - Wide Operating Input Voltage Protection from +2.1V to +28V
  - 4.5A Continuous Current Capability
  - Integrated 38mΩ (typ) n-Channel MOSFET Switch
  - Fast 100ns (typ) Response Time
- Flexible Design
  - Adjustable Overvoltage-Protection Trip Level
  - Wide Adjustable OVLO Threshold Range from +4V to +20V
  - Preset Internal Accurate OVLO Threshold: 13.75V
  - Microphone Mode for Microphone Signals on IN
- Additional Protection Features Increase System Reliability
  - Surge Immunity to +100V
  - Soft-Start to Minimize In-Rush Current
  - Internal 21ms Startup Debounce
  - Thermal-Shutdown Protection
- Minimize PCB Area
  - 12-Bump WLP (1.3mm x 2mm) Package
- -40°C to +85°C Operating Temperature Range

Typical Application Circuit



Ordering Information **appears at end of data sheet.**

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Absolute Maximum Ratings

(All voltages referenced to GND.)
IN (Note 1)..... -0.3V to +29V
OUT.....-0.3V to (V_{IN} + 0.3V)
OVLO, $\overline{ACOK}$ .....-0.3V to +14V
$\overline{EN}$ .....-0.3V to +6V
Continuous IN, OUT Current.....4.5A
(Note: Continuous Current Limited by Thermal Design)
Peak IN, OUT Current (10ms).....8A

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 13.7mW/°C above +70°C).....1095mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....73°C/W

Note 1: Survives burst pulse up to 100V with 2Ω series resistance.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +2.1V to +28V, C_{IN} = 1nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5.0V, I_{IN} ≤ 3A, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		2.1		28	V
Input Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 10mA, T_A = +25°C		33		V
Input Supply Current	I_{IN}	V_{IN} = 5V, V_{IN} < V_{OVLO}		116	180	µA
OVP						
Internal Overvoltage Trip Level	V_{IN_OVLO}	V_{IN} rising, T_A = +25°C	13.70	13.75	13.80	V
		V_{IN} falling	13.50			
OVLO Set Threshold	V_{OVLO_TH}		1.18	1.204	1.22	V
Adjustable OVLO Threshold Range			4		20	V
External OVLO Select Threshold	V_{OVLO_SELECT}		0.2		0.3	V

Electrical Characteristics (continued)

(V_{IN} = +2.1V to +28V, C_{IN} = 1nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5.0V, I_{IN} ≤ 3A, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OVLO Switch On-Resistance	R_{ON}	V_{IN} = 5V, I_{OUT} = 1A, T_A = +25°C		38	53	mΩ
OUT Leakage Current	I_{OUT_LEAK}	V_{IN} = V_{IN_OVLO}, V_{OUT} = 5V		7.6	12	µA
OUT Load Capacitance	C_{OUT}	V_{IN} = 5V			100	µF
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO} = V_{OVLO_TH}	-100		+100	nA
IN Leakage Voltage by OVLO	V_{IN_LEAK}	V_{OVLO} = 14V, V_{IN} = unconnected, R_{OVLO} = 1MΩ			0.25	V
$\overline{EN}$						
$\overline{EN}$ Input Low Current	$I_{\overline{EN}}$	0V < $V_{\overline{EN}}$ < 5.5V	-1	0	+1	µA
$\overline{EN}$ Input Voltage High	V_{IH}		1.4			V
$\overline{EN}$ Input Voltage Low	V_{IL}				0.4	V
DIGITAL SIGNALS ($\overline{ACOK}$)						
$\overline{ACOK}$ Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA			0.4	V
$\overline{ACOK}$ Leakage Current	I_{ACOK_LEAK}	$V_{I/O}$ = 3.3V, $\overline{ACOK}$ deasserted	-1		+1	µA
TIMING CHARACTERISTICS (Figure 1)						
Debounce Time	t_{DEB}	Time from 2.1V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 10% of V_{IN}		21		ms
Soft-Start Time	t_{SS}	V_{OUT} = 10% of V_{IN} to soft-start off		1.26		ms
Switch Turn-Off Response Time	t_{OFF_RES}	V_{IN} > V_{OVLO} to V_{OUT} stop rising		100		ns
THERMAL PROTECTION						
Thermal Shutdown				150		°C
Thermal-Shutdown Hysteresis				20		°C
ESD PROTECTION						
IN		Human Body Model		±15		kV
		IEC 61000-4-2 Air-Gap		±15		
		IEC 61000-4-2 Contact Discharge		±8		
All Pins		Human Body Model		±2		kV

Note 3: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design.

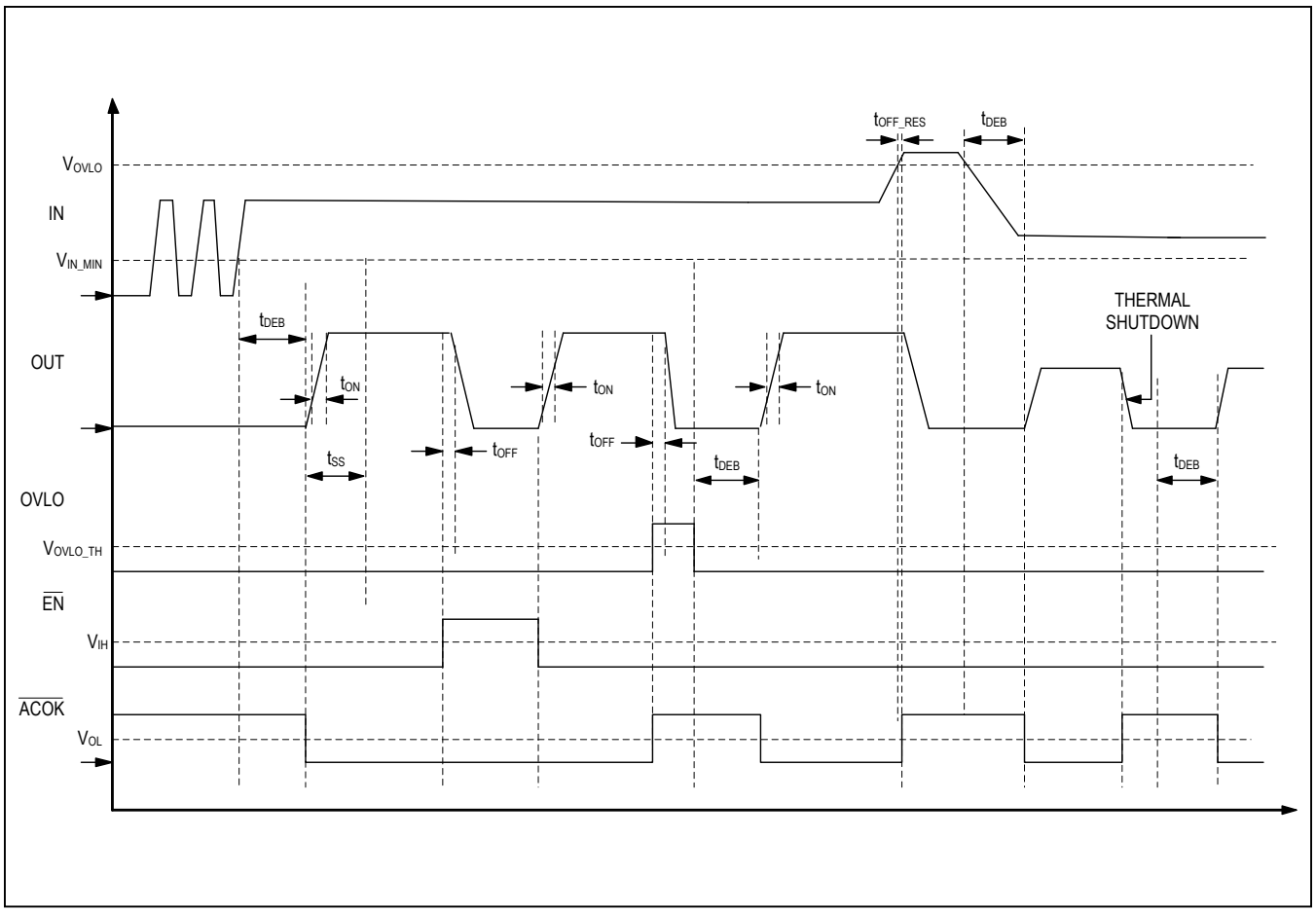
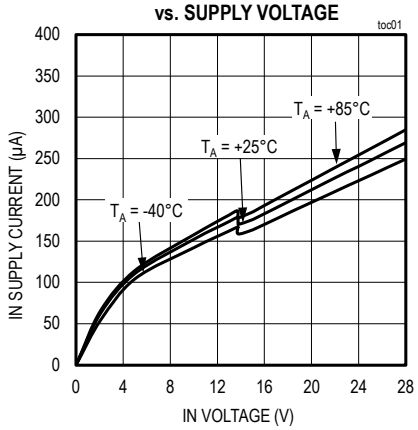


Figure 1. Timing Diagram

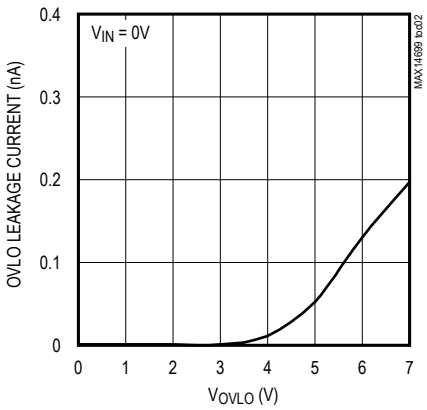
Typical Operating Characteristics

(V_{IN} = +5.0V, C_{IN} = 1nF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

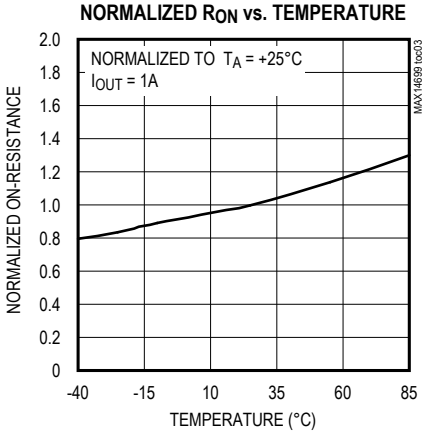
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



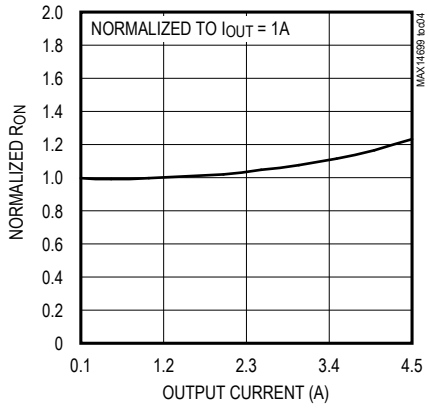
OVLO LEAKAGE CURRENT vs. V_{OVLO}



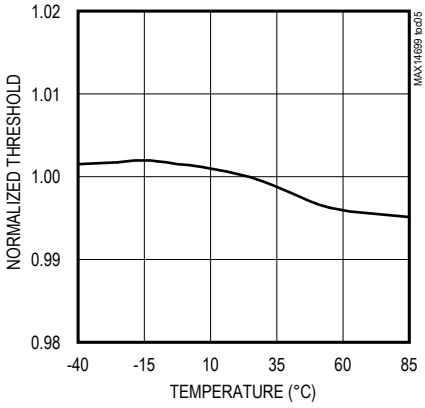
NORMALIZED R_{ON} vs. TEMPERATURE



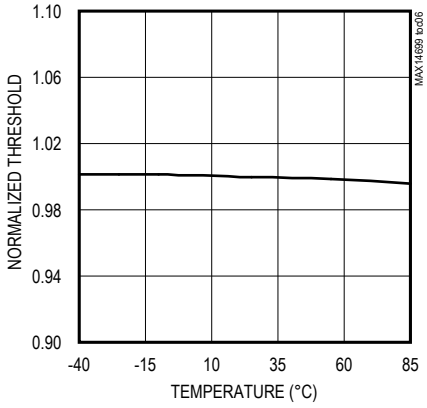
NORMALIZED ON-RESISTANCER_{ON} vs. OUTPUT CURRENT



NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



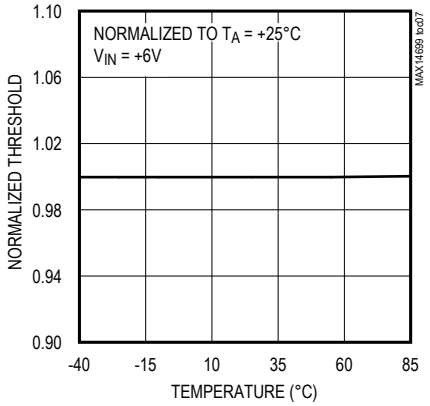
NORMALIZED EXTERNAL OVLO SET THRESHOLD vs. TEMPERATURE



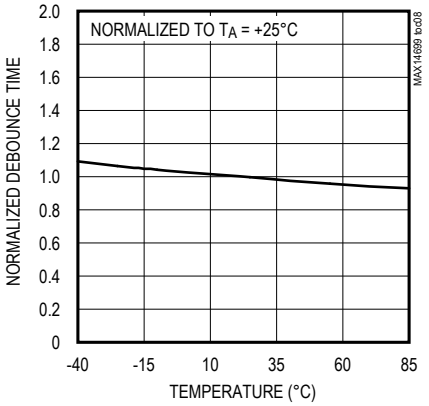
Typical Operating Characteristics (continued)

(V_{IN} = +5.0V, C_{IN} = 1nF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

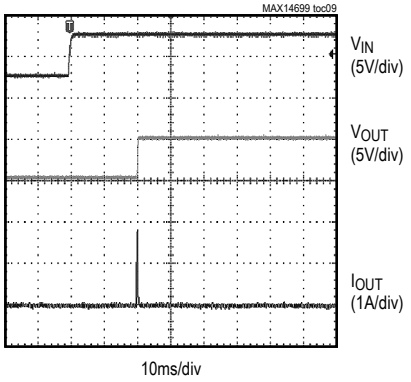
NORMALIZED EXTERNAL OVLO SELECT THRESHOLD vs. TEMPERATURE



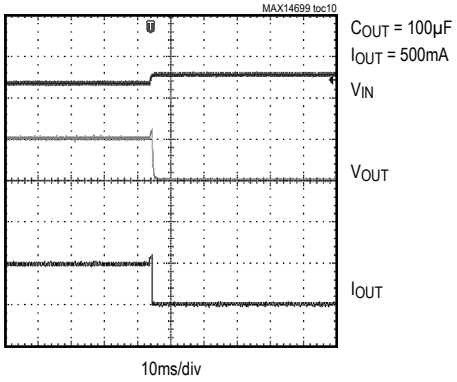
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



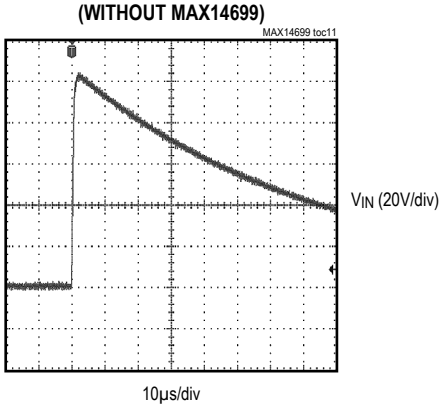
POWER-UP RESPONSE (C_{OUT} = 100µF)



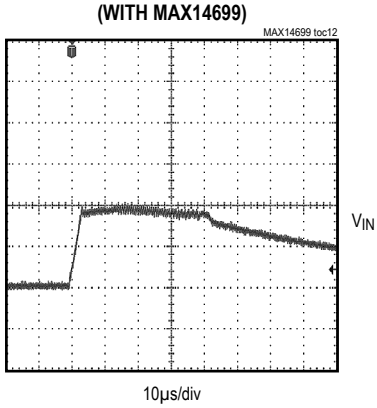
OVERVOLTAGE FAULT RESPONSE



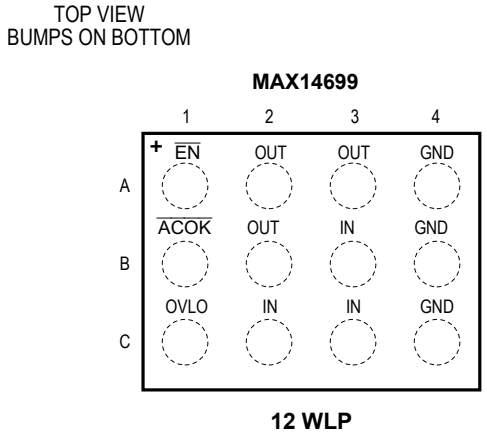
100V SURGE TEST WAVEFORM (WITHOUT MAX14699)



100V SURGE TEST WAVEFORM (WITH MAX14699)



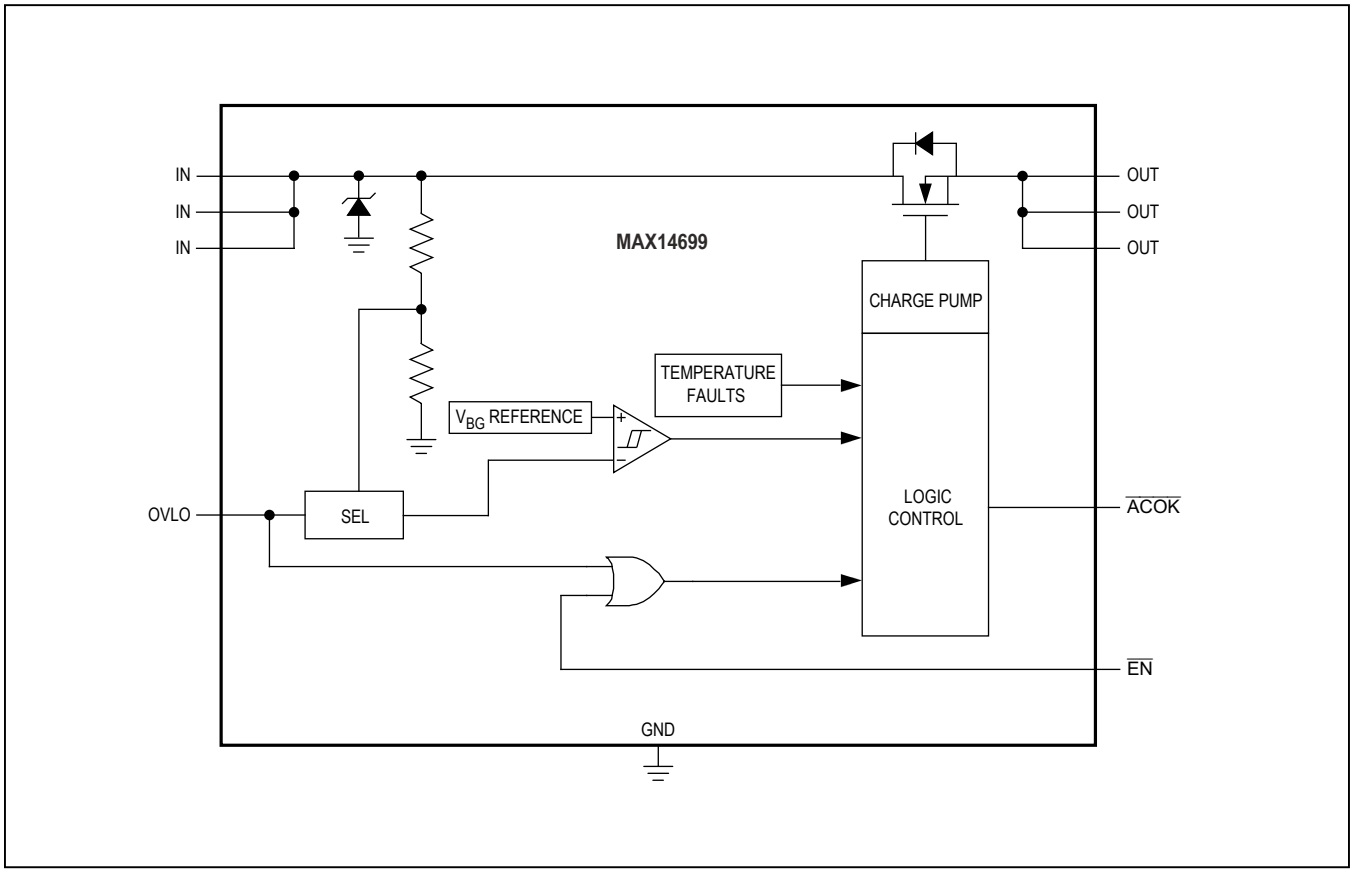
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	$\overline{EN}$	Active-Low Enable Input
A2, A3, B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.
B1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.
B3, C2, C3	IN	Voltage Input. Bypass IN with a 1nF ceramic capacitor as close as possible to the device to obtain ±15kV Human Body Model (HBM) ESD protection. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

Functional Diagram



Detailed Description

The MAX14699 overvoltage protection (OVP) device features a low 38mΩ (typ) on-resistance (R_{ON}) internal FET and protects low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the device from surges up to +100V with minimal voltage rise on OUT. When the input voltage exceeds the overvoltage threshold, the internal FET is quickly turned off to prevent damage to the protected downstream components.

The overvoltage protection threshold can be adjusted with optional external resistors to any threshold between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the MAX14699 automatically selects the accurate internal trip threshold. The internal overvoltage threshold (OVLO) is preset to 13.75V (typ). The MAX14699 is also protected against overcurrent events by an internal thermal shutdown.

Device Operation

The device contains timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when $V_{IN} < V_{IN\_OVLO}$, if internal trip thresholds are used, or when $V_{IN} < V_{OVLO\_TH}$, if external trip thresholds are used. The charge-pump startup, which occurs after a 21ms debounce delay, turns the internal FET on (see the *Functional Diagram*). After the debounce time, soft-start limits the FET inrush current for 1.26ms (typ). At any time, if V_{IN} rises above the OVLO threshold, OUT is disconnected from IN.

Internal Switch

The MAX14699 incorporates an internal FET with a 38mΩ (typ) R_{ON} connecting IN and OUT. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Overvoltage Lockout (OVLO)

The MAX14699 has a 13.75V (typ) overvoltage threshold. For voltages on IN above this threshold, the internal FET is turned off and OUT is disconnected from IN.

Thermal-Shutdown Protection

The MAX14699 contains thermal-shutdown circuitry. The internal FET turns off when the junction temperature exceeds +150°C (typ). The device exits thermal shutdown after the junction temperature cools by +20°C (typ).

Applications Information

IN Bypass Capacitor

For most applications, bypass IN to GND with a 1nF ceramic capacitor as close as possible to the device to reduce EMI. There is no capacitor required at IN for ESD. If the power source has significant inductance due to long lead length, the device takes care of overshoots due to the LC tank circuit and provides protection as necessary to prevent exceeding the +29V absolute maximum rating on IN.

OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the MAX14699 to charge an output capacitor up to 100µF without turning off due to an overcurrent condition.

External OVLO Adjustment Functionality

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor-divider. R_1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_THRESH}, and R_1 are known, R_2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_THRESH} \times \left[1 + \frac{R_1}{R_2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider. A pure external resistor-divider can slow down the OVLO intervention time, reducing the surge protection voltage. A compensated RC divider must be used to ensure high-speed OVLO. The capacitor can be selected according to the formula:

$$C_1 > 5 \times t_R \times \left[\frac{R_1 + R_2}{R_1 \times R_2}\right]$$

where t_R is the rise time of the worst-case input transient as measured from the beginning of the rising edge to the time at which V_{IN_OVLO} is reached. See Figure 2.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX14699 is specified for ±15kV (HBM) typical ESD resistance on IN without any input capacitor.

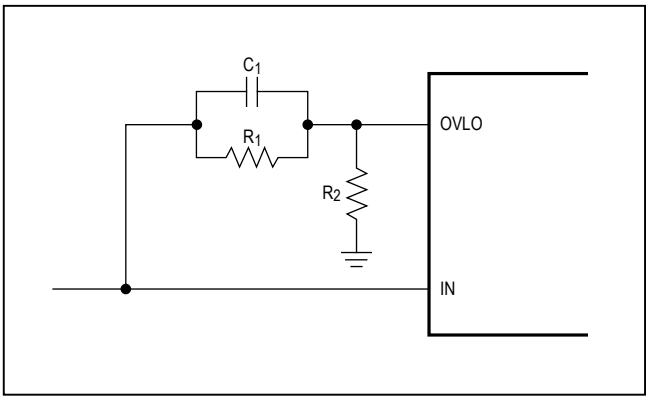


Figure 2. External OVLO Set Circuit

HBM ESD Protection

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 5 shows the IEC 61000-4-2 model, and Figure 6 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

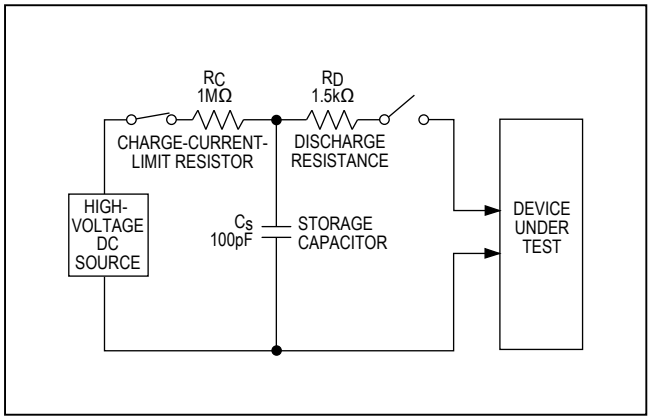


Figure 3. Human Body ESD Test Model

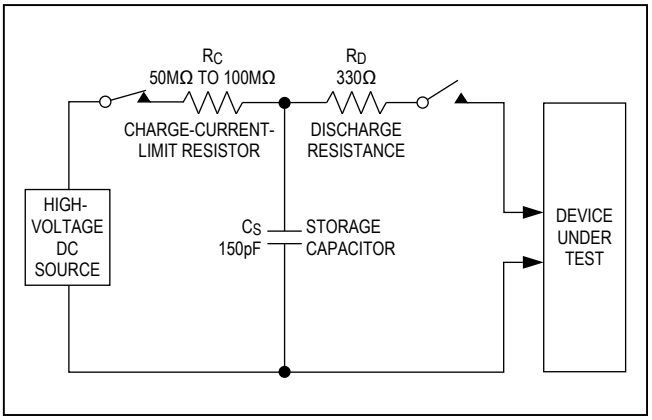


Figure 5. IEC 61000-4-2 ESD Test Model

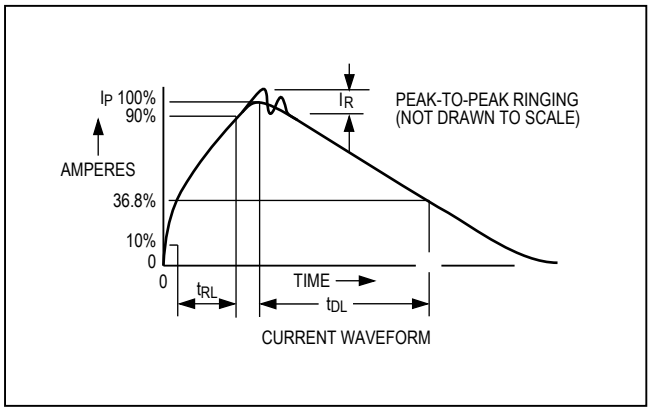


Figure 4. Human Body Current Waveform

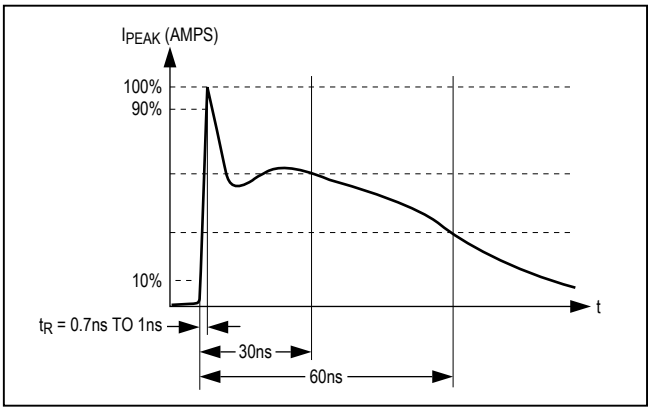


Figure 6. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	OVLO (V)
MAX14699EWC+T	12 WLP	ADC	13.75

Note: *All devices are specified over the -40°C to +85°C temperature range.*

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 WLP	W121F2+1	**21-0542**	Refer to **Application Note 1891**