MAX1471

315MHz/434MHz Low-Power, 3V/5V ASK/FSK Superheterodyne Receiver

General Description

The MAX1471 low-power, CMOS, superheterodyne, RF dual-channel receiver is designed to receive both amplitude-shift-keyed (ASK) and frequency-shift-keyed (FSK) data without reconfiguring the device or introducing any time delay normally associated with changing modulation schemes. The MAX1471 requires few external components to realize a complete wireless RF digital data receiver for the 300MHz to 450MHz ISM bands.

The MAX1471 includes all the active components required in a superheterodyne receiver including: a lownoise amplifier (LNA), an image-reject (IR) mixer, a fully integrated phase-locked loop (PLL), local oscillator (LO), 10.7MHz IF limiting amplifier with received-signal strength indicator (RSSI), low-noise FM demodulator, and a 3V voltage regulator. Differential peak-detecting data demodulators are included for both the FSK and ASK analog baseband data recovery. The MAX1471 includes a discontinuous receive (DRX) mode for lowpower operation, which is configured through a serial interface bus.

The MAX1471 is available in a 32-pin thin QFN package and is specified over the automotive -40°C to +125°C temperature range.

Applications

- Automotive Remote Keyless Entry (RKE)
- Tire Pressure Monitoring Systems
- Garage Door Openers
- Wireless Sensors
- Wireless Keys
- Security Systems
- Medical Systems
- Home Automation
- Local Telemetry Systems

Benefits and Features

- ASK and FSK Demodulated Data on Separate Outputs
- Specified over Automotive -40°C to +125°C Temperature Range
- Low Operating Supply Voltage Down to 2.4V
- On-Chip 3V Regulator for 5V Operation
- Low Operating Supply Current
  - 7mA Continuous Receive Mode
  - 1.1µA Deep-Sleep Mode
- Discontinuous Receive (DRX) Low-Power Management
- Fast-On Startup Feature < 250µs
- Integrated PLL, VCO, and Loop Filter
- 45dB Integrated Image Rejection
- RF Input Sensitivity*
  - ASK: -114dBm
  - FSK: -108dBm
- Selectable IF BW with External Filter
- Programmable Through Serial User Interface
- RSSI Output and High Dynamic Range with AGC
- AEC-Q100 Qualified (MAX1471ATJ/V+ Only)

**0.2% BER, 4kbps, Manchester-encoded data, 280kHz IF BW*

19-3272; Rev 5; 7/17

maxim integrated™

Absolute Maximum Ratings

High-Voltage Supply, HVIN to DGND ..... -0.3V, +6.0V
Low-Voltage Supply, AVDD and DVDD to AGND ... -0.3V, +4.0V
SCLK, DIO, $\overline{CS}$, ADATA,
FDATA..... (DGND - 0.3V) to (HVIN + 0.3V)
All Other Pins ..... (AGND - 0.3V) to (AVDD + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C above +70°C)...1702mW

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434 MHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Supply Voltage (5V)	HVIN	AVDD and DVDD unconnected from HVIN, but connected together		4.5	5.0	5.5	V
Supply Voltage (3V)	V_{DD}	HVIN, AVDD, and DVDD connected to power supply		2.4	3.0	3.6	V
Supply Current	I_{DD}	T_A < +85ºC	Operating		7.0	8.4	mA
			Polling duty cycle: 10% duty cycle		705	855	µA
			DRX mode OFF current		5.0	14.2	
			Deep-sleep current		1.1	7.1	
		T_A < +105ºC (Note 2)	Operating			8.5	mA
			Polling duty cycle: 10% duty cycle			865	µA
			DRX mode OFF current			15.5	
			Deep-sleep current			13.4	
		T_A < +125ºC (Note 2)	Operating			8.6	mA
			Polling duty cycle: 10% duty cycle			900	µA
			DRX mode OFF current			44.1	
			Deep-sleep current			36.4	
Startup Time	t_{ON}	Time for final signal detection, does not include baseband filter settling (Note 2)			200	250	µs
DIGITAL OUTPUTS (DIO, ADATA, FDATA)							
Output High Voltage	V_{OH}	I_{SOURCE} = 250µA (Note 2)		V_{HVIN} - 0.15			V
Output Low Voltage	V_{OL}	I_{SINK} = 250µA (Note 2)			0.15		V
DIGITAL INPUTS ($\overline{CS}$, DIO, SCLK)							
Input High Threshold	V_{IH}			0.9 x V_{HVIN}			V
Input Low Threshold	V_{IL}			.		0.1 x V_{HVIN}	V

Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434 MHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-High Leakage Current	I_{IH}	(Note 2)			-20	µA
Input-Low Leakage Current	I_{IL}	(Note 2)			20	µA
Input Capacitance	C_{IN}	(Note 2)			2.0	pF
VOLTAGE REGULATOR						
Output Voltage	V_{REG}	V_{HVIN} = 5.0V, I_{LOAD} = 7.0mA		3.0		V

AC Electrical Characteristics

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434 MHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Receiver Sensitivity	RF_{IN}	0.2% BER, 4kbps Manchester Code, 280kHz IF BW, 50Ω	ASK		-114		dBm
			FSK		-108		
Maximum Receiver Input Power Level	RF_{MAX}				0		dBm
Receiver Input Frequency Range	f_{RF}			300		450	MHz
Receiver Image Rejection	IR	(Note 3)			45		dB
LNA/MIXER (Note 4)							
LNA Input Impedance	Z_{IN_LNA}	Normalized to 50Ω	f_{RF} = 315MHz		1 - j4.7		
			f_{RF} = 434MHz		1 - j3.4		
Voltage Conversion Gain (High-Gain Mode)					47.5		dB
Input-Referred 3rd-Order Intercept Point (High-Gain Mode)					-38		dBm
Voltage Conversion Gain (Low-Gain Mode)					12.2		dB
Input-Referred 3rd-Order Intercept Point (Low-Gain Mode)					-5		dBm
LO Signal Feedthrough to Antenna					-90		dBm
Mixer Output Impedance	Z_{OUT_MIX}				330		Ω
IF							
Input Impedance	Z_{IN_IF}				330		Ω
Operating Frequency	f_{IF}				10.7		MHz
3dB Bandwidth					10		MHz
FM DEMODULATOR							
Demodulator Gain	G_{FM}				2.2		mV/kHz

AC Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +2.4V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434 MHz, T_A = +25°C, unless otherwise noted.) (Note 1)

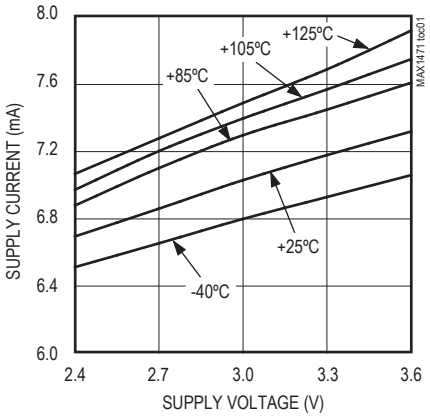
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG BASEBAND						
Maximum Data Filter Bandwidth	BW_{DF}			50		kHz
Maximum Data Slicer Bandwidth	BW_{DS}			100		kHz
Maximum Peak Detector Bandwidth	BW_{PD}			50		kHz
Maximum Data Rate		Manchester coded		33		kbps
		Nonreturn to zero (NRZ)		66		
CRYSTAL OSCILLATOR						
Crystal Frequency	f_{XTAL}		9.04		13.728	MHz
Frequency Pulling by V_{DD}				3		ppm/V
Crystal Load Capacitance				3		pF
DIGITAL INTERFACE TIMING (see Figure 8)						
Minimum SCLK Setup to Falling Edge of $\overline{CS}$	t_{SC}			30		ns
Minimum $\overline{CS}$ Falling Edge to SCLK Rising-Edge Setup Time	t_{CSS}			30		ns
Minimum $\overline{CS}$ Idle Time	t_{CSI}			125		ns
Minimum $\overline{CS}$ Period	t_{CS}			2.125		µs
Maximum SCLK Falling Edge to Data Valid Delay	t_{DO}			80		ns
Minimum Data Valid to SCLK Rising-Edge Setup Time	t_{DS}			30		ns
Minimum Data Valid to SCLK Rising-Edge Hold Time	t_{DH}			30		ns
Minimum SCLK High Pulse Width	t_{CH}			100		ns
Minimum SCLK Low Pulse Width	t_{CL}			100		ns
Minimum $\overline{CS}$ Rising Edge to SCLK Rising-Edge Hold Time	t_{CSH}			30		ns
Maximum $\overline{CS}$ Falling Edge to Output Enable Time	t_{DV}			25		ns
Maximum $\overline{CS}$ Rising Edge to Output Disable Time	t_{TR}			25		ns

Note 1: Production tested at T_A = +85°C. Guaranteed by design and characterization over entire temperature range.
Note 2: Guaranteed by design and characterization. Not production tested.
Note 3: The oscillator register (0x3) is set to the nearest integer result of f_{XTAL} / 100kHz (see the *Oscillator Frequency Register* section).
Note 4: Input impedance is measured at the LNAIN pin. Note that the impedance at 315MHz includes the 15nH inductive degeneration from the LNA source to ground. The impedance at 434MHz includes a 10nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is 50Ω in series with 2.2pF. The voltage conversion gain is measured with the LNA input matching inductor, the degeneration inductor, and the LNA/mixer resonator in place, and does not include the IF filter insertion loss.

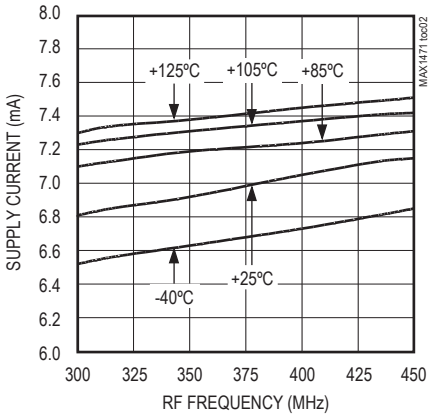
Typical Operating Characteristics

(*Typical Application Circuit*, $V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V$, $f_{RF} = 434MHz$, $T_A = +25°C$, unless otherwise noted.)

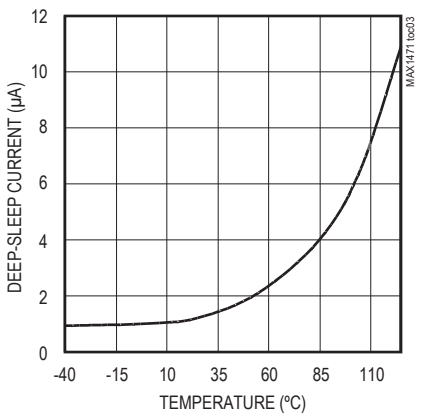
SUPPLY CURRENT vs. SUPPLY VOLTAGE



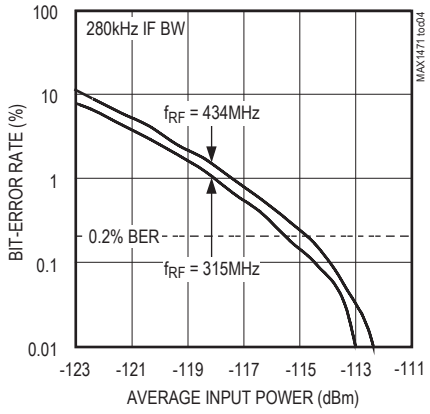
SUPPLY CURRENT vs. RF FREQUENCY



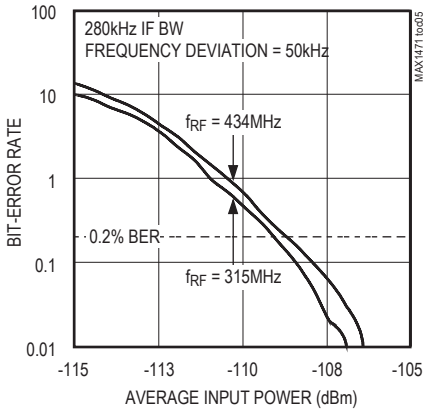
DEEP-SLEEP CURRENT vs. TEMPERATURE



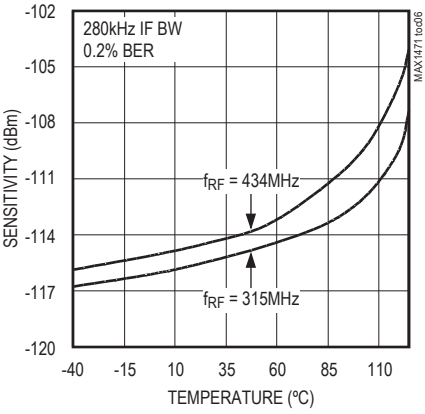
BIT-ERROR RATE vs. AVERAGE INPUT POWER (ASK DATA)



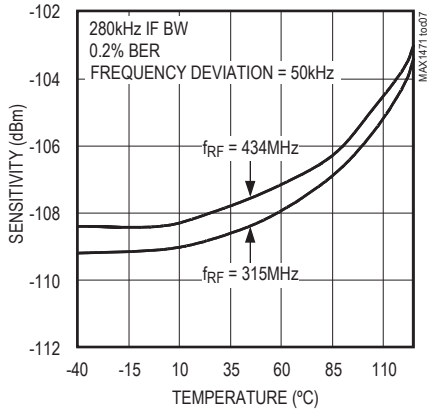
BIT-ERROR RATE vs. AVERAGE INPUT POWER (FSK DATA)



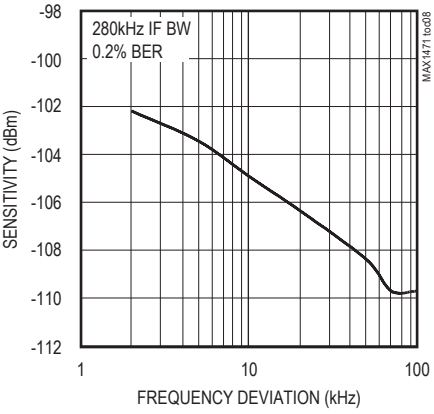
SENSITIVITY vs. TEMPERATURE (ASK DATA)



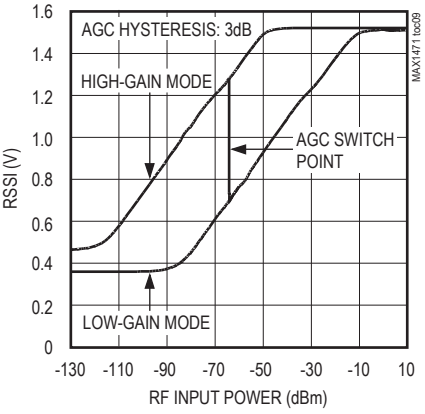
SENSITIVITY vs. TEMPERATURE (FSK DATA)



SENSITIVITY vs. FREQUENCY DEVIATION (FSK DATA)



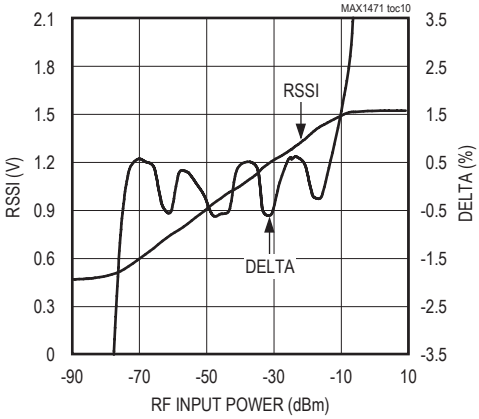
RSSI vs. RF INPUT POWER



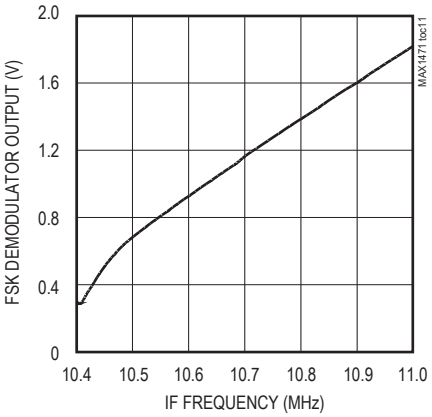
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434MHz, T_A = +25°C, unless otherwise noted.)

RSSI AND DELTA vs. IF INPUT POWER



FSK DEMODULATOR OUTPUT vs. IF FREQUENCY



SYSTEM VOLTAGE GAIN vs. IF FREQUENCY

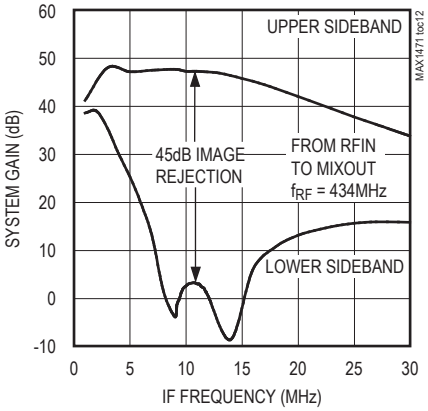
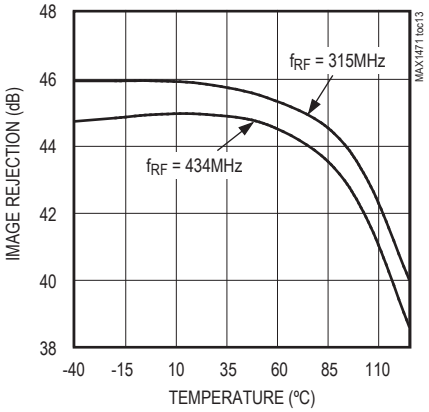
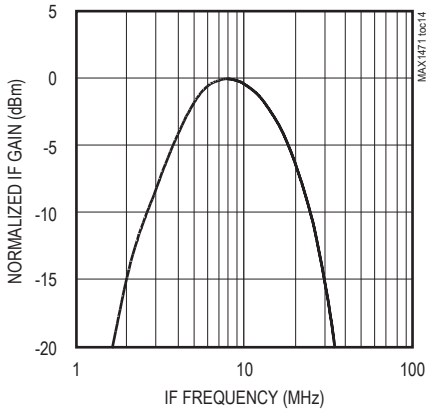


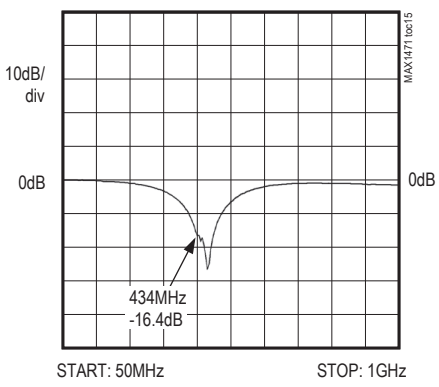
IMAGE REJECTION vs. TEMPERATURE



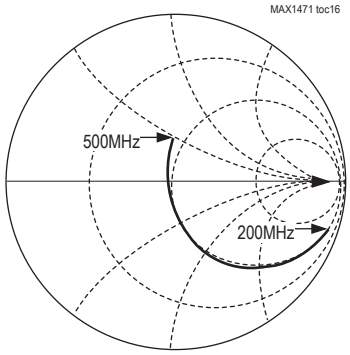
NORMALIZED IF GAIN vs. IF FREQUENCY



S11 LOG-MAGNITUDE PLOT WITH MATCHING NETWORK OF RFIN (434MHz)



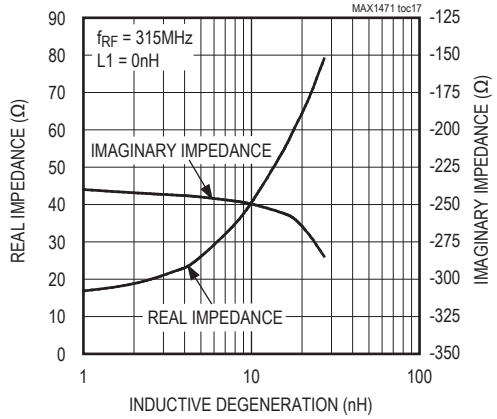
S11 SMITH CHART OF RFIN (434MHz)



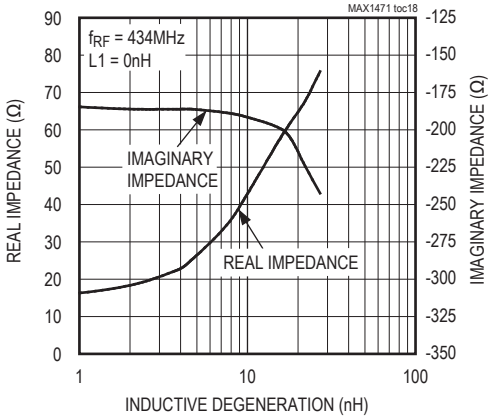
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{AVDD} = V_{DVDD} = V_{HVIN} = +3.0V, f_{RF} = 434MHz, T_A = +25°C, unless otherwise noted.)

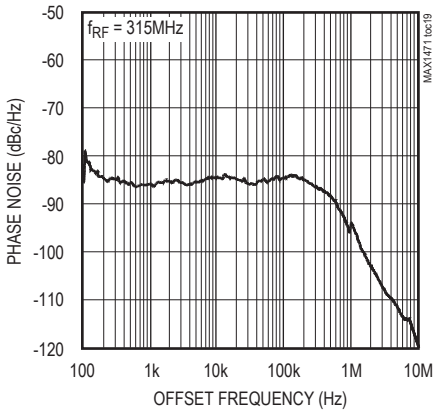
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



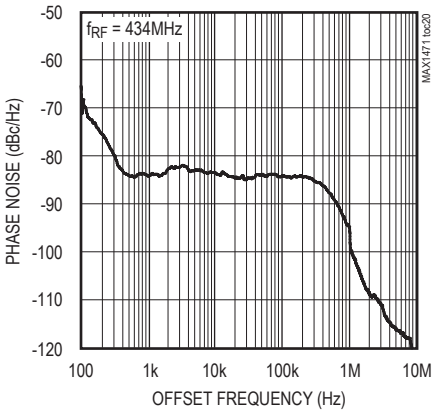
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



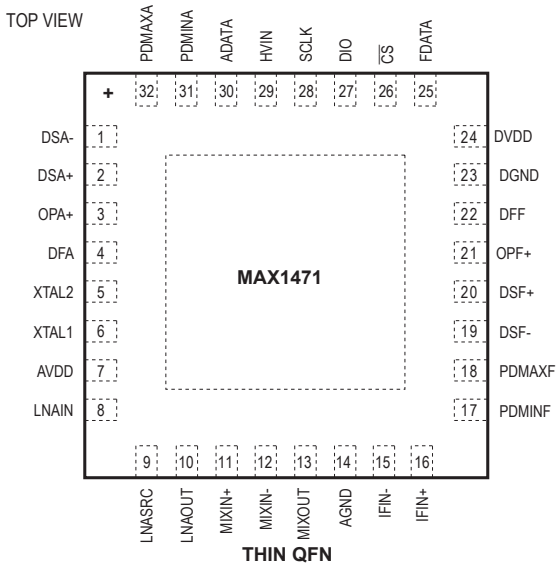
PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY



Pin Configuration



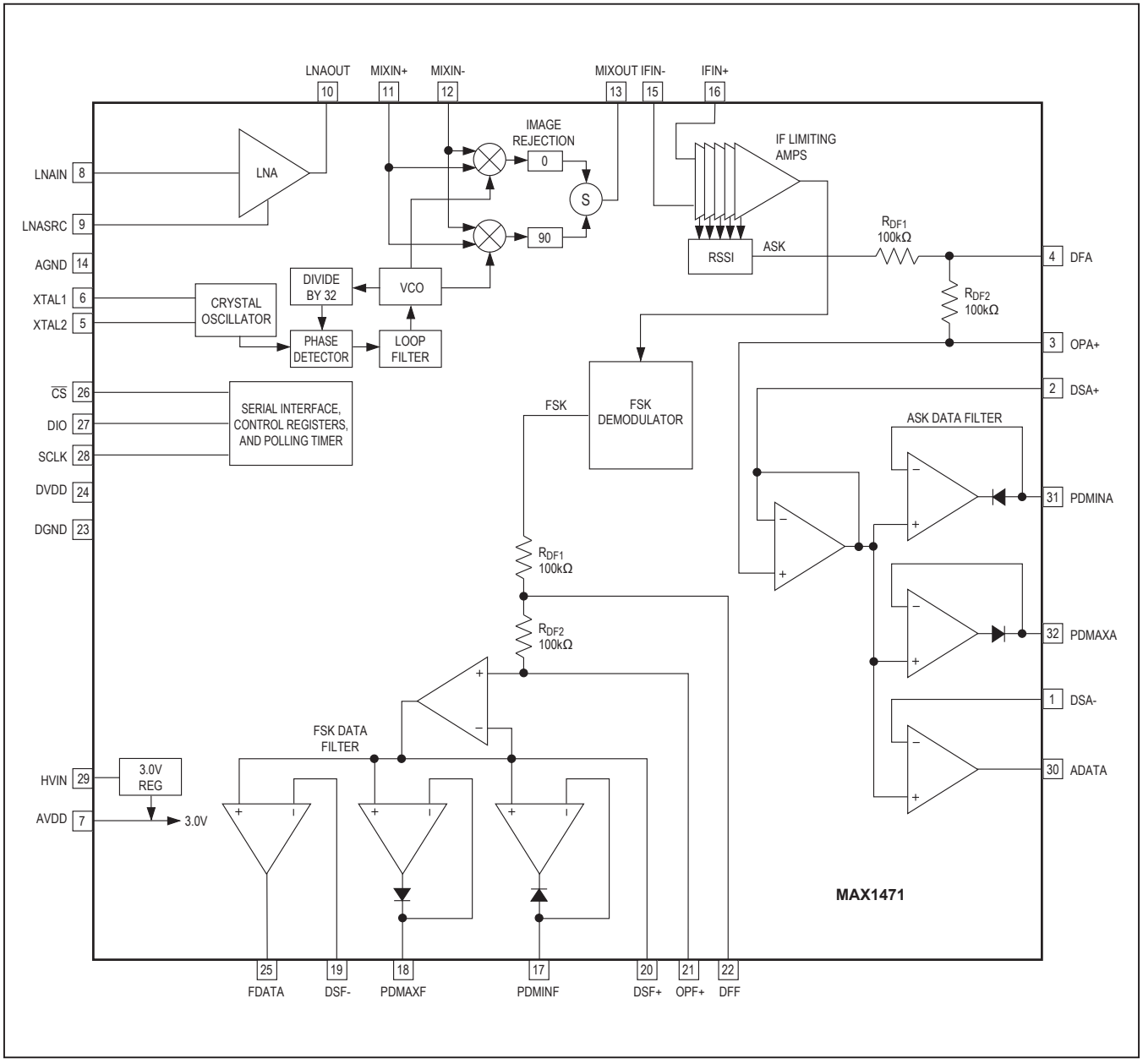
Pin Description

PIN	NAME	FUNCTION
1	DSA-	Inverting Data Slicer Input for ASK Data
2	DSA+	Noninverting Data Slicer Input for ASK Data
3	OPA+	Noninverting Op-Amp Input for the ASK Sallen-Key Data Filter
4	DFA	Data-Filter Feedback Node. Input for the feedback of the ASK Sallen-Key data filter.
5	XTAL2	2nd Crystal Input
6	XTAL1	1st Crystal Input
7	AVDD	Analog Power-Supply Voltage for RF Sections. AVDD is connected to an on-chip +3.0V low-dropout regulator. Decouple to AGND with a 0.1µF capacitor.
8	LNAIN	Low-Noise Amplifier Input
9	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect an inductor to AGND to set LNA input impedance.
10	LNAOUT	Low-Noise Amplifier Output. Connect to mixer through an LC tank filter.
11	MIXIN+	Differential Mixer Input. Must be AC-coupled to driving input.
12	MIXIN-	Differential Mixer Input. Bypass to AGND with a capacitor.
13	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz IF filter.
14	AGND	Analog Ground
15	IFIN-	Differential 330Ω IF Limiter Amplifier Input. Bypass to AGND with a capacitor.
16	IFIN+	Differential 330Ω IF Limiter Amplifier Input. Connect to output of the 10.7MHz IF filter.
17	PDMINF	Minimum-Level Peak Detector for FSK Data. Connect to ground if peak detector is not used. See the *Peak Detectors* section.
18	PDMAXF	Maximum-Level Peak Detector for FSK Data. Connect to ground if peak detector is not used. See the *Peak Detectors* section.
19	DSF-	Inverting Data Slicer Input for FSK Data
20	DSF+	Noninverting Data Slicer Input for FSK Data

Pin Description (continued)

PIN	NAME	FUNCTION
21	OPF+	Noninverting Op-Amp Input for the FSK Sallen-Key Data Filter
22	DFF	Data-Filter Feedback Node. Input for the feedback of the FSK Sallen-Key data filter.
23	DGND	Digital Ground
24	DVDD	Digital Power-Supply Voltage for Digital Sections. Connect to AVDD. Decouple to DGND with a 10nF capacitor.
25	FDATA	Digital Baseband FSK Demodulator Data Output
26	CS	Active-Low Chip-Select Input
27	DIO	Serial Data Input/Output
28	SCLK	Serial Interface Clock Input
29	HVIN	High-Voltage Supply Input. For 3V operation, connect HVIN to AVDD and DVDD.
30	ADATA	Digital Baseband ASK Demod Data Output
31	PDMINA	Minimum-Level Peak Detector for ASK Output. Connect to ground if peak detector is not used. See the *Peak Detectors* section.
32	PDMAXA	Maximum-Level Peak Detector for ASK Output. Connect to ground if peak detector is not used. See the *Peak Detectors* section.
—	EP	Exposed Pad. Connect to ground.

Functional Diagram



Detailed Description

The MAX1471 CMOS superheterodyne receiver and a few external components provide a complete ASK/FSK receive chain from the antenna to the digital output data. Depending on signal power and component selection, data rates as high as 33kbps using Manchester Code (66kbps nonreturn to zero) can be achieved.

The MAX1471 is designed to receive binary FSK or ASK data on a 300MHz to 450MHz carrier. ASK modulation uses a difference in amplitude of the carrier to represent logic 0 and logic 1 data. FSK uses the difference in frequency of the carrier to represent a logic 0 and logic 1.

Low-Noise Amplifier (LNA)

The LNA is a cascode amplifier with off-chip inductive degeneration that achieves approximately 28dB of voltage gain that is dependent on both the antenna-matching network at the LNA input, and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a flexible match to low input impedances such as a PCB trace antenna. A nominal value for this inductor with a 50Ω input impedance is 15nH at 315MHz and 10nH at 434MHz, but the inductance is affected by PCB trace length. See the *Typical Operating Characteristics* to see the relationship between the inductance and input impedance. The inductor can be shorted to ground to increase sensitivity by approximately 1dB, but the input match is not optimized for 50Ω.

The LC tank filter connected to LNAOUT comprises L2 and C9 (see the *Typical Application Circuit*). Select L2 and C9 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where L_{TOTAL} = L2 + $L_{PARASITICS}$ and C_{TOTAL} = C9 + $C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation should be done to optimize the center frequency of the tank.

Automatic Gain Control (AGC)

When the AGC is enabled, it monitors the RSSI output. When the RSSI output reaches 1.28V, which corresponds to an RF input level of approximately -64dBm, the AGC switches on the LNA gain reduction attenuator. The attenuator reduces the LNA gain by 35dB, thereby reducing the RSSI output by about 0.55V. The LNA resumes high-gain mode when the RSSI output level drops back below 0.68V (approximately -67dBm at the RF input) for a programmable interval called the AGC dwell time. The AGC has a hysteresis of approximately 3dB. With the AGC function, the RSSI dynamic range is increased, allowing the MAX1471 to reliably produce an ASK output for RF input levels up to 0dBm with a modulation depth of 18dB. AGC is not necessary and can be disabled when utilizing only the FSK data path.

The MAX1471 features an AGC lock controlled by the AGC lock bit (see Table 8). When the bit is set, the LNA is locked in its present gain state.

Mixer

A unique feature of the MAX1471 is the integrated image rejection of the mixer. This device was designed to eliminate the need for a costly front-end SAW filter for many applications. The advantage of not using a SAW filter is increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double-balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz intermediate frequency (IF) with low-side injection (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve approximately 45dB of image rejection. Low-side injection is required as high-side injection is not possible due to the on-chip image rejection. The IF output is driven by a source follower, biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. The voltage conversion gain driving a 330Ω load is approximately 19.5dB. Note that the MIXIN+ and MIXIN- inputs are functionally identical.

Phase-Locked Loop (PLL)

The PLL block contains a phase detector, charge pump/integrated loop filter, voltage-controlled oscillator (VCO), asynchronous 32x clock divider, and crystal oscillator. This PLL does not require any external components. The relationship between the RF, IF, and reference frequencies is given by:

$$f_{REF} = (f_{RF} - f_{IF})/32$$

To allow the smallest possible IF bandwidth (for best sensitivity), the tolerance of the reference must be minimized.

Intermediate Frequency (IF)

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. It contains five AC-coupled limiting amplifiers with a bandpass-filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz.

For ASK data, the RSSI circuit demodulates the IF to baseband by producing a DC output proportional to the log of the IF signal level with a slope of approximately 16mV/dB. For FSK, the limiter output is fed into a PLL to demodulate the IF.

FSK Demodulator

The FSK demodulator uses an integrated 10.7MHz PLL that tracks the input RF modulation and determines the difference between frequencies as logic-level ones and zeros. The PLL is illustrated in Figure 1. The input to the PLL comes from the output of the IF limiting amplifiers. The PLL control voltage responds to changes in the frequency of the input signal with a nominal gain of 2.2mV/kHz. For example, an FSK peak-to-peak deviation of 50kHz generates a $110mV_{P-P}$ signal on the control line. This control line is then filtered and sliced by the FSK baseband circuitry.

The FSK demodulator PLL requires calibration to overcome variations in process, voltage, and temperature. For more information on calibrating the FSK demodulator, see the *Calibration* section. The maximum calibration time is 120µs. In DRX mode, the FSK demodulator calibration occurs automatically just before the IC enters sleep mode.

Crystal Oscillator

The XTAL oscillator in the MAX1471 is used to generate the local oscillator (LO) for mixing with the received signal. The XTAL oscillator frequency sets the received signal frequency as:

$$f_{RECEIVE} = (f_{XTAL} \times 32) + 10.7MHz$$

The received image frequency at:

$$f_{IMAGE} = (f_{XTAL} \times 32) - 10.7MHz$$

is suppressed by the integrated quadrature imagerejection circuitry.

For an input RF frequency of 315MHz, a reference frequency of 9.509MHz is needed for a 10.7MHz IF frequency (low-side injection is required). For an input RF frequency of 433.92MHz, a reference frequency of 13.2256MHz is required.

The XTAL oscillator in the MAX1471 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$fp = \frac{C_m}{2}\left(\frac{1}{C_{case} + C_{load}} - \frac{1}{C_{case} + C_{spec}}\right) \times 10^6$$

where:

f_p is the amount the crystal frequency pulled in ppm.

C_m is the motional capacitance of the crystal.

C_{case} is the case capacitance.

C_{spec} is the specified load capacitance.

C_{load} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{load} = C_{spec}$, the frequency pulling equals zero.

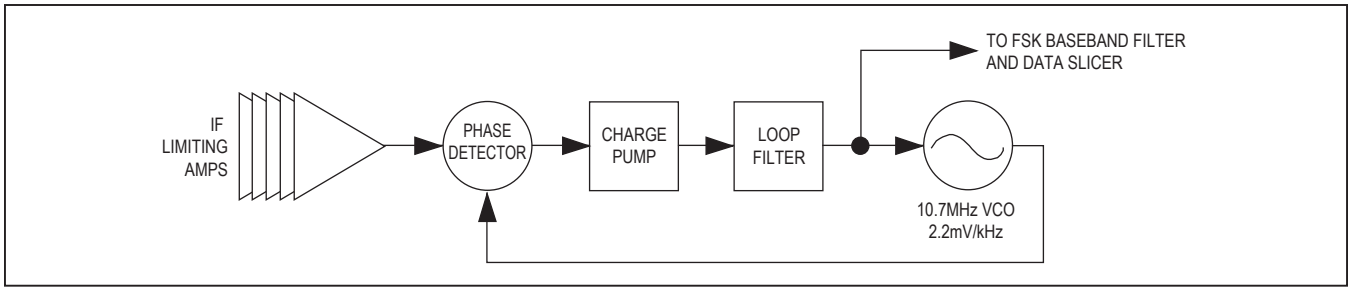


Figure 1. FSK Demodulator PLL Block Diagram

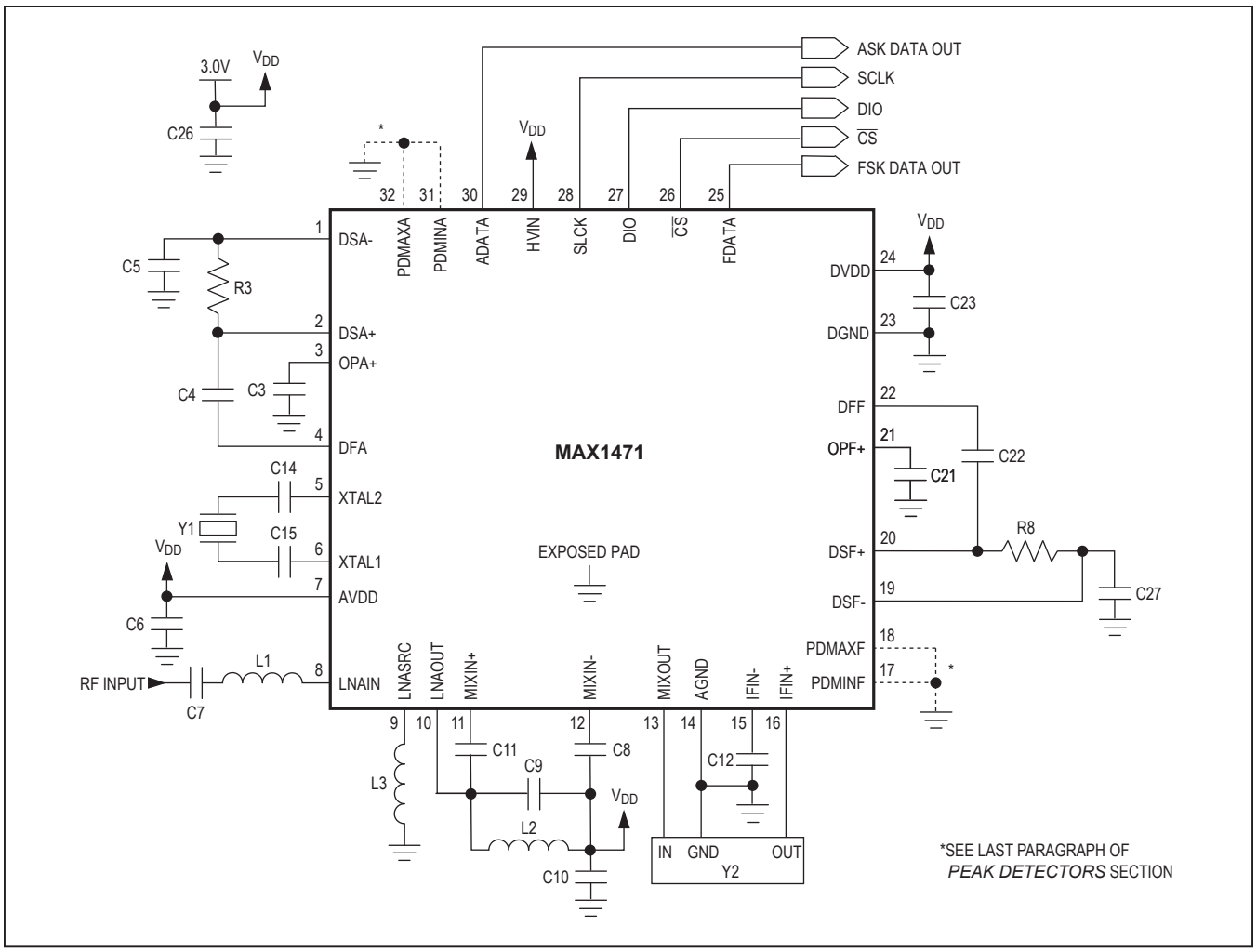


Figure 2. Typical Application Circuit

Data Filters

The data filters for the ASK and FSK data are implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two onchip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency in kHz should be set to approximately 1.5 times the fastest expected Manchester data rate in kbps from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 3 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of the capacitors, use the following equations, along with the coefficients in Table 2:

$$C_{F1} = \frac{b}{a(100k)(\pi)(f_C)}$$

$$C_{F2} = \frac{a}{4(100k)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency. For example, choose a Butterworth filter response with a corner frequency of 5kHz:

Table 1. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR 433.92MHz RF	VALUE FOR 315MHz RF	DESCRIPTION (%)
C3	220pF	220pF	10
C4	470pF	470pF	5
C5	0.047µF	0.047µF	10
C6	0.1µF	0.1µF	10
C7	100pF	100pF	5
C8	100pF	100pF	5
C9	1.0pF	2.2pF	Q0.1pF
C10	220pF	220pF	10
C11	100pF	100pF	5
C12	1500pF	1500pF	10
C14	15pF	15pF	5
C15	15pF	15pF	5
C21	220pF	220pF	10
C22	470pF	470pF	5
C23	0.01µF	0.01µF	10
C26	0.1µF	0.1µF	10
C27	0.047µF	0.047µF	10
L1	56nH	100nH	5 or better*
L2	16nH	30nH	5 or better*
L3	10nH	15nH	5 or better*
R3	25kΩ	25kΩ	5
R8	25kΩ	25kΩ	5
Y1	13.2256MHz	9.509MHz	Crystek or Hong Kong X'tals
Y2	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata SFECV10.7 series

Note: *Component values vary depending on PCB layout.*
**Wire wound recommended.*

$$C_{F1} = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C_{F2} = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C_{F1} to 470pF and C_{F2} to 220pF. In the *Typical Application Circuit*, C_{F1} and C_{F2} are named C4 and C3, respectively, for ASK data, and C21 and C22 for FSK data.

Data Slicers

The purpose of a data slicer is to take the analog output of a data filter and convert it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. The threshold voltage is set by the voltage on the DSA- pin for the ASK receive chain (DSF- for the FSK receive chain), which is connected to the negative input of the data slicer comparator.

Numerous configurations can be used to generate the data-slicer threshold. For example, the circuit in Figure 4 shows a simple method using only one resistor and one capacitor. This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The sizes of R and C affect how fast the threshold tracks to the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

With this configuration, a long string of NRZ zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

Table 2. Coefficients to Calculate C_{F1} and C_{F2}

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

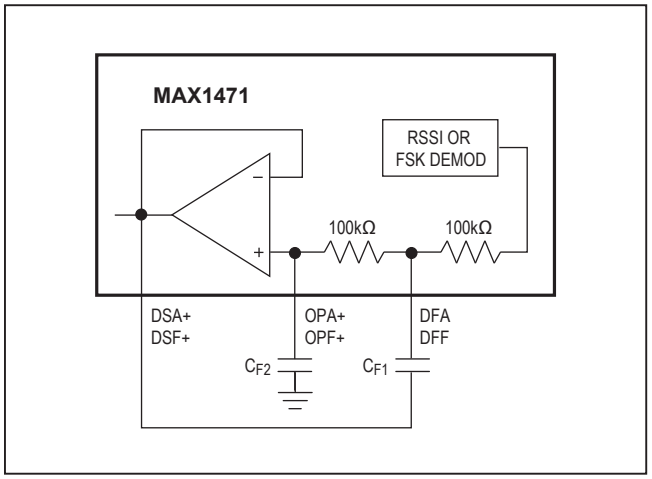


Figure 3. Sallen-Key Lowpass Data Filter

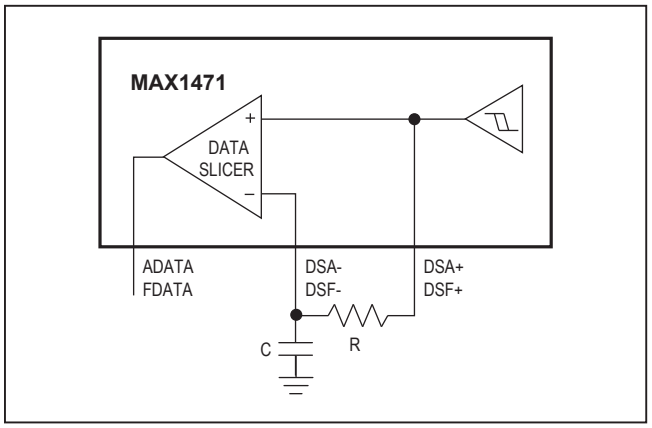


Figure 4. Generating Data-Slicer Threshold Using a Lowpass Filter

Figure 5 shows a configuration that uses the positive and negative peak detectors to generate the threshold. This configuration sets the threshold to the midpoint between a high output and a low output of the data filter.

Peak Detectors

The maximum peak detectors (PDMAXA for ASK, PDMAXF for FSK) and minimum peak detectors (PDMINA for ASK, PDMINF for FSK), in conjunction with resistors and capacitors shown in Figure 5, create DC output voltages proportional to the high and low peak values of the filtered ASK or FSK demodulated signals. The resistors provide a path for the capacitors to discharge, allowing the peak detectors to dynamically follow peak changes of the data-filter output voltages.

The maximum and minimum peak detectors can be used together to form a data-slicer threshold voltage at a midvalue between the maximum and minimum voltage levels of the data stream (see the *Data Slicers* section and Figure 5). The RC time constant of the peakdetector combining network should be set to at least 5 times the data period.

If there is an event that causes a significant change in the magnitude of the baseband signal, such as an AGC gain switch or a power-up transient, the peak detectors may “catch” a false level. If a false peak is detected, the slicing level is incorrect. The MAX1471 has a feature called peak-detector track enable (TRK_EN), where the peak-detector outputs can be reset (see Figure 6). If TRK_EN is set (logic 1), both the maximum and minimum peak detectors follow the input signal. When TRK_EN is cleared (logic 0), the peak detectors revert to their normal operating mode. The TRK_EN function is automatically enabled for a short time and then disabled whenever the IC recovers from the sleep portion of DRX mode, or when an AGC gain switch occurs. Since the peak detectors exhibit a fast attack/slow decay response, this feature allows for an extremely fast startup or AGC recovery. See Figure 7 for an illustration of a fast-recovery sequence. In addition to the automatic control of this function, the TRK_EN bits can be controlled through the serial interface (see the *Serial Control Interface* section).

If the peak detectors are not used, make sure that the FSKPD_EN and ASKPD_EN bits in Register 0x0 are maintained at the default setting of logic 0 and short each of the four PD pins directly to ground or through a capacitor whose value is approximately 1000pF. If a peak detector pin is left open, the FDATA and ADATA signals can potentially couple back into the DSA+ or the DSA- lines (depending on circuit design and layout), causing an oscillation at the output of the data slicer comparator. The PDMINA peak detector is particularly vulnerable to this coupling because its pin (31) is next to the ADATA pin (30).

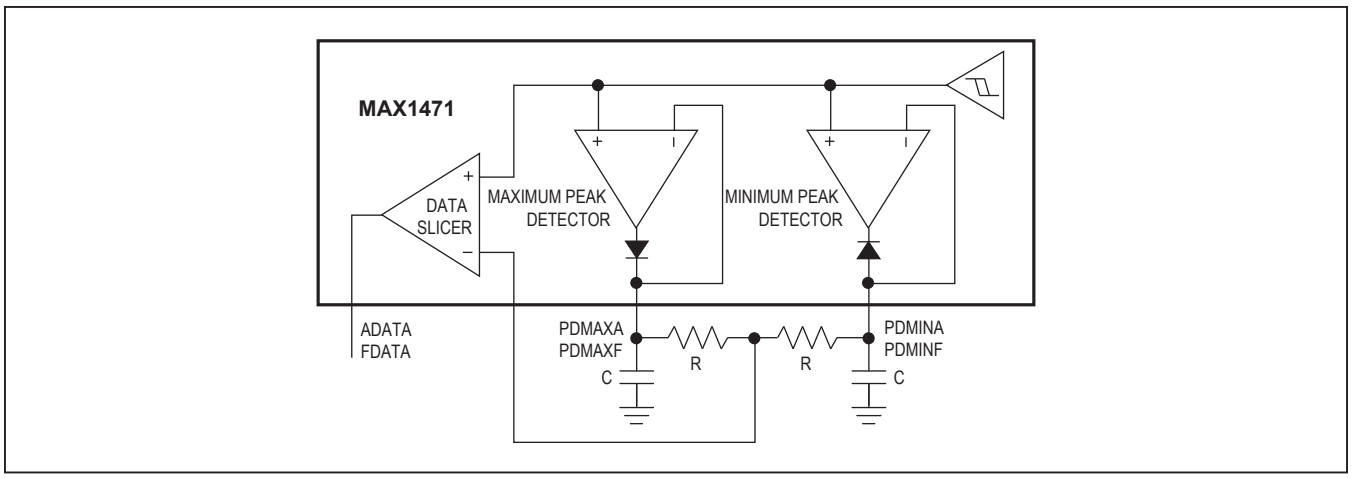


Figure 5. Generating Data-Slicer Threshold Using the Peak Detectors

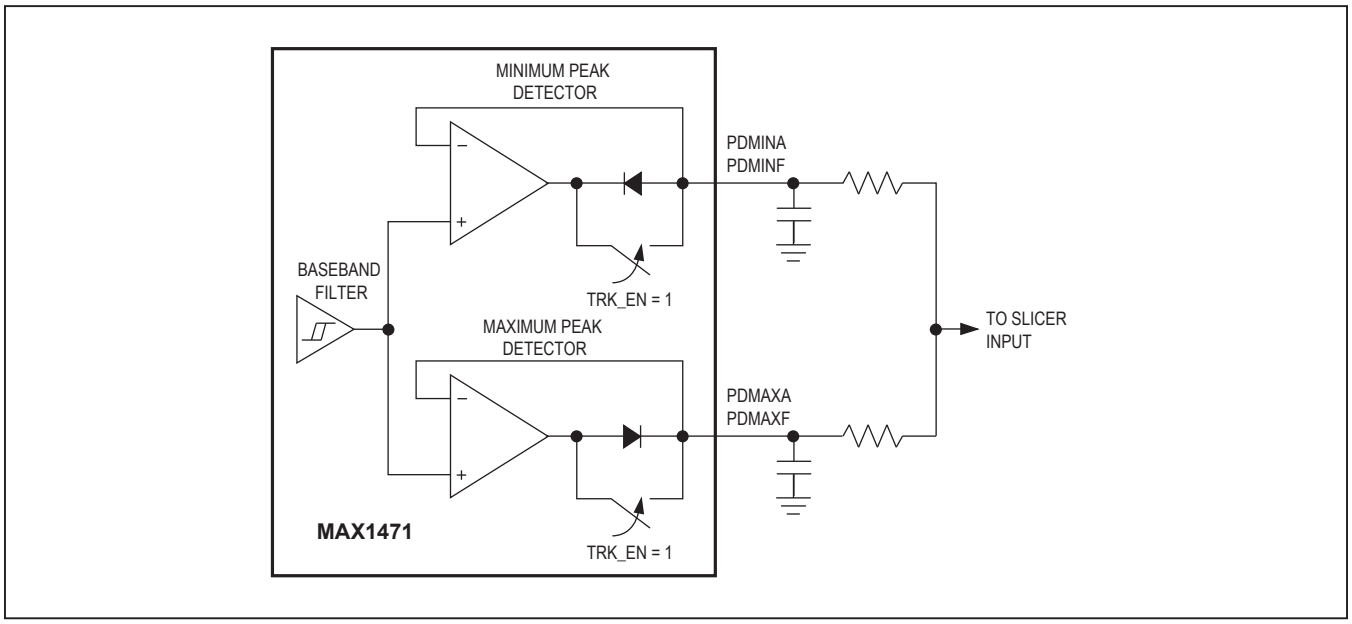


Figure 6. Peak-Detector Track Enable

Power-Supply Connections

The MAX1471 can be powered from a 2.4V to 3.6V supply or a 4.5V to 5.5V supply. The device has an onchip linear regulator that reduces the 5V supply to 3V needed to operate the chip.

To operate the MAX1471 from a 3V supply, connect DVDD, AVDD, and HVIN to the 3V supply. When using a 5V supply, connect the supply to HVIN only and connect AVDD and DVDD together. In both cases, bypass DVDD and HVIN with a 0.01µF capacitor and AVDD with a 0.1µF capacitor. Place all bypass capacitors as close as possible to the respective supply pin.

Control Interface Considerations

When operating the MAX1471 with a +4.5V to +5.5V supply voltage, the $\overline{CS}$, DIO, and SCLK pins can be driven by a microcontroller with either 3V or 5V interface logic levels. When operating the MAX1471 with a +2.4V to +3.6V supply, only 3V logic from the microcontroller is allowed.

Serial Control Interface

Communication Protocol

The MAX1471 can use a 4-wire interface or a 3-wire interface (default). In both cases, the data input must follow the timing diagrams shown in Figures 8 and 9.

Note that the DIO line must be held LOW while $\overline{CS}$ is high. This is to prevent the MAX1471 from entering discontinuous receive mode if the DRX bit is high. The data is latched on the rising edge of SCLK, and therefore must be stable before that edge. The data sequencing is MSB first, the command (C[3:0]; see Table 3), the register address (A[3:0]; see Table 4) and the data (D[7:0]; see Table 5).

The mode of operation (3-wire or 4-wire interface) is selected by DOUT_FSK and/or DOUT_ASK bits in the configuration register. Either of those bits selects the ASKOUT and/or FSKOUT line as a SERIAL data output. Upon receiving a read register command (0x2), the serial interface outputs the data on either pin, according to Figure 10.

If neither of these bits are 1, the 3-wire interface is selected (default on power-up) and the DIO line is effectively a bidirectional input/output line. DIO is selected as an output of the MAX1471 for the following $\overline{CS}$ cycle whenever a READ command is received. The CPU must tri-state the DIO line on the cycle of $\overline{CS}$ that follows a read command, so the MAX1471 can drive the data output line. Figure 11 shows the diagram of the 3-wire interface. Note that the user can choose to send either 16 cycles of SCLK, as in the case of the 4-wire interface, or just eight cycles, as all the registers are 8-bits wide. The user must drive DIO low at the end of the read sequence.

The MASTER RESET command (0x3) (see Table 3) sends a reset signal to all the internal registers of the MAX1471 just like a power-off and power-on sequence would do. The reset signal remains active for as long as $\overline{CS}$ is high after the command is sent.

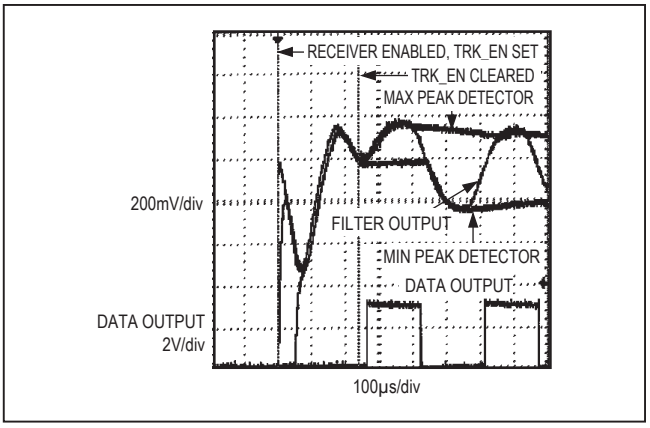


Figure 7. Fast Receiver Recovery in FSK Mode Utilizing Peak Detectors

Continuous Receive Mode (DRX = 0)

In continuous receive mode, individual analog modules can be powered on directly through the power configuration register (register 0x0). The SLEEP bit (bit 0) overrides the power settings of the remaining bits and puts the part into deep-sleep mode when set. It is also necessary to write the frequency divisor of the external crystal in the oscillator frequency register (register 0x3) to optimize image rejection and to enable accurate calibration sequences for the polling timer and the FSK demodulator. This number is the integer result of f_{XTAL}/100kHz.

If the FSK receive function is selected, it is necessary to perform an FSK calibration to improve receive sensitivity. Polling timer calibration is not necessary. See the *Calibration* section for more information.

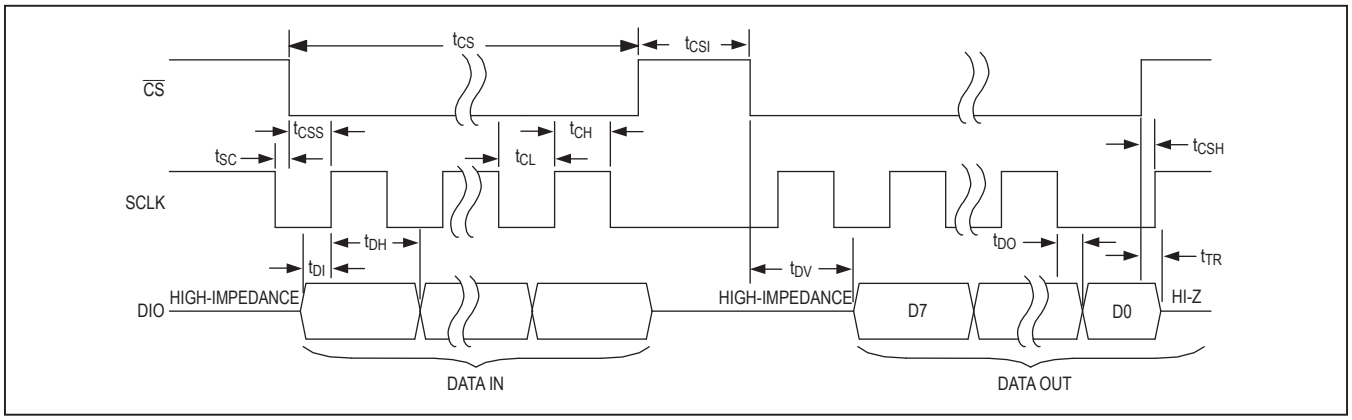


Figure 8. Digital Communications Timing Diagram

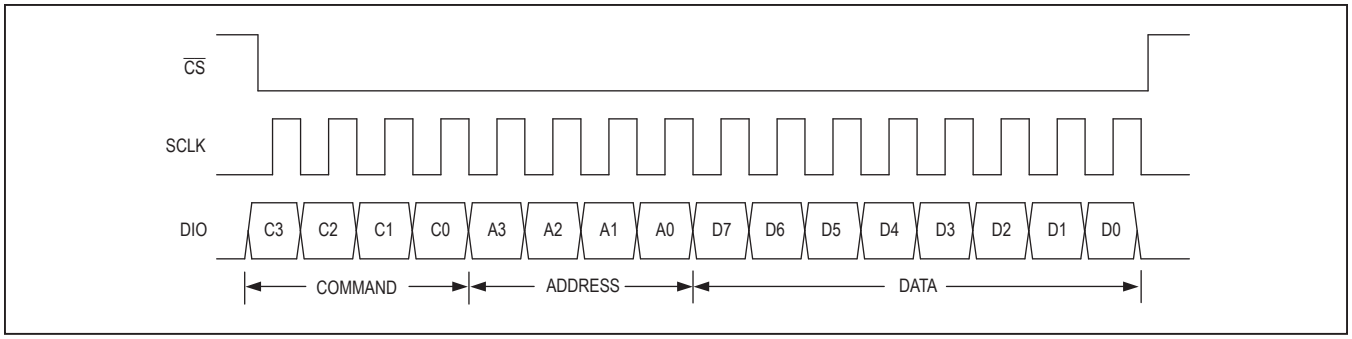


Figure 9. Data Input Diagram

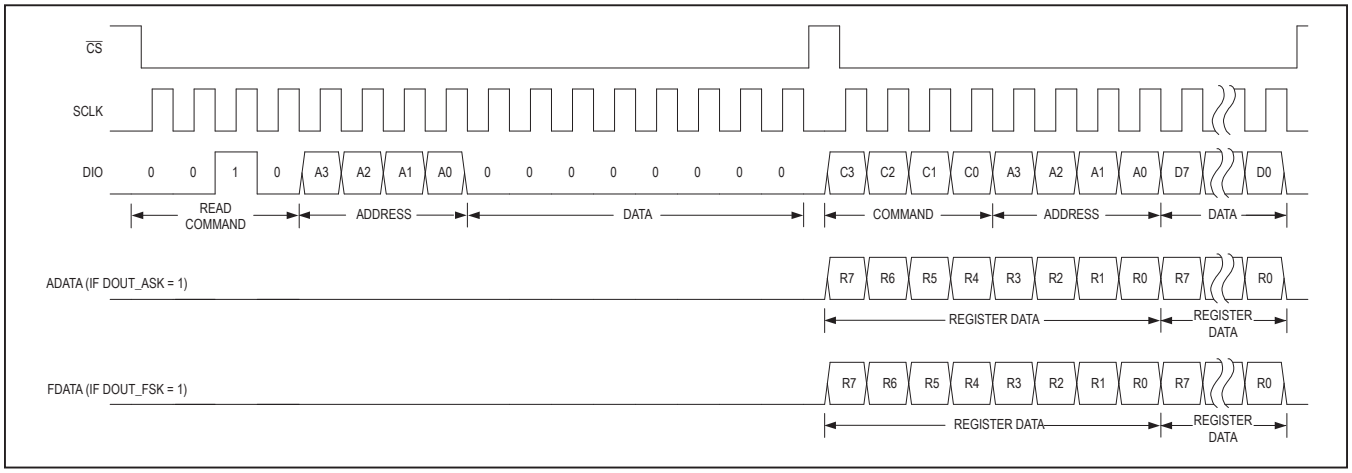


Figure 10. Read Command on a 4-Wire SERIAL Interface

Discontinuous Receive Mode (DRX = 1)

In the discontinuous receive mode (DRX = 1), the power signals of the different modules of the MAX1471 toggle between OFF and ON, according to internal timers t_{OFF}, t_{CPU}, and t_{RF}. It is also necessary to write the frequency divisor of the external crystal in the oscillator frequency register (register 0x3). This number is the integer result of f_{XTAL}/100kHz. Before entering the discontinuous receive mode for the first time, it is also necessary to calibrate the timers (see the *Calibration* section).

The MAX1471 uses a series of internal timers (t_{OFF}, t_{CPU}, and t_{RF}) to control its power-up. The timer sequence begins when both $\overline{CS}$ and DIO are one. The MAX1471 has an internal pullup on the DIO pin, so the user must tri-state the DIO line when $\overline{CS}$ goes high.

The external CPU can then go to a sleep mode during t_{OFF}. A high-to-low transition on DIO, or a low level on DIO serves as the wake-up signal for the CPU, which must then start its wake-up procedure, and drive DIO low before t_{LOW} expires (t_{CPU} + t_{RF}). Once t_{RF} expires, the MAX1471 enables the FSKOUT and/or ASKOUT data outputs. The CPU must then keep DIO low for as long as it may need to analyze any received data. Releasing DIO causes the MAX1471 to pull up DIO, reinitiating the t_{OFF} timer.

Oscillator Frequency Register (Address: 0x3)

The MAX1471 has an internal frequency divider that divides down the crystal frequency to 100kHz. The MAX1471 uses the 100kHz clock signal when calibrating itself and also to set the image-rejection frequency. The hexadecimal value written to the oscillator frequency register is the nearest integer result of f_{XTAL}/100kHz.

For example, if data is being received at 315MHz, the crystal frequency is 9.509375MHz. Dividing the crystal frequency by 100kHz and rounding to the nearest integer gives 95, or 0x5F hex. So for 315MHz, 0x5F would be written to the oscillator frequency register.

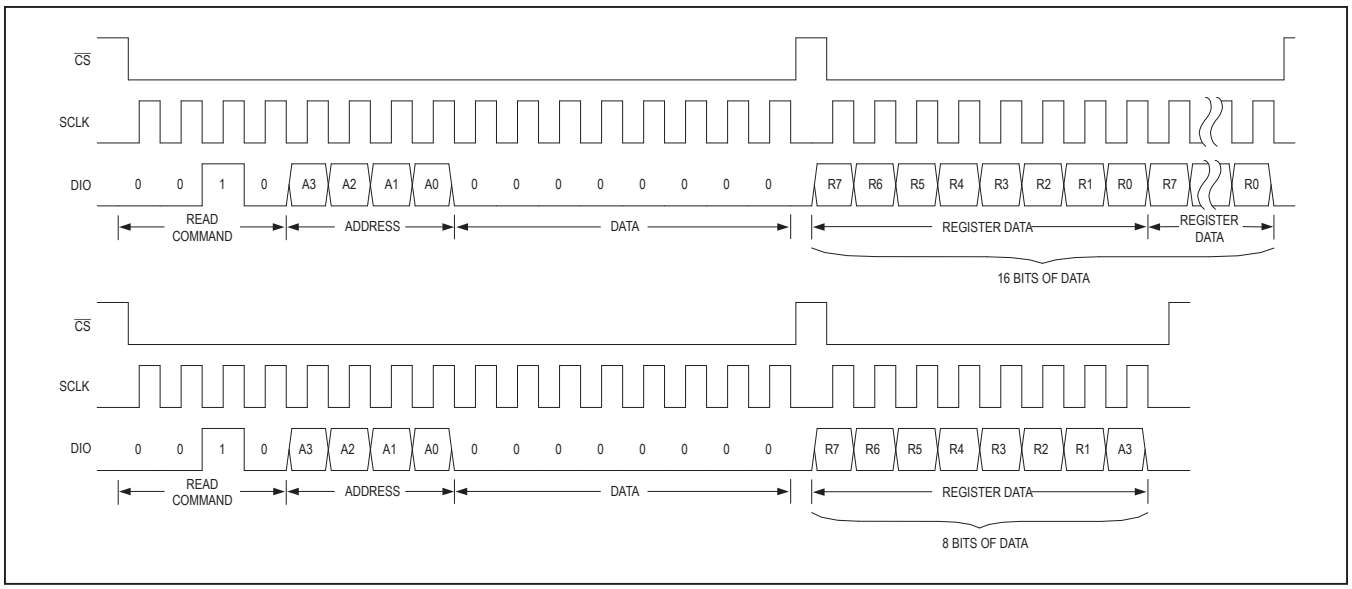


Figure 11. Read Command in 3-Wire Interface

Table 3. Command Bits

C[3:0]	DESCRIPTION
0x0	No operation
0x1	Write data
0x2	Read data
0x3	Master reset
0x4–0xF	Not used

AGC Dwell Timer Register (Address: 0xA)

The AGC dwell timer holds the AGC in low-gain state for a set amount of time after the power level drops below the AGC switching threshold. After that set amount of time, if the power level is still below the AGC threshold, the LNA goes into high-gain state. This is important for ASK since the modulated data may have a high level above the threshold and a low level below the threshold, which without the dwell timer would cause the AGC to switch on every bit.

The AGC dwell time is dependent on the crystal frequency and the bit settings of the AGC dwell timer register. To calculate the dwell time, use the following equation:

$$\text{Dwell Time} = \frac{2^{\text{Reg0xA}}}{f_{XTAL}}$$

where Reg 0xA is the value of register 0xA in decimal.

To calculate the value to write to register 0xA, use the following equation and use the next integer higher than the calculated result:

$$\text{Reg 0xA} \geq 3.3 \times \log_{10} (\text{Dwell Time} \times f_{XTAL})$$

For Manchester Code (50% duty cycle), set the dwell time to at least twice the bit period. For nonreturn-tozero (NRZ) data, set the dwell to greater than the period of the longest string of zeros or ones. For example, using Manchester code at 315MHz (f_{XTAL} = 9.509375MHz) with a data rate of 4kbps (bit period = 125µs), the dwell time needs to be greater than 250µs:

$$\text{Reg 0xA} \geq 3.3 \times \log_{10} (250\mu s \times 9.509375MHz) \approx 11.14$$

Choose the register value to be the next integer value higher than 11.14, which is 12 or 0x0C hex.

The default value of the AGC dwell timer on power-up or reset is 0x0D.

Calibration

The MAX1471 must be calibrated to ensure accurate timing of the off timer in discontinuous receive mode or when receiving FSK signals. The first step in calibration is ensuring that the oscillator frequency register (address: 0x3) has been programmed with the correct divisor value (see the *Oscillator Frequency Register* section). Next, enable the mixer to turn the crystal driver on.

Table 4. Register Summary

REGISTER A[3:0]	REGISTER NAME	DESCRIPTION
0x0	Power configuration	Enables/disables the LNA, AGC, mixer, baseband, peak detectors, and sleep mode (see Table 6).
0x1	Configuration	Sets options for the device such as output enables, off-timer prescale, and discontinuous receive mode (see Table 7).
0x2	Control	Controls AGC lock, peak-detector tracking, as well as polling timer and FSK calibration (see Table 8).
0x3	Oscillator frequency	Sets the internal clock frequency divisor. **This register must be set to the integer result of f_{XTAL}/100kHz** (see the *Oscillator Frequency Register* section).
0x4	Off timer—t_{OFF} (upper byte)	Sets the duration that the MAX1471 remains in low-power mode when DRX is active (see Table 10).
0x5	Off timer—t_{OFF} (lower byte)	
0x6	CPU recovery timer—t_{CPU}	Increases maximum time the MAX1471 stays in lower power mode while CPU wakes up when DRX is active (see Table 11).
0x7	RF settle timer—t_{RF} (upper byte)	During the time set by the settle timer, the MAX1471 is powered on with the peak detectors and the data outputs disabled to allow time for the RF section to settle. DIO must be driven low at any time during $t_{LOW} = t_{CPU} + t_{RF}$ or the timer sequence restarts (see Table 12).
0x8	RF settle timer—t_{RF} (lower byte)	
0x9	Status register (read only)	Provides status for PLL lock, AGC state, crystal operation, polling timer, and FSK calibration (see Table 9).
0xA	AGC dwell timer	Controls the dwell (release) time of the AGC.

Calibrate the polling timer by setting POL_CAL_EN = 1 in the configuration register (register 0x1). Upon completion, the POL_CAL_DONE bit in the status register (register 0x8) is 1, and the POL_CAL_EN bit is reset to zero. If using the MAX1471 in continuous receive mode, polling timer calibration is not needed.

FSK receiver calibration is a two-step process. Set FSKCALLSB = 1 (register 0x1) or to reduce the calibration time, accuracy can be sacrificed by setting the FSKCALLSB = 0. Next, initiate FSK receiver calibration, set FSK_CAL_EN = 1. Upon completion, the FSK_CAL_DONE bit in the status register (register 0x8) is one, and the FSK_CAL_EN bit is reset to zero.

When in continuous receive mode and receiving FSK data, recalibrate the FSK receiver after a significant change in temperature or supply voltage. When in discontinuous receive mode, the polling timer and FSK receiver (if enabled) are automatically calibrated during every wake-up cycle.

Off Timer (t_{OFF})

The first timer, t_{OFF} (see Figure 12), is a 16-bit timer that is configured using: register 0x4 for the upper byte, register 0x5 for the lower byte, and bits PRESCALE1 and PRESCALE0 in the configuration register (register 0x1). Table 10 summarizes the configuration of the t_{OFF} timer. The PRESCALE1 and PRESCALE2 bits set the size of the shortest time possible (t_{OFF} time base). The data written to the t_{OFF} registers (0x4 and 0x5) is multiplied by the time base to give the total t_{OFF} time. On power-up, the off timer registers are set to zero and must be written before using DRX mode.

During t_{OFF}, the MAX1471 is operating with very low supply current (5.0µA typ), where all of its modules are turned off, except for the t_{OFF} timer itself. Upon completion of the t_{OFF} time, the MAX1471 signals the user by asserting DIO low.

Table 5. Register Configuration

ADDRESS	DATA							
A3 A2 A1 A0	D7	D6	D5	D4	D3	D2	D1	D0
POWER CONFIGURATION (0x0)								
0 0 0 0	LNA_EN	AGC_EN	MIXER_ EN	FSKBB_ EN	FSKPD_ EN	ASKBB_ EN	ASKPD_ EN	SLEEP
CONFIGURATION (0x1)								
0 0 0 1	X	GAIN SET*	FSKCALL SB	FSK_ DOUT	ASK_ DOUT	TOFF_ PS1	TOFF_ PS0	DRX_ MODE
CONTROL (0x2)								
0 0 1 0	X	AGC LOCK	X	X	FSKTRK _EN	ASKTRK _EN	POL_ CAL_EN	FSK_ CAL_EN
OSCILLATOR FREQUENCY (0x3)								
0 0 1 1	d7	d6	d5	d4	d3	d2	d1	d0
OFF TIMER (upper byte) (0x4)								
0 1 0 0	t15	t14	t13	t12	t11	t10	t9	t8
OFF TIMER (lower byte) (0x5)								
0 1 0 1	t7	t6	t5	t4	t3	t2	t1	t0
CPU RECOVERY TIMER (0x6)								
0 1 1 0	t7	t6	t5	t4	t3	t2	t1	t0
RF SETTLE TIMER (upper byte) (0x7)								
0 1 1 1	t15	t14	t13	t12	t11	t10	t9	t8
RF SETTLE TIMER (lower byte) (0x8)								
1 0 0 0	t7	t6	t5	t4	t3	t2	t1	t0
STATUS REGISTER (read only) (0x9)								
1 0 0 1	LOCK DET	AGCST	CLK ALIVE	X	X	X	POL_CAL _DONE	FSK_CAL _DONE
AGC DWELL TIMER (0xA)								
1 0 1 0	X	X	X	dt4	dt3*	dt2*	dt1	dt0*

**Power-up state = 1. All other bits, power-up state = 0.*

CPU Recovery Timer (t_{CPU})

The second timer, t_{CPU} (see Figure 12), is used to delay the power-up of the MAX1471, thereby providing extra power savings and giving a CPU the time required to complete its own power-on sequence. The CPU is signaled to begin powering up when the DIO line is pulled low by the MAX1471 at the end of t_{OFF}. t_{CPU} then begins counting down, while DIO is held low by the MAX1471. At the end of t_{CPU}, the tRF counter begins.

t_{CPU} is an 8-bit timer, configured through register 0x6. The possible t_{CPU} settings are summarized in Table 11. The data written to the t_{CPU} register (0x6) is multiplied by 120µs to give the total t_{CPU} time. On power-up, the CPU timer register is set to zero and must be written before using DRX mode.

RF Settle Timer (t_{RF})

The third timer, t_{RF} (see Figure 12), is used to allow the RF sections of the MAX1471 to power up and stabilize before ASK or FSK data is received. t_{RF} begins counting once t_{CPU} has expired. At the beginning of t_{RF}, the modules selected in the power control register (register 0x0) are powered up with the exception of the peak detectors and have the t_{RF} period to settle.

Table 6. Power Configuration Register (Address: 0x0)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	POWER-UP STATE	FUNCTION
LNA_EN	LNA enable	7	0	1 = Enable LNA 0 = Disable LNA
AGC_EN	AGC enable	6	0	1 = Enable AGC 0 = Disable AGC
MIXER_EN	Mixer enable	5	0	1 = Enable mixer 0 = Disable mixer
FSKBB_EN	FSK baseband enable	4	0	1 = Enable FSK baseband 0 = Disable FSK baseband
FSKPD_EN	FSK peak detector enable	3	0	1 = Enable FSK peak detectors 0 = Disable FSK peak detectors
ASKBB_EN	ASK baseband enable	2	0	1 = Enable ASK baseband 0 = Disable ASK baseband
ASKPD_EN	ASK peak detector enable	1	0	1 = Enable ASK peak detectors 0 = Disable ASK peak detectors
SLEEP	Sleep mode	0	0	1 = Deep-sleep mode 0 = Normal operation

At the end of t_{RF}, the MAX1471 stops driving DIO low and enables ADATA, FDATA, and peak detectors if chosen to be active in the power configuration register (0x0). The CPU must be awake at this point, and must hold DIO low for the MAX1471 to remain in operation. The CPU must begin driving DIO low any time during $t_{LOW} = t_{CPU} + t_{RF}$. If the CPU fails to drive DIO low, DIO is pulled high through the internal pullup resistor, and the timer sequence is restarted, leaving the MAX1471 powered down. Any time the DIO line is driven high while the DRX = 1, the DRX sequence is initiated, as defined in Figure 12.

t_{RF} is a 16-bit timer, configured through registers 0x7 (upper byte) and 0x8 (lower byte). The possible t_{RF} settings are in Table 12. The data written to the t_{RF} register (0x7 and 0x8) is multiplied by 120µs to give the total t_{RF} time. On power-up, the RF timer registers are set to zero and must be written before using DRX mode.

Typical Power-Up Procedure

Here is a typical power-up procedure for receiving either ASK or FSK signals at 315MHz in continuous mode:

1) Write 0x3000 to reset the part.
2) Write 0x10FE to enable all RF and baseband sections.
3) Write 0x135F to set the oscillator frequency register to work with a 315MHz crystal.
4) Write 0x1120 to set FSKCALLSB for an accurate FSK calibration.
5) Write 0x1201 to begin FSK calibration.
6) Read 0x2900 and verify that bit 0 is 1 to indicate FSK calibration is done.

The MAX1471 is now ready to receive ASK or FSK data.

Due to the high sensitivity of the receiver, it is recommended that the configuration registers be changed only when not receiving data. Receiver desensitization may occur, especially if odd-order harmonics of the SCLK line fall within the IF bandwidth.

Table 7. Configuration Register (Address: 0x1)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	POWER-UP STATE	FUNCTION
X	Don't care	7	0	Don't care.
GAINSET	Gain set	6	1	0 = LNA low-gain state. 1 = LNA high-gain state. For manual gain control, enable the AGC (AGC_EN = 1), set LNA gain state to desired setting, then disable the AGC (AGC_EN = 0).
FSKCALLSB	FSK accurate calibration	5	0	FSKCALLSB = 1 enables a longer, more accurate FSK calibration. FSKCALLSB = 0 provides for a quick, less accurate FSK calibration.
DOUT_FSK	FSKOUT enable	4	0	This bit enables the FDATA pin to act as the serial data output in 4-wire mode. (See the *Communication Protocol* section.)
DOUT_ASK	ASKOUT enable	3	0	This bit enables the ADATA pin to act as the serial data output in 4-wire mode. (See the *Communication Protocol* section.)
TOFF_PS1	Off-timer prescale	2	0	Sets LSB size for the off timer. (See the *Off Timer* section.)
TOFF_PS0	Off-timer prescale	1	0	
DRX_MODE	Receive mode	0	0	1 = Discontinuous receive mode. (See the *Discontinuous Receive Mode* section.) 0 = Continuous receive mode. (See the *Continuous Receive Mode* section.)

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power lane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all V_{DD} or HVIN connections.

Table 8. Control Register (Address: 0x2)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	POWER-UP STATE	FUNCTION
X	None	7	Don't care	Don't care.
AGCLOCK	AGC lock	6	0	Locks the LNA gain in its present state.
X	None	5, 4		Don't care.
FSKTRK_EN	FSK peak detector track enable	3	0	Enables the tracking mode of the FSK peak detectors when FSKTRK_EN = 1. (See the *Peak Detectors* section.)
ASKTRK_EN	ASK peak detector track enable	2	0	Enables the tracking mode of the ASK peak detectors when ASKTRK_EN = 1. (See the *Peak Detectors* section.)
POL_CAL_EN	Polling timer calibration enable	1	0	POL_CAL_EN = 1 starts the polling timer calibration. Calibration of the polling timer is needed when using the MAX1471 in discontinous receive mode. POL_CAL_EN resets when calibration completes properly. (See the *Calibration* section.)
FSK_CAL_EN	FSK calibration enable	0	0	FSK_CAL_EN starts the FSK receiver calibration. FSK_CAL_EN resets when calibration completes properly. (See the *Calibration* section.)

Table 9. Status Register (Read Only) (Address: 0x9)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
LOCKDET	Lock detect	7	0 = Internal PLL is not locked so the MAX1471 will not receive data. 1 = Internal PLL is locked.
AGCST	AGC state	6	0 = LNA in low-gain state. 1 = LNA in high-gain state.
CLKALIVE	Clock/crystal alive	5	0 = No valid clock signal seen at the crystal inputs. 1 = Valid clock at crystal inputs.
X	None	4, 3, 2	Don't care.
POL_CAL_DONE	Polling timer calibration done	1	0 = Polling timer calibraton in progress or not completed. 1 = Polling timer calibration is complete.
FSK_CAL_DONE	FSK calibration done	0	0 = FSK calibration in progress or not completed. 1 = FSK calibration is compete.

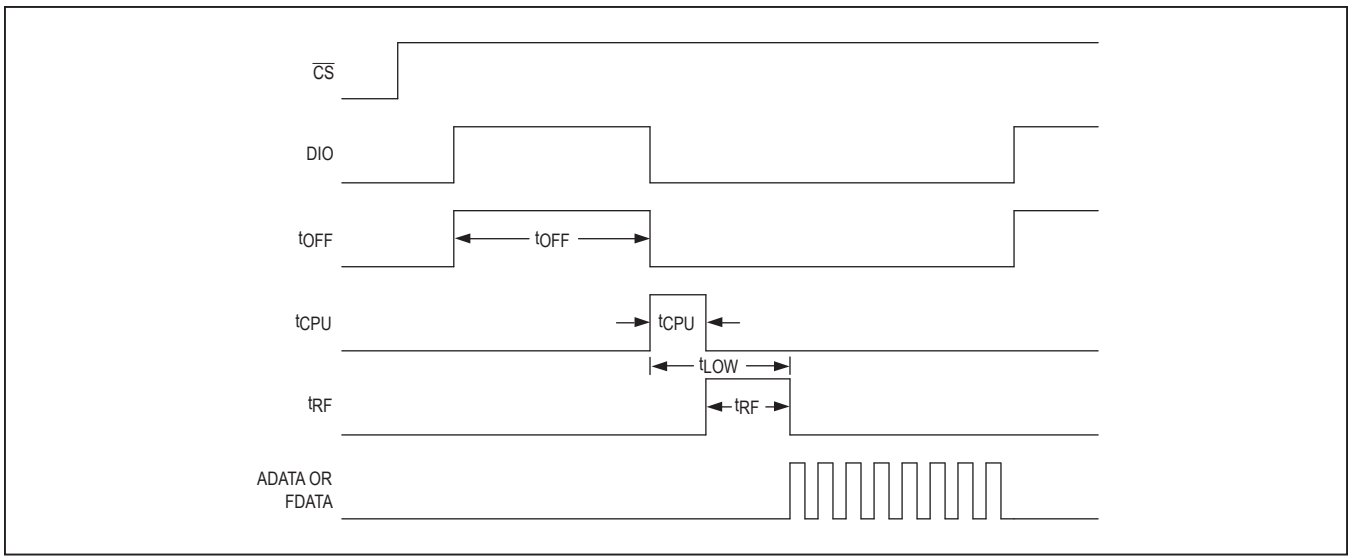


Figure 12. DRX Mode Sequence of the MAX1471

Table 10. Off-Timer (t_{OFF}) Configuration

PRESCALE1	PRESCALE0	t_{OFF} TIME BASE (1 LSB)	MIN t_{OFF} REG 0x4 = 0x00 REG 0x5 = 0x01	MAX t_{OFF} REG 0x4 = 0xFF REG 0x5 = 0xFF
0	0	120µs	120µs	7.86s
0	1	480µs	480µs	31.46s
1	0	1920µs	1.92ms	2 min 6s
1	1	7680µs	7.68ms	8 min 23s

Table 11. CPU Recovery Timer (tCPU) Configuration

TIME BASE (1 LSB)	MIN t_{CPU} REG 0x6 = 0x01	MAX t_{CPU} REG 0x6 = 0xFF
120µs	120µs	30.72ms

Table 12. RF Settle Timer (t_{RF}) Configuration

TIME BASE (1 LSB)	MIN t_{RF} REG 0x7 = 0x00 REG 0x8 = 0x01	MAX t_{RF} REG 0x7 = 0xFF REG 0x8 = 0xFF
120µs	120µs	7.86s

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1471ATJ+	-40°C to +125°C	32 Thin QFN-EP**
MAX1471ATJ/V+	-40°C to +125°C	32 Thin QFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
***EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	**21-0140**	**90-0001**