MAX14727/MAX14728/ MAX14731

Dual-Input, Bidirectional Overvoltage Protector with Automatic Path Control

General Description

The MAX14727/MAX14728/MAX14731 provide protection to valuable consumer circuits against two positive voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to 100V. The devices automatically select the input source, with channel A being the primary supply.

These devices feature reverse bias-blocking capabilities. Unlike other overvoltage protectors, when the devices are disabled, the voltage applied to OUT does not feed back into either INA or INB. These devices also feature two OTG enable pins (OTG_ENA, OTG_ENB) that allow OUT voltage to supply the corresponding input when OUT is higher than the output startup voltage.

These overvoltage-protection devices feature high-voltage, low on-resistance (73mΩ, typ) internal FETs, effectively minimizing a voltage drop across the device. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The devices also have thermal-shutdown protection against overload conditions.

The overvoltage-protection threshold can be adjusted with optional external resistors to any voltage between 4V and 14V. The devices automatically choose the appropriate internal trip thresholds when the overvoltage-lockout input is set lower than the external OVLO select voltage. The internal OVLO are preset to 13.75V (typ) (MAX14727), 10V (typ) (MAX14728), or 5.92V (typ) (MAX14731).

The devices are specified over the extended -40°C to +85°C temperature range, and are available in a 30-bump, wafer-level package (WLP).

Applications

- Smartphones
- Tablets
- e-Readers

Benefits and Features

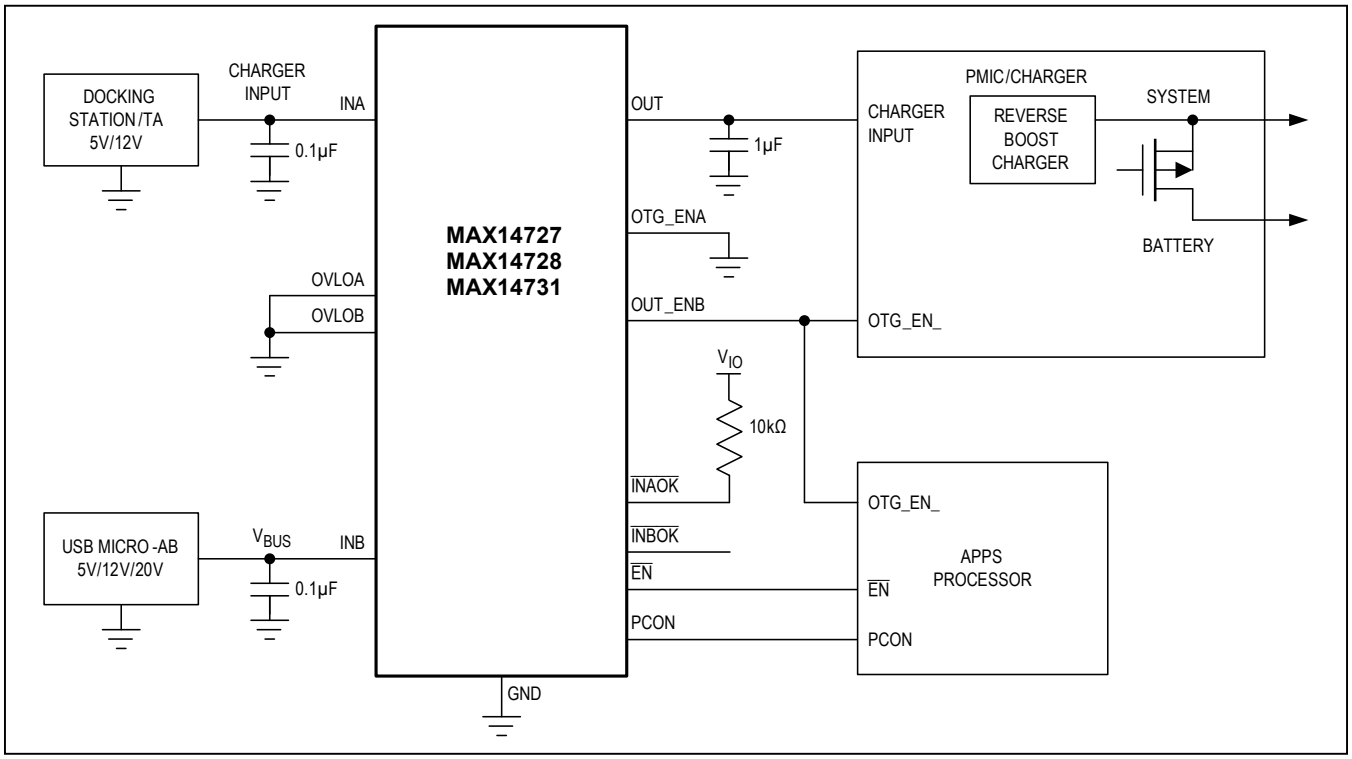
- Protects Portable Devices with Dual-Input Power
  - Wide Operating Input-Voltage Protection from 3V to 28V
  - 5A Continuous-Current Capability
  - Integrated 73mΩ (typ) nMOSFET Switch
- Allows Flexible and Precise Design in OVLO Implementation
  - Wide Adjustable OVLO Threshold Range from 4V to 14V
  - OTG Enables Allow OUT Supply INA/INB
  - Preset Accurate Internal OVLO Thresholds:
    13.75V ±2% (MAX14727)
    10V ±2% (MAX14728)
    5.92V ±2% (MAX14731)
- Increases System Reliability Through Premium Security
  - Surge Immunity Over +100V
  - Soft-Start to Minimize In-Rush Current
  - Internal 15ms Startup Debounce
  - Thermal Shutdown Protection
- Minimizes Board Space With Compact Package
  - 30-Bump, 2.6mm x 2.2mm WLP

Ordering Information ***appears at end of data sheet.***

19-7577; Rev 1; 6/15

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

(All voltages are referenced to GND.)
INA, INB (Note 1) .....-0.3V to +30V
OUT .....-0.3V to +16V
INA, OUT .....-16V to +30V
INB, OUT .....-16V to +30V
OTG_ENA, OTG_ENB,
PCON, $\overline{INAOK}$, $\overline{INBOK}$, $\overline{EN}$.....-0.3V to +6V
OVLOA, OVLOB.....-0.3V to +16V
Continuous-Current into INA, INB, OUT (Note 2)
WLP .....±5A

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 20.25mW/°C above +70°C).....1620mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Survive-to-burst pulse up to 100V, with 2Ω series resistance and hot plugs recur. Above the input clamp voltage, input must be a surge in nature with limited energy.

Note 2: Limited by the PCB thermal design.

Package Thermal Characteristics (Note 3)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....49.38°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

($V_{INA,INB}$ = 3V to 28V, V_{OUT} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{INA,INB}$ = 5V, T_A = +25°C) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Startup-Voltage Threshold	V_{IN_ST}			2.65	3.2	V
Input Sustaining Voltage	V_{IN_SU}	I_{OUT} = 0A		1.95	2.35	V
Input Valid-Voltage Threshold	V_{IN_VAL}		3.9	4.1	4.3	V
Input Clamp Voltage	V_{IN_CLAMP}	$I_{INA,INB}$ = 10mA, T_A = +25°C		34		V
Input Supply Current	$I_{INA,INB}$	$V_{\overline{OVLOA,OVLOB}}$ = 0V, $V_{INA,INB}$ = 5V, $\overline{INAOK}$, $\overline{INBOK}$ is unconnected, I_{OUT} = 0A (Note 6)		230	360	µA
Output Startup-Voltage Threshold	V_{OUTST}			2.65	3.2	V
Output Sustaining Voltage	V_{OUTSU}	$I_{INA,INB}$ = 0A		1.95	2.35	V
Output Supply Current	I_{OUT}	$V_{OVLOA,OVLOB}$ = 0V, V_{OUT} = 5V, $I_{INA,INB}$ = 0A, V_{OTG_ENA,OTG_ENB} = 1.8V		275	420	µA
Output Shutdown Current	I_{SHDN}	$V_{OVLOA,OVLOB}$ = 3V, V_{OUT} = 5V, $V_{INA,INB}$ = 0V, V_{OTG_ENA,OTG_ENB} = 0V		6.5	14	µA
Input Leakage Voltage		V_{OUT} = 14V, INA, INB unconnected, V_{OTG_ENA,OTG_ENB} = 0V		0.001	0.1	V
Input Discharge Current		$V_{INA,INB}$ = V_{OUT} = 5V, INA, INB discharge current after an OTG_ENA, OTG_ENB transition from high to low		130	200	mA

Electrical Characteristics (continued)

($V_{INA,INB}$ = 3V to 28V, V_{OUT} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{INA,INB}$ = 5V, T_A = +25°C) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVP (INA,INB TO OUT)							
On-Resistance (INA to OUT)	R_{ONA}	V_{INA} = 5V, I_{OUT} = 100mA, T_A = +25°C			68	115	mΩ
On-Resistance (INB to OUT)	R_{ONB}	V_{INB} = 5V, I_{OUT} = 100mA, T_A = +25°C			68	115	mΩ
Internal Overvoltage-Trip Level	V_{IN_OVLO}	MAX14727	V_{IN} rising	13.5	13.75	14.0	V
			V_{IN} falling	13.0			
		MAX14728	V_{IN} rising	9.85	10	10.15	
			V_{IN} falling	9.5			
		MAX14731	V_{IN} rising	5.83	5.92	6.01	
			V_{IN} falling	5.6			
OVLOA, OVLOB Set Threshold	V_{OVLO_TH}			1.2		1.24	V
Adjustable OVLOA, OVLOB Threshold Range	V_{OVLO_EXT}			4		14	V
External OVLOA,OVLOB Select Threshold	V_{OVLO_SEL}			0.2	0.25	0.3	V
Active OUT Discharge Current	I_{OUT_DIS}	V_{OUT} = $V_{INA,INB}$ = 5V, OUT discharge current during a transition between channel A and B when PCON = 0			130		mA
DIGITAL SIGNALS ($\overline{INAOK}$, $\overline{INBOK}$, OTG_ENA, OTG_ENB, PCON, $\overline{EN}$)							
$\overline{INAOK}$, $\overline{INBOK}$ Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA				0.4	V
$\overline{INAOK}$, $\overline{INBOK}$ Leakage Current		$V_{I/O}$ = 3.3V, $\overline{INAOK}$, $\overline{INBOK}$ deasserted				1	µA
OTG_ENA, OTG_ENB, PCON, $\overline{EN}$ Input Logic-High	V_{IH}			1.6			V
OTG_ENA, OTG_ENB, PCON, $\overline{EN}$ Input Logic-Low	V_{IL}					0.4	V
OTG_ENA, OTG_ENB, PCON, $\overline{EN}$ Input Leakage Current	I_{IN}	0V ≤ V_{IN} ≤ V_{IL} or V_{IH} ≤ V_{IN} ≤ 5.5V		-1		+1	µA
TIMING CHARACTERISTICS							
INA, INB Debounce Time	t_{DEB}	$V_{INA,INB}$ = 5V to charge pump on (10% of $V_{INA,INB}$), R_{LOAD} = 100Ω, C_{LOAD} = 10µF			17		ms
INA, INB Soft-Start Time	t_{SS}	$V_{INA,INB}$ = 5V, $\overline{INAOK}$, $\overline{INBOK}$ assert to V_{OUT} = 90% of $V_{INA,INB}$, C_{LOAD} = 1000µF			5		ms
INA, INB Break-Before-Make Time	t_{BBM}	V_{INB} = 5V, V_{INA}= 0V to 5V or 5V to 0V, C_{LOAD} = 10µF			8		ms

Electrical Characteristics (continued)

($V_{INA,INB}$ = 3V to 28V, V_{OUT} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{INA,INB}$ = 5V, T_A = +25°C) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT Discharge Pulse Duration	t_{OUT_DIS}		7.2	8	8.8	ms
INA, INB OVP Turn-Off Response Time	t_{OFF}	From $V_{INA,INB}$ > $V_{OVLOA,OVLOB}$ to V_{OUT} = 80% of $V_{INA,INB}$, R_{LOAD} = 100Ω		100		ns
OTG Turn-On Time	t_{OTG_ON}	Time from OTG_ENA, OTG_ENB high to $V_{INA,INB}$ = 80% of V_{OUT}, V_{OUT} = 5V, $C_{INA,INB}$ = 10µF		30		µs
INA, INB Discharge Pulse Duration		$V_{INA,INB}$ = V_{OUT} = 5V, current pulse duration after an OTG_ENA, OTG_ENB transition from high to low		16		ms
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal Hysteresis	T_{HYST}			20		°C
ESD PROTECTION						
Human Body Model		INA, INB		±15		kV
IEC 61000-4-2 Contact Discharge		INA, INB		±8		kV
IEC 61000-4-2 Air Gap Discharge		INA, INB		±15		kV

Note 4: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 5: The input is considered not present when it is lower than a rough threshold of T_P = 1.5V (typ). When the B path is active and the INA > T_P is connected, the device goes to the A path (since it has the priority), but the INA has to be higher than the startup voltage to turn on the switch.

Note 6: When both inputs are connected, supply current is drawn from the highest one.

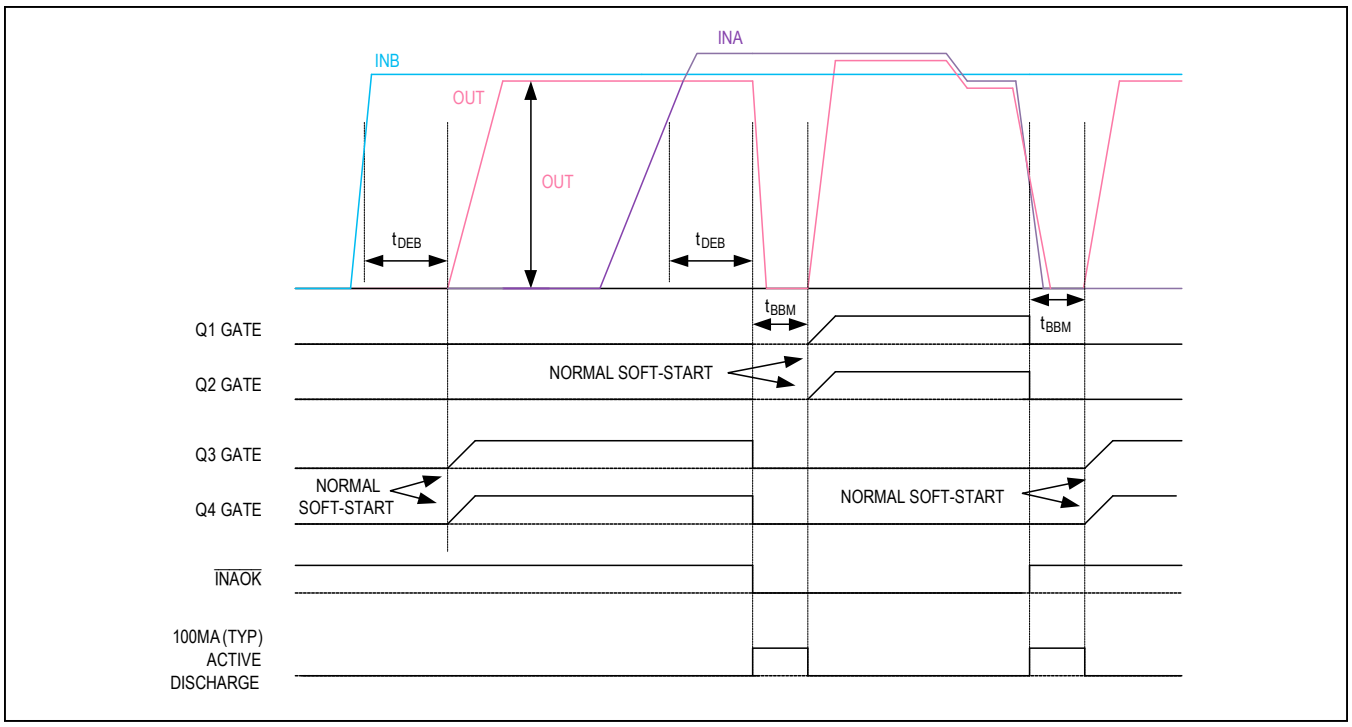


Figure 1. Automatic Switch Operation, PCON = 0

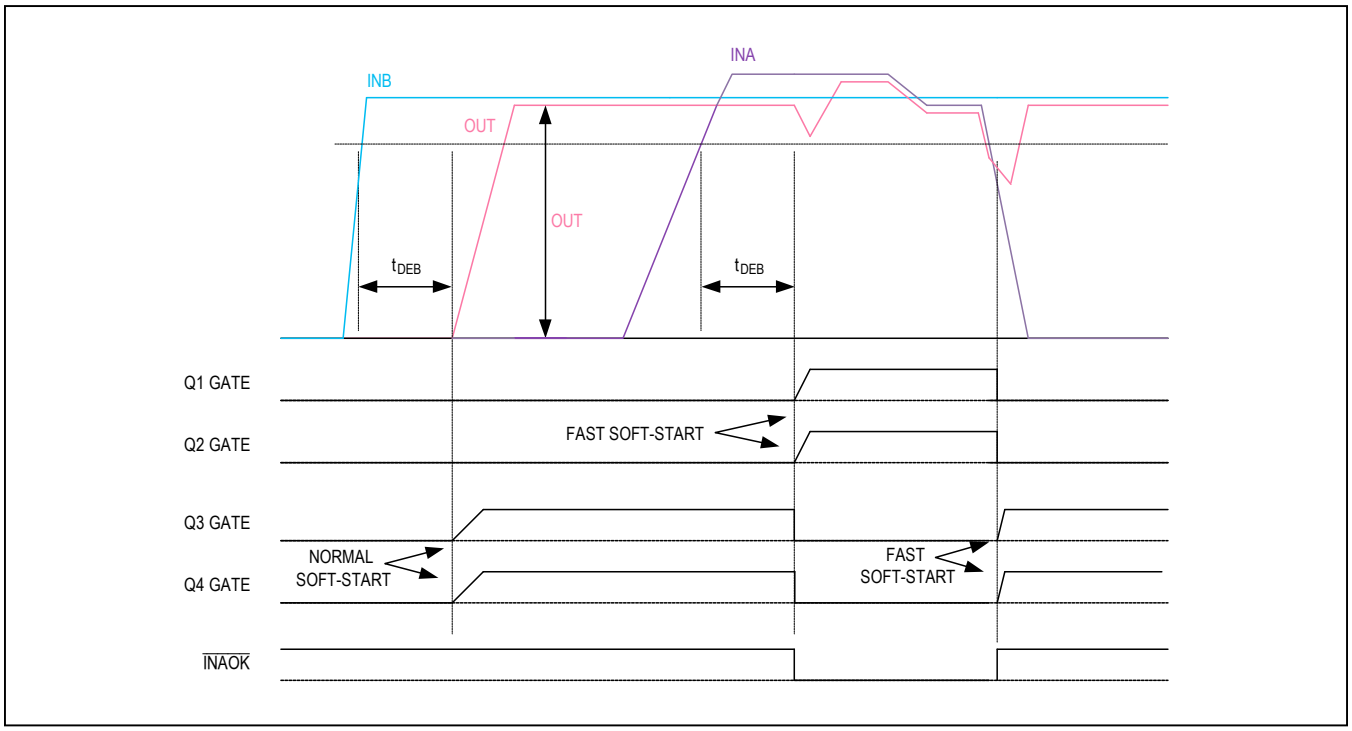
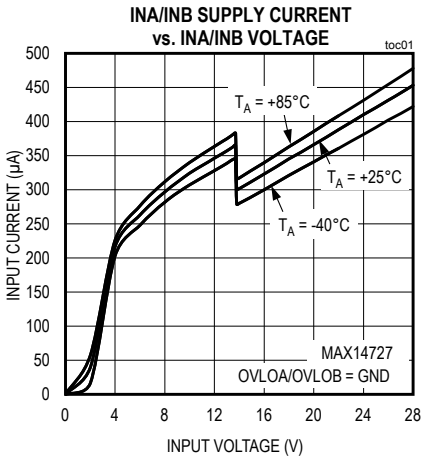
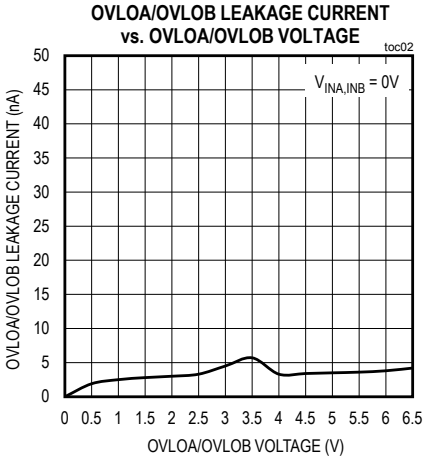


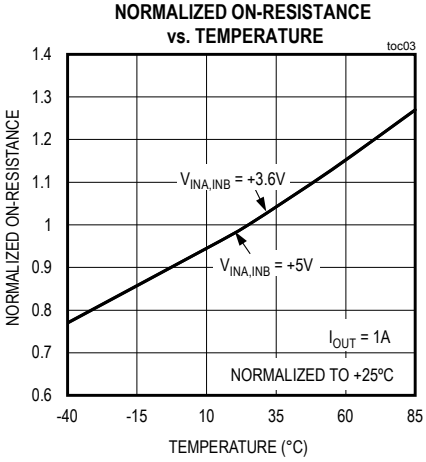
Figure 2. Automatic Switch Operation, PCON = 1

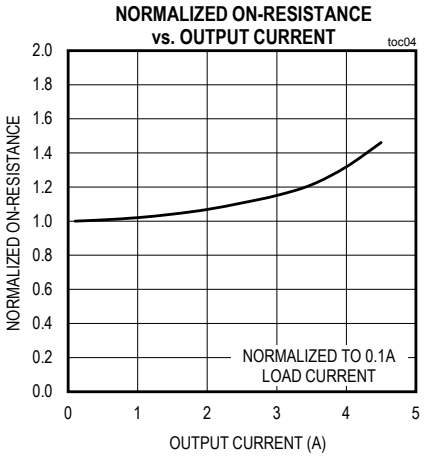
Typical Operating Characteristics

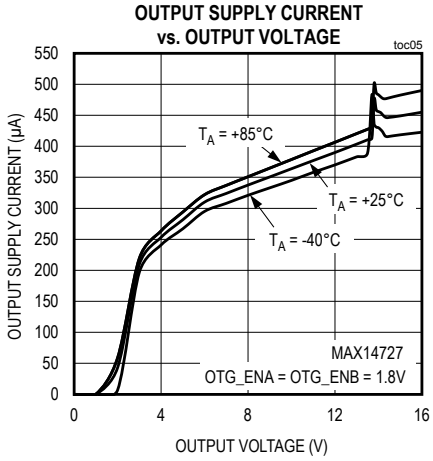
($V_{INA, INB}$ = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

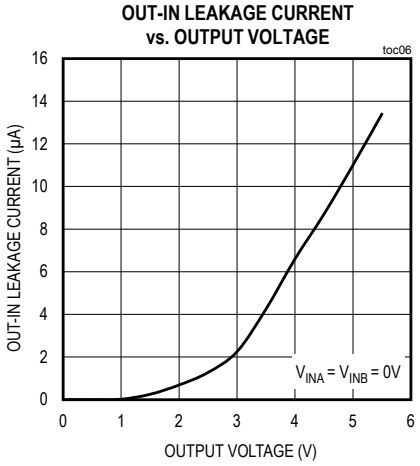


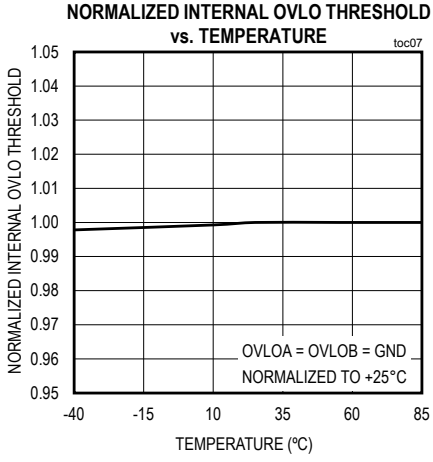






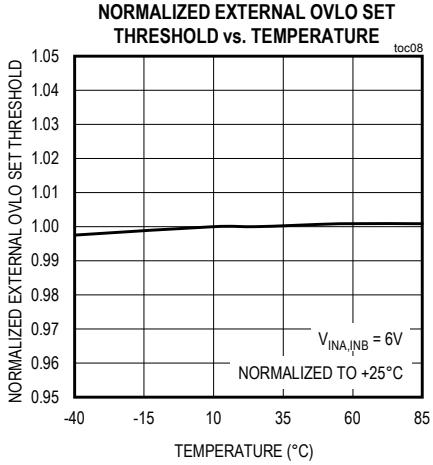


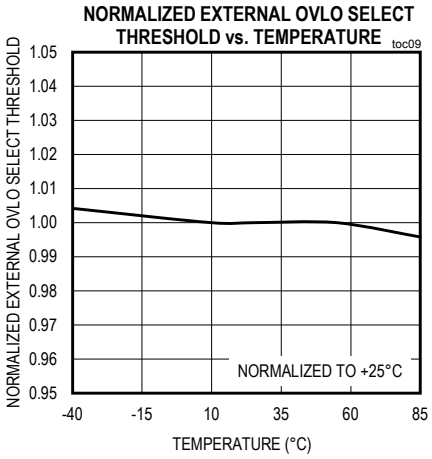


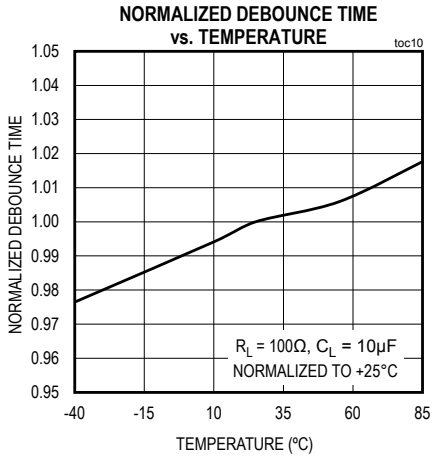


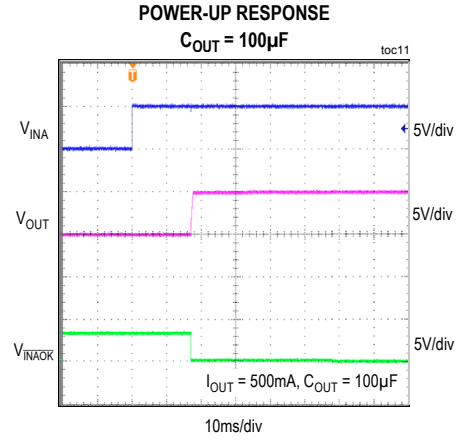
Typical Operating Characteristics (continued)

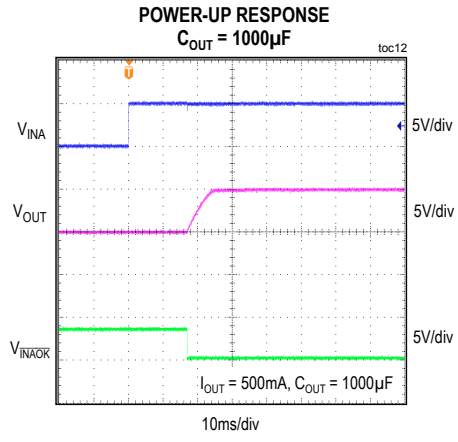
($V_{INA, INB}$ = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

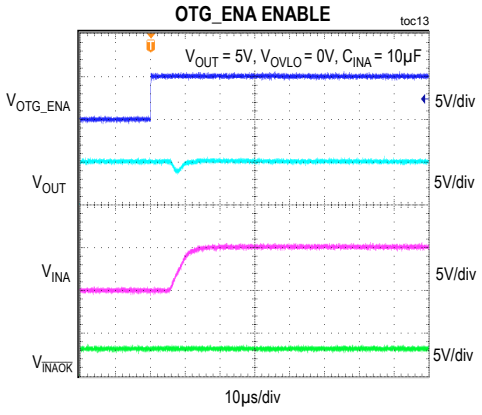








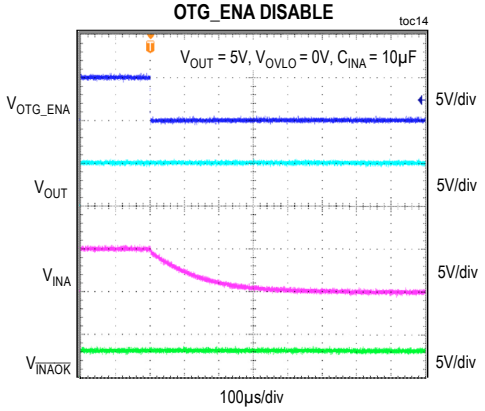




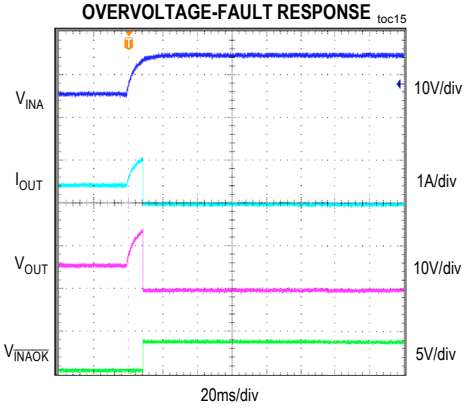
Typical Operating Characteristics (continued)

($V_{INA, INB}$ = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

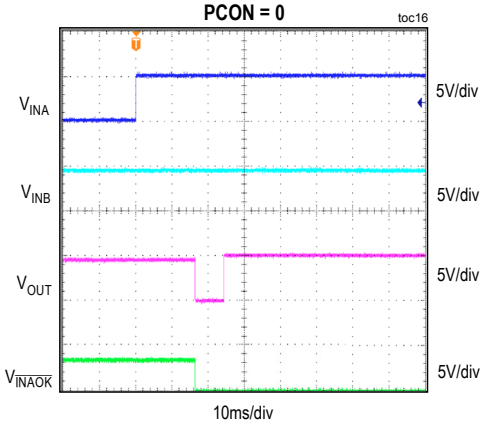
OTG_ENA DISABLE



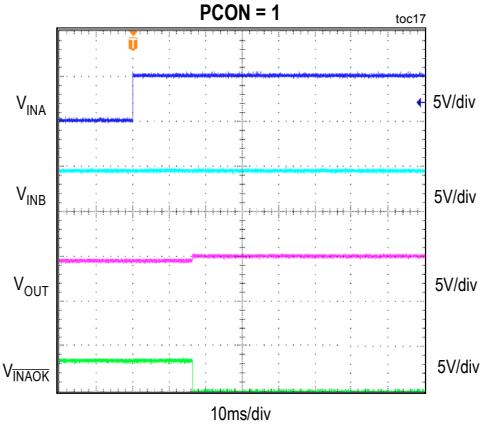
OVERVOLTAGE-FAULT RESPONSE



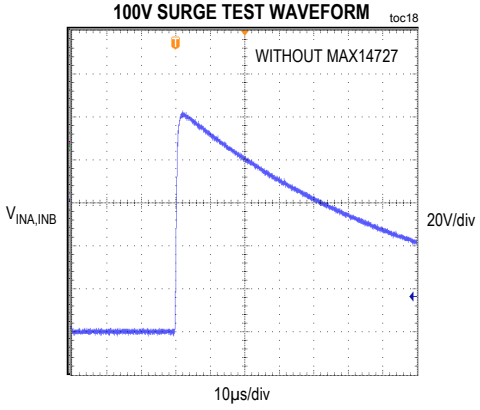
INPUT TRANSIENT
PCON = 0



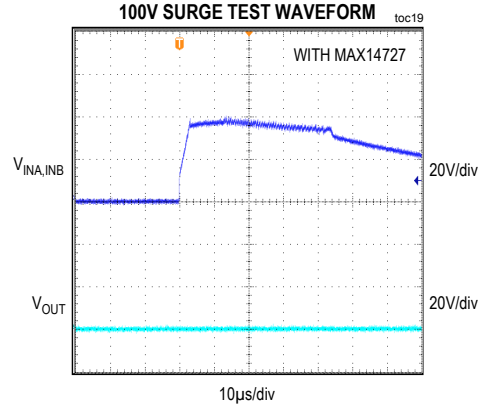
INPUT TRANSIENT
PCON = 1



100V SURGE TEST WAVEFORM



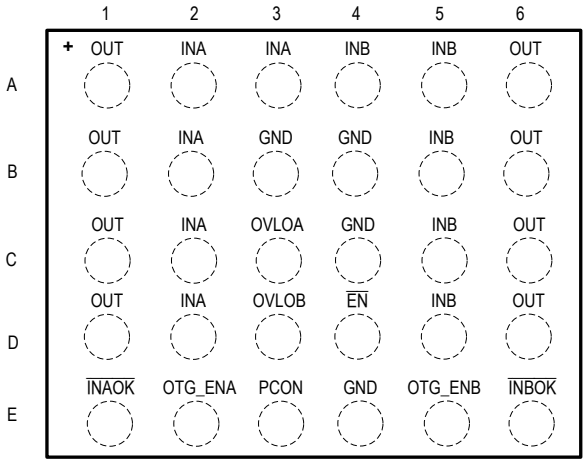
100V SURGE TEST WAVEFORM



Bump Configurations

TOP VIEW
BUMP-SIDE DOWN

MAX14727/MAX14728/MAX14731



WLP

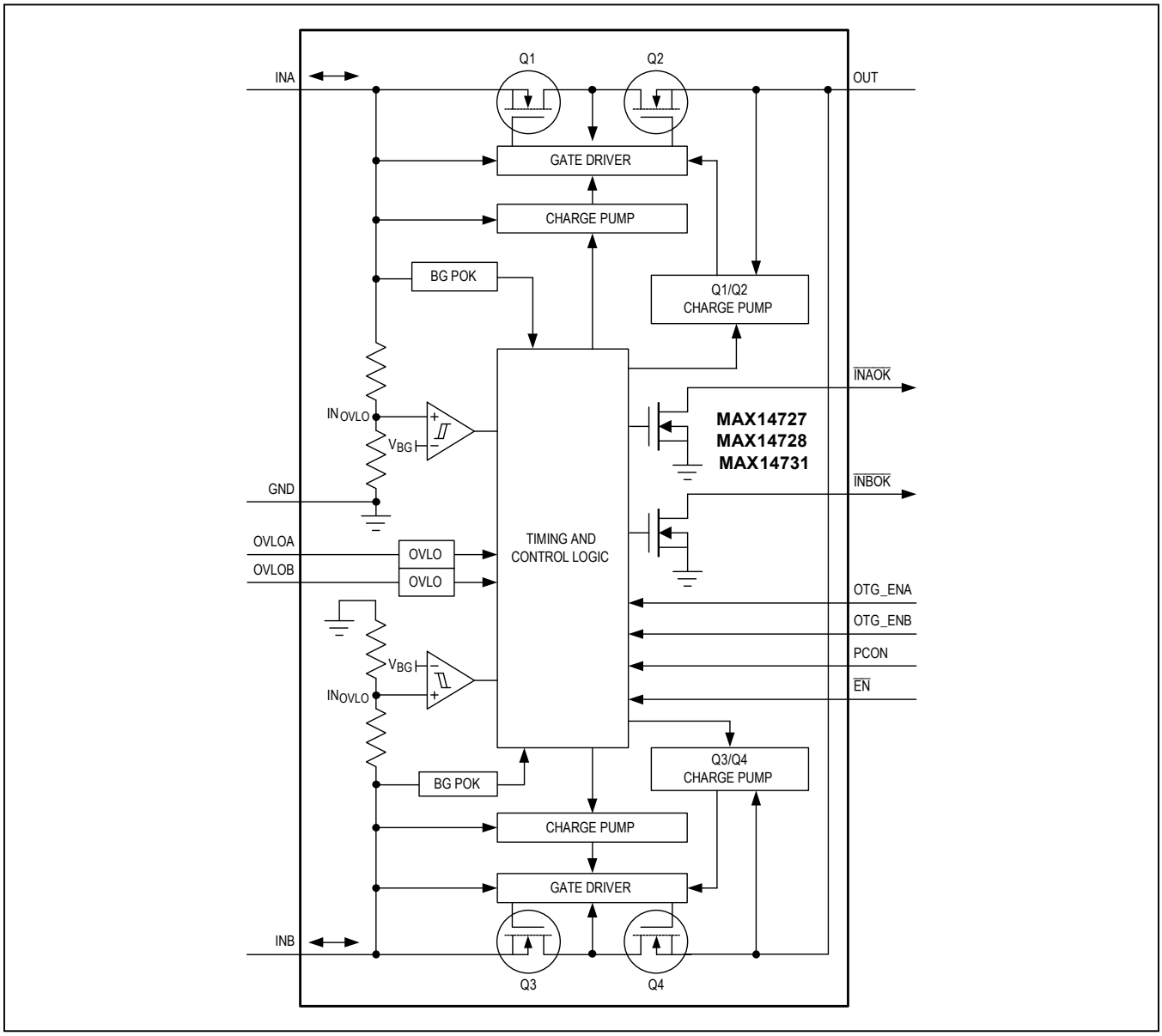
Bump Description

BUMP	NAME	FUNCTION
A1, A6, B1, B6, C1, C6, D1, D6	OUT	Overvoltage-Protection Output. Bypass OUT with a 1µF ceramic capacitor. Externally connect all OUT together.
A2, A3, B2, C2, D2	INA	Overvoltage-Protection Input A. Bypass INA with a 0.1µF ceramic capacitor as close as possible to the device. Externally connect all INA together.
A4, A5, B5, C5, D5	INB	Overvoltage-Protection Input B. Bypass INB with a 0.1µF ceramic capacitor as close as possible to the device as possible. Externally connect all INB together.
B3, B4, C4, E4	GND	Ground
C3	OVLOA	Overvoltage-Lockout Input A. Connect OVLOA to GND to use internal OVLO threshold for channel A. Connect OVLOA to a resistor divider for different voltage threshold for channel A.
D3	OVLOB	Overvoltage-Lockout Input B. Connect OVLOB to GND to use internal OVLO threshold for channel B. Connect OVLOB to a resistor divider for different voltage threshold for channel B.
D4	$\overline{EN}$	Active-Low Enable for Both OVP. When $\overline{EN}$ is high, both channels are off. When $\overline{EN}$ is low, both channels are active. $\overline{EN}$ does not affect $\overline{INAOK}$ or $\overline{INBOK}$.
E1	$\overline{INAOK}$	Open-Drain Flag Output. $\overline{INAOK}$ is driven low after INA voltage is stable between minimum V_{IN} and V_{OVLO} when OTG_ENA = 0. Connect a pullup resistor from $\overline{INAOK}$ to the logic I/O voltage of the host system.
E2	OTG_ENA	Enable Input for Channel A OTG Supply Operation. When OTG_ENA is low, channel A OTG operation is disabled. When OTG_ENA is high, channel A OTG operation is enabled, and OUT is connected to INA.
E3	PCON	Path Overlap Control. When PCON is low, there is a break-before-make time, 8ms (typ). When PCON is high, there is no break-before-make time. See the *Automatic Switch Operation* section.

Bump Description (continued)

BUMP	NAME	FUNCTION
E5	OTG_ENB	Enable Input for Channel B OTG Supply Operation. When OTG_ENB is low, channel B OTG operation is disabled. When OTG_ENB is high, channel B OTG operation is enabled, and OUT is connected to INB.
E6	$\overline{\text{INBOK}}$	Open-Drain Flag Output. $\overline{\text{INBOK}}$ is driven low after INB voltage is stable between minimum V_{IN} and V_{OVLO} when OTG_ENB = 0. Connect a pullup resistor from $\overline{\text{INBOK}}$ to the logic I/O voltage of the host system.

Functional Diagram



Detailed Description

The MAX14727/MAX14728/MAX14731 provide overvoltage protection for applications with two input sources. The devices feature low on-resistance and protect low-voltage systems against voltage faults up to $28V_{DC}$. An internal clamp also protects the devices from surges up to 100V. If the input voltage exceeds the overvoltage threshold, the output is disconnected from the input to prevent damage to the protected components. The 15ms debounce time prevents false turn-on of the internal FETs during startup.

Automatic Input Power Path Control

Automatic power path select has two modes of operation based on PCON. At least one of the inputs has to cross the startup voltage (2.75V, typ) at power-up for the circuitry to work. INA always has priority and INB only takes over INA when either INB is the only present input or when INB is valid (> 4.1V, typ) and INA is invalid (< 4.1V, typ) (Figure 1 and Figure 2).

When PCON = 0 (Figure 1):

When there is an input source change, the device has a break-before-make time (8ms, typ) with active discharge of 100mA (typ) during the off period. Additionally, during the off period, the battery-charger mode can reset so the charger can draw the proper amount of current.

$\overline{INAOK}$ and $\overline{INBOK}$ assert when the appropriate INA, INB is above the sustaining voltage (1.9V, typ) and below the OVLOA, OVLOB threshold.

When PCON = 1 (Figure 2):

When INA is detected valid while INB is valid, channel B is turned off and channel A is turned on quickly, with a higher soft-start current. Therefore, the transition from INB charging to INA charging is without shutoff. When INA becomes invalid while INB is still valid, channel B is turned on immediately, without debounce time, by using a higher soft-start current again.

$\overline{INAOK}$ and $\overline{INBOK}$ assert when the respective INA,INB is above valid voltage (4.1V, typ) and below the OVLOA, OVLOB threshold.

Table 1. Functionality Table

OVLOA OVLOB	OTG_ENA	OTG_ENB	$\overline{EN}$	$\overline{INAOK}$	$\overline{INBOK}$	CHANNEL A	CHANNEL B
0	0	0	0	INA status (Note 7)	INB status (Note 7)	(Note 8)	(Note 8)
0	0	0	1	INA status (Note 9)	INB status (Note 9)	Open	Open
0	0	1	0	INA status (Note 7)	High	Based on INA status	Close
0	0	1	1	INA status (Note 9)	High	Open	Open
0	1	0	0	High	INB status (Note 7)	Close	Based on INB status
0	1	0	1	High	INB status (Note 9)	Open	Open
0	1	1	0	High	High	Close	Close
0	1	1	1	High	High	Open	Open
1	X	X	X	High when OVLOA high	High when OVLOB high	Open when OVLOA high	Open when OVLOB high

X = Don't care.

Note 7: PCON = 0, INAOK, INBOK asserts low when respective INA,INB is greater than sustaining voltage (1.9V, typ). PCON = 1, INAOK, and INBOK assert low when respective INA,INB is greater than valid voltage (4.1V, typ).

Note 8: INA always has priority. INB takes over INA when INB is the only present input or when INB is valid (above 4.1V, typ) and INA is invalid (below 4.1V, typ).

Note 9: When EN is high, both channels are open and the minimum input functionality voltage is startup voltage (2.75V, typ).

Soft-Start

To minimize inrush current, the devices feature a soft-start capability to slowly turn on the internal FETs. Soft-start begins when $\overline{INAOK}$ and $\overline{INBOK}$ are asserted, and ends after 15ms (typ).

Overvoltage Lockout (OVLOA, OVLOB)

Connect OVLOA, OVLOB to ground to use the internal OVLO comparator with the internally set OVLO value. When INA, INB go above the overvoltage-lockout threshold (V_{IN_OVLO}), OUT is disconnected from INA, INB and $\overline{INAOK}$ and $\overline{INBOK}$ is deasserted. When INA, INB drops below V_{IN_OVLO}, the debounce time starts counting. After the debounce time, OUT follows INA, INB again and $\overline{INAOK}$ and $\overline{INBOK}$ is asserted.

The OVLOA, OVLOB input can be used as an additional enable input (Table 2).

External OVLO Adjustment Functionality

When an external resistor-divider is connected to OVLOA, OVLOB, and V_{OVLOA}, V_{OVLOB} exceeds the OVLOA, OVLOB select voltage (V_{OVLO_SEL}), the internal OVLOA, OVLOB comparator read $\overline{INA}$,INB by the external resistor-divider.

R1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_TH}, and R1 are known, R2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left[1 + \frac{R1}{R2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

Table 2. Truth Table

SWITCH OPEN/CLOSE		OVLOA, OVLOB	
		Low	High
$\overline{EN}$	Low	Close	Open
	High	Open	Open

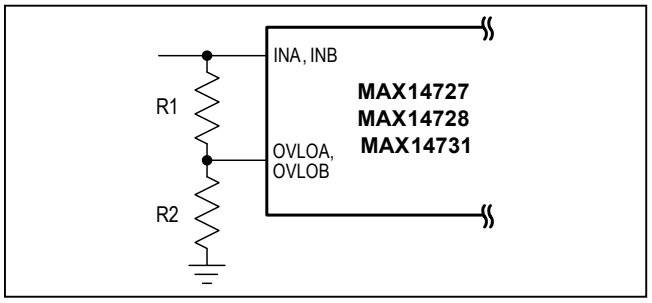


Figure 3. External OVLO Adjustment

Reverse-Bias Blocking

The devices feature reverse-bias blocking. When INA, INB voltage is below the input startup voltage and OTG_ENA and OTG_ENB is low, the switch between INA, INB and OUT is open and the two back-to-back diodes of the two series switches block reverse bias. Therefore, when the voltage is applied at the output, current does not travel back to the input.

OTG Enable

The devices feature reverse-turn-on capability. OTG_ENA and OTG_ENB can be used to turn on the switch for OUT to feed back to INA, INB when voltage applied at OUT is above the startup voltage (2.75V, typ). When OTG_ENA, OTG_ENB is high, $\overline{INAOK}$ and $\overline{INBOK}$ is deasserted. During the OTG operation, if INA, INB go above OVLOA, OVLOB, the OVP switch turns off. It is recommended that power be supplied to OUT prior to OTG operation. Power is also removed from OUT prior to disabling OTG operation. When either OTG_ENA or OTG_ENB is on, the internal power path control is disabled.

Thermal-Shutdown Protection

The devices feature thermal-shutdown protection to protect the device from overheating. The internal FETs turn off when the junction temperature exceeds +150°C (typ). The device returns to normal operation once the temperature drops by approximately 20°C (typ).

Applications Information

Input Bypass Capacitor

For most applications, bypass INA and INB to GND with a 0.1µF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection by clamping the overshoot.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the device to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition.

When PCON = 0, the output is actively discharged during the channel B to channel A switchover event. The inductance of the input cable with a small input capacitance (0.1µF) would cause an input voltage drop. This might trigger a switch back to channel B and output latchoff. Therefore, the output capacitor should be limited so that the input voltage stays above a valid voltage during the output recharge event. Usually, the output capacitor value of 33µF or less is recommended for 1m charger cable.

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ≤ 2kV (Human Body Model) encountered during handling and assembly. INA and INB are further protected against ESD up to ±15kV (Human Body Model), ±15kV (Air-Gap Discharge method described in IEC 61000-4-2) and ±8kV (Contact discharge method described in IEC 61000-4-2) without damage.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the devices continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model ESD Protection

Figure 4 shows the HBM and Figure 5 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 6 shows the IEC 61000-4-2 model. Figure 7 shows the current waveform for the IEC 61000-4-2 ESD contact discharge test.

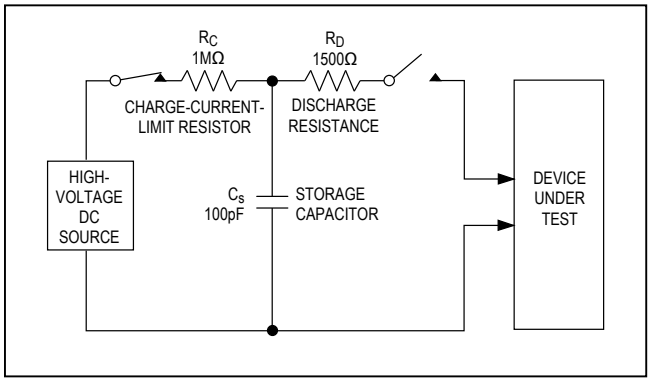


Figure 4. Human Body ESD Test Model

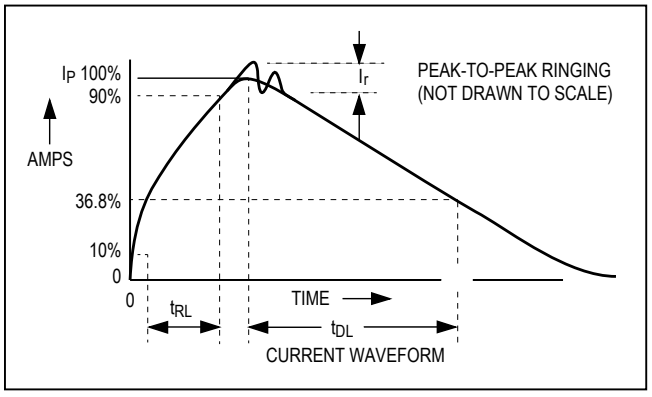


Figure 5. Human Body Current Waveform

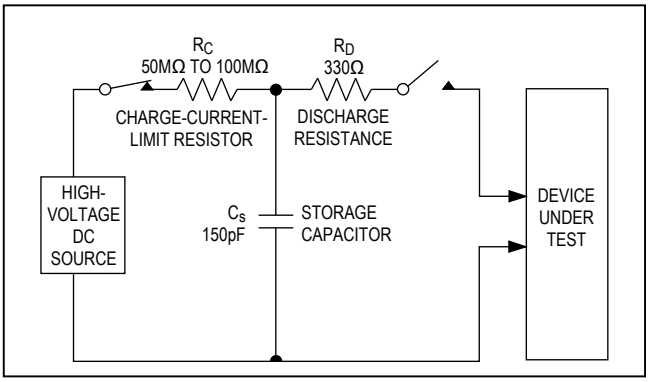


Figure 6. IEC 61000-4-2 ESD Test Model

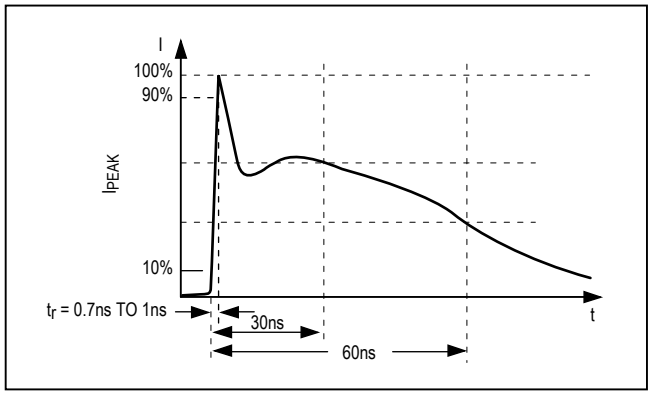


Figure 7. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information/Selector Guide

PART	OVLO (V)	PIN-PACKAGE	TEMP
MAX14727EWV+	13.75	30 WLP	-40°C TO +85°C
MAX14728EWV+	10	30 WLP	-40°C TO +85°C
MAX14731EWV+	5.92	30 WLP	-40°C TO +85°C

+Denotes a lead(Pb)-free package/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30 WLP	W302F2+1	**21-0762**	Refer to **Application Note 1891**