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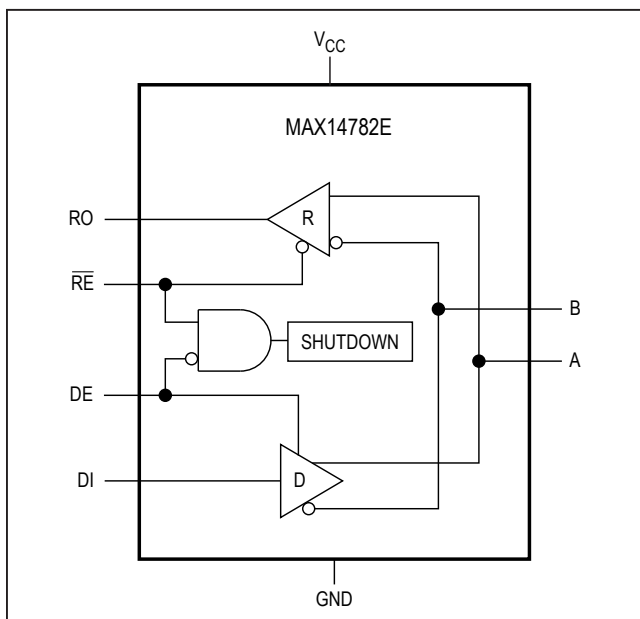
MAX14782E

500Kbps 3.3V to 5V RS-485/RS-422 Transceiver with $\pm 35\text{kV}$ HBM ESD Protection

General Description

The MAX14782E is a half duplex RS-485/422 transceiver that operates at either 3.3V or 5V rails with high $\pm 35\text{kV}$ ESD performance and up to 500kbps data rate.

Functional Diagram



Benefits and Features

- Integrated Protection Increases End Equipment Up-Time
 - High ESD Protection
 - $\pm 35\text{kV}$ HBM ESD per JEDEC JS-001-2012
 - $\pm 20\text{kV}$ Air Gap ESD per IEC 61000-4-2
 - $\pm 12\text{kV}$ Contact ESD per IEC 61000-4-2
 - $\pm 4\text{kV}$ EFT per IEC 61000-4-4
 - Short-Circuit-Protected Outputs
 - True Fail-Safe Receiver Prevents False Transition-on Receiver Input Short or Open Events
 - Hot-Swap Capability Eliminates False Transitions During Power-Up or Hot Insertion
- 3V to 5.5V Supply Voltage Range
- Data Rates up to 500kbps
- -40°C to $+125^{\circ}\text{C}$ Operating Temperature
- Allows Up to 32 Transceivers On the Bus
- Low $10\mu\text{A}$ (max) Shutdown Current for Lower Power Consumption

Applications

- Motion Controllers
- Field Bus Networks
- Encoder Interfaces
- Backplane Buses

[Ordering Information/Selector Guide](#) appear at end of data sheet.

Absolute Maximum Ratings

(Voltages referenced to GND.)

| | |
|------------------------------------------------|-----------------------------------|
| V _{CC} | -0.3V to +6.0V |
| RO | -0.3V to (V _{CC} + 0.3V) |
| RE, DE, DI | -0.3V to +6.0V |
| A, B (V _{CC} ≥ 3.6V) | -8.0V to +13.0V |
| A, B (V _{CC} < 3.6V) | -9.0V to +13.0V |
| Short-Circuit Duration (RO, A, B) to GND | Continuous |
| Operating Temperature Range | |
| MAX14782EA_ | -40°C to +125°C |

| | |
|-------------------------------------------------------|-----------------|
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Continuous Power Dissipation (T _A = +70°C) | |
| SO (derate at 7.6mW/°C above +70°C) | 606mW |
| TDFN-EP (derate at 24.4mW/°C above +70°C) | 1951mW |
| μMAX (derate at 4.8mW/°C above +70°C) | 387mW |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

| | |
|---------------------------------------------|-------------------------|
| PACKAGE TYPE: 8 SO | |
| Package Code | S8+4 |
| Outline Number | 21-0041 |
| Land Pattern Number | 90-0096 |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction to Ambient (θ _{JA}) | 132°C/W |
| Junction to Case (θ _{JC}) | 38°C/W |

| | |
|---------------------------------------------|-------------------------|
| PACKAGE TYPE: 8 TDFN | |
| Package Code | T833+2 |
| Outline Number | 21-0137 |
| Land Pattern Number | 90-0059 |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction to Ambient (θ _{JA}) | 41°C/W |
| Junction to Case (θ _{JC}) | 8°C/W |

| | |
|---------------------------------------------|-------------------------|
| PACKAGE TYPE: 8 μMAX | |
| Package Code | U8+1 |
| Outline Number | 21-0036 |
| Land Pattern Number | 90-0092 |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction to Ambient (θ _{JA}) | 206°C/W |
| Junction to Case (θ _{JC}) | 42°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical values are at $V_{CC} = +5\text{V}$ and $T_A = +25^\circ\text{C}$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------------------------------------|-----------------|-----------------------------------------------------------------------------------------|------------------------|------|---------|---------------|
| POWER SUPPLY | | | | | | |
| Supply Voltage | V_{CC} | | 3.0 | | 5.5 | V |
| Supply Current | I_{CC} | $DE = V_{CC}$, $\overline{RE} = \text{GND}$, no load | | 1.9 | 4 | mA |
| Shutdown Supply Current | I_{SHDN} | $DE = \text{GND}$, $\overline{RE} = V_{CC}$ | | | 10 | μA |
| DRIVER | | | | | | |
| Differential Driver Output | V_{OD} | $V_{CC} = 4.5\text{V}$, $R_L = 54\Omega$, Figure 1 | 2.1 | | V | |
| | | $V_{CC} = 3\text{V}$, $R_L = 100\Omega$, Figure 1 | 2.0 | | | |
| | | $V_{CC} = 3\text{V}$, $R_L = 54\Omega$, Figure 1 | 1.5 | | | |
| Change in Magnitude of Differential Output Voltage | ΔV_{OD} | $R_L = 54\Omega$ or 100Ω , Figure 1 (Note 3) | -0.2 | 0 | +0.2 | V |
| Driver Common-Mode Output Voltage | V_{OC} | $R_L = 54\Omega$ or 100Ω , Figure 1 | $V_{CC} / 2$ | | 3 | V |
| Change in Magnitude of Common-Mode Voltage | ΔV_{OC} | $R_L = 54\Omega$ or 100Ω , Figure 1 (Note 3) | -0.2 | | +0.2 | V |
| Single-Ended Driver Output High | V_{OH} | A or B output, $I_{A \text{ or } B} = -20\text{mA}$ | 2.2 | | | V |
| Single-Ended Driver Output Low | V_{OL} | A or B output, $I_{A \text{ or } B} = 20\text{mA}$ | | | 0.8 | V |
| Differential Output Capacitance | C_{OD} | $DE = \overline{RE} = V_{CC}$, $f = 4\text{MHz}$ | 12 | | | pF |
| Driver Short-Circuit Output Current | $ I_{OST} $ | $0 \leq V_{OUT} \leq +12\text{V}$, output low | | | 250 | mA |
| | | $-7\text{V} \leq V_{OUT} \leq V_{CC}$, output high | | | 250 | |
| RECEIVER | | | | | | |
| Input Current | $I_{A, B}$ | $DE = \text{GND}$, $V_{CC} = \text{GND}$ or $+5.5\text{V}$ | $V_{IN} = +12\text{V}$ | 400 | 1000 | μA |
| | | | $V_{IN} = -7\text{V}$ | -800 | +300 | |
| Differential Input Capacitance | $C_{A, B}$ | Between A and B, $DE = \text{GND}$, $f = 4\text{MHz}$ | 12 | | | pF |
| Receiver Differential Threshold Voltage | V_{TH} | $-7\text{V} \leq V_{CM} \leq +12\text{V}$ | -200 | -105 | -10 | mV |
| Receiver Input Hysteresis | ΔV_{TH} | $V_{CM} = 0\text{V}$ | 10 | | | mV |
| Receiver Input Resistance | R_{IN} | $-7\text{V} \leq V_{CM} \leq +12\text{V}$ | 12 | | | k Ω |
| LOGIC INTERFACE (DI, DE, \overline{RE}, RO) | | | | | | |
| Input-Voltage High | V_{IH} | DE, DI, \overline{RE} | 2.0 | | | V |
| Input-Voltage Low | V_{IL} | DE, DI, \overline{RE} | | | 0.8 | V |
| Input Hysteresis | V_{HYS} | DE, DI, \overline{RE} | 50 | | | mV |
| Input Current | I_{IN} | DE, DI, \overline{RE} | | | ± 1 | μA |
| Input Impedance on First Transition | | DE, \overline{RE} | 1 | | 10 | k Ω |
| RO Output-Voltage High | V_{OHRO} | $\overline{RE} = \text{GND}$, $I_{RO} = -2\text{mA}$, $(V_A - V_B) > 200\text{mV}$ | $V_{CC} - 0.4$ | | | V |
| RO Output-Voltage Low | V_{OLRO} | $\overline{RE} = \text{GND}$, $I_{RO} = 2\text{mA}$, $(V_A - V_B) < -200\text{mV}$ | | | 0.4 | V |

Electrical Characteristics (continued)(V_{CC} = +3.0V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|-------------------|-----------------------------------------------------|-----|------|------|-------|
| Receiver Three-State Output Current | I _{OZR} | $\overline{RE} = V_{CC}, 0 \leq V_{RO} \leq V_{CC}$ | | | ±1 | μA |
| Receiver Output Short-Circuit Current | I _{OSR} | $0 \leq V_{RO} \leq V_{CC}$ | | | ±110 | mA |
| PROTECTION | | | | | | |
| Thermal-Shutdown Threshold | T _{SHDN} | Temperature rising | | +160 | | °C |
| Thermal-Shutdown Hysteresis | | | | 15 | | °C |
| ESD Protection on A and B Pins | | IEC 61000-4-2 Air-Gap Discharge to GND | | ±20 | | kV |
| | | IEC 61000-4-2 Contact Discharge to GND | | ±12 | | |
| | | Human Body Model | | ±35 | | |
| ESD Protection, All Other Pins | | Human Body Model | | ±2 | | kV |

Switching Characteristics(V_{CC} = +3V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2, 4)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------|-----|-----|------|-------|
| DRIVER | | | | | | |
| Driver Propagation Delay | t _{DPLH} | R _L = 54Ω, C _L = 50pF, Figures 2 and 3 | | | 20 | ns |
| | t _{DPHL} | | | | 20 | |
| Driver Differential Output Rise or Fall Time | t _{HL} , t _{LH} | R _L = 54Ω, C _L = 50pF, Figures 2 and 3 | 200 | | 600 | ns |
| Differential Driver Output Skew t _{DPLH} - t _{DPHL} | t _{DSKEW} | R _L = 54Ω, C _L = 50pF, Figures 2 and 3 | | | 140 | ns |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Driver Enable to Output High | t _{DZH} | R _L = 110Ω, C _L = 50pF, Figures 4 and 5 (Note 5) | | | 2500 | ns |
| Driver Enable to Output Low | t _{DZL} | R _L = 110Ω, C _L = 50pF, Figures 4 and 5 (Note 5) | | | 2500 | ns |
| Driver Disable Time from Low | t _{DLZ} | R _L = 110Ω, C _L = 50pF, Figures 4 and 5 | | | 100 | ns |
| Driver Disable Time from High | t _{DHZ} | R _L = 110Ω, C _L = 50pF, Figures 4 and 5 | | | 100 | ns |
| Driver Enable from Shutdown to Output High | t _{DLZ(SHDN)} | R _L = 110Ω, C _L = 15pF, Figures 4 and 5 (Note 5) | | | 5.5 | μs |
| Driver Enable from Shutdown to Output Low | t _{DHZ(SHDN)} | R _L = 110Ω, C _L = 15pF, Figures 4 and 5 (Note 5) | | | 5.5 | μs |
| Time to Shutdown | t _{SHDN} | (Note 6) | 50 | 340 | 700 | ns |

Switching Characteristics MAX14782E (continued)(V_{CC} = +3V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2, 4)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------------------|------------------------|-------------------------------------------------------------------------|-----|-----|-----|---------------|
| RECEIVER | | | | | | |
| Receiver Propagation Delay | t _{RPLH} | C _L = 15pF, Figures 6 and 7 | | | 200 | ns |
| | t _{RPHL} | | | | 200 | |
| Receiver Output Skew | t _{RSKEW} | C _L = 15pF, Figures 6 and 7 (Note 6) | | | 30 | ns |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Receiver Enable to Output High | t _{RZH} | R _L = 1k Ω , C _L = 15pF, Figure 8 (Note 5) | | | 50 | ns |
| Receiver Enable to Output Low | t _{RZL} | R _L = 1k Ω , C _L = 15pF, Figure 8 (Note 5) | | | 50 | ns |
| Receiver Disable Time from Low | t _{RLZ} | R _L = 1k Ω , C _L = 15pF, Figure 8 | | | 50 | ns |
| Receiver Disable Time from High | t _{RHZ} | R _L = 1k Ω , C _L = 15pF, Figure 8 | | | 50 | ns |
| Receiver Enable from Shutdown to Output High | t _{RLZ(SHDN)} | R _L = 1k Ω , C _L = 15pF, Figure 8 (Note 5) | | | 5.5 | μs |
| Receiver Enable from Shutdown to Output Low | t _{RHZ(SHDN)} | R _L = 1k Ω , C _L = 15pF, Figure 8 (Note 5) | | | 5.5 | μs |
| Time to Shutdown | t _{SHDN} | (Note 6) | 50 | 340 | 700 | ns |

Note 1: All devices 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.**Note 2:** All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to ground, unless otherwise noted.**Note 3:** ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.**Note 4:** Capacitive load includes test probe and fixture capacitance.**Note 5:** Guaranteed by design; not production tested.**Note 6:** The timing parameter refers to the driver or receiver enable delay, when the device has exited the initial hot-swap protect state and is in normal operating mode.

Test and Timing Diagrams

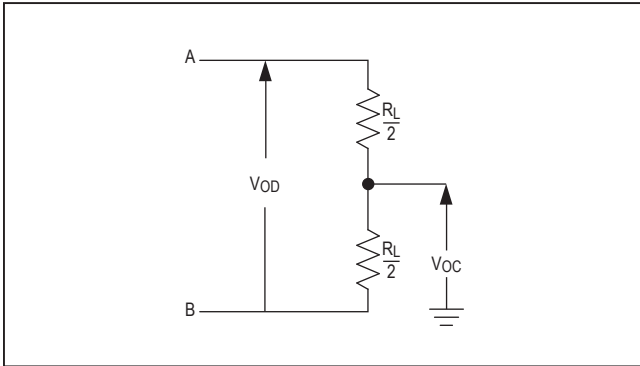


Figure 1. Driver DC Test Load

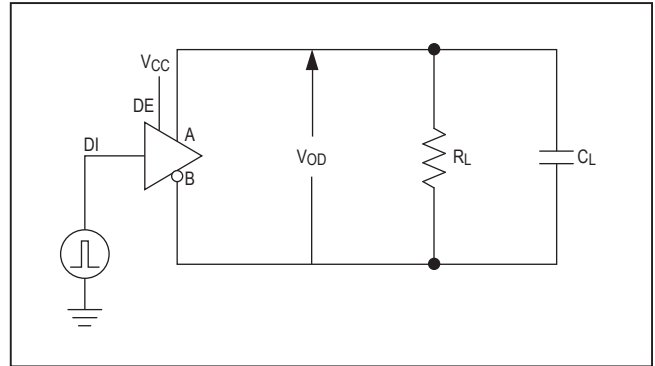


Figure 2. Driver Timing Test Circuit

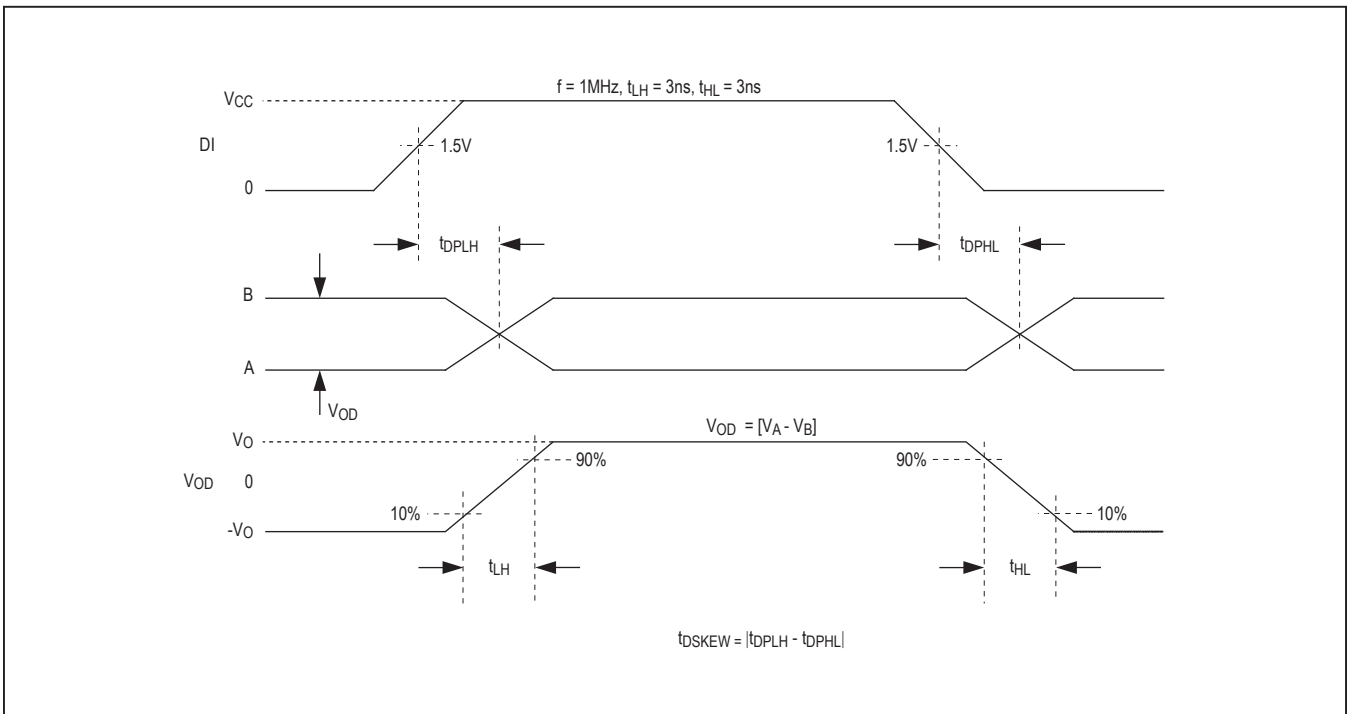


Figure 3. Driver Propagation Delays

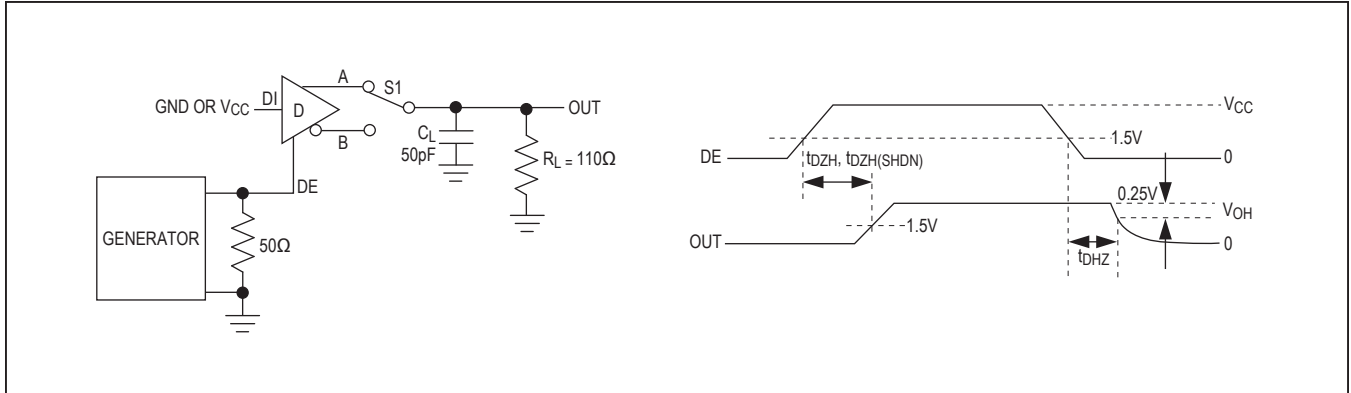


Figure 4. Driver Enable and Disable Times (t_{DZH} , t_{DZH})

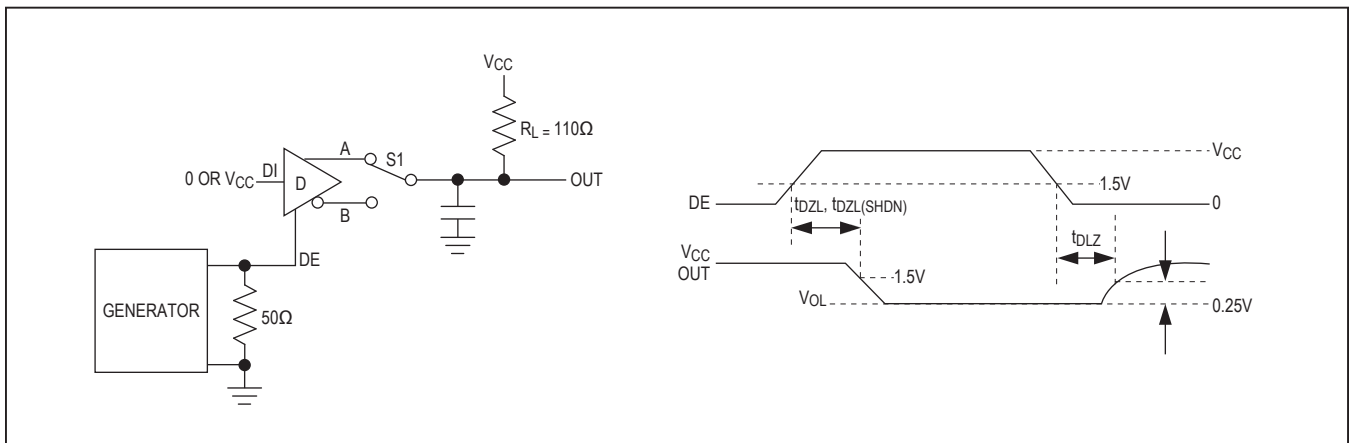


Figure 5. Driver Enable and Disable Times (t_{DZL} , t_{DZL})

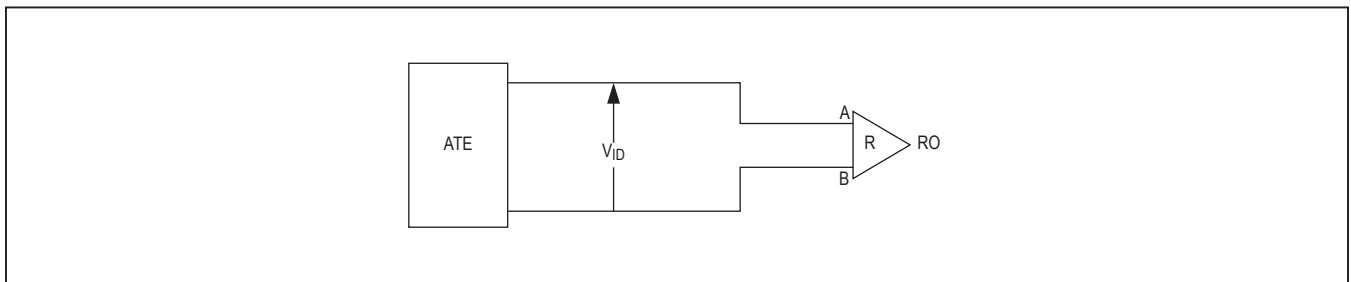


Figure 6. Receiver Propagation Delay Test Circuit

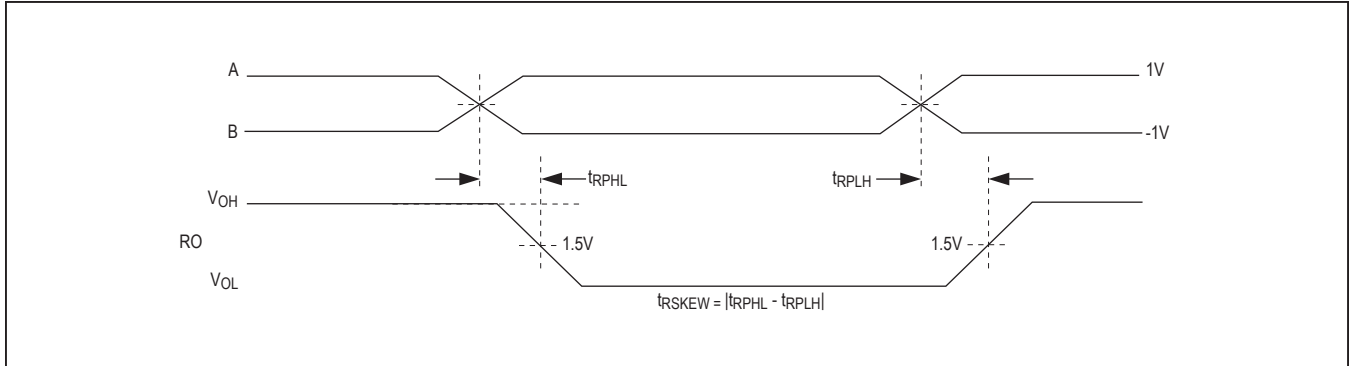


Figure 7. Receiver Propagation Delays

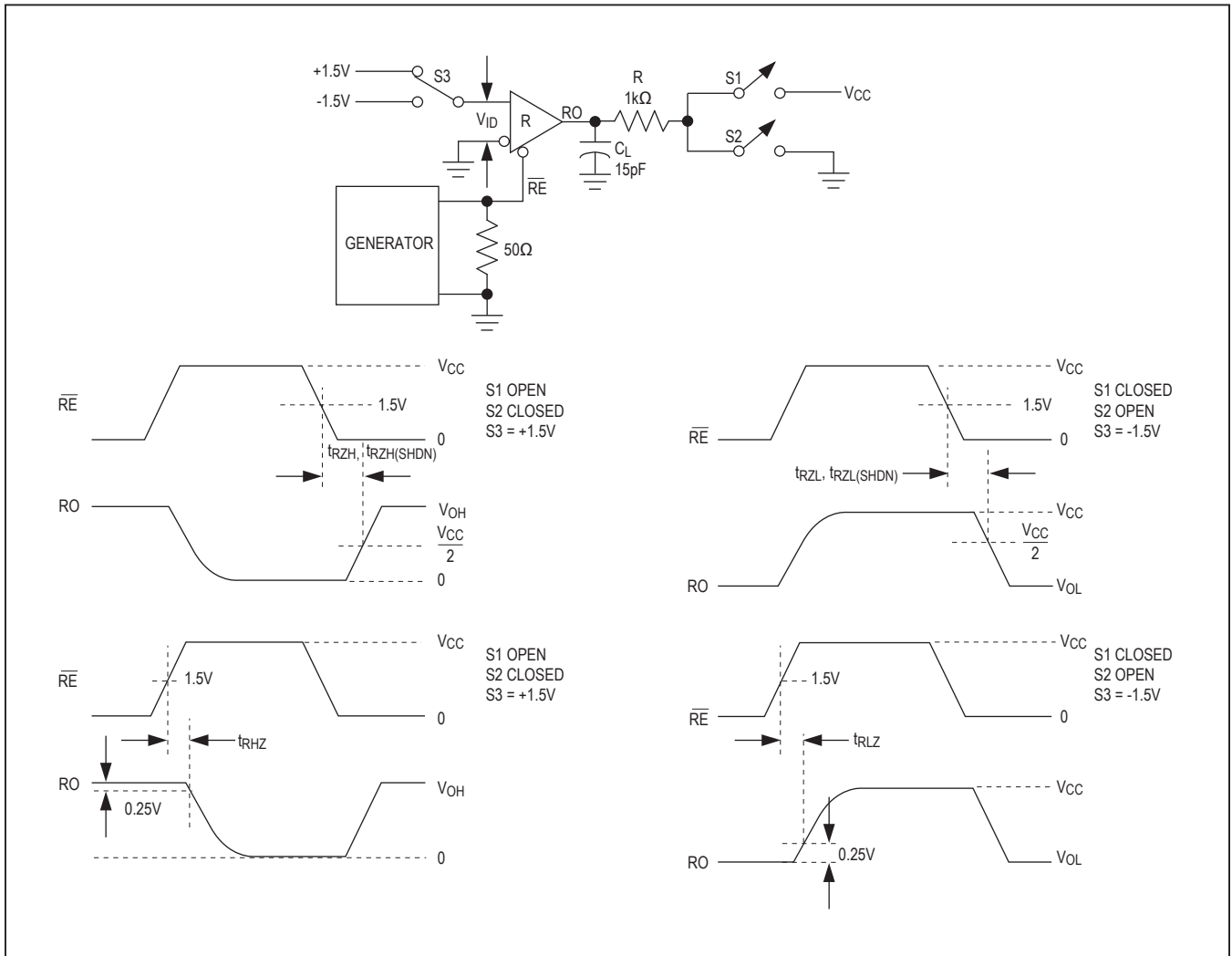
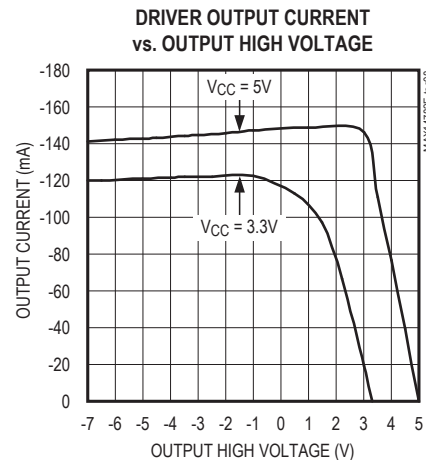
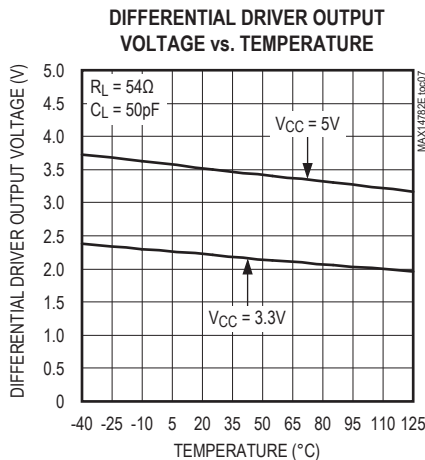
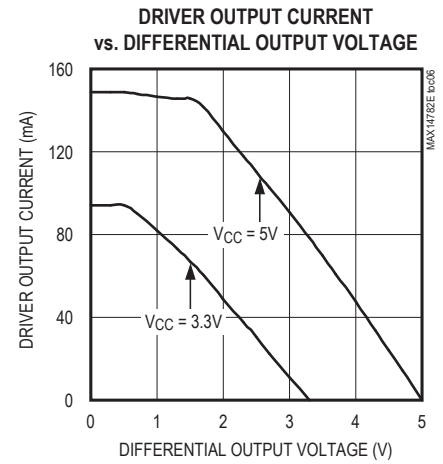
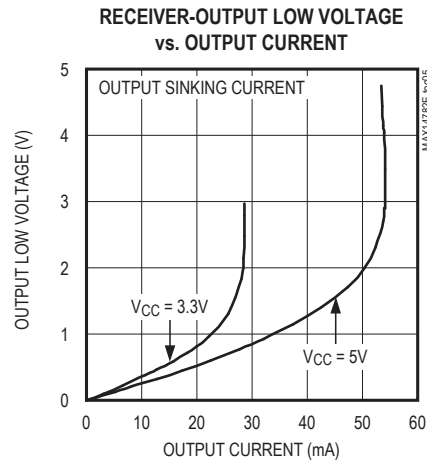
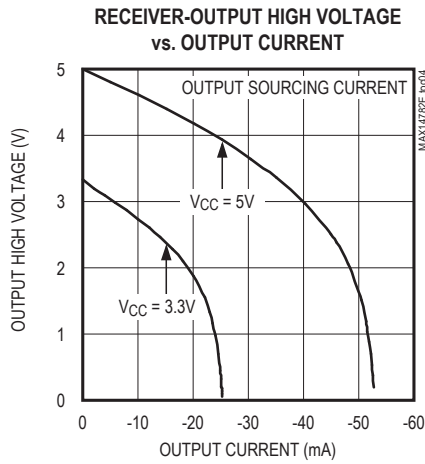
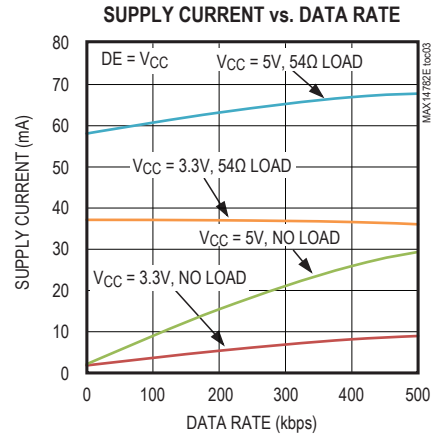
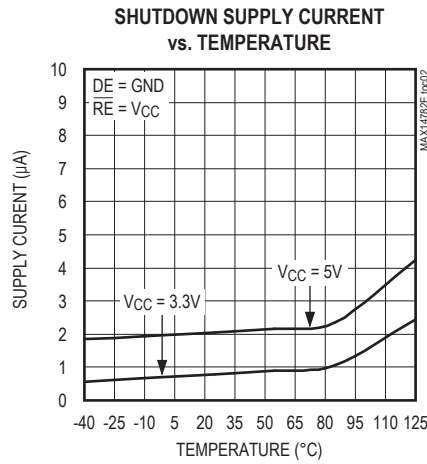
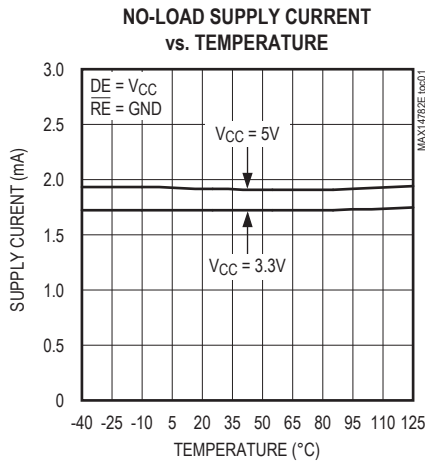


Figure 8. Receiver Enable and Disable Times

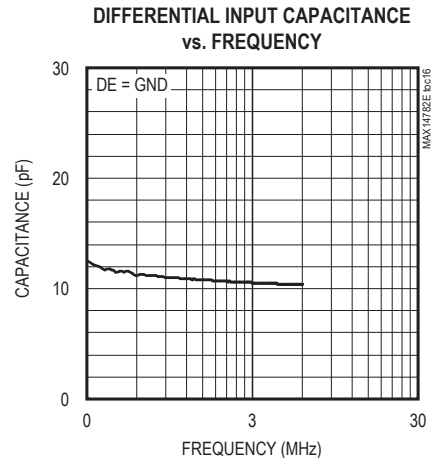
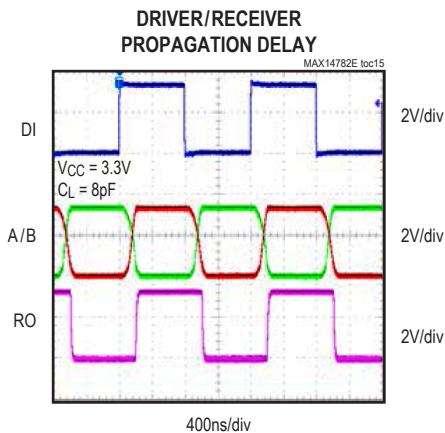
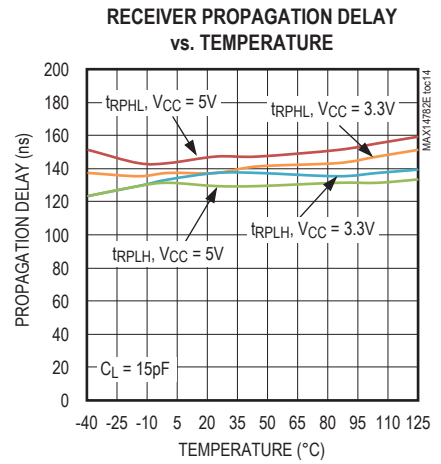
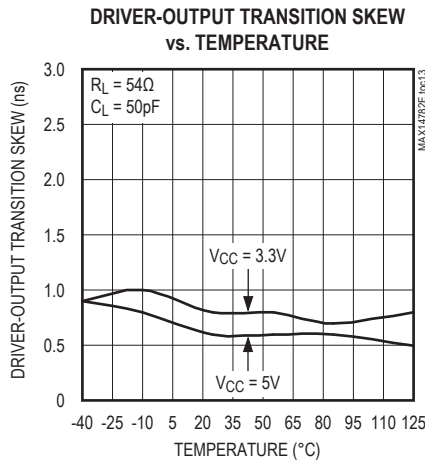
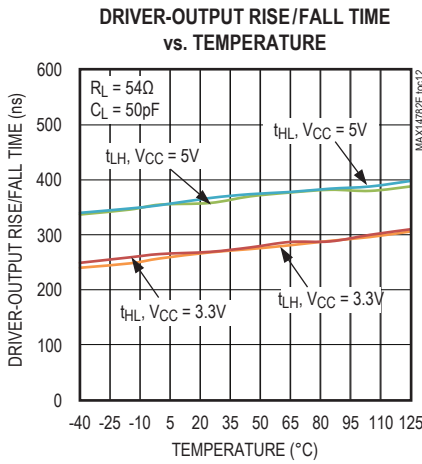
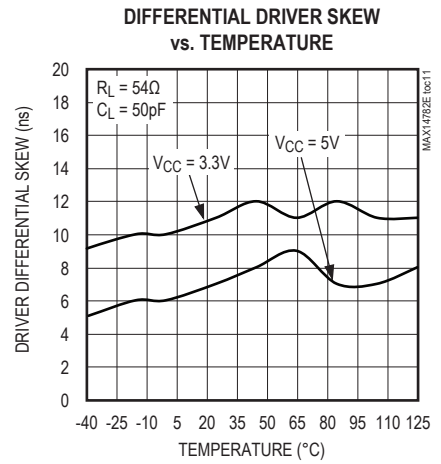
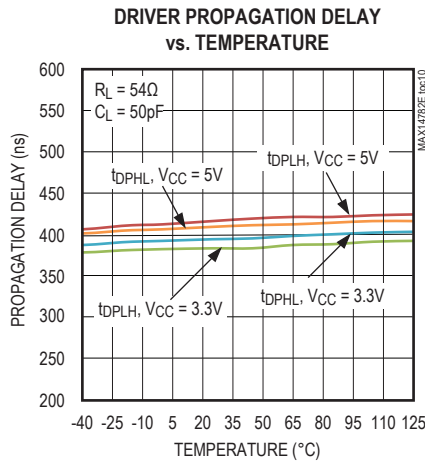
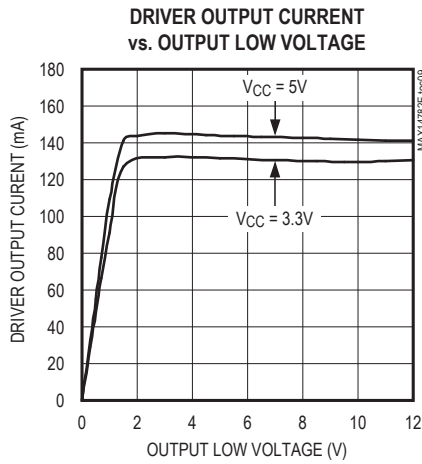
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise specified.)

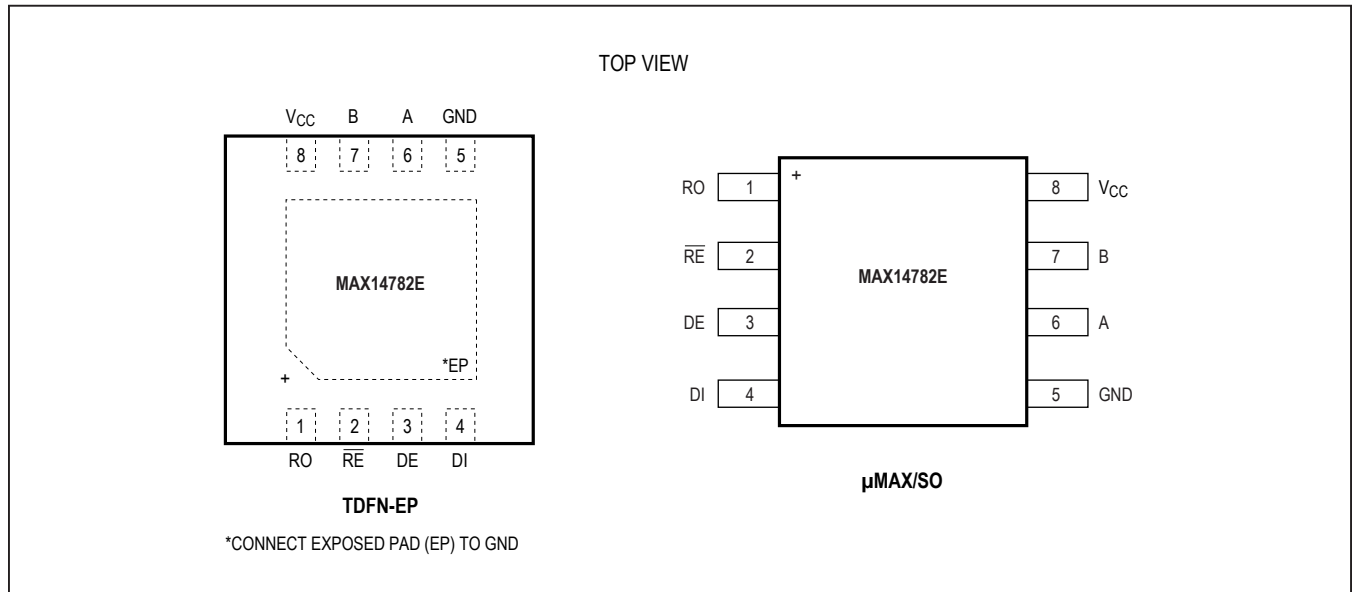


Typical Operating Characteristics (continued)

(V_{CC} = +3.0V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)



Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-----|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | RO | Receiver Output. See <i>Function Tables</i> . |
| 2 | \overline{RE} | Receiver Output Enable. Drive \overline{RE} low to enable RO. Drive \overline{RE} high to disable the receiver. RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and pull DE low to enter low-power shutdown mode. |
| 3 | DE | Driver Output Enable. Drive DE high to enable the driver. Drive DE low to disable the driver. Driver outputs are high-impedance when the driver is disabled. Drive \overline{RE} high and pull DE low to enter low-power shutdown mode. |
| 4 | DI | Driver Input. With DE high, a low on DI forces the A output low and the B output high. Similarly, a high on DI forces the A output high and B output low. |
| 5 | GND | Ground |
| 6 | A | Noninverting RS-485/RS-422 Receiver Input and Driver Output |
| 7 | B | Inverting RS-485/RS-422 Receiver Input and Driver Output |
| 8 | V _{CC} | Positive Supply Voltage Input. Bypass V _{CC} with a 0.1μF ceramic capacitor to ground. |
| — | EP | Exposed Pad (TDFN only). Connect EP to GND. |

Function Tables

| TRANSMITTING | | | | | |
|--------------|----|----|----------------|---|-----------------|
| INPUTS | | | OUTPUTS | | MODE |
| RE | DE | DI | B | A | |
| X | 1 | 1 | 0 | 1 | Active |
| X | 1 | 0 | 1 | 0 | Active |
| 0 | 0 | X | High Impedance | | Driver Disabled |
| 1 | 0 | X | High Impedance | | Shutdown |

| RECEIVING | | | | | |
|-----------|----|----------------------|----------------|--------|-------------------|
| INPUTS | | | OUTPUTS | MODE | |
| RE | DE | A-B | RO | | |
| 0 | X | $\geq -10\text{mV}$ | 1 | Active | |
| 0 | X | $\leq -200\text{mV}$ | 0 | Active | |
| 0 | X | Open/Shorted | 1 | Active | |
| 1 | 1 | X | High Impedance | | Receiver Disabled |
| 1 | 0 | X | High Impedance | | Shutdown |

X = Don't care

Detailed Description

The MAX14782E is a 3.3V to 5V ESD-protected RS-485/RS-422 transceiver intended for high-speed, half-duplex communications. Integrated hot-swap functionality eliminates false transitions on the bus during power-up or hot insertion.

The device features fail-safe receiver inputs guaranteeing a logic-high receiver output when inputs are shorted or open. The IC has a 1-unit load receiver input impedance, allowing up to 32 transceivers on the bus.

True Fail Safe

The MAX14782E guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. If the differential receiver input voltage (A–B) is greater than or equal to -10mV , RO is logic-high.

Driver Single-Ended Operation

The A and B outputs can either be used in the standard differential operating mode, or can be used as single-ended outputs. Since the A and B driver outputs swing rail-to-rail, they can individually be used as standard TTL logic outputs.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted in a hot or powered backplane, disturbances on the enable inputs and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the processor output drivers are high impedance and are unable to drive the DE and $\overline{\text{RE}}$ inputs of the MAX14782E to a defined logic level. Leakage currents up to $10\mu\text{A}$ from the high-impedance outputs of a controller could cause DE and $\overline{\text{RE}}$ to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE and $\overline{\text{RE}}$. These factors could improperly enable the driver or receiver. The MAX14782E features integrated hot-swap inputs that help to avoid these potential problems.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{\text{RE}}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap-tolerable inputs.

Hot-Swap Input Circuitry

The DE and $\overline{\text{RE}}$ enable inputs feature hot-swap capability. At the input, there are two nMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from 0V, an internal $10\mu\text{s}$ timer turns on M2 and sets the SR latch that also turns

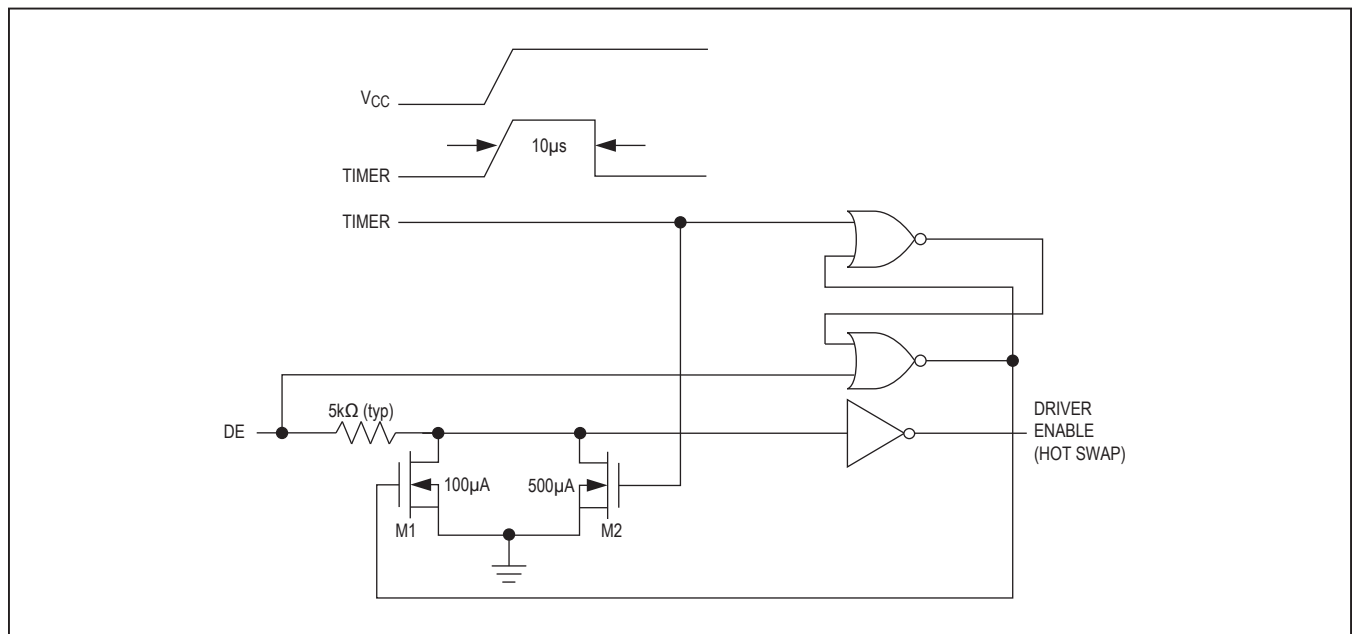


Figure 9. Simplified Structure of the Driver Enable (DE) Pin

on M1. Transistors M2 (a 500µA current sink) and M1 (a 100µA current sink) pull DE to GND through a 5kΩ (typ) resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

A complementary circuit employing two pMOS devices pulls RE to V_{CC}.

±35kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14782E have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX14782E keeps working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14782E are characterized for protection to the following limits:

- ±35kV HBM
- ±20kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±12kV using the Contact Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 10 shows the HBM, and Figure 11 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14782E helps in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

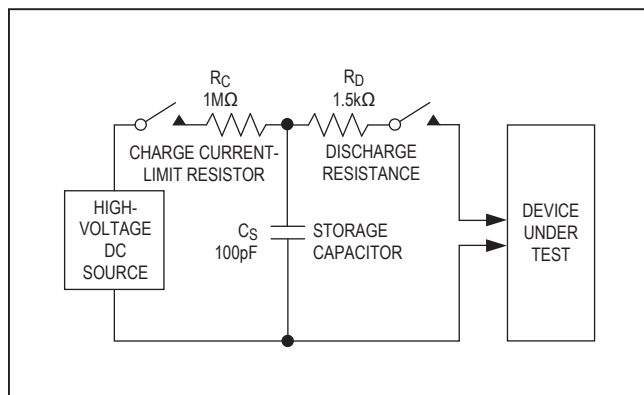


Figure 10. Human Body ESD Test Model

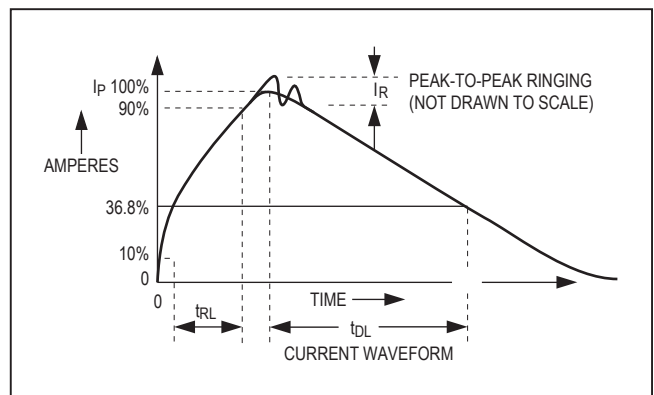


Figure 11. Human Body Current Waveform

Figure 12 shows the IEC 61000-4-2 model, and Figure 13 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Applications Information

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus connection. The first, a current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing \overline{RE} high and DE low. In shutdown, the devices draw less than 10µA of supply current.

\overline{RE} and DE can be connected together and driven simultaneously. The MAX14782E is guaranteed not to enter shutdown if \overline{RE} is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns (max), the device is guaranteed to enter shutdown.

Typical Applications

The MAX14782E transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 14 shows a typical network application circuit. To minimize reflections, terminate the line at both ends with its characteristic impedance and keep stub lengths off the main line as short as possible.

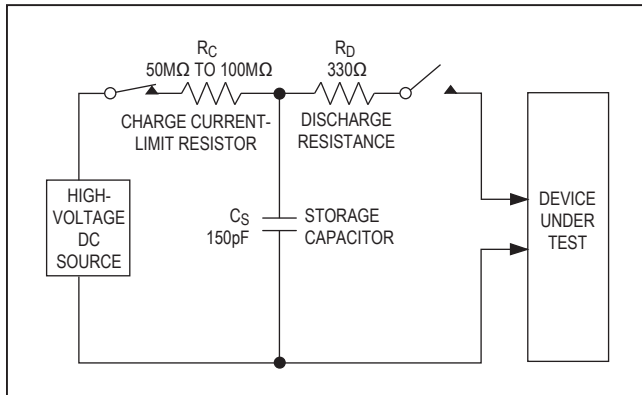


Figure 12. IEC 61000-4-2 ESD Test Model

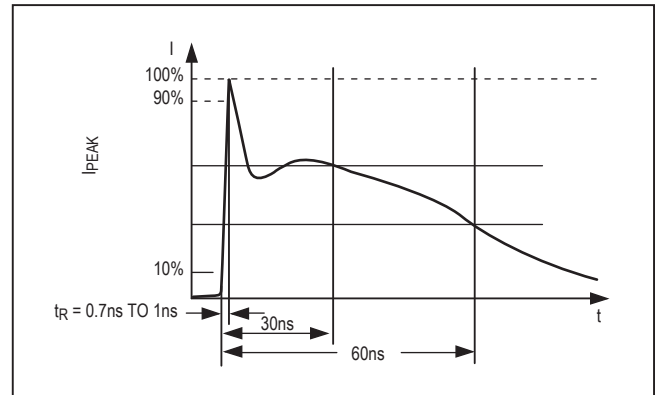


Figure 13. IEC 61000-4-2 ESD Generator Current Waveform

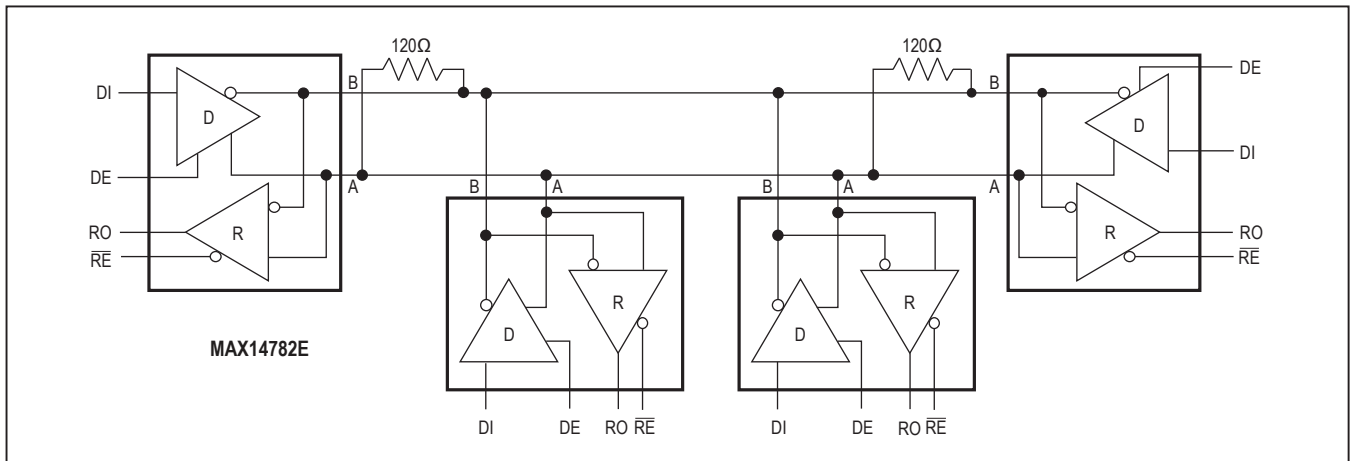


Figure 14. Typical Half-Duplex RS-485 Network

MAX14782E

500Kbps 3.3V to 5V RS-485/RS-422 Transceiver
with $\pm 35\text{kV}$ HBM ESD Protection

Ordering Information/Selector Guide

| PART | SUPPLY RANGE | DATA RATE (MAX) | TEMP RANGE | PIN-PACKAGE |
|----------------|--------------|-----------------|-----------------|-------------|
| MAX14782EASA+ | 3.0V to 5.5V | 500kbps | -40°C to +125°C | 8 SO |
| MAX14782EATA+ | 3.0V to 5.5V | 500kbps | -40°C to +125°C | 8 TDFN-EP* |
| MAX14782EAUJA+ | 3.0V to 5.5V | 500kbps | -40°C to +125°C | 8 μ MAX |

μ Max is a registered trademark of Maxim Integrated Products, Inc.

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed paddle.*

Chip Information

PROCESS: BiCMOS