Click here for production status of specific part numbers.

MAX14813

Ultra-Compact Octal 3L/Quad 5L Pulser with T/R Switches and Beamforming Capability

General Description

The MAX14813 is a very high density, high-voltage ultrasound transmitter (pulser) in a wafer-level package (WLP). It is particularly aimed to address ultrasound imaging applications in which PCB space is a concern.

It features eight 3-level channels operating from two independent pairs of HV supplies. Each channel can transmit up to $170V_{P-P}$ with up to 2.1A current capability. The current capability can be programmed down to 0.35A with 4 steps of programmability. It also features an integrated 1A active clamp (Return to Zero).

The MAX14813 can also be configured as a quad 5-levels (2.1A) pulser plus quad active T/R switches.

The MAX14813 features embedded digital resources (SRAM and state machine) that can be used to support transmit beamforming resulting in a dramatic saving of the number of interconnects and FPGA I/Os. The embedded digital resources are programmed through an high speed serial interface and supports sophisticated transmit techniques likewise pulse width modulation for burst-shaping and apodization for beam shaping.

Alternatively, the device can be controlled in a conventional manner by an external digital source (FPGA or similar) through dedicated CMOS logic inputs.

The MAX14813 features independent active T/R switches. The T/R switches can possibly be externally configured to support Receive Multiplexing in which a fewer number of receive than transmit channels are used.

The MAX14813 is packaged into a 6.33mm x 6.65mm WLP, with a 12 x 13 ball grid array.

Applications

- Ultrasound Medical Imaging
- Ultrasound Industrial Applications (NDT)

Ordering Information appears at end of data sheet.

Benefits and Features

- Optimized for Compact and Portable Applications
  - High Density Eight Channels 3 Levels Pulser in a 6.33mm x 6.65mm WLP
  - Integrated Low-Power, Low-Noise, Active T/R Switches
  - Direct-Drive Architecture Eliminates External Floating Power Supply (FPS) and HV Signal Capacitors
  - Embedded Beamforming Eliminates Transmit FPGA, Simplifies PCB Layout, and Eases Synchronization
- Flexibility
  - Support Receive Multiplexing
  - Can Use Internal/External Beamforming Resources
  - Can Operate as Octal 3 Levels or Quad 5 Levels
- Embedded Digital Resources for Beamforming
  - 8K Samples (Per Channel) Pulse Wave Table SRAM Stores Up to 1024 Unique Patterns
  - Line Number Memory Stores Beamforming Line Information For Up To 1.5K Lines (3 Levels) or 3K Lines (5 Levels)
  - 128 Line Type Registers Stores Setting Information for All the Channels
  - State Machine for Delay Beamforming with 5ns Time Resolution
  - Programmable Number of Cycles and Pattern Time Base (Pulse Width)
- High Performance (Designed to Enhance Image Quality)
  - Excellent Second Harmonic distortion and Pulse Inversion Performances
  - Low Propagation Delay 12ns (typ) Ensures Excellent Phase Noise for Doppler Modes and Excellent Part-to-Part Matching
  - Fast Rising Falling Edges Enables Fine Resolution PWM or Acoustic Power Control
- Low Power
  - Low Quiescent Power Dissipation (4.1mW/Channel in Octal Mode)
  - Programmable Current Capability Down to 0.35A for CWD and Low-Voltage Modes
- Robustness
  - Thermal Warning at 110°C
  - Thermal Shutdown at 150°C

19-100096; Rev 1; 7/19

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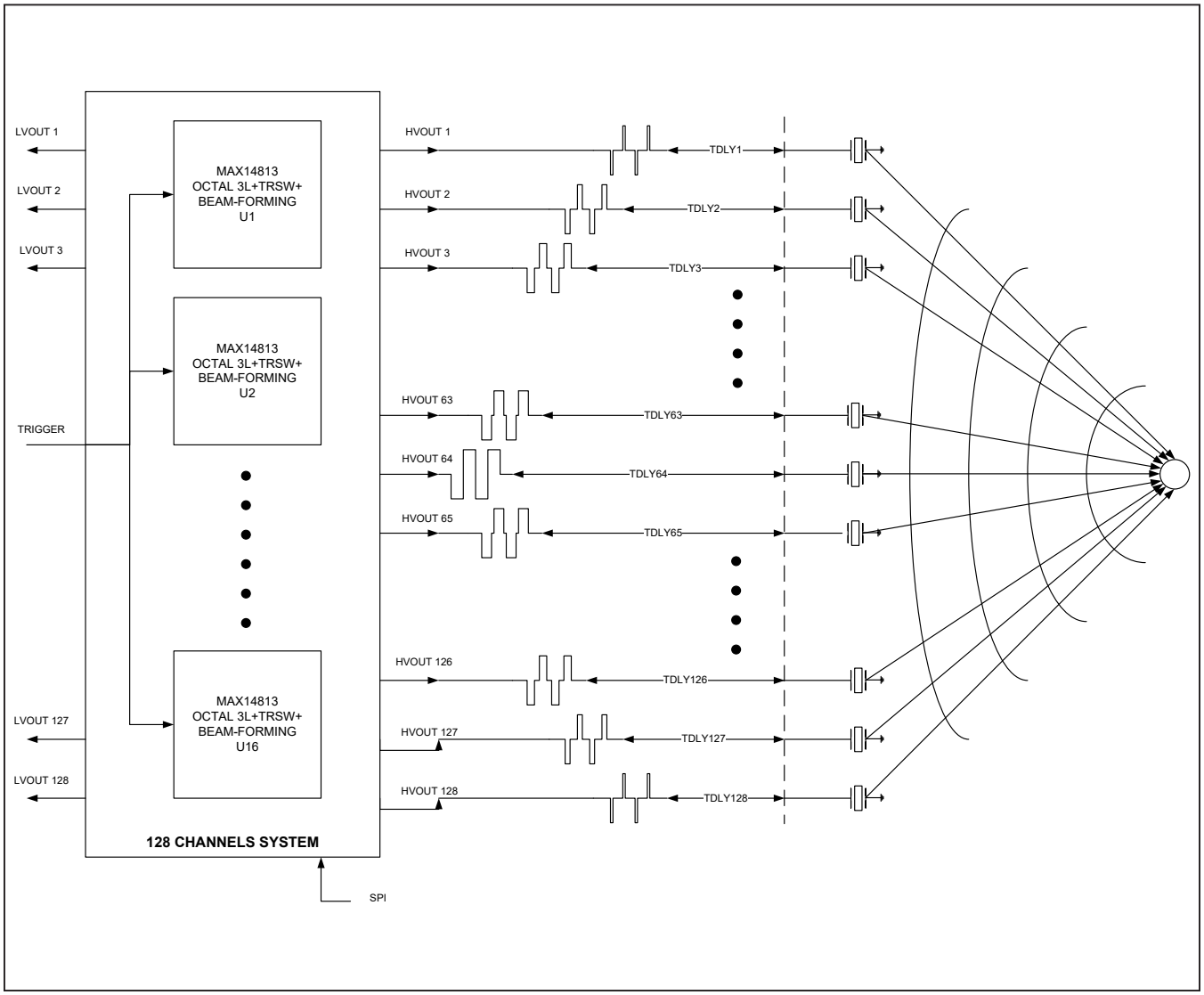
Simplified Block Diagram



Absolute Maximum Ratings

V_{IO} to GND.....-0.3V to +5.6V
V_{DD} to GND .....-0.3V to +2V
V_{CC} to GND .....-0.3V to +5.6V
V_{EE} to GND.....-5.6V to +0.3V
V_{PPA} to GND.....-0.3V to +110V
V_{NNA} to GND .....-110V to +0.3V
V_{NNB} to GND ..... V_{NNA} - 0.3V to +0.3V
V_{PPB} to GND.....-0.3V to V_{PPA} + 0.3V
V_{GNB} to GND ..... V_{NNB} - 0.3V to V_{NNB} + 5.6V
V_{GPA} to GND ..... V_{PPA} - 5.6V to V_{PPA} + 0.3V
V_{GNA} to GND ..... V_{NNA} - 0.3V to V_{NNA} + 5.6V
V_{GPB} to GND ..... V_{PPB} - 5.6V to V_{PPB} + 0.3V
HVOUTx to GND (x = 1..8) ..... V_{NNA} - 0.6V to V_{PPA} + 0.6V
LVOUTx to GND (x = 1..8) –
Current Limited at ±100mA.....-1V to +1V
THP to GND .....-0.3V to +5.6V
DINNx to GND (x = 1..8) .....-0.3V to +5.6V
DINPx to GND (x = 1..8) .....-0.3V to +5.6V
MODE2 to GND.....-0.3V to +5.6V
MODE1 to GND.....-0.3V to +5.6V
CLK to GND .....-0.3V to +5.6V
SYNC/INT to GND.....-0.3V to +5.6V
CC0 to GND .....-0.3V to V_{IO} + 0.3V
CC1 to GND .....-0.3V to V_{IO} + 0.3V
Operating Temperature Range.....0°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP156 6.65mm x 6.33mm

PACKAGE CODE	W1566A6+1
Outline Number	21-100007
Land Pattern Number	See Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	19
Junction to Case (θ_{JC})	NA

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range, $\overline{CC0}$ = 0V, $\overline{CC1}$ = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING VOLTAGE RATING						
I/O Logic Supply Voltage	V_{IO}		1.7		3.3	V
Positive Drive Supply Voltage	V_{CC}		4.75	5	5.25	V
Negative Drive Supply Voltage	V_{EE}		-5.25	-5	-4.75	V
High-side Supply Voltage	V_{PPA}		0		85	V
	V_{PPB}		0		V_{PPA}	
Low-side Supply Voltage	V_{NNA}		-85		0	V
	V_{NNB}		V_{NNA}		0	
LOGIC I/O PINS SPECIFICATIONS						
Low-level Input	V_{IL}				0.33 x V_{IO}	V
High-level Input	V_{IH}		0.66 x V_{IO}			V
Logic Input Pulldown Resistor	R_{IN}	Pins: MODE_, CC_, CLK	70	100	130	KΩ
Logic Input Pulldown Resistor	R_{IN}	Pin SYNC	40	60	80	KΩ
Logic Input Differential Resistor	R_{DIFF}	PINS: INNx, INPx	70	100	130	kΩ
Input Leakage on Logic Inputs Pins	I_{LEAK}	All logic input pins aside MODE_, SYNC, CLK, CC_ Logic Input connected to V_{IO} or GND	-1		1	µA
Low Level Output Voltage pins THP (All Modes) and INT (Beamforming Mode Only)	V_{OL}	R_{PULLUP} = 1kΩ			0.1 x V_{IO}	V
Logic Input Capacitance	C_{IN}			4		pF
CURRENT CONSUMPTION SHUTDOWN MODE						
VIO Supply Current	I_{IO}	All Inputs connected to GND or V_{IO}.		5	12	µA
V_{EE} Supply Current	I_{EE}	All Inputs connected to GND or V_{IO}.		10	20	µA
V_{CC} Supply Current	I_{CC}	All Inputs connected to GND or V_{IO}.		70	120	µA
V_{NN} Supply Current	$I_{NN\_}$	All Inputs connected to GND or V_{IO}.		0	5	µA
V_{PP} Supply Current	$I_{PP\_}$	All Inputs connected to GND or V_{IO}.		0	5	µA
Total Power Dissipation in Shutdown		Shutdown Mode. Total power dissipation (8 channels)		0.4		mW

Electrical Characteristics (continued)

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range, $\overline{CC0}$ = 0V, $\overline{CC1}$ = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CURRENT CONSUMPTION/QUIESCENT–Direct-Mode Octal 3 Levels						
V_{IO} Supply Current - Quiescent	I_{IOQ}	All channels in receive mode		5	12	µA
V_{EE} Supply Current - Quiescent	I_{EEQ}	All channels in receive mode		210	350	µA
V_{CC} Supply Current - Quiescent	I_{CCQ}	All channels in receive mode		350	540	µA
V_{NN} Total Supply Current - Quiescent	I_{NNQ}	All channels in receive mode		150	250	µA
V_{PP} Total Supply Current - Quiescent	I_{PPQ}	All channels in receive mode		150	250	µA
Total Quiescent Power Dissipation per Channel	P_{DIS1}	Receive mode. Quiescent power per channel		4.1		mW
OPERATING CURRENT CONSUMPTION/CWD MODE–Normal Drop–Direct Mode Octal 3 Levels (Note 2)						
V_{IO} Supply Current	I_{IO1}	8 chs running CW mode		60	100	µA
V_{EE} Supply Current	I_{EE1}	8 chs running CW mode		8.8	13	mA
V_{CC} Supply Current	I_{CC1}	8 chs running CW mode		7.9	11	mA
V_{NN} Supply Current	I_{NN1}	8 chs running CW mode		90	130	mA
V_{PP} Supply Current	I_{PP1}	8 chs running CW mode		90	130	mA
Total CWD Power Dissipation per Channel	P_{dCW}	CWD Normal power per channel		122		mW
OPERATING CURRENT CONSUMPTION/CWD MODE–Low Drop–Beamforming Mode (Note 3)						
VIO Supply Current	I_{IO2}	8 chs running CW mode		6	12	µA
V_{EE} Supply Current	I_{EE2}	8 chs running CW mode		8.8	13	mA
V_{CC} Supply Current	I_{CC2}	8 chs running CW mode		10.4	14	mA
V_{NN} Supply Current	I_{NN2}	8 chs running CW mode		83	120	mA
V_{PP} Supply Current	I_{PP2}	8 chs running CW mode		83	120	mA
Total CWD Power Dissipation per channel	P_{dCW}	CWD Low drop power per channel		95		mW
OPERATING CURRENT CONSUMPTION / B MODE–Direct Mode Octal 3 Levels (Note 4)						
V_{IO} Supply Current	I_{IO3}	8 chs running B-mode		6	12	µA
V_{EE} Supply Current	I_{EE3}	8 chs running B-mode		0.25	0.6	mA
V_{CC} Supply Current	I_{CC3}	8 chs running B-mode		0.4	0.9	mA
V_{NN} Supply Current	I_{NN3}	8 chs running B-mode		2.9	4.6	mA
V_{PP} Supply Current	I_{PP3}	8 chs running B-mode		2	3	mA
Total B Mode Power Dissipation per Channel	PdB	B-mode power per channel		62		mW

Electrical Characteristics (continued)

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range, $\overline{CC0}$ = 0V, $\overline{CC1}$ = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVOUT - LVOUT PIN CHARACTERISTIC						
Small-Signal Total Parasitic Capacitor on HVOUT	CHVOUTSS	Vs = 100mV_{P-P}. T/R switch ON		30		pF
Equivalent Large-Signal Parasitic Capacitor on HVOUT	CHVOUTLS	Vs = 200V_{P-P} (Note 5)		55		pF
Bleed Resistor on HVOUT	R_{BLEED}	T/R switch OFF	15	27	38	KΩ
Bleed Resistor on LVOUT	R_{BLEED}	Small signal. T/R switch off.	33	55	67	KΩ
THERMAL PROTECTION SPECIFICATIONS						
Thermal warning Threshold	THP			110		°C
Thermal Warning Hysteresis	T_{HYS}			5		°C
Thermal Shutdown Threshold	T_{SHD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
1.8V LDO						
LDO Output Voltage	V_{DD}	Quiescent	1.72	1.8	1.87	V
LDO Dropout	Drop	I = 20mA		2.5		mV
FUNCTIONAL TIMINGS (Note 7)						
Output Enable Time From Shutdown Mode to Any Other Mode	T_{EN}				0.5	ms
Output Disable Time From Any Other Mode to Shutdown Mode	TDI		0.5		3	µs
Time From One Operating Mode to Any Other Mode (Except Shutdown)	T_{MODE}	From MODE [2:1] change to entering in new operating mode	0.5		3	µs
Transmit Setup Time (Direct Mode)	T_{SETTX}	From T/R switch off to start of transmission (Note 6)	0.8			µs
FUNCTIONAL TIMINGS (Note 7)/Beamforming Mode Timings						
Master Clock Frequency	Fmax				200	MHz
Master Clock Input Duty Cycle	Ckduty		40		60	%
TRIG to CLK Setup Time	Tset	Beamforming mode only.	1.25			ns
TRIG to CLK Hold Time	Thold	Beamforming mode only.	1.25			ns

Electrical Characteristics (continued)

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range, $\overline{CC0}$ = 0V, $\overline{CC1}$ = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FUNCTIONAL TIMINGS (Note 7)/Direct Mode Functional Timings						
Master Clock Frequency	F_{MAX}				200	MHz
Master Clock Input Duty Cycle	CK_{DUTY}		40		60	%
Data to CLK Setup Time	T_{SET}		1.25			ns
Data to CLK Hold Time	T_{HOLD}		1.25			ns
SPI–(Beamforming Mode Only)						
SCLK Write Period	T_{SCLKW}	Beamforming mode only. Serial Data Write.	20			ns
SDIO to SCLK Setup Time	t_{WS}	Beamforming mode only. Serial Data Write.	5			ns
SDIO to SCLK Hold Time	t_{WH}	Beamforming mode only. Serial Data Write	5			ns
SCLK to CS Setup Time	T_{CSS}	Beamforming mode only	5			ns
SCLK to CS Hold Time	T_{CSH}	Beamforming mode only	5			ns
SCLK to SDIO Output Data Delay at 2.5V	SDIOdly	Beamforming mode only. Serial Data Read. C_{LOAD} = 15pF.	7	14	22	ns
SCLK to SDO Output Data Delay at 2.5V	SDOdly	Beamforming Mode only. Serial Data Read. C_{LOAD} = 15pF.	7	14	22	ns
CS Min High Level Interval	T_{IDLE}	From CS rising edge to CS falling edge	5			ns
SCLK Pulse-Width High	T_{PWH}		9			ns
SCLK pulse width low	T_{PWL}		9			ns

Note 1: All devices are 100% production tested at T_A = +85C. Limits over the operating temperature range are guaranteed by design.

Note 2: CWD Mode 1: Continuous Wave Doppler, f = 5MHz, V_{IO} = +2.5V, Direct mode, CC0 = CC1 = 1, V_{PPB} = -V_{NNB} = +5V. Load: 1KΩ//220pF. Normal Drop mode.

Note 3: CWD Mode 2: Continuous Wave Doppler, f = 5MHz, V_{IO} = +2.5V, Beamforming–Low Drop Mode, CC0 = CC1 =1 , V_{PPB} = -V_{NNB} = +4V. Load:1KΩ//220pF.

Note 4: B mode: Direct mode, CC0 = CC1 = 0, f = 5MHz, PRF = 5KHz, 1 period, V_{IO} = +2.5V, V_{PP} = -V_{NN} = +85V. Load: 1KΩ//220pF.

Note 5: The equivalent high signal output capacitance (CHS) is calculated as the ratio between the pulser output current (I_{OLS} and I_{OHS}) and the output slew rate at 0V when the pulser is not loaded.

$$C = IO/(dV/dt) \text{ at } 0V$$

Note 6: Both the T/R switch and Damp are designed to be self-protected against the HV transmission. The part is not damaged even if the Transmit setup time is not respected.

Note 7: Setup/hold timings as well as the maximum frequency specifications, assume input rise/fall edges (from 20% to 80%) faster than 0.6ns.

Electrical Characteristics—Pulser

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, CC0 = 0V, CC1 = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PULSER DC SPECIFICATIONS CC0 = 0 CC1 = 0						
Low-Side Output Impedance	R_{OLS}	I_{OUT} = 50mA		13	29	Ω
High-Side Output Impedance	R_{OHS}	I_{OUT} = -50mA		13	29	Ω
Low-Side Output Current	I_{OLS}	V_{DS} = +85V		2.1		A
High-Side Output Current	I_{OHS}	V_{DS} = +85V		2.1		A
PULSER DC SPECIFICATIONS CC0 = 1 CC1 = 0						
Low-Side Output Impedance	R_{OLS}	I_{OUT} = 50mA		16	33	Ω
High-Side Output Impedance	R_{OHS}	I_{OUT} = -50mA		16	33	Ω
Low-Side Output Current	I_{OLS}	V_{DS} = +85V		1.75		A
High-Side Output Current	I_{OHS}	V_{DS} = +85V		1.75		A
PULSER DC SPECIFICATIONS CC0 = 0 CC1 = 1						
Low-Side Output Impedance	R_{OLS}	I_{OUT} = 50mA		30	55	Ω
High-Side Output Impedance	R_{OHS}	I_{OUT} = -50mA		40	76	Ω
Low-Side Output Current	I_{OLS}	V_{DS} = +85V		0.7		A
High-Side Output Current	I_{OHS}	V_{DS} = +85V		0.7		A
PULSER DC SPECIFICATIONS CC0 = 1 CC1 = 1						
Low-Side Output Impedance	R_{OLS}	I_{OUT} = 50mA		61.5	130	Ω
High-Side Output Impedance	R_{OHS}	I_{OUT} = -50mA		81	155	Ω
Low-Side Output Current	I_{OLS}	V_{DS} = +85V		0.35		A
High-Side Output Current	I_{OHS}	V_{DS} = +85V		0.35		A
CLAMP E DAMP DC SPECIFICATIONS						
CLAMP nFET Output Impedance	R_{ONG}	I_{OUT} = 50mA, 5 levels		8		Ω
		I_{OUT} = 50mA, 3 levels		16	33	
CLAMP pFET Output Impedance	R_{OPG}	I_{OUT} = -50mA, 5 levels		8		Ω
		I_{OUT} = -50mA, 3 levels		16	33	
CLAMP nFET Output Current	I_{ONG}	V_{DS} = +85V, 5 levels		2		A
		V_{DS} = +85V, 3 levels		1		
CLAMP pFET Output Current	I_{OPG}	V_{DS} = +85V, 5 levels		2		A
		V_{DS} = +85V, 3 levels		1		
DAMP Output Impedance	R_{DAMP}			130	240	Ω

Electrical Characteristics—Pulser (continued)

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, CC0 = 0V, CC1 = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PULSER AC SPECIFICATIONS 3 Levels Mode						
Logic Input to Output Low-to-High Propagation Delay	T_{PLH}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: from CLK rising edge at 50% to output at 10% of the transition swing		12	18	ns
Logic Input to Output High-to-Low Propagation Delay	T_{PHL}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: From CLK rising edge at 50% to output at 10% of the transition swing		12	18	ns
Logic Input to Output Low-to-GND Propagation Delay	T_{PL0}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: from CLK rising edge at 50% to output at 10% of the transition swing		11.5	18	ns
Logic Input-to-Output High to GND Propagation Delay	T_{PH0}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: from CLK rising edge at 50% to output at 10% of the transition swing		11.5	18	ns
Logic Input-to-Output GND to High Propagation Delay	T_{P0H}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: From CLK rising edge at 50% to output at 10% of the transition swing		12.7	18	ns
Logic Input to Output GND to Low Propagation Delay	T_{P0L}	Trasparent mode: from I_{NP}/I_{NN} at 50% to output at 10% of the transition swing Clocked mode: From CLK rising edge at 50% to output at 10% of the transition swing		12.7	18	ns
OUT_ Fall Time ($V_{PP\_}$ to $V_{NN\_}$)	T_{FPN}	From 0.8 x $V_{PP\_}$ to 0.8 x $V_{NN\_}$, V_{PP} = -V_{NN} = 80V		18.7		ns
OUT_ Rise Time ($V_{NN\_}$ to $V_{PP\_}$)	T_{RNP}	From 0.8xVNN_ to 0.8 x $V_{PP\_}$, V_{PP} = -V_{NN} = 80V		18.7		ns
OUT_ Rise Time (GND to $V_{PP\_}$)	T_{R0P}	From 0.2 x $V_{PP\_}$ to 0.8 x $V_{PP\_}$, V_{PP} = 80V		8.5		ns

Electrical Characteristics—Pulser (continued)

(V_{CC} = 5V±5%, V_{EE} = -5V ±5%, V_{PPA} = +85V, V_{NNA} = -85V, V_{PPB} = +85V, V_{NNB} = -85V, VIO = +1.7V to +3.3V, Direct Mode, CC0 = 0V, CC1 = 0V, SYNC = 0V, HVOUT Load = 1KΩ//220pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, $V_{PP\_}$ = $V_{NN\_}$ = +85V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range)

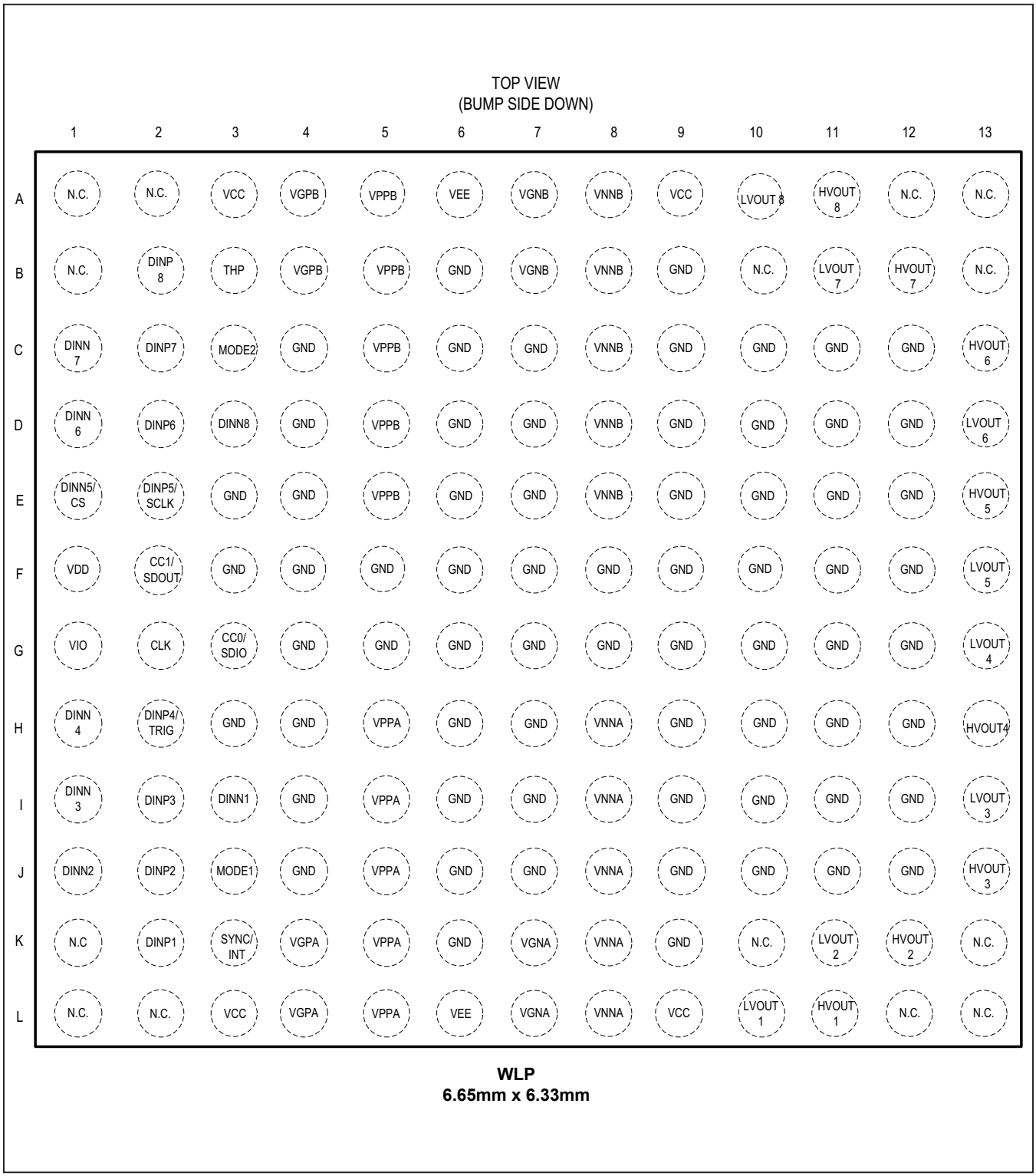
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_ Fall Time (GND to $V_{NN\_}$)	T_{F0N}	From 0.2 x $V_{NN\_}$ to 0.8 x $V_{NN\_}$, V_{NN} = -80V		8.5		ns
OUT_ Rise Time ($V_{NN\_}$ to GND)	T_{RN0}	From 0.8 x $V_{NN\_}$ to 0.2 x $V_{NN\_}$, V_{NN} = -80V		17		ns
OUT_ Fall Time ($V_{PP\_}$ to GND)	T_{FP0}	From 0.8 x $V_{PP\_}$ to 0.2 x $V_{PP\_}$, V_{PP} = 80V		17		ns
Slew Rate 220pF	SR1	C_L = 220pF $V_{PP\_}$ = -$V_{NN\_}$ = 60V		6.5		V/ns
Slew Rate 70pF//100Ω	SR2	C_L = 70pF, R_L = 100Ω $V_{PP\_}$ = -$V_{NN\_}$ = 60V		20		V/ns
2nd Harmonic Distortion	THD2	f_{OUT} = 5MHz, $V_{PP\_}$ =-$V_{NN\_}$ = 80V, square wave (20 cycles)		-40		dBc
Pulse Cancellation 1 Fundamental	PC1	$f_{OUT\_}$ = 1MHz - 5MHz, $V_{PP\_}$ =-$V_{NN\_}$ = 80V, 2 cycles.		-40		dBc
Pulse Cancellation 2 Second Harmonic	PC2	$f_{OUT\_}$ = 1MHz - 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = 80V, 2 cycles.		-40		dBc
Pulser Bandwidth	BW	$V_{PP\_}$ = -$V_{NN\_}$ = +60V. Defined as the maximum frequency at which the pulser is capable of driving at least 90% of the transition.		25		MHz
PULSER AC SPECIFICATIONS						
CWD Voltage Drop	V_{DROP}	Drop between supply voltage and output voltage levels CWD, I_{OUT} = ±10mA, f = 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = 5V		2.1		V
CWD Voltage Drop–Low Drop Mode (Beamforming Mode Only)	V_{DROP}	Drop between supply voltage and output voltage levels CWD, I_{OUT} = ±10mA, f = 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = 5V		1.4		V
Propagation Delay Part-to-Part Matching (Skew)	ΔTp	3 std: between different parts. Same temperature same voltage supplies.		± 2		ns

Electrical Characteristics—T/R Switch

(V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, VIO = +1.7V to +3.3V, Direct Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are VIO = +2.5V, V_{CC} = -V_{EE} = 5V, T_A = +25°C, Limits are 100% tested at T_A = +85°C and guaranteed by design in the entire temperature range)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
T/R SWITCH DC SPECIFICATIONS						
T/R Switch Power Consumption per Channel	T_{RPOW}			<0.1		mW
LVOUT_ Output Voltage Linear Range	LVRANGE	Sinusoidal tone on HVOUT. f = 1MHz to 20MHz. Load on LVOUT = 100Ω, THD < 1%		±0.53		V
Equivalent Small-Signal Shunt Capacitance on Pin LVOUT_	COFFLV	0.1V_{P-P}, f = 5MHz sinusoidal tone signal T/R switch off		4.5		pF
T_{RSW} On Impedance	RTRON	f = 1MHz to 15MHz. Measured between HVOUT_ and LVOUT_		12	22	Ω
T_{RSW} On DC Output Voltage	LVOFFON	No load on HVOUT and LVOUT	-4	0	+4	mV
T_{RSW} Off DC Output Voltage	LVOFFOFF	No load on HVOUT and LVOUT	-4	0	+4	mV
T/R SWITCH AC SPECIFICATIONS						
T_{RSW} Turn-On time	T_{ONTRSW}			0.5	1	µs
T_{RSW} Turn-Off time	$T_{OFFTRSW}$				0.2	µs
T_{RSW} Harmonic Distortion THD	T_{HDTRSW}	R_{LOAD} = 200Ω, V_{SIGN} = 100mV_{PP}, f = 1MHz to 20MHz		-60		dB
T_{RSW} Turn On Voltage Spike on HVOUT	V_{PKHVON}	20pF//200Ω load on HVOUT, 20pF//200Ω load on LVOUT Low-pass filtered at 20MHz		55		mV_{P-P}
T_{RSW} Turn OFF Voltage Spike on HVOUT	$V_{PKHVOFF}$	20pF//200Ω load on HVOUT, 20pF//200Ω load on LVOUT Low-Pass Filtered at 20MHz		6		mV_{P-P}
T_{RSW} Off Isolation	OFFISO	f = 5MHz. Measured between HVOUT and LVOUT		-64		dB
Power Supply Modulation Ratio on V_{CC}	PSMR	T_{RSW} on. Sinusoidal tone (1KHz, 500mVRMS) superimposed onto VCC DC level. Sinusoidal tone on HVOUT (5MHz, 200mVRMS). LVOUT: terminated with 50Ω		-58		dB
Power Supply Modulation Ratio on V_{EE}	PSMR	TRSW on. Sinusoidal tone (1KHz, 500mV_{RMS}) superimposed onto V_{EE} DC level. Sinusoidal tone on HVOUT (5MHz, 200mVRMS). LVOUT: terminated with 50Ω		-80		dB

Pin Configuration



WLP
6.65mm x 6.33mm

Pin Description

PIN	NAME	FUNCTION
POWER		
H5, J5, K5, L5, M5	VPPA	HV Positive Power Supply Input. Connect HV bypass capacitor between V_{PPA} and GND as close as possible to the device. Capacitor value depends on the application and typically varies in a range from 100nF to 1µF.
A5, B5, C5, D5, E5	VPPB	HV Positive Power Supply Input. Connect HV bypass capacitor between V_{PPB} and GND as close as possible to the device. Capacitor value depends on the application and typically varies in a range from 100nF to 1µF.
M8, L8, K8, J8, H8	VNNA	HV Negative Power Supply Input. Connect HV bypass capacitor between V_{NNA} and GND as close as possible to the device. Capacitor value depends on the application and typically varies in a range from 100nF to 1µF.
A8, B8, C8, D8, E8	VNNB	HV Negative Power Supply Input. Connect HV bypass capacitor between V_{NNB} and GND as close as possible to the device. Capacitor value depends on the application and typically varies in a range from 100nF to 1µF.
M3, A3, M9, A9	VCC	V_{CC} Positive Analog Supply Voltage Input. Connect 220nF or greater bypass capacitors to GND, one per side, as close as possible to the device.
M6, A6	VEE	V_{EE} Negative Analog Supply Voltage Input. Connect 220nF or greater bypass capacitors to GND, one per side, as close as possible to the device
F1	VDD	LDO Output. 1.8V typ. Connect 1µF bypass capacitor between V_{DD} and GND as close as possible to the device.
G1	VIO	Logic I/O Voltage Supply. Connect > 0.1µF bypass capacitor between VIO and GND as close as possible to the device.
M4, L4	VGPA	High-Side Driver Floating Power Supply Output. Connect 1µF bypass capacitor between V_{GPA} and V_{PPA} as close as possible to the device.
A4, B4	VGPB	High-Side Driver Floating Power Supply Output. Connect 1µF bypass capacitor between V_{GPB} and V_{PPB} as close as possible to the device.
M7, L7	VGNA	Low-Side Driver Floating Power Supply Output. Connect 1µF bypass capacitor between V_{GNA} and V_{NNA} as close as possible to the device.
A7, B7	VGNB	Low-Side Driver Floating Power Supply Output. Connect 1µF bypass capacitor between V_{GNB} and V_{NNB} as close as possible to the device.
E3, F3, H3, C4, D4, E4, F4, G4, H4, J4, K4, F5, G5, B6, C6, D6, E6, F6, G6, H6, J6, K6, L6, C7, D7, E7, F7, G7, H7, J7, K7, F8, G8, B9, C9, D9, E9, F9, G9, H9, J9, K9, L9, C10, D10, E10, F10, G10, H10, J10, K10, C11, D11, E11, F11, G11, H11, J11, K11, C12, D12, E12, F12, G12, H12, J12, K12	GND	Ground

Pin Description (continued)

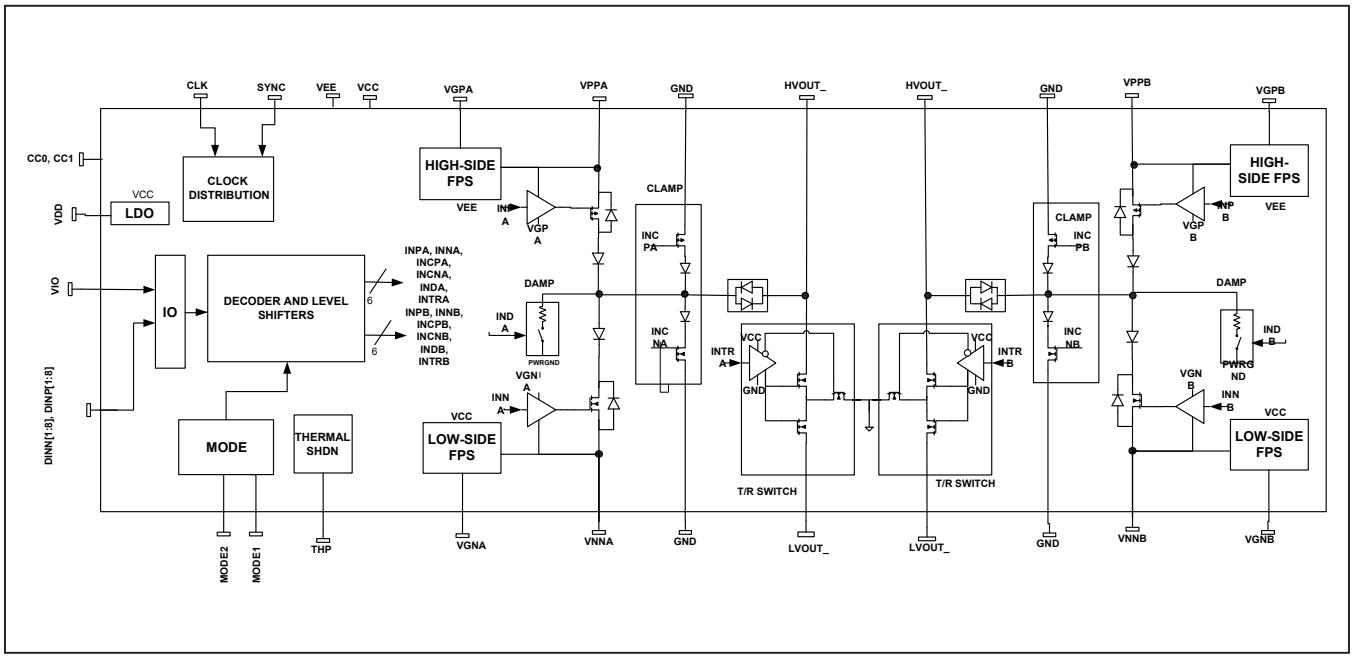
PIN	NAME	FUNCTION
Pulser HV Outputs		
M11	HVOUT1	HV Output Channel 1
L12	HVOUT2	HV Output Channel 2
K13	HVOUT3	HV Output Channel 3
H13	HVOUT4	HV Output Channel 4
E13	HVOUT5	HV Output Channel 5
C13	HVOUT6	HV Output Channel 6
B12	HVOUT7	HV Output Channel 7
A11	HVOUT8	HV Output Channel 8
T/R Switch LV Outputs		
M10	LVOUT1	LV Output (T/R Switch Output) Channel 1
L11	LVOUT2	LV Output (T/R Switch Output) Channel 2
J13	LVOUT3	LV Output (T/R Switch Output) Channel 3
G13	LVOUT4	LV Output (T/R Switch Output) Channel 4
F13	LVOUT5	LV Output (T/R Switch Output) Channel 5
D13	LVOUT6	LV Output (T/R Switch Output) Channel 6
B11	LVOUT7	LV Output (T/R Switch Output) Channel 7
A10	LVOUT8	LV Output (T/R Switch Output) Channel 8
Control Logic Digital Inputs/Outputs		
K3	MODE1	CMOS Logic Input
C3	MODE2	CMOS Logic Input
B3	THP	Open Drain Output. Thermal warning.
L3	SYNC/ INT	CMOS Logic Input in Direct Mode, Interrupt Open-Drain Output in Beamforming Mode. When in Direct mode, connect SYNC/INT logic-high to operate in Clocked mode whereas connect SYNC/INT logic-low to operate in Transparent mode. When in Beamforming mode, SYNC/INT is an open-drain output which carries interrupt signals (refer to the beamforming description). Connect 1KΩ external resistor to V_{IO}.
G3	CC0/ SDIO	CMOS Logic Current Control Input in Direct Mode (CC0) SPI Data Input-Output in Beamforming Mode (SDIO)
F2	CC1/SD-OUT	CMOS Logic Current Control Input in Direct Mode (CC1) SPI Data Output in Beamforming Mode (SDOUT)

Pin Description (continued)

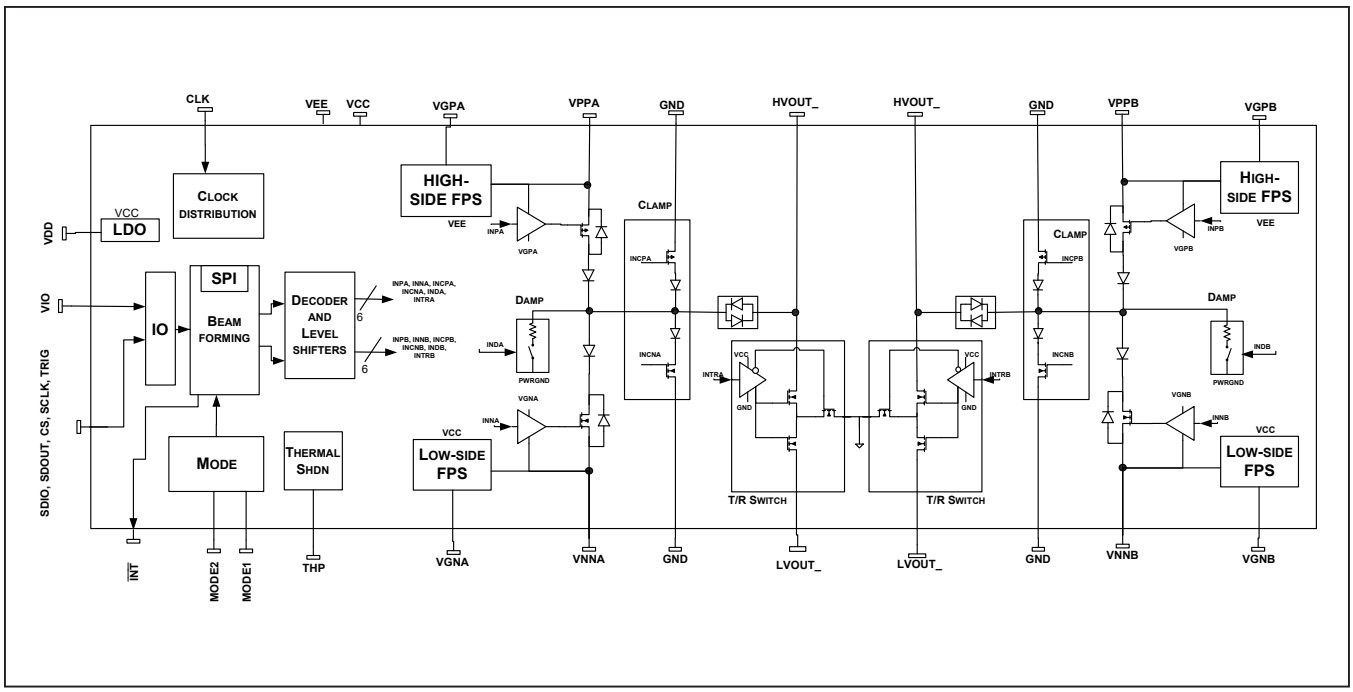
PIN	NAME	FUNCTION
Logic Input Signal Pins		
L2	DINP1	CMOS Positive Logic Input for Channel 1
K2	DINP2	CMOS Positive Logic Input for Channel 2
J2	DINP3	CMOS Positive Logic Input for Channel 3
H2	DINP4/ TRIG	CMOS Positive Logic Input for Channel 4 in Direct Mode (DINP4) CMOS Trigger Login Input in Beam Forming Mode (TRIG)
E2	DINP5/ SCLK	CMOS Positive Logic Input for Channel 5 in Direct Mode (DINP5) SPI Clock Input in Beamforming Mode (SCLK)
D2	DINP6	CMOS Positive Logic Input for Channel 6
C2	DINP7	CMOS Positive Logic Input for Channel 7
B2	DINP8	CMOS Positive Logic Input for Channel 8
J3	DINN1	CMOS Negative Logic Input for Channel 1
K1	DINN2	CMOS Negative Logic Input for Channel 2
J1	DINN3	CMOS Negative Logic Input for Channel 3
H1	DINN4	CMOS Negative Logic Input for Channel 4
E1	DINN5/ CS	CMOS Negative Logic Input for Channel 5 in Direct mode (DINN5) SPI Chip Select (Active-Low) in Beamforming mode (CS)
D1	DINN6	CMOS Negative Logic Input for Channel 6
C1	DINN7	CMOS Negative Logic Input for Channel 7
D3	DINN8	CMOS Negative Logic Input for Channel 8
Master clock pins		
G2	CLK	Clock Input
NC		
A1, B1, L1, M1, A2, M2, B10, L10, A12, M12, A13, B13, L13, M13	NC	Not internally connected

Functional Diagrams

Functional Diagram Direct Mode–2 Channels Out of 8 Shown



Functional Diagram Beamforming Mode–2 Channels Out of 8 Shown



Detailed Description

The MAX14813 is a very high density, high-voltage ultrasound transmitter (pulser) in a wafer-level package (WLP). It is particularly aimed to address ultrasound imaging applications in which PCB space is a concern.

It features eight 3-Level channels operating from two independent pairs of HV supplies. Each channel can transmit up to $170V_{P-P}$ with up to 2.1A current capability. The current capability can be programmed down to 0.35A with 4 steps of programmability. It also features an integrated 1A active clamp (Return to Zero).

The MAX14813 can also be configured as a quad 5-level (2.1A) pulser plus quad active T/R switches.

The MAX14813 features embedded digital resources (SRAM and state machine) that can be used to support transmit beamforming resulting in a dramatic saving of the number of interconnects and FPGA I/Os. The embedded digital resources are programmed through a high-speed serial interface and supports sophisticated transmit techniques likewise pulse-width modulation for burst shaping and apodization for beam shaping.

Alternatively, the device can be controlled in a conventional manner by an external digital source (FPGA or similar) through dedicated CMOS logic inputs.

The MAX14813 features independent Active T/R switches. The T/R switches can possibly be externally configured to support receive multiplexing in which a fewer number of receive than transmit channels are used.

The MAX14813 is packaged into a 6.33mm x 6.65mm WLP with a 12 x 13 ball grid array.

Operating Modes

Operating Modes Table

Operating Modes Truth Table

MODE2	MODE1	MODE NAME	DESCRIPTION
0	0	SHUTDOWN	Shutdown Mode. Power is minimized. Trasmission and reception are disabled.
0	1	Direct Mode 3 Levels	3 Levels Transmission (8 channels). Direct Mode. Pulser is controlled by external digital resource.
1	0	Direct Mode 5 Levels	5 Levels Transmission (4 channels). Direct Mode. Pulser is controlled by external digital resource.
1	1	Beamforming Mode	In this mode, the device is programmed through SPI. Embedded digital resources are used to support in chip beam-formation.

Shutdown Mode

This is the lowest power dissipation mode. No transmission is allowed. Pulser Output (HVOUT) is in high-impedance and the T/R switch is off. The beamforming state machine is disabled.

It takes 0.5ms max to exit from this mode and entering in any other transmit modality.

The following Truth Table shows HVOUT and LVOUT state in shutdown mode.

Shutdown Mode Truth Table

DINNX	DINPX	HVOUTX	LVOUTX
X	X	High Impedance	High Impedance (T/R switch OFF)

Direct Mode–3 Levels

In this mode the transmitter and the T/R switches are both enabled and are controlled through logic input signals. The embedded beamforming capability is disabled. The MAX14813 operates as an Octal 3L pulser with eight independent channe ls. Two logic input signals per channel allow transmitting 3 levels waveforms according to the following Truth Table.

Direct Mode–3 Levels Truth Table

DINNX	DINPX	HVOUTX	LVOUTX
x = 1..8 (V_{PPA} = V_{PPB}, V_{NNA} = V_{NNB})			
0	0	Clamp ON Damp OFF	TR Switch OFF LVOUT = Hi-Z
1	0	VNN Damp OFF	TR Switch OFF LVOUT = Hi-Z
0	1	VPP Damp OFF	TR Switch OFF LVOUT = Hi-Z
1	1	Clamp ON Damp ON	TR Switch ON

Direct Mode–5 Levels Mode

In this mode the transmitter and the T/R switches are both enabled. The part shall be externally configured as a Quad 5 levels pulser. This implies that pairs of pulser output pins (HVOUT) are connected as follows:

HVOUTx = HVOUTy with (x,y) = (1,5), (2,6), (3,7), (4,8)

The T/R switch outputs are internally connected to pins LVOUTx, x = 1, 2, 3, 4. Therefore, the remaining LVOUT pins (namely LVOUTy, y = 5, 6, 7, 8) are unused and can be left floating.

In 5 Levels Configurations (either Direct Mode-5 Levels or Beamforming-5 Levels), transmission is permitted only if both the conditions $V_{PPA} \geq V_{PPB}$ and $V_{NNA} \leq V_{NNB}$ are satisfied.

Pulser Output and T/R switch Output are controlled by four control CMOS input per channel, as shown in the following Truth Table.

As referenced in the Direct Mode 5 Levels Truth Table below, DINPy is a Return To Zero (RTZ) Enable pin. Therefore, DINPy can be tied to the positive rail (V_{IO}) so that 3 Control inputs only would be required(DINNx, DINPx, DINNy) for 5 levels operations.

Direct Mode 5 Levels Truth Table

DINNX X = 1, 2, 3, 4	DINPX X = 1, 2, 3, 4	DINNY “SEL” Y = 5, 6, 7, 8	DINPY “RTZ” Y = 5, 6, 7, 8	HVOUTX = HVOUTY	LVOUTX X = 1, 2, 3, 4	LVOUTY Y = 5, 6, 7, 8
0	0	X	0	Hi-Z Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
0	0	X	1	Clamp On Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
0	1	0	X	V_{PPA} Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
1	0	0	X	V_{NNA} Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
0	1	1	X	V_{PPB} Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
1	0	1	X	V_{NNB} Damp Off	TR Switch Off LVOUT = Hi-Z	TR Switch Off LVOUT = Hi-Z
1	1	X	X	Clamp ON Damp ON	TR Switch ON	TR Switch Off LVOUT = Hi-Z

Direct Mode–Clocked or Transparent Operating Modes

The device can operate either in Transparent or Clocked mode.

When in Transparent mode, the output directly reflects input changes after the signal propagation delay.

In Clocked mode input data are clocked in and synchronized on the rising edge of the master clock. The master clock (CLK pin) can run up to 200MHz.

A dedicated digital logic input (SYNC) allows configuring the part either in Transparent or Clocked mode.

Direct Mode–Setting the Pulser Strength (Driving Current)

In Direct mode, the pulser driver current for all the channels can be set by mean of two logic CMOS Input pins (CC1, CC0). The following Truth Table shows the current setting in the 4 cases.

Beamforming Mode

In this mode the MAX14813 pulser is programmed through the SPI bus. Embedded digital resources are used to support in chip beam-formation. Moreover, the Low Drop mode, and the pulser current setting can be programmed by writing bits into the device registers.

The embedded Beamforming function dramatically reduces the number of system interconnects as well as the FPGA total I/Os count resulting in PCB space and system cost savings. Digital pulser inputs are generated by on chip digital waveform resources.

Refer to the *Detailed Description–Transmit Beamforming* section for further details

Low Drop Mode–(Beamforming Mode Only)

In beamforming mode, a low R_{ON} switch can be activated to bypass the grass-clipping diodes and reduce the output drop (Low Drop mode). The Low Drop mode results in greater transmit efficiency whenever the grass clipping diodes isolation is not requested. In particular its use is recommended for transmit channels in CWD mode. This function is available in Beamforming mode only. The Low Drop mode is enabled and disabled by a specific bit into the Line Type register.

Refer to the beamforming section for further details.

Setting the Driving Current Truth Table

C1	CC0	PULSER OUTPUT CURRENT (TYP)
0	0	2.1A
0	1	1.75A
1	0	0.7A
1	1	0.35A

Thermal Warning and Shutdown Management

A precise thermal sensor senses the pulser junction temperature.

As soon as the junction temperature exceeds 110°C a thermal warning is sent out by asserting a dedicated open drain output pin (THP). The THP is de-asserted if the temperature drops back under 105C.

If the junction temperature exceeds 150°C then the transmission is disabled. The transmission is enabled back when the temperature drops below 130°C.

In beamforming mode, dedicated bits are reserved for logging thermal events.

Refer to *Detailed Description–Transmit Beamforming* (Fault Detection Strategy paragraph) for further details

Detailed Description T/R Switch and Damp

T/R Switches

Each channel features a low-power low glitch Transmit/Receive switch.

For proper operation in Direct Mode, the T/R switch has to be turned off driving both DINN and DINP low at least 0.8µs before starting the (see *Electrical Characteristics* table "Transmit Setup Time").

T/R switch Truth Tables in Direct mode are shown in the "*Direct Mode–3 Levels*" and *Direct Mode–5 Levels Mode* paragraphs for 3L and 5L, respectively.

In beamforming mode, the embedded state machine controls the T/R switch and automatically insert a programmable latency during which the T/R switch is turned OFF before the transmission initiates (see *Detailed Description–Transmit Beamforming* for further details).

The T/R switch recovery time after the transmission is less than 1µs.

Damp Function

An active damp circuit is integrated between the internal pulser output node (before grass-clipping diodes) and GND. The purpose of this circuit is to fully discharge the pulser output internal node so that the node is not left in high-impedance condition as soon as the transmit burst is over. This results in two main advantages:

1) The grass-clipping isolation is more effective.

2) Suppression of any low-frequency oscillation of the internal pulser output node that could be detrimental for Doppler mode performances.

Floating Power Supplies

The device features integrated floating regulators that supply the driver circuitry of the HV power FETs. The output of these regulators are named V_{GPA}, V_{GPB}, V_{GNA}, V_{GNB} and are referred to V_{PPA}, V_{PPB}, V_{NNA}, V_{NNB} respectively.

In Direct mode these regulators are automatically turned on (both for 3 levels and 5 levels).

In Beamforming mode, it is possible to enable/disable the internal regulators by means of dedicated bits into the configuration register. Refer to the *Detailed Description–Transmit Beamforming* section for further details.

HVOUT Overvoltage Protections

The device features Overvoltage Protection (OVP) connected between each HVOUT pin and the V_{PPA}, V_{NNA} positive and negative input voltage supply pins. These protection are aimed to absorb kick back currents which can result from driving resonant loads in ultrasound systems.

OVP are not shown in the functional diagrams.

Test Diagrams

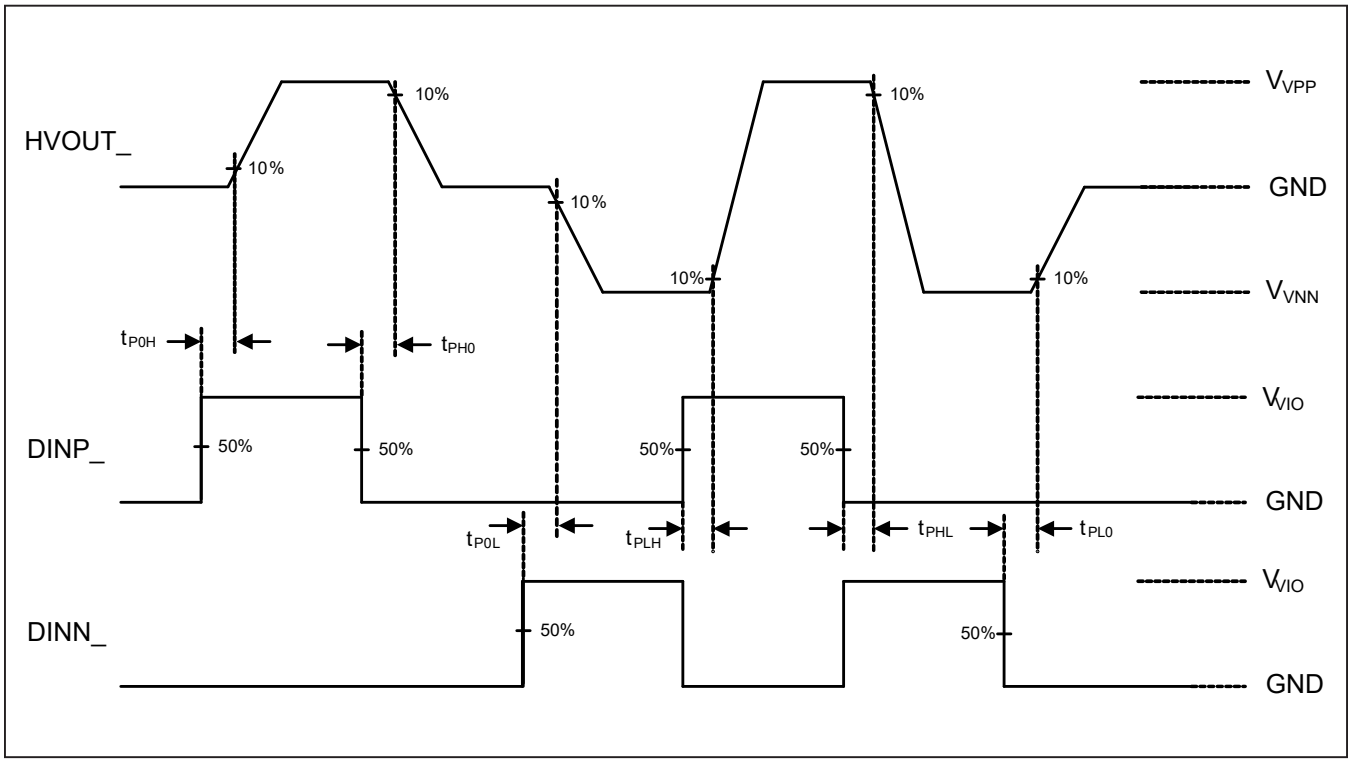


Figure 1: Propagation Delay Timing Diagram

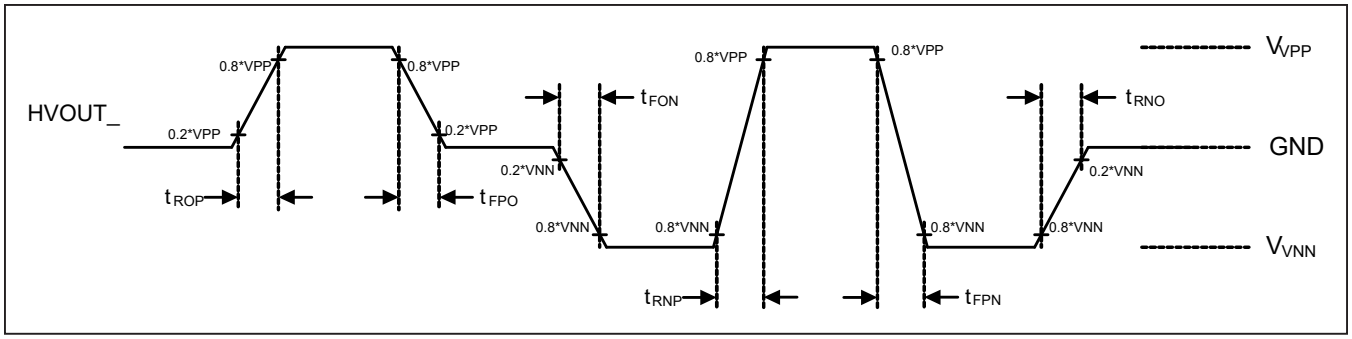


Figure 2. Rise and Fall Timings Diagram

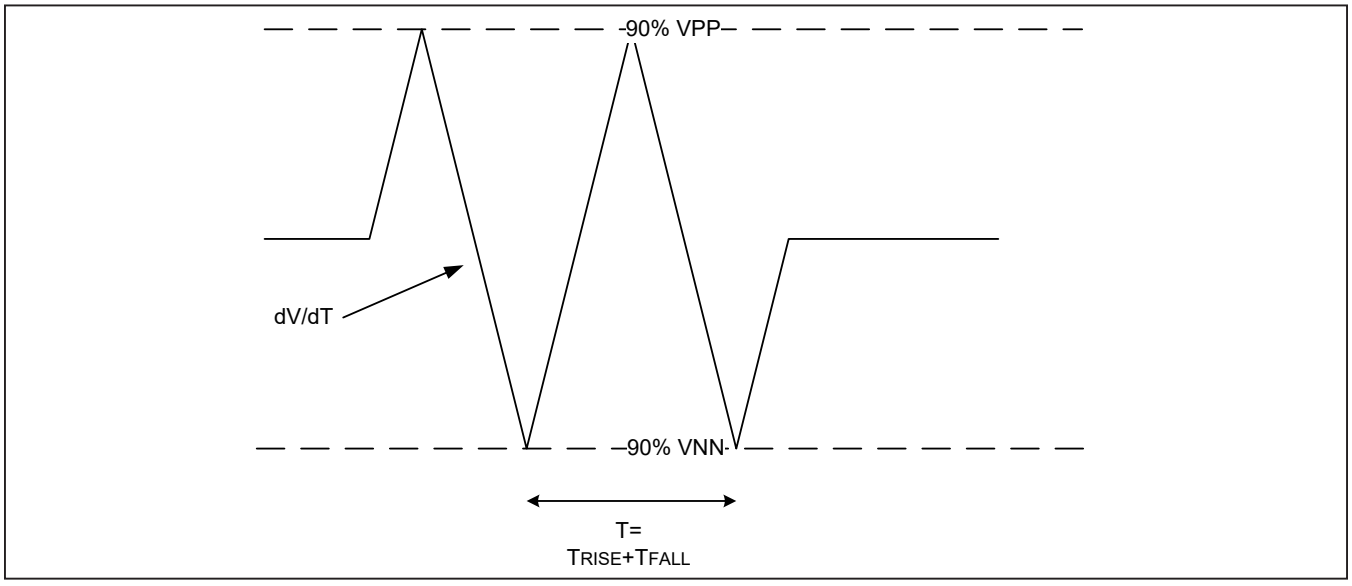


Figure 3. Bandwidth Diagram

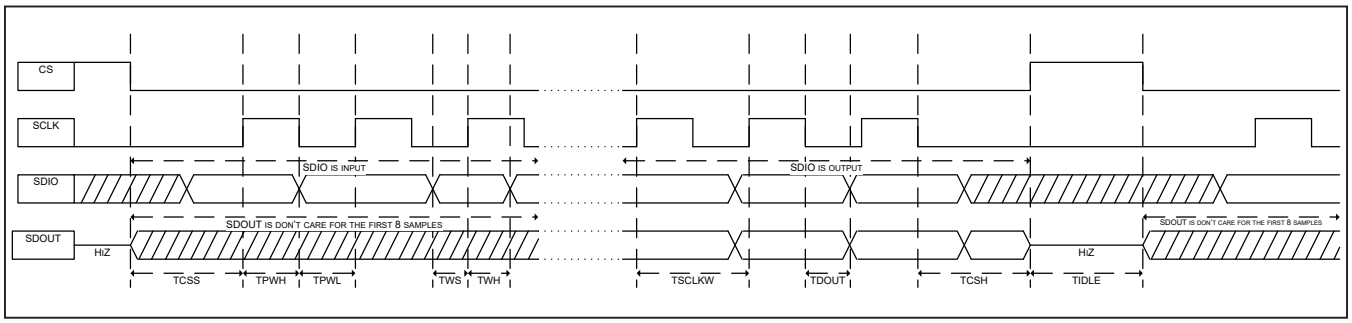


Figure 4. SPI Timings Diagram

Detailed Description–Transmit Beamforming

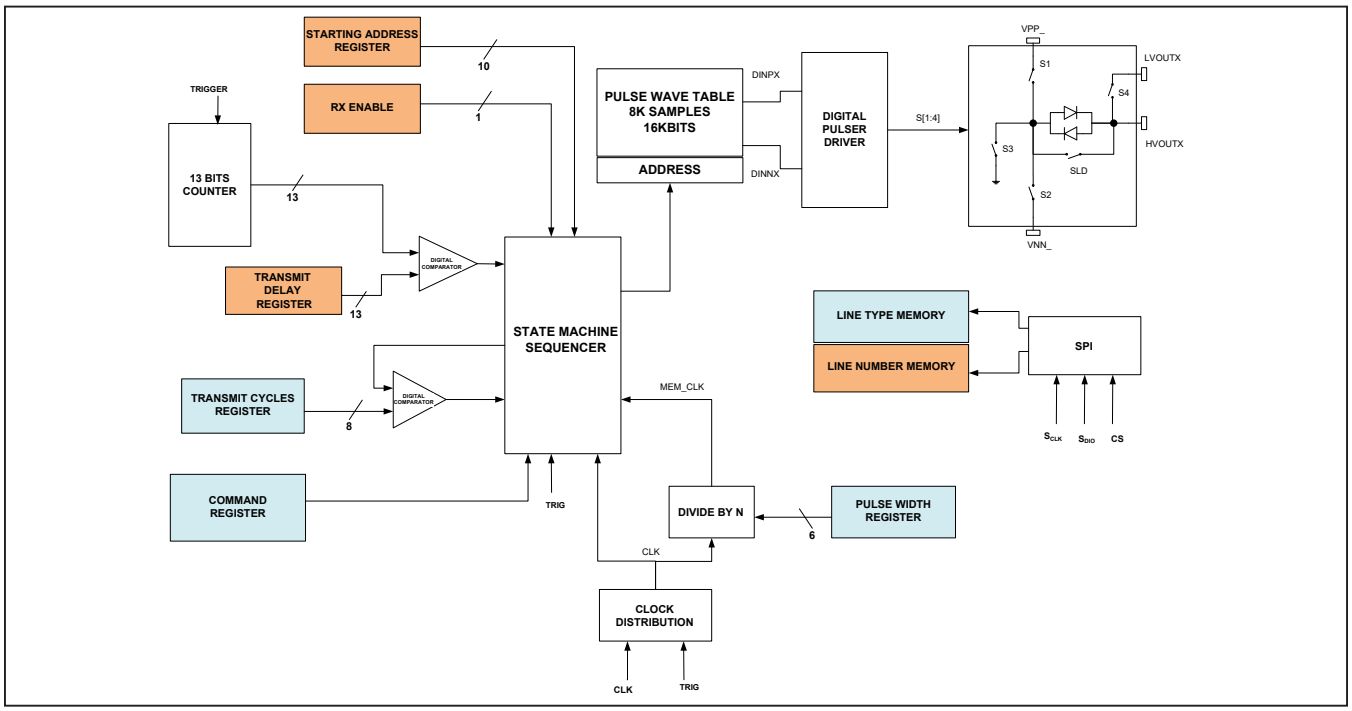


Figure 5. Transmit Beamforming 3 Levels Diagram

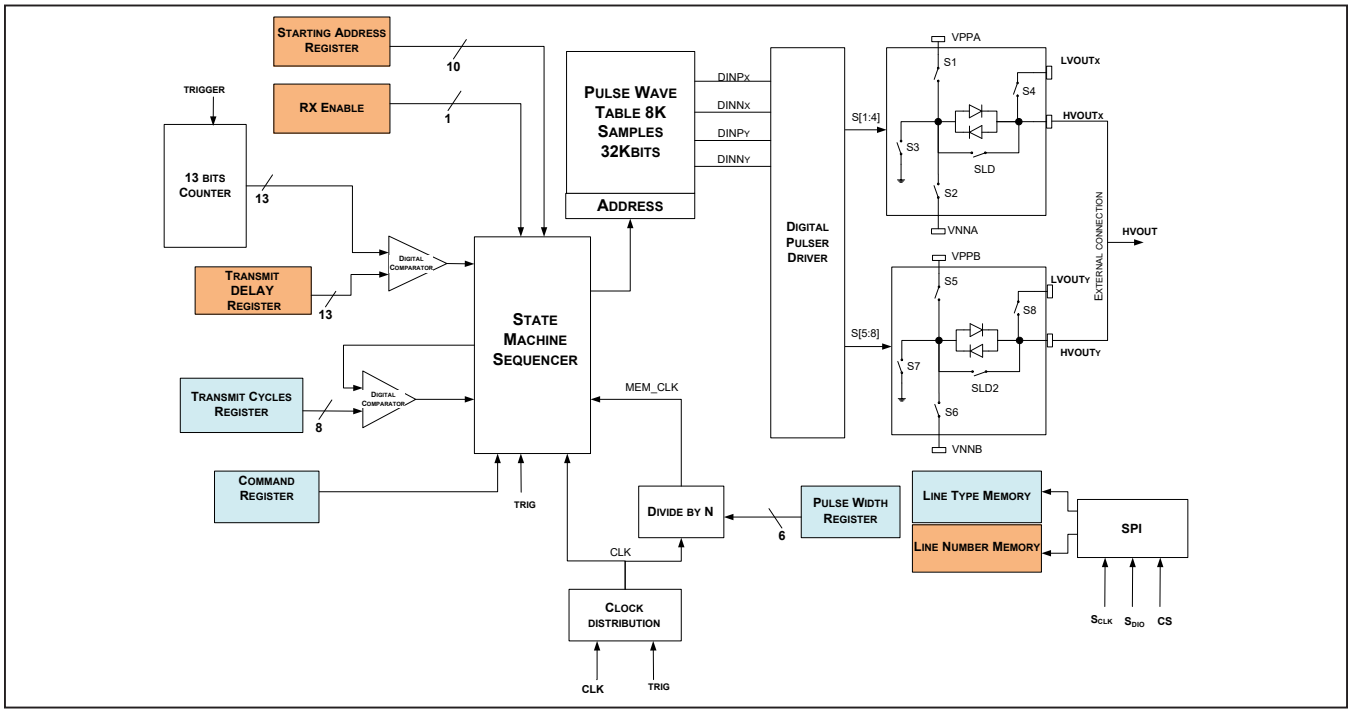


Figure 6. Transmit Beamforming 5 Levels Diagram

State Machine General Description

Four main registers control the beamforming state machine: **Starting Address Register, Transmit Delay Register, Pulse Width Register** and **Transmit Cycles Register** (refer to the Beamforming Functional Diagram)

These registers are set every time a “Set New Line” command is provided through SPI.

When trigger (TRIG) is low the delay and the cycles counters are cleared. A rising-edge of the trigger signal initiates the transmission.

The Master Clock (CLK) synchronizes the State Machine operation. The master clock can run up to 200MHz, resulting in a beamforming time resolution up to 5ns (lambda/16 resolution at12.5MHz).

Trigger is sampled on the rising-edge of the master clock.

Each channel transmits the preprogrammed pattern stored into the **Pulse Wave Table (PWT)**, according to the content of the **Starting Address Register.** If the programming bit **Invert** is set high, the pattern is transmitted with opposite polarity.

The pattern is transmitted after a delay according to the content of the **Transmit Delay Register**.

The memory read out frequency, and hence the single pulse width, is determined by the content of the **Pulse Width Register**.

The very same pattern, ending with the End-of-Pattern (EOP) symbol is repeated according to the content of the **Transmit Cycles Register**.

Each channel has its own Starting Address and Transmit Delay registers. The Pulse Width and the Transmit Cycles registers are common for all channels.

Memory Description

Memory Description

The Line and Waveform information processed by the Beamforming State Machine are pre-stored into three memories (SRAM).

The following tables show a high level description of the three memories for 3 Levels and 5 Levels operation respectively

Transmit Beamforming Memory Sizes - 3 Levels operations

MEMORY NAME	NUMBER OF BANKS	SIZE (WORDS X BITS)	DESCRIPTION
Pulse Wave Table (PWT Memory)	8 (one per channel)	1024 x 16	Stores the basic patterns, 8 samples per word. It can store up to 8K samples per channel. Each sample is 2 bits.
Line Number Memory (LN Memory)	8 (one per channel)	153 x 24	Each memory word stores the line information. Up to 1536 different lines can be stored. Line information include: 1) Delay (DLY) 2) Pulse Wave Table Starting address (PWT Address) 3) Receive Enable bit (RX)
Line Type Memory (LT Memory)	1 (common for all channels)	128 x 24	Stores the line type information – Common for all the channels 1) Number of iteration (cycles) 2) Pulse width duration 3) Programmable current levels 4) CWD operation bit 5) Sequence Line repetition 6) Sequence Line inversion 7) Low Drop bit

Beamforming Memory Sizes - 5 Levels operations

MEMORY NAME	NUMBER OF BANKS	SIZE (WORDS X BITS)	DESCRIPTION
Pulse Wave Table (PWT Memory)	4 (one per channel)	1024x32	Stores the basic patterns, 8 samples per word. It can store up to 8K samples per channel. Each sample is 4 bits.
Line Number Memory (LN Memory)	4 (one per channel)	3072x24	Each memory word stores the line information. Up to 3072 different lines can be stored. Line information include: 1) Delay (DLY) 2) Pulse Wave Table Starting address (PWT Address) 3) Receive Enable bit (RX)
Line Type Memory (LT Memory)	1 (common for all channels)	128x24	Stores the Line type information – Common for all the channels 1) Number of iteration (cycles) 2) Pulse width duration 3) Programmable current levels 4) CWD operation bit 5) Sequence Line repetition 6) Sequence Line inversion 7) Low Drop bit

3 Levels - Pulse Wave Table (PWT) Memory– Detailed Description

The Pulse Wave Table Memory stores all possible patterns (waveforms) for every channel.

It is made by 8 banks of 1Kx16 bits and can store up to 8K samples.

Each sample corresponds to two bits (DINP, DINN). Waveforms are stored for each individual channel by writing the "Pulse Wave Table (PWT) chx" register into the PWT memory (see *Memory Register Map*).

Up to 1K different patterns (waveforms), 8 samples each, can be addressed for each channel. A pattern can be longer than 8 samples as it can extend into contiguous memory segments.

Transmission proceeds sequentially starting from the most significant bit of the location pointed by the Starting Address.

In order to shorten the programming time, it is made possible to program all the Pulse Wave tables in parallel instead of programming each individual memory bank. In this case, all the channels memories will store identical data.

Refer to the *Memory Register Map* for further details.

5 Levels–Pulse Wave Table (PWT) Memory– Detailed Description

The Pulse Wave Table Memory stores all possible patterns (waveforms) for every channel.

It is made by 4 banks of 1024x32 bits and can store up to 8K samples. Each bank consists of two 3 levels PWT banks merged together.

Every sample corresponds to four bits (DINPx, DINNx, DINPy, DINNy) in which (x,y) is one of the possible pairs (1,5), (2,6), (3,7), (4,8).

With reference to the register map, the first two bits (DINPx, DINNx) of each sample are physically stored into "Pulse Wave Table (PWT) chx" in which x = 1,2,3,4 whereas the other two bits (DINPy, DINNy) are physically stored into the "Pulse Wave Table (PWT) chy" in which y = 5,6,7,8.

Up to 1024 different patterns (waveforms), 8 samples each, can be addressed for each channel. A pattern can be longer than 8 samples as it can extend into contiguous memory segments.

Transmission proceeds sequentially starting from the most significant bit of the location pointed by the Starting Address.

In order to shorten the programming time, it is made possible to program all the Pulse Wave tables in parallel instead of programming each individual memory bank. In this case, all the channels memories will store identical data.

Refer to the *Memory Register Map* for further details.

Line Number (LN) Memory - Detailed Description

For 3-Levels operation the LN memory is 1.5K x 24 bits so that it can support up to 1.5K different lines.

For 5-Levels operation the LN memory is 3K x 24 bits so that it can support up to 3K different lines. It consists of two 3 levels LN Memories concatenated together.

Line Number Memory (LN) Data Description shows the data description for one single word into the LN memory.

Line Number Memory (LN) Data Description

REGISTER NAME	BITS PER REGISTER	DESCRIPTION
Transmit Delay Register (DLY)	13	The "Transmit Delay Register" determines the Beamforming delay (BF Delay) of each channel following one Trigger event. The BF delay is stored as a 13 bits word so that it can be programmed from zero to 2^13 clock periods. The total delay is the sum of the above mentioned BF delay and a fixed latency delay (refer to "Latency calculation" paragraph for more information about the Latency).
Starting Address Register (PWT_ADD)	10	This register stores the Pulse Wave Table Memory Address of the first pattern which will be sent out during the next transmission (MSB first).
Receive Enable bit (RX)	1	Set the Receive Enable bit high to enable the receiving for that channel: the T/R switch is on after the transmission. Set the Receive Enable bit low to disable the receiving for that channel: the T/R switch is off after the transmission. This feature allow supporting RX multiplexing schemes.
Total Bits	24	

Line Type (LT) Memory - Detailed Description

The Line Type Memory (LT) stores the line type information such as the number of consecutive transmit cycles and the transmit pulse width. This information is common for all the channels. Up to 128 different Line types can be stored.

The Set New Line 1, 2, 3 commands (see *Beam forming Programming Modes - Setting a New Line* section) point to the Line Type address to be used for the next transmission.

Line Type Memory Data Description shows the LT memory data description.

Refer to Memory Register Map–Data Description for further details.

Line Type Memory Data Description

REGISTER NAME	BITS PER REGISTER	DESCRIPTION
Transmit Cycles Register	8	The content of this register determines the number of iteration (cycles) the same pattern is repeated consecutively. The unique pattern into the Pulse Wave Table ends with an EOP symbol. When the EOP is found the cycling counter is incremented and the starting address is re-loaded for a new cycle transmission. This iterative process ends when the cycling counter reaches the value stored into the Transmit Cycles register. During the iteration of the pattern, the EOP symbol is not transmitted out. Up to 256 consecutive cycles can be transmitted.
Pulse Width Register	6	The "Pulse Width Register" determines the duration of a single pulse width from 1xTclk to 64xTclk in which Tclk is the master clock period. In other words, the content of this registers determines the time base of the pattern stored into the Pulse Wave Table Memory. The content of this register does not affect the timing resolution of the delay profile which is always given by Tclk.

Line Type Memory Data Description (continued)

REGISTER NAME	BITS PER REGISTER	DESCRIPTION
CWD Mode	1	When set high all the channels enter in CWD mode and the patterns are continuously transmitted until the Trigger signal is high (Transmit Cycles Register is don't-care in CWD Mode)
Pulser current register	2	Pulser current setting can be programmed in 4 steps. Refer to the "Line Type Memory Register - Setting the pulser current" paragraph for further details.
Line Sequencer Repeat Same Line	5	When the Line Sequencer is enabled, the content of this field determines the number of iterations of the same line. A single line can be transmitted consecutively up to 32 times before the line number and the line type are incremented by the sequencer. Refer to the "Line Sequencer Detailed Description" paragraph for further details.
Line Sequencer Invert Line	1	When the Line Sequencer is enabled, this bit enables the invert Line function causing the next Line in the sequence to be fired with inverted polarity. Used in conjunction with the "Sequencer Repeat Same Line", this bit allows the sequencer to address pulse inversion imaging. When this bit is set high and the "Sequencer Repeat same Line" is set equal to two, then the first trigger event will produce an in phase line while the second trigger event will produce an out of phase (inverted) line. Set this bit low to disable the Invert Line function. Refer to the "Line Sequencer Detailed Description" paragraph for further details.
Low Drop Mode	1	Low Drop Mode bit. Set this bit High to enter in Low Drop Mode. In Low Drop Mode the switch SLD_ (refer to Transmit Beamforming Diagram) is closed in order to bypass the grass clipping diodes and increase the transmit efficiency. This mode is normally used in CWD. Set this bit low (default) for Normal Operation (SLD_ is open)
Total Bits	24	

Line Type Memory Register–Setting the Pulser current

By setting the bits CC1, CC0 in the Line Type Memory, it is possible to program the driving current capability of the transmitter, and hence its strength, as shown in the following Truth Table:

Pulser Current Setting Truth Table

CC1	CC0	PULSER OUTPUT CURRENT (TYP)
0	0	2.1A
0	1	1.75A
1	0	0.7A
1	1	0.35A

Beam forming Programming Modes - Setting a New Line

In Beamforming mode, three different Programming Modes for setting a new transmit line (namely setting the Starting Address, Transmit Delay, Pulse Width and Transmit Cycles registers for every channels) are supported. The selected Programming Mode is determined by the command bits of the SPI programming word.

The following modes are supported:

Transmit Beamforming Programming Modes

BEAMFORMING PROGRAMMING MODES	DESCRIPTION	SPI COMMAND NAME	SPI COMMAND LENGTH (BYTES)
Internal Line Memory Mode	The device uses the internal Line Number Memory. The line information (transmit delay and starting address) are stored into the embedded LN Memory. In between the lines, the LN and LT addresses are provided by Set New Line 1 command.	Set New Line 1	4
External Line Memory with Apodization Mode	The device uses an external Line Number memory. The embedded LN Memory is not used. Apodization is supported. In between the lines, the LT address, the transmit delay and the starting address (PWT_ADD) for each individual channel are provided by Set New Line 2 command.	Set New Line 2	26
External Line Memory Without Apodization Mode	The device uses an external Line Number memory. The embedded LN Memory is not used. Apodization is not supported. In between the lines, the LT address, the transmit delay information for each individual channel and the starting address (PWT_ADD) common for all channels are provided by Set New Line 3 command.	Set New Line 3	20

Transmit Line Set New Line Data Structure

In order to prepare the state machine for the next transmission, the user has to transfer a "Set New Line" Command (reference register map)

The data structure of the 3 "Set New Line" Commands for the 3 different beamforming modes is shown below:

Set New Line Command Data Structure

BEAMFORMING MODE COMMAND TYPE	REGISTER NAME	SPI INTER LINE PROGRAMMING LENGTH (BYTES)	SPI COMMAND DESCRIPTION (REFER TO THE REGISTER MAP)	DESCRIPTION
Internal line memory mode	Set New Line 1	1 address byte + 3 data bytes= 4bytes	(ADD[7:0])+(00000,LN[10:0],LT[6:0],INV)	Register SPI Address + Line Number + Line Type + Invert Bit
External line memory mode with apodization	Set New Line 2	1 address byte + 25 data bytes= 26 bytes	(ADD[7:0])+ (LT[6:0],INV) + 8 x (DLY[12:0],PWT_ ADD[9:0],RX)	Register SPI Address + (Line Type + Invert Bit) + 8 x (Transmit delay + Pulse Wave Table Address + Rx enable)
External line memory mode without apodization	Set New Line 3	1 address byte +19 data bytes=20 bytes	(ADD[7:0]) + (LT[6:0],INV) + (000000,PWT_ ADD[9:0]) + 8 x (0,DLY[12:0],RX,TX)	Register SPI Address + (Line type + Invert bit) + Pulse Wave Table Address + 8 x (Transmit delay + RX enable + TX enable)

	LEGEND
ADD[7:0]	Register SPI Address. The MSB (R/W Bit) is zero while ADD[6:0] bits are the actual SPI register address.
LN[10:0]	Line Number Pointer (11 bits)
LT[6:0]	Line Type Pointer (7 bits)
DLY[12:0]	Channel Transmit Delay (13 bits)
PWT_ADD[9:0]	Pulse Wave Table Starting Address (10 bits)
INV	Invert bit (1 bit)
RX	Receiver Enable (1 bit)
TX	TX Enable (1 bit)

Beamforming Description - Waveform Description

The transmission starts at the address pointed by the Starting Address Register and ends as soon as the End-of-Pattern EOP symbol is found and the Transmit Cycles counting is elapsed.

For 3 Levels transmission [DINP,DINN] = [11] is considered as an End-of-Pattern symbol (EOP).

For 5 Levels Transmission [DINPx, DINNx, DINPy, DINNy] = [11XX]is considered as an End-of-Pattern symbol (EOP).

Memory is read out sequentially. Transmission ends if one of the events below occur:

1) The EOP symbol is found AND the Transmit Cycles counting is completed (except CWD mode)
2) TRIGGER signal is zeroed

Every channel transmit independently of the others. Different channels can possibly transmit different patterns if apodization needs to be supported.

Depending on the Beamforming Programming mode, the starting address information for each individual channel can be either embedded into the Line Number Memory for each channel (reference "Set New Line 1" Command) or can be programmed in between the lines through SPI (Ref. "Set New Line 2" and "Set New Line 3" Commands).

The Transmit Cycle information are stored into the Line Type memory and are global for all the channels. Each "Set New Line" command includes a pointer to the Line Type Memory.

Refer to the Line Type Memory Description for more information.

Waveform Description Truth Table–3 Levels

For 3 Levels operations, each sample stored into the PWT Memory consists of 2 bits (DINNx, DINPx) and corresponds to 4 different status as described in Transmit Beamforming Mode Control–3 Level Operation.

Transmit Beamforming Mode Control–3 Level Operation

DINPX	DINNX	HVOUTX	LVOUTX	STATUS
0	0	Clamp on Damp off	T/R Switch off	Return to Zero (Clamp) (*)
0	1	$V_{VNN\_}$	T/R Switch off	Transmit Negative Pulse (V_{NN}) (*)
1	0	$V_{VPP\_}$	T/R Switch off	Transmit Positive Pulse (V_{PP}) (*)
1	1	Clamp on Damp on	T/R Switch on	T/R Switch on - Receive (**) End of Pattern symbol (EOP)

**TX Enable bit is high*

***RX Enable bit is high*

Waveform Description Truth Table–5 Levels

For 5 Levels operations, the high Voltage outputs (HVOUT pins) must be externally hardwired two by two:

HVOUT1 shorted to HVOUT5, HVOUT2 shorted to HVOUT6, HVOUT3 shorted to HVOUT7, HVOUT4 shorted to HVOUT8.

Each sample stored into the PWT Memory consists of 4 bits: DINPx, DINNx , DINPy, DINNy in which (x,y) = (1,5); (2,6); (3,7); (4,8).

DINPx and DINNx are stored into the corresponding memory banks (Pulse Wave Table Chx, x = 1,2,3,4)

DINPy and DINNy are stored into the corresponding memory banks (Pulse Wave Table Chy, y = 5,6,7,8)

Each sample corresponds to 7 different status as described in Waveform Description Truth Table–5 Level Operation.

Waveform Description Truth Table–5 Level Operation

DINPX X = 1,2,3,4	DINNX X = 1,2,3,4	DINPY Y = 5,6,7,8 (***)	DINNY Y = 5,6,7,8 (****)	OUTX = OUTY X-Y = 1-5,2-6,3-7,4-8	LVOUTX X = 1,2,3,4	LVOUTY Y = 5,6,7,8	STATUS
0	0	0	X	Hi-Z Damp off	T/R Switch off	T/R Switch off	High-Impedance Mode
0	0	1	X	Clamp on Damp off	T/R Switch off	T/R Switch off	Return to Zero (Clamp) (*)
1	0	X	0	V_{VPPA} Damp off	T/R Switch off	T/R Switch off	Transmit Positive Pulse to V_{PPA} (*)
0	1	X	0	V_{VNNA} Damp off	T/R Switch off	T/R Switch off	Transmit Negative Pulse to V_{NNA} (*)
1	0	X	1	V_{VPPB} Damp off	T/R Switch off	T/R Switch off	Transmit Positive Pulse to V_{PPB} (*)
0	1	X	1	V_{VNNB} Damp off	T/R Switch off	T/R Switch off	Transmit Negative Pulse to V_{NNB} (*)
1	1	X	X	Clamp on Damp on	T/R Switch on	T/R Switch off	T/R Switch On–Receive Receive on LVOUTx x = 1,2,3,4 (**) End-of-Pattern Symbol (EOP)

**) TX Enable is High*

***) RX Enable is High*

****) DINPy is a clamp (return to zero) enable.*

*****) DINNy determines whether the "A" or "B" pulsing is enabled (Selection bit).*

Transmit Delay and Pulse Width Description

The Transmit delay is calculated from the positive edge of the Trigger (TRIG) signal.

The delay is the sum of a fixed delay (latency), same for all the channels, plus a beamforming variable delay (BF delay) which is different for each individual channel. Refer to the "Configuration Register "BF cfg" (bits[1:0]) - Latency" paragraph for further information about the fixed delay.

The BF delay can be programmed for each individual channel from zero to (2^{13}-1) clock periods (13 bits register), with one clock period time resolution. Assuming a 200 MHz master clock, this means 5ns of BF delay resolution and about 40.9µs maximum BF delay.

Depending on the Beamforming Programming mode, the BF Delay information for each individual channel can be either embedded into the Line Number Memory for each channel (reference "Set New Line 1" Command) or can be programmed in between the lines through SPI (reference "Set New Line 2" and "Set New Line 3" Commands).

The Pulse Width information (i.e. the time base for each transmitted pulse) are stored into the Line Type Memory and are global for all the channels. Each "Set New Line" command includes a pointer to the Line Type Memory.

Refer to Line Type (LT) Memory - Detailed Description for further details.

Transmit Timings

Transmission starts at the rising edge of the Trigger signal, sampled on rising edge of the master clock. After a fixed latency (see latency calculation paragraph) plus the beamforming delay, each channel transmits the preprogrammed waveform. During the entire transmission phase, the Trigger (TRIG) must stay logic-high. The Trigger must be driven logic low only after the latest channels completed the transmission. A new configuration setting (for instance a new "Set new line" command) can be transferred through SPI after at least 21 clock cycles from the falling-edge of the Trigger signal.

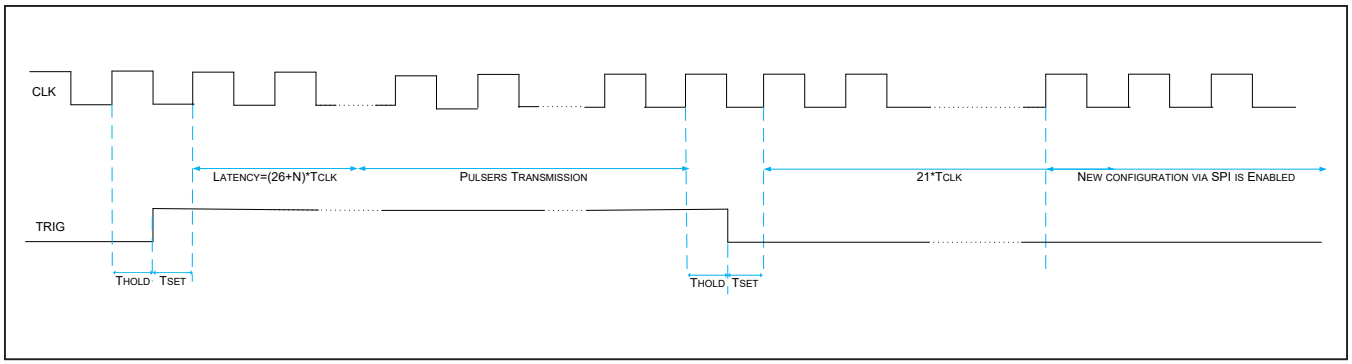


Figure 7. MAX14813 Transmit Timings

Configuration Registers

Configuration

Different device configurations are supported depending on the content of a few configuration registers.

The first SPI Commands after entering in Beamforming Mode must be used to properly configure the device.

The most important configuration settings are described in the next paragraphs.

Configuration Register "BF cfg" (bits [7:6]) - Operating Modes

Configuration Bits–Operating Modes Bits

BIT NAME	BIT #	DESCRIPTION
BF Enable	7	When set Low (default), the Beamforming (BF) is disabled and the Device is set in Shut down mode. Transmission and reception are disabled. Pulsers and T/R switches are OFF. The Floating Power Supplies are disabled. This is the default mode at power up and every-time the device is entered in Beamforming Mode. When set high this bit enables the beamforming, the Finite State Machine and the floating power supplies (see also Floating power supplies Enable registers). It takes 0.5ms to enable the device from this mode.
3/5 Levels	6	When set low (default), the device operates in 3 Levels mode . When set high, the device operates in 5 Levels mode.

Configuration Register "BF cfg" (bits[5:4]) - Line Sequencer Enable

It is made possible to automatically transmit a sequence of consecutive lines which are transmitted at each trigger event provided that no any "set New Line command" is received. This function is referred as a Line Sequencer.

Two bits in the Configuration register (BF CFG reg) enable the Line Sequencer:

1) Line Number Sequence Enable Bit (LNSE): if set high then the LN memory address is automatically calculated at every trigger event unless a "set new line command" is received via SPI.
2) Line Type Sequence Enable Bit (LTSE): if set high then the LT memory address is automatically calculated at every trigger event unless a "set new line command" is received via SPI.

If both the LNSE and LTSE are low then the sequencer is disabled (Default at power up).

Refer to the Line sequencer description paragraph for further information about this function.

Configuration Register "BF cfg" (bits[1:0]) - Latency

Two bits in the BF CFG register, determine the latency delay (i.e., the fixed-term in the delay calculation). The latency can be varied among 4 different values and **must be longer than 300ns** for proper operation. The user can pick up the proper value depending on the master clock frequency.

The delay between the rising edge of the Trigger signal and the actual start of the transmission for a given channel and a given line is calculated as the sum of a fixed-term (latency) plus the pre-programmed beamforming delay.

The fixed term (latency) is an integer multiple of the master clock period and must be the same for all the channels in the system. The total latency is given by the following formula:

Latency = (26+N) x Tclk_periods

in which the integer N, is made programmable among 4 different values 64, 32, 16, 8. The programmable N value is determined by the content of the configuration register BF CFG reg[1:0]. Default value at power up is N = 64.

The recommended multiplier factor (N) and the programming bits for different master clock frequencies are shown below:

Latency Calculation–Recommended N Value by CLK Frequency

CLK FREQUENCY (MHZ)	N VALUE	BF CFG REG [1]	BF CFG REG [0]
From 101 to 200	64	0	0
From 51 to 100	32	0	1
From 26 to 50	16	1	0
Less than or equal to 25	8	1	1

Configuration Register "Floating pwr supply enable" (Bits[1:0]) - Floating Power Supplies Enable bits

The device features embedded Floating Power Supplies (FPSs) which generate the supply voltages for the driver of the transmitter HV output stage. With reference to the functional diagram, there exist two pairs of FPS which output the regulated voltages named V_{GPA}, V_{GNA} and V_{GPB}, V_{GNB}.

Two bits in the "Floating pwr supply enable register" allow the user to enable and disable independently each of the two pairs. Even if the embedded FPSs are disabled, operation is still permitted provided that the floating supply voltages are sourced from the exterior.

One typical use of this function is to share the regulated voltages among adjacent devices in the system. When this approach is used, the device with enabled FPSs supplies the adjacent device which must have its corresponding FPSs disabled. This is required to avoid contention which can result in damages. The FPSs sharing approach allows to further reduce the total system quiescent power dissipation.

Set these bits high to enable the FPSs. It takes 0.5ms time (max) from the moment when these bits are set high to the moment when the Floating Power Supply reaches the nominal value and transmission can start.

Set these bits low (default at power-up) to disable the FPSs.

Configuration Register "SPI Configuration Register" (Bits[7:0])

The SPI interface as well as the Fault management strategy can be configured by programming the SPI Configuration Register.

Moreover bits [3:0] allow to fine tune the TRIG and CLOCK delays to compensate PCB related skews and ease the synchronization.

BIT NAME	BIT #	DESCRIPTION
Enable Data Output on SDIO	7	The SDIO is initially set as an Input pin only (default at power up). Set this bit high to configure the SDIO pin as an I/O bidirectional pin and enable read operation through it. Set this bit low (default) to configure the SDIO pin as an Input pin only
Force CRC Check Mode Enable	6	Set this bit high to force a CRC check after each SPI command. When set High, a specific SPI Command has to be transmitted after each SPI programming to check the data integrity of the previous SPI programming. If bit 4 of this register is set logic High, the transmit finite state machine is enabled and the command is accepted only if the check is successful. Set this bit low (default) to inhibit this check. Refer. to the CRC function description for further details.
Enable Interrupt on SYNC/ INT pin	5	When set high any detected fault condition causes an interrupt signal to be sent out onto the SYNC/INT active low pin. When set low (default) the interrupt on SYNC/INT is disabled
Enable "stop TRIG on Fail Function"	4	When set high (default) any detected fault condition causes the transmission to be inhibited and any TRIG signal to be ignored. When set low the transmission is still possible even in presence of detected fault conditions.
TRIG Delay	3:2	These two bits allow setting the trigger delay in order to ease synchronization with the master clock signal (refer to Trigger synchronization paragraph)
CLK Delay	1:0	These two bits allow setting the master clock delay in order to ease synchronization with the trigger signal (refer to Trigger synchronization paragraph)

Configuration Register "SPI Configuration" (Bits[3:0])–Synchronization Bits

The system trigger signal needs to be synchronized with the master clock signal. In order to ease the synchronization between clock and trigger and compensate possible skews between the correspondent PCB traces, the device features programmable delay lines on both clock and trigger internal signals. The clock and trigger internal propagation delays can be independently increased so that internal clock and trigger line can be typically re-aligned in presence of skew. The programmable delay ranges between 0 to +0.6ns with 3 steps of 0.2ns typical. The configuration Bits (TRIG delay and CLK delay) are in the "SPI configuration" register. The default value is 0.
Timing diagram and the truth table are shown below.

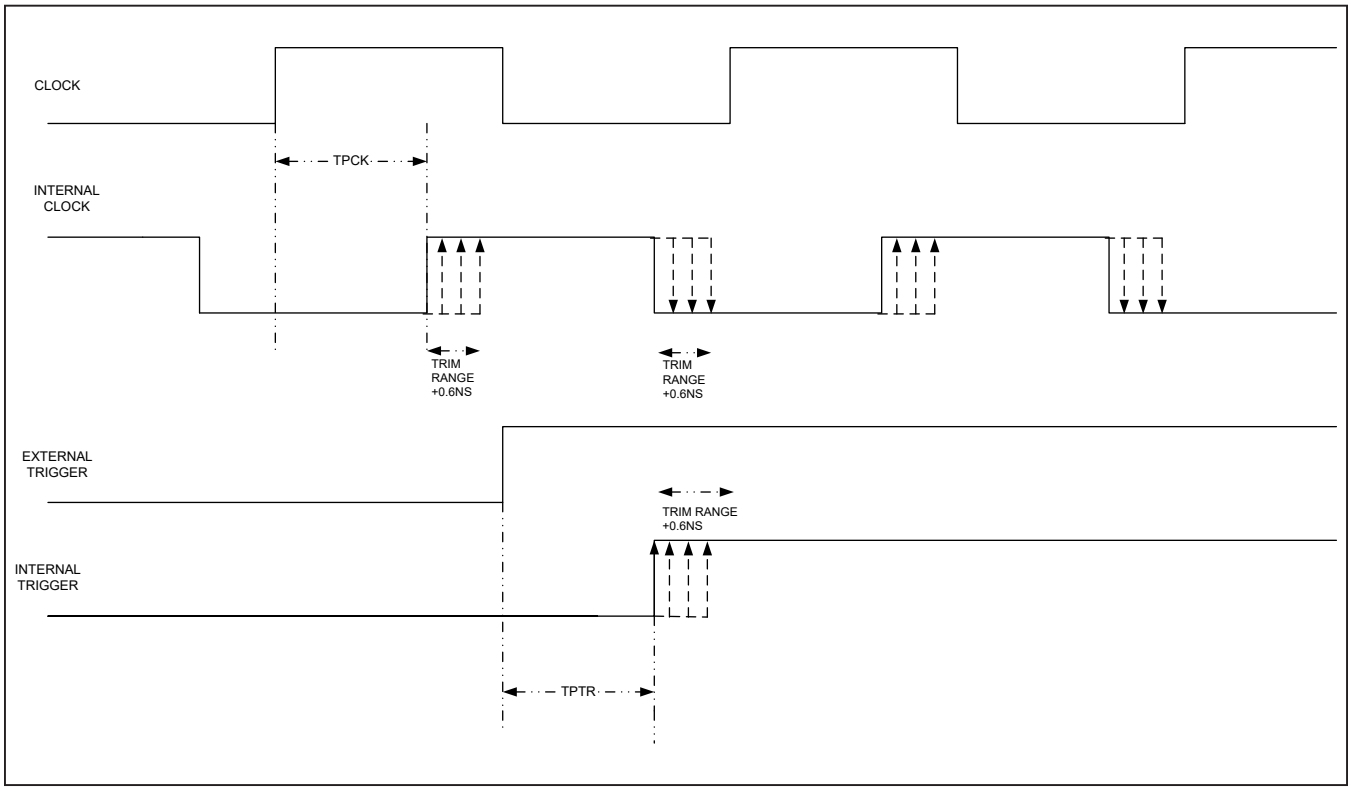


Figure 8. Trigger and Clock Synchronization Timings

Table 1. Trig and Clock Fine Tuning Delay Truth Table

SPI CONFIGURATION REGISTER				SPI CONFIGURATION REGISTER		
TRIG Delay				CLK Delay		
0x01 [3]	0x01 [2]	Typ Delay (ns)		0x01 [1]	0x01 [0]	Typ Delay (ns)
0	0	0		0	0	0
0	1	0.2		0	1	0.2
1	0	0.4		1	0	0.4
1	1	0.6		1	1	0.6

Channel Enable and TX Enable Registers

Channels can be individually enabled by programming the "CH ena reg" and the "TX ena reg".

The following table applies.

Channel Enable/Disable Registers - Table

	Bits per register	Description
CH ENA Reg	8	The content of this register enables (bit set logic high) or disable (bit set logic low), the correspondent channel. For further information, see the TX/RX Enable Truth Table in the next paragraph and the Register Map Description.
TX ENA Reg	8	The content of this register enables (bit set logic high) or disable (bit set logic low), the transmission of the correspondent channel. For further information, see the TX/RX Enable Truth Table in the next paragraph and the Register Map Data Description.

TX/RX Enable Truth Table

TX and RX can be independently enabled/disabled for each channel by mean of three bits:

1) The CH ENA bits allows enabling/disabling each channel. These bits are stored into the "CH ENA reg" Register.
2) The TX ENA bits allows enabling/disabling the transmission for each channel. These bits are stored into "TX ENA reg" Register or are supplied inter-lines whenever the External Line Memory Mode without Apodization is used (refer to "Set new Line 3" command).
3) The RX ENA bit allows enabling/disabling the receive (T/R switch) for each channel. These bits are stored into the Line Number Memory for each Line and for each channel (Internal Line Memory Mode) or are sent interlines when the External Line Memory Modes are used (refer to "Set new Line 2" and "Set new Line 3" commands).

The Truth Table below summarizes the priorities among the three bits.

Tx/Rx Enable Truth Table SPI Description

CH ENA	TX ENA	RX ENA	BEAMFORMING FSM
0	X	X	Transmission is Disabled, T/R switch is Disabled
1	1	0	Transmission is Enabled, T/R switch is Disabled
1	1	1	Transmission is Enabled, T/R switch is Enabled
1	0	0	Transmission is Disabled, T/R switch is Disabled
1	0	1	Transmission is Disabled, T/R switch is Enabled

SPI Description

SPI Port Description

The interface allows read/write access to all the registers that configure the device and the on chip SRAMs.

SPI interface pins are SCLK, CS, SDIO and SDOUT.

The SPI operates as a standard synchronous serial communication port. Refer to Figure 2 for TX SPI Timings.

For Write operation, SPI operates up to 50MHz.

For Read operation, the clock frequency must be set to accommodate the SCLK to SDOUT or the SCLK to SDIO delay (see Electrical Characteristics). Note that this parameter depends on the equivalent capacitance on the SPI output pin which is PCB dependent.

SDIO is data input pin and it is sampled on SCLK rising edge.

SDOUT is data output pin, data are output on SCLK falling edge. SDOUT is in High-Impedance state (Hi-z) when CS = 1.

Data can also be sent out using the bidirectional SDIO pin. To avoid contentions, at power up the SDIO pin is set as an Input pin. It can be declared as an Input/Output pin by writing the SPI configuration register (bit 7). When the SDIO is enabled as a bidirectional pin, data are output on the SCLK falling edge.

CS is an active-low chip select. When CS goes low, SPI address and data transfer begins. Data transfers are byte oriented: a transfer is made by 2 or more bytes.

CS can change only when SCLK is logic-low (refer to SPI Timing in Figure 3)

For single Register Read and Write operations, the first byte (ADD[7:0]) is made by the Read/Write bit (ADD[7] = R/W) followed by the actual Register Address (ADD[6:0]). The following bytes are data bytes. Single Registers data size can be 1 byte, 2 bytes, 3 bytes, 19 bytes, 25 bytes long. (refer to Register Map–Data Description Table).

When a Read operation is performed (ADD[7] = 1, the content of the register is output on SDOUT and/or on SDIO (when enabled as a bidirectional pin).

For LN Memory, PWT Memory and LT Memory Read and Write operations, the following procedures are required.

To write a Memory word, the first byte identifies the Memory block (0,ADD[6:0]), while the following two bytes represent the Memory Address (MEM_ADD[15:0]) . They are followed by the data bytes. Contiguous words of the Memory block can be written in burst mode so that multiple words can be written in a single transfer. In this case, the word addresses are calculated incrementally starting from the initial word address.

To read a Memory word, two consecutive SPI transfers are necessary. The first SPI transfer sets the memory block (0,ADD[6:0]) and the memory address (MEM_ADD[15:0]) to be used for the next read operation. The second SPI transfer, which is headed by the (1, ADD[6:0]) byte, effectively outputs the word data either on SDOUT or SDIO (when enabled as a bidirectional pin).

Contiguous words of the RAM blocks can also be read in burst mode so that multiple data bytes can be read in single transfer. In this case, the word addresses are calculated incrementally starting from the initial word address.

The Transmit SPI Timing Diagrams in Figure 3 and Figure 4 show all the possible cases.

Also refer to the Register Map–Data Description Table for further information about the SPI Data structure.

Registers Read and Write Operation

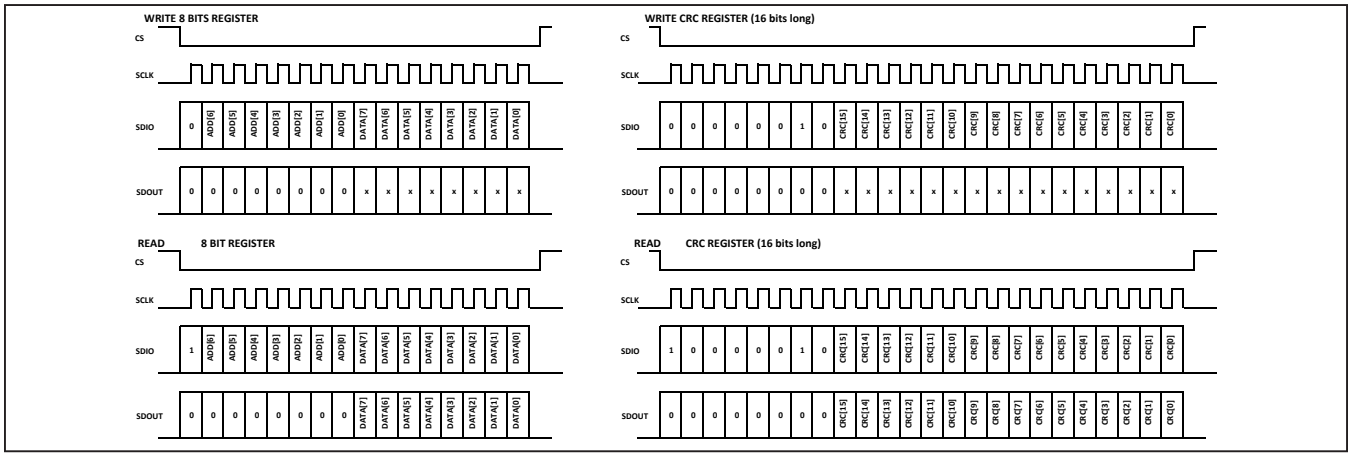


Figure 9. Read and Write Operation

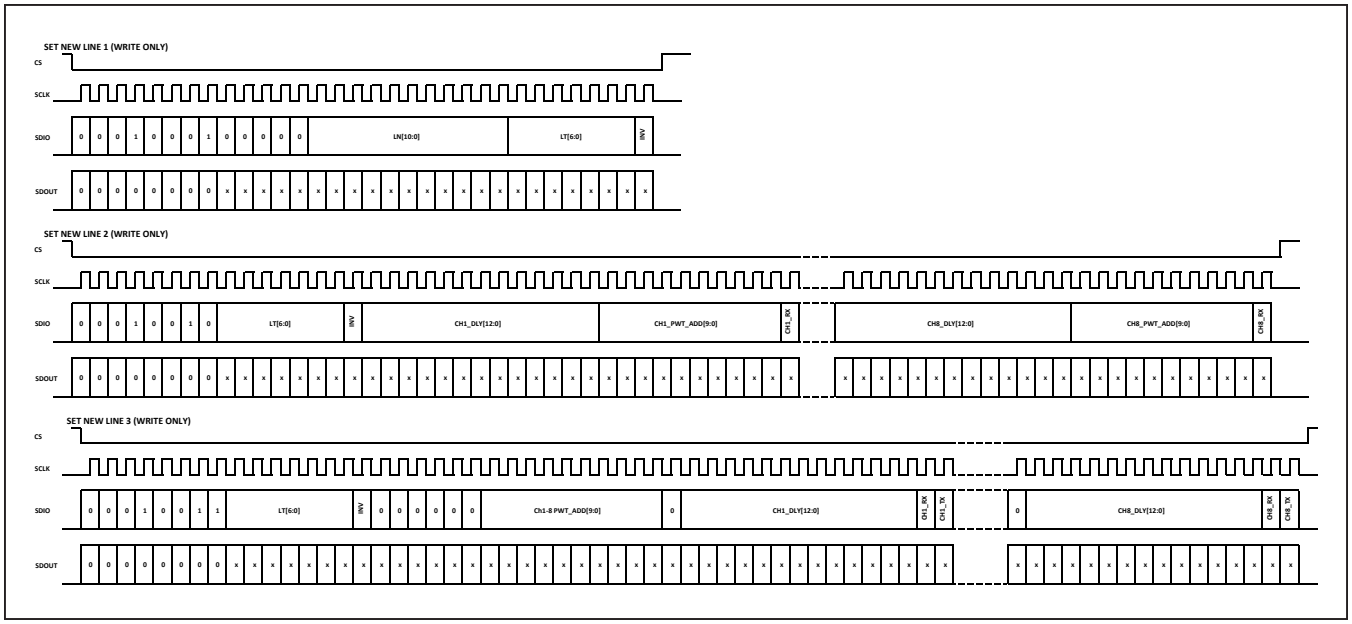


Figure 10. Registers Read and Write Operation

Memory Read and Write Operation

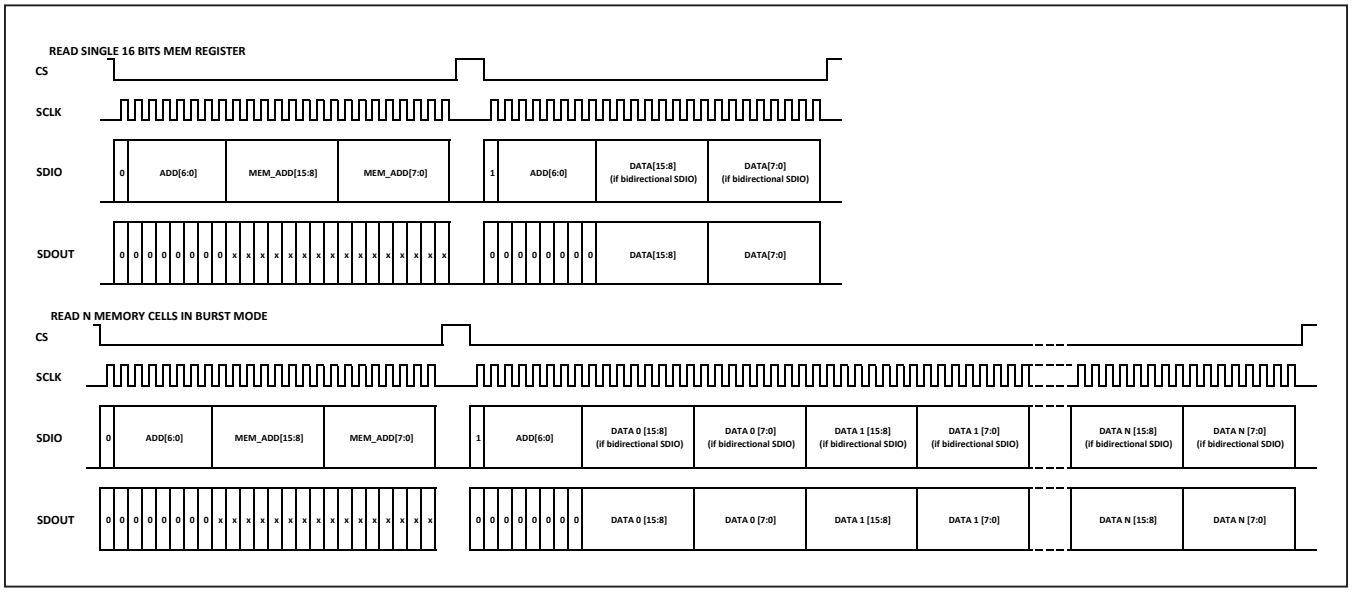


Figure 11. Memory Read and Write Operation

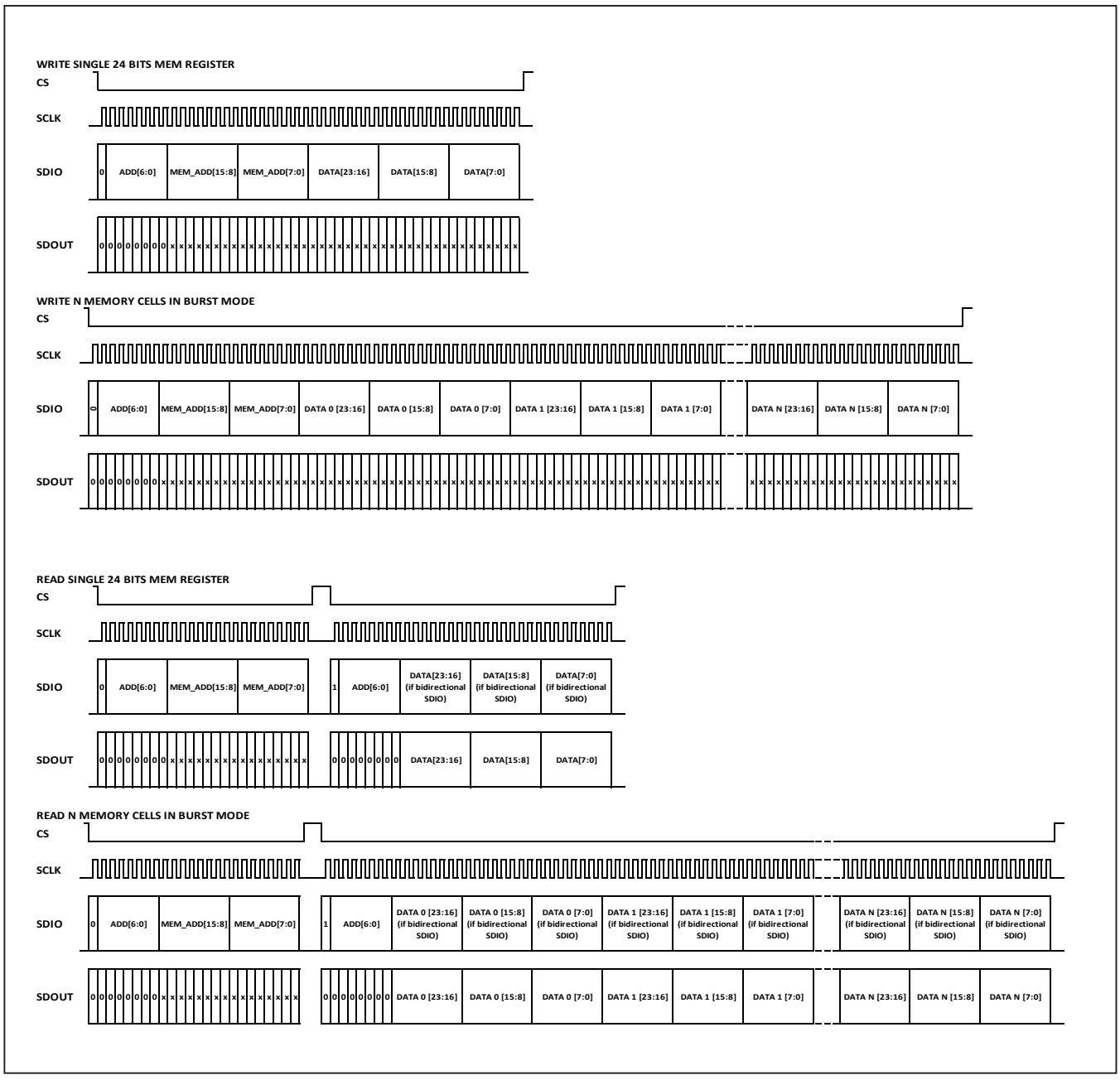


Figure 12. Memory Read and Write Operation

CRC–Cyclic Redundancy Check

An optional 16-bit CRC (cyclic redundancy check) is integrated to check the integrity of the data communication through the SPI. The CRC is based on the USB 16 bits CRC standard (CRC-16-IBM)

adopting the following generator polynomial: $x^{16} + x^{15} + x^2 + 1$.

The device calculates the CRC at each programming session and stores it into the CRC register. There are two manners to verify the CRC16 signature:

1) Reading the CRC register. In this case the former CRC16 signature calculated on the last SPI command, is output and possible mismatches can be checked outside the device.
2) Writing the CRC register. In this case the CRC16 signature is written into the device. Such a signature is compared with the former CRC16 signature computed during the previous SPI transfer: in case of mismatch a fault is generated.

In the latter case, in which the CRC verification is left to the device itself, any CRC mismatches cause the “CRC error bit” (register 0x8F, bit 1) to be flagged and made available for later interrogations. Moreover, an interrupt is signaled out asserting the open drain output pin SYNC/INT provided that this function is enabled (see register 0x01, bit 5). Finally, if the "Enable stop TRIG on fail function" is enabled (register 0x01, bit 4), the device is inhibited to transmit and any subsequent trigger event is ignored until the error register is read.

The CRC is optional. To Force the CRC check, the "Force CRC check mode" bit into the SPI Configuration Register must be set High. In this case after each SPI command the CRC register must be written so that the signature can be verified as per above description.

CRC–Cyclical Redundancy Check Detailed Description

At the beginning of the SPI transfer (CSB falling edge), the 16-bit CRC register is initialized with “all-ones” value: 0xFFFF.

Afterwards, the CRC signature is computed based on serial data sampled on SDIO on every SCLK rising edge as shown in Figure 13.

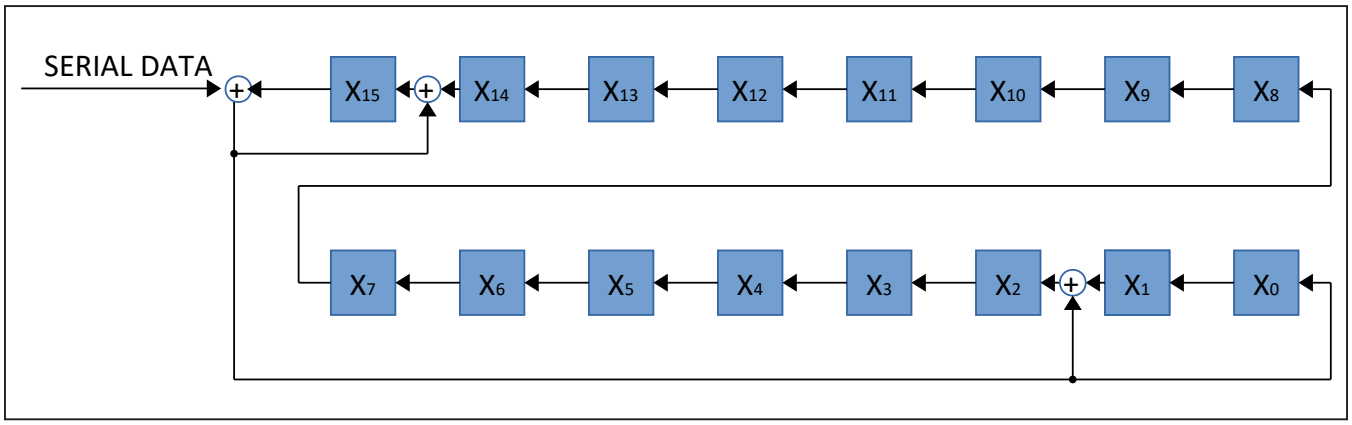


Figure 13. CRC Algorithm Diagram

Note: CRC is computed on sampled data on SDIO pin, regardless whether the SDIO is used as an Input or an output pin.

At the end of each SPI transfer (CSB rising edge), the current CRC signature is stored into a temporary register to be checked on following SPI transfers.

For example, let's suppose you have to write register 0x08 with the value 0x56. The corresponding SPI data transfer is 0000-1000-0101-0110. As a result, the computed CRC signature for such a data transfer, will be 0x31FA as shown in Figure 14.

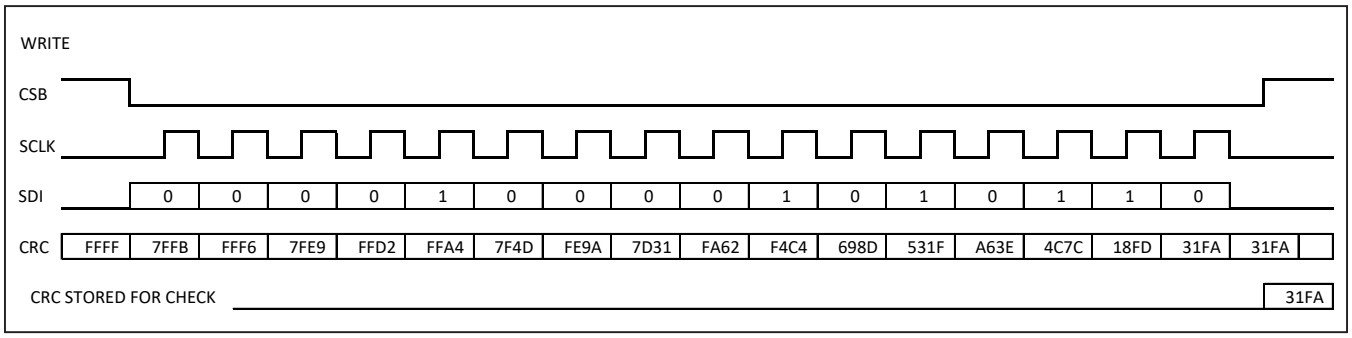


Figure 14. CRC computation Example

At the end of the transfer the CRC code is stored into register 0x02 for future interrogations.

There are two possible ways to use register 0x02 for CRC: reading it or writing it.

When the register 0x02 is read, the 16-bit CRC code related to the previous data transfer is sent out. Continuing the example above, the next figure shows what you would get by reading register 0x02 (data are the 16 LSBs). In this case, external digital resources are supposed the do the CRC verification.

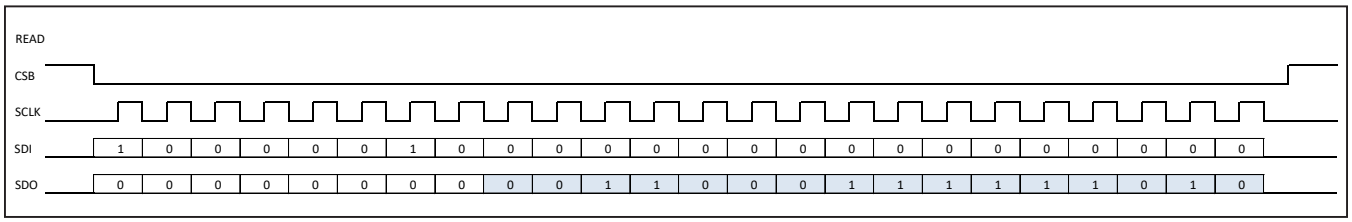


Figure 15. Reading the CRC register Example

Alternatively, you can write the CRC into the register 0x02 and let the device itself to make the CRC verification.

Continuing the example above, this means that you have to write 0x31FA into the register 0x02.

Now, if the written value does not match the CRC code from the previous transfer, then the CRC error bit (reg. 0x0F bit 7) will be set high. Moreover the interrupt will be asserted causing the $\overline{INT}$ to go low (assuming this function is enabled according to bit 5 of reg.0x01)

On the contrary, if the written value matches the CRC from the previous transfer, then the CRC error bit will be set to zero and no any interrupt will be sent out on /INT pin.

The next two figures show the two cases respectively:

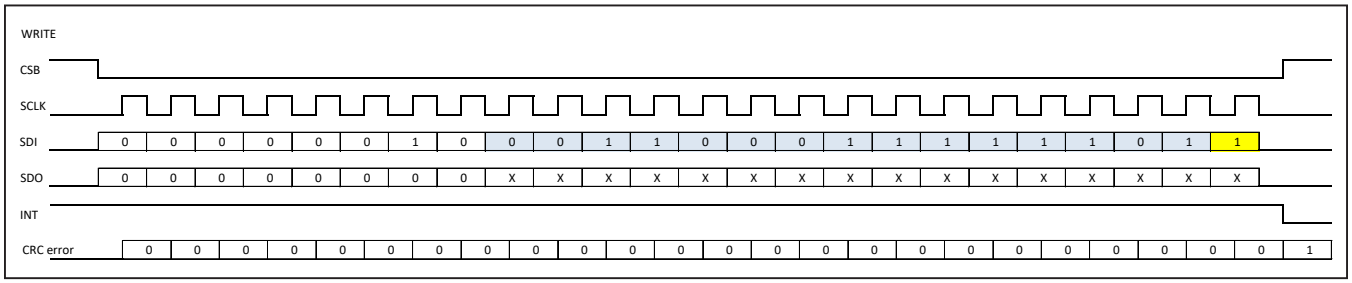


Figure 16. Polling the CRC by Writing the CRC—CRC Does Not Match.

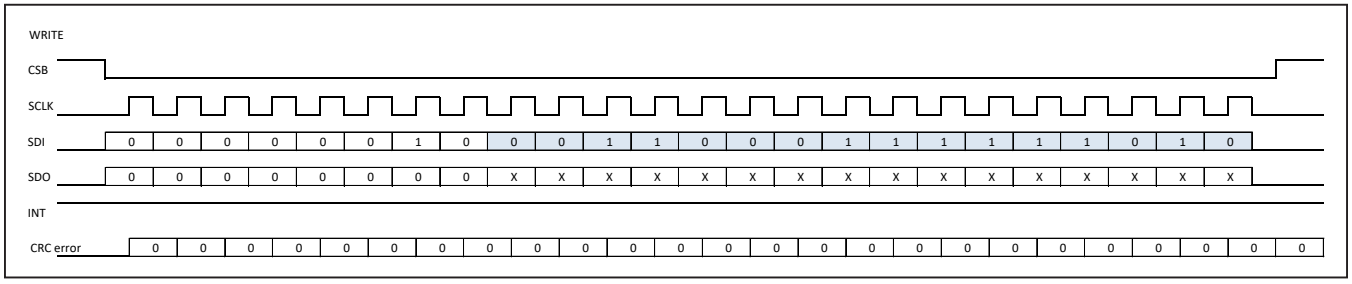


Figure 17. Polling the CRC by Writing the CRC—CRC Matches.

You can force the CRC check by setting high bit 6 into register reg. 0x01. Doing that, after each SPI transfer, you are required to verify the CRC by writing the reg. 0x02, otherwise “CRC check CMD not received” error will be set (register 0x8F, bit 6). If two consecutive write operations are executed onto register 0x02 without any SPI transfer in between, then a “CRC check CMD after CRC check CMD” error will be set (register 0x8F, bit 5).

Fault Detection Strategy

Four categories of faults are detected and signaled:

1) Address Errors (reference "Address Errors" register): these are mainly overflow kind of errors. Every time an address error occurs the corresponding bit is asserted. Refer to the Register Map–Data Description Table for the full list of address errors. The register is cleared on read.
2) SPI Errors (reference "SPI Errors" register): this category includes CRCs related errors and SPI data inconsistency errors. Every time an SPI error occurs, the corresponding bit is asserted. Refer to the Register Map–Data Description Table for the full list of SPI Errors. The register is cleared on read.
3) TRIG Errors (reference "Trigger Errors" register): These errors are signaled every time a TRIG falling edge is detected during waveform generation (with the exception of CWD). When the failure occurs, bits corresponding to the failed channels into the Trigger Errors register are set logic-high. The register is cleared on read.
4) Thermal Errors (ref "Thermal status" register): if the junction temperature exceeds 110C the "Thermal Warning" bit is output on pin THP and the "Thermal Warning (latched)" bit is latched high. If the junction temperature exceeds 150C the "Thermal shutdown" bit is set high disabling the transmission. Moreover, the "Thermal shutdown (latched)" bit is latched high. The register is cleared on read.

Whenever one (or more) among Address, SPI and Trigger error is detected, an interrupt is output on SYNC/INT pin provided that the "Enable interrupt on SYNC/INT pin" into the “SPI configuration” register is set logic high. Moreover the transmit functionality can be inhibited and any subsequent TRIG event ignored provided that the "Enable stop TRIG on fail function" bit into the SPI configuration register is set logic high. The interrupt is de-asserted and normal operation is restored as soon as the error registers are read.

Line Sequencer Description

It is possible to automatically transmit a sequence of consecutive lines. Lines are transmitted in sequence at each trigger event. This function is described here below.

When the sequencer is enabled, then after each line transmission, the Line Number (LN) and Line Type (LT) of the subsequent line are automatically calculated. If no any new "Set New Line Command" is received via SPI, the next Trigger event will cause the "next in sequence" line to be fired.

Two bits in the BF Configuration register ("BF cfg reg") enable the sequencer:

1) Bit 5: Line Number Sequence Enable Bit (LNSE): if set High then the LN memory address is automatically calculated at every trigger event unless a "set new line command" is received via SPI.
2) Bit 4: Line Type Sequence Enable Bit (LTSE): if set High then the LT memory address is automatically calculated at every trigger event unless a "set new line command" is received via SPI.

If both the LNSE and LTSE are low (Default) then the Line Sequencer is disabled.

If the Sequencer is enabled, then the sequencing is determined by

1) 5 bits in the Line Type registers
2) The “Line Number Stop Sequencing” registers (LNSS)
3) The “Line Type Stop Sequencing” register (LTSS)
4) The sequencing starts when a first "Set New Line command" is received.
5) The "Sequencer Repeat Same Line" field into the LT register determines how many times the same line is transmitted (from 1 to 32 times).
6) If LNSE=1 and the "Sequencer Repeat Same Line" counting is completed then the LN is automatically incremented by one.
7) If LTSE=1 and the "Sequencer Repeat Same Line" counting is completed then the LT is automatically incremented by one.
8) When the LN reaches the LNSS then the LN sequence is repeated starting form the first LN (set by the last Set New Line Command)
9) When the LT reaches the LTSS then the LT sequence is repeated starting form the first LT (set by the last Set New Line Command)

In addition, if the sequencer is enabled, an Invert bit into the LT register allows to alternate in phase and out of phase (inverted) patterns in order to support pulse inversion imaging (see Line Type Register description for details).

The user must ensure that the LN and LT cycles are consistent so that the LN and LT remain aligned at every repetition.

Any new "set new line command" interrupts the sequencing and clear the counters.

TX Beamformer Memory Writing Timings

INTER-MODE PROGRAMMING TIME	NUMBER OF BITS	SPI FREQUENCY (MHZ)	PROGRAMMING TIME (MS)
Pulse Wave Table (Kb)	131072	50	2.62*
Transmit Line Number Programming Registers	294912	50	5.9
Transmit Line Type Programming register	3072	50	0.06
Total	429056	50	8.6

Programming time for writing the memories assuming a 50MHz SPI are shown in the Table below

**Note: The 8 benches of the Pulse Wave Table can be also programmed in parallel. In this case the Programming Time for this specific memory is reduced by a factor 8.*

TX Beamformer Inter-Line Programming Timings

The Inter-line programming time depends on the operating mode. The table below summarizes the timings assuming a 50MHz SPI.

OPERATING MODE		NUMBER OF BYTES	SPI (MHZ)	INTER-LINE PROGRAMMING TIME (µS)
Internal Line Memory		4	50	0.64
External Line Memory	Without Apodization	20	50	3.2
	With Apodization	26	50	4.16

Register Maps

- RO = Read-Only Register, R/W= Read/Write Register, WO = Write-Only Register
- The MSB of the address is the Read/Write bit.
- The CRC register data is 2 bytes long. The Set New Line1, Set New Line 2, and Set New Line 3 data registers are 3, 25, and 19 bytes long, respectively. All the other data registers are 1 byte long only.
- Write all the RFUs at 0
- Data are transferred MSB first

ADDRESS (HEX)	READ/WRITE	POR STATE	FUNCTION
0x80	RO	0x00	Chip ID / Rev ID
0x01 Write 0x81 Read	R/W	0x10	SPI configuration
0x02 Write 0x82 Read	R/W	NA	CRC register
0x03 Write 0x83 Read	R/W	0x00	Line Type Stop Sequencing (LTSS)
0x04 Write 0x84 Read	R/W	0x00	Line Number Stop Sequencing - LNSS (MSB)
0x05 Write 0x85 Read	R/W	0x00	Line Number Stop Sequencing - LNSS (LSB)
0x06 Write 0x86 Read	R/W	0x00	BF CFG reg Beam Forming Configuration Register
0x08 Write 0x88 Read	R/W	0x00	CH ENA reg Channel Enable Register
0x09 Write 0x89 Read	R/W	0x00	TX ENA reg Transmit Enable Register
0x0B Write 0x8B Read	R/W	0x00	Floating Power Supply Enable Register
0x8C	RO	N/A	Thermal status
0x8D	RO	N/A	Trigger Errors
0x8E	RO	N/A	Address Errors
0x8F	RO	N/A	SPI errors
0x11	WO	N/A	Set new line 1
0x12	WO	N/A	Set new line 2
0x13	WO	N/A	Set new line 3

Register Map–Data Description Table

FUNCTION	DATA LENGTH	DATA FORMAT
Chip ID/Rev ID	1 byte	NA
SPI Configuration	1 byte	[7]: Enable SDO output on SDIO [6]: Force CRC check mode enable [5]: Enable interrupt on THP/INT pin [4]: Enable "stop TRIG on fail function" [3:2]: TRIG delay [1:0]: CLK delay
CRC Register	2 bytes	[15:8]: CRC16 MSB [7:0]: CRC16 LSB
Line Type Stop Sequencing (LTSS)	1 byte	[7]: 0 [6:0]: Stop Address of the sequencer Line Type Counter
Line Number Stop Sequencing–LNSS (MSB)	1 byte	[7:3]: 0 [2:0]: Three MSB of the Stop Address of the sequencer Line Number Counter
Line Number Stop Sequencing–LNSS (LSB)	1 byte	[7:0]: Eight LSB of the Stop Address of the sequencer Line Number Counter
BF cfg reg Beamforming Configuration Register	1 byte	[7]: Beamforming FSM enable [6]: Beamforming 5 levels (1) or 3 levels (0) mode [5]: Line Number Sequence Enable Bit (LNSE) [4]: Line Type Sequence Enable Bit (LTSE) [3:2]: 0 [1:0]: TR switch setup before transmit (latency)
CH ena reg Channel Enable Register	1 byte	[7]: Channel 8 Enable [6]: Channel 7 Enable [5]: Channel 6 Enable [4]: Channel 5 Enable [3]: Channel 4 Enable [2]: Channel 3 Enable [1]: Channel 2 Enable [0]: Channel 1 Enable
TX ena reg Transmit Enable Register	1 byte	[7]: Transmit 8 Enable [6]: Transmit 7 Enable [5]: Transmit 6 Enable [4]: Transmit 5 Enable [3]: Transmit 4 Enable [2]: Transmit 3 Enable [1]: Transmit 2 Enable [0]: Transmit 1 Enable
Floating Power Supply Enable Register	1 byte	[7:2]: RFU [1]: Floating Power supply A enable [0]: Floating Power supply B enable
Thermal Dtatus	1 byte	[7:4]: RFU [3]: Thermal Warning (latched) [2]: Thermal Warning [1]: Thermal Shutdown (latched) [0]: Thermal Shutdown

Register Map–Data Description Table (continued)

FUNCTION	DATA LENGTH	DATA FORMAT
Trigger Errors	1 byte	[7]: Trigger error on Ch 8 [6]: Trigger error on Ch 7 [5]: Trigger error on Ch 6 [4]: Trigger error on Ch 5 [3]: Trigger error on Ch 4 [2]: Trigger error on Ch 3 [1]: Trigger error on Ch 2 [0]: Trigger error on Ch 1
Address Errors	1 byte	[7]: SCLK high on CSB rising edge [6]: RFU [5]: LTSS[7:0] is greater than 0x7F (1) [4]: Bits [143:138],[127],[111], .. , [15] not zero in “Set New Line 3” transfer (2) [3]: Line Number is greater than LNSS[15:0] when LNSE=1 or Line Type is greater than LTSS[7:0] when LTSE=1 (1) [2]: Line Number is greater than 0x5FF (1) [1]: LNSS[15:0] is greater than 0x5FF (1) [0]: RAM Address Write overflow for all RAM transfers Notes (1) This check is performed at the end of “Set New Line 1” transfer (2) This check is performed at the end of “Set New Line 3” transfer
SPI Errors	1 byte	[7]: CRC error [6]: CRC check CMD not received in force CRC check mode [5]: CRC check CMD after CRC check CMD in force CRC check mode [4]: Not-existent command received [3]: Wrong byte # received in RAM R/W CMD [2]: Error: received only 1 byte [1]: Wrong byte # received in other CMDs [0]: SPI received data was not 8-bit multiple
Set New Line 1	3 bytes	[23:19]: 0 [18:8]: Line Number (LN) [7:1]: Line Type (LT) [0]: Invert Bit (INV)

Register Map–Data Description Table (continued)

FUNCTION	DATA LENGTH	DATA FORMAT
Set New Line 2	25 bytes	[199:193]: Line Type (LT) [192]: Invert Bit (INV) [191:179]: Channel 1 Delay (DLY) [178:169]: Channel 1 Pulse Wave Table (PWT) Address [168]: Channel 1 T/R switch Enable (RX) [167:155]: Channel 2 Delay (DLY) [154:145]: Channel 2 Pulse Wave Table (PWT) Address [144]: Channel 2 T/R switch Enable (RX) . . . . [23:11]: Channel 8 Delay (DLY) [10:1]: Channel 8 Pulse Wave Table (PWT) Address [0]: Channel 8 T/R switch Enable (RX)
Set New Line 3	19 bytes	[151:145]: Line Type (LT) [144]: Invert Bit (INV) [143:138]: 0 [137:128]: Channels 1-8 Pulse Wave Table (PWT) Address [127]: 0 [126:114]: Channel 1 Delay (DLY) [113]: Channel 1 T/R switch Enable (RX) [112]: Channel 1 Transmit Enable (TX) [111]: 0 [110:98]: Channel 2 Delay (DLY) [97]: Channel 2 T/R switch Enable (RX) [96]: Channel 2 Transmit Enable (TX) . . . . [15]: 0 [14:2]: Channel 8 Delay (DLY) [1]: Channel 8 T/R switch Enable (RX) [0]: Channel 8 Transmit Enable (TX)

Memory Register Map

- RO = Read-Only Register, R/W= Read/Write Register, WO = Write-Only Register
- All the data are 3 bytes long.
- Memory Read operations require two consecutive SPI transfers. The first transfer sets the memory address of interest while the second command effectively outputs the corresponding data on either SDOUT or SDIO. Refer to the SPI Timing Diagrams.
- Memory Write and Read operations can be done in burst mode also.
- Data are transferred MSB first

ADDRESS (HEX)	TYPE	POR STATE	FUNCTION
0x100000 - 0x10007F Write 0x100000+0x90 - 0x10007F+0x90 Read	R/W	NA	Line Type Table (LT)
0x1E0000 - 0x1E03FF	WO	NA	Pulse Wave Table (PWT) ch1-4
0x1F0000 - 0x1F03FF	WO	NA	Pulse Wave Table (PWT) ch5-8
0x200000 - 0x2003FF	WO	NA	Pulse Wave Table (PWT) ch1-8
0x210000 - 0x2103FF Write 0x210000+0xA1 - 0x2103FF+0xA1 Read	R/W	NA	Pulse Wave Table (PWT) ch1
0x220000 – 0x2203FF Write 0x220000+0XA2 – 0x2203FF+0XA2 Read	R/W	NA	Pulse Wave Table (PWT) ch2
0x230000 - 0x2303FF Write 0x230000+0XA3 - 0x2303FF+0xA3 Read	R/W	NA	Pulse Wave Table (PWT) ch3
0x240000 - 0x2403FF Write 0x240000+0xA4 - 0x2403FF+0xA4 Read	R/W	NA	Pulse Wave Table (PWT) ch4
0x250000 - 0x2503FF Write 0x250000+0xA5 - 0x2503FF+0xA5 Read	R/W	NA	Pulse Wave Table (PWT) ch5
0x260000 - 0x2603FF Write 0x260000+0xA6 - 0x2603FF+0xA6 Read	R/W	NA	Pulse Wave Table (PWT) ch6
0x270000 - 0x2703FF Write 0x270000+0xA7 - 0x2703FF+0xA7 Read	R/W	NA	Pulse Wave Table (PWT) ch7
0x280000 - 0x2803FF Write 0x280000+0xA8 - 0x2803FF+0xA8 Read	R/W	NA	Pulse Wave Table (PWT) ch8
0x300000 – 0x3005FF	WO	NA	Line Number Table (LN) ch1-8
0x310000 – 0x3105FF Write 0x310000+0xB1 – 0x3105FF+0xB1 Read	R/W	NA	Line Number Table (LN) ch1
0x320000 – 0x3205FF Write 0x320000+0xB2 – 0x3205FF+0xB2 Read	R/W	NA	Line Number Table (LN) ch2
0x330000 – 0x3305FF Write 0x330000+0xB3 – 0x3305FF+0xB3 Read	R/W	NA	Line Number Table (LN) ch3
0x340000 – 0x3405FF Write 0x340000+0xB4 – 0x3405FF+0xB4 Read	R/W	NA	Line Number Table (LN) ch4
0x350000 – 0x3505FF Write 0x350000+0xB5 – 0x3505FF+0xB5 Read	R/W	NA	Line Number Table (LN) ch5
0x360000 – 0x3605FF Write 0x360000+0xB6 – 0x3605FF+0xB6 Read	R/W	NA	Line Number Table (LN) ch6
0x370000 – 0x3705FF Write 0x370000+0xB7 – 0x3705FF+0xB7 Read	R/W	NA	Line Number Table (LN) ch7
0x380000 – 0x3805FF Write 0x380000+0xB8 – 0x3805FF+0xB8 Read	R/W	NA	Line Number Table (LN) ch8

Memory Register Map–Data Description

FUNCTION	DATA LENGTH	MEMORY TYPE	DATA FORMAT
Line Type Table (LT)	3 bytes	128 x 24 bit	[23:16]: Cycles Number (CYCLES[7:0]) [15]: LDM = Low Drop Mode [14]: SEQINV bit. Alternate in-phase and out of phase lines when sequencer is enabled. [13:8]: Program Pulse Width (PW[5:0]) [7:3]: Define number of line iterations of the sequencer (SEQRPT[4:0]) [2]: Continuous Wave Doppler Mode bit (CWD) [1:0]: Set pulser driving current (CC1, CC0]
Pulse Wave Table (PWT) ch1-4	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch5-8	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch1-8	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch1	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch2	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]

Memory Register Map–Data description (continued)

FUNCTION	DATA LENGTH	MEMORY TYPE	DATA FORMAT
Pulse Wave Table (PWT) ch3	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch4	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch5	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch6	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch7	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]
Pulse Wave Table (PWT) ch8	2 bytes	1024 x 16 bit	[15:14]: First symbol [DINP0, DINN0] [13:12]: Second symbol [DINP1, DINN1] [11:10]: Third symbol [DINP2, DINN2] [9:8]: Fourth symbol [DINP3, DINN3] [7:6]: Fifth symbol [DINP4, DINN4] [5:4]: Sixth symbol [DINP5, DINN5] [3:2]: Seventh symbol [DINP6, DINN6] [1:0]: Eighth symbol [DINP7, DINN7]

Memory Register Map–Data description (continued)

FUNCTION	DATA LENGTH	MEMORY TYPE	DATA FORMAT
Line Number Table (LN) ch1-8	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch1	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch2	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch3	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch4	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch5	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch6	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch7	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit
Line Number Table (LN) ch8	3 bytes	1536 x 24 bit	[23:11]: Delay (DLY) [10:1]: Pulse Wave Table (PWT) Address [0]: T/R switch Enable (RX) bit

Applications Information

Bypass capacitor on HV supplies

In order to minimize the parasitic inductance of the connecting trace, HV Bypassing capacitors between the HV supply input pins and ground (pins $V_{PP\_}$, $V_{NN\_}$) must be placed as close as possible to the device. The usage of capacitors with low ESL and ESR is recommended.

Bypass capacitors Floating Power Regulators Outputs

Connect 1µF bypass capacitors between each pin ($V_{GP\_}$, $V_{GN\_}$) and the paired voltage supply ($V_{PP\_}$, V_{NN}) as per the pin description.

Place capacitors as close as possible to the device and minimize trace lengths.

Use SMD bypass capacitance with voltage rating greater than 6V, low ESR, and ESL.

Cell PCB layout

A symmetrical PCB cell layout is recommended in order to have same performances amid the right and left channels. This implies using same bypass capacitors placement for each power supply input ($V_{PP\_}$, $V_{NN\_}$, $V_{GP\_}$, $V_{GN\_}$, $V_{CC\_}$ $V_{EE\_}$) on the right and left side of the device.

Thermal considerations

The inner balls of the ball grid array must be connected to GND. To aid heat dissipation, having multiple ground planes connecting the device GND balls on the top layer and inner layers of the PCB is recommended. Multiple vias must be used to ensure a good thermal and electrical conduction between the top and inner layers.

Power UP/DW Sequencing

For 3 Levels operation in which V_{PPA} and V_{PPB} as well as V_{NNA} and V_{NNB} are externally hardwired, there is not any power up/dw sequencing to be followed. The low voltage supplies (V_{IO}, V_{CC}, V_{EE}) and the HV supplies (V_{PP}, V_{NN}) can be turned on and off with whatever sequencing.

In 5 Levels Configurations (either Direct Mode-5 Levels or Beamforming-5 Levels), the following conditions must be satisfied all the time:

$$V_{PPA} \geq V_{PPB} \text{ and } V_{NNA} \leq V_{NNB}$$

Violating these condition could result in damages of the device.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX14813EWX+T	0°C to +85°C	156pins - W1566A6+1

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.