MAX14821

IO-Link Device Transceiver

General Description

The MAX14821 transceiver is suitable for IO-Link® devices and 24V binary sensors/actuators. All specified IO-Link data rates are supported. In IO-Link applications, the transceiver acts as the physical layer interface to a microcontroller running the data-link layer protocol. Additional 24V digital inputs and outputs are provided. Two internal linear regulators generate common sensor and actuator power requirements: 5V and 3.3V.

On-board C/Q and DO drivers are independently configurable for push-pull, high-side (PNP), or low-side (NPN) operation. The device detects the IO-Link C/Q wake-up condition and generates a wake-up signal on the active-low $\overline{WU}$ output. The C/Q and DI inputs have selectable current loads for use in actuators.

An SPI™ interface allows configuration and monitoring of the device. Extensive alarm conditions are detected and communicated through the $\overline{IRQ}$ output and the SPI interface. The device features reverse-polarity, short-circuit, and thermal protection. All power lines are monitored for undervoltage conditions.

The C/Q and DO drivers are specified for sourcing/sinking up to 100mA.

The device is available in a 2.5mm x 2.5mm, 25-pin wafer-level package (WLP) and a 4mm x 4mm, 24-pin TQFN package. Both are specified over the extended -40°C to +85°C temperature range.

Applications

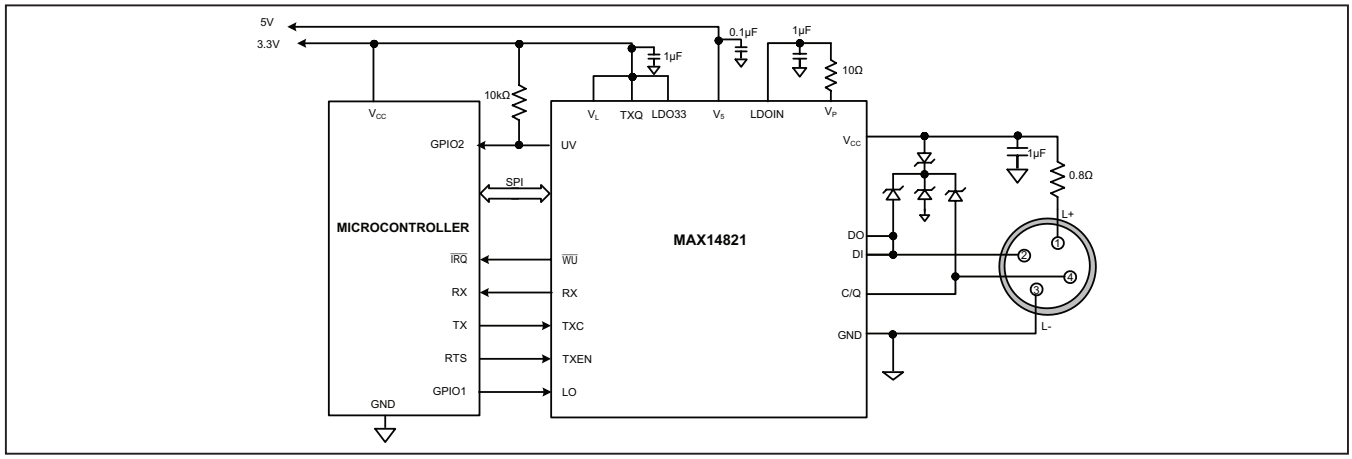
- IO-Link Sensors Industrial Sensors and Actuators
- IO-Link Actuators

Benefits and Features

- Standards Compliance Ensures Future-Proof Solutions
  - IO-Link Versions 1.0 and 1.1.2
  - IEC IEC61131.9 SDCI
- High Configurability and Integration Reduces SKUs
  - Push-Pull, PNP, or NPN Driver Configuration
  - Supports COM1, COM2, and COM3 Data Rates
  - SPI Interface for Control and Monitoring
  - 2.5V to 5V Logic Interface Levels
  - Auxiliary 24V, 100mA Digital Output (DO)
  - Auxiliary 24V Digital Input (DI)
  - 100mA Specified C/Q output Drive
  - Integrated 5V and 3.3V Regulators
- Integrated Protection Enables Robust Solutions
  - Extensive Fault-Monitoring and Reporting
  - Reverse-Polarity and Short-Circuit Protection on All 24V Outputs/Inputs
  - Reverse-Polarity Protected 24V Supply Output -40°C to +105°C Operating Temperature Range
- Small Package Supports Sensor Miniaturization
  - 2.5mm x 2.5mm WLP and 4mm x 4mm TQFN Package

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



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SPI is a trademark of Motorola, Inc.

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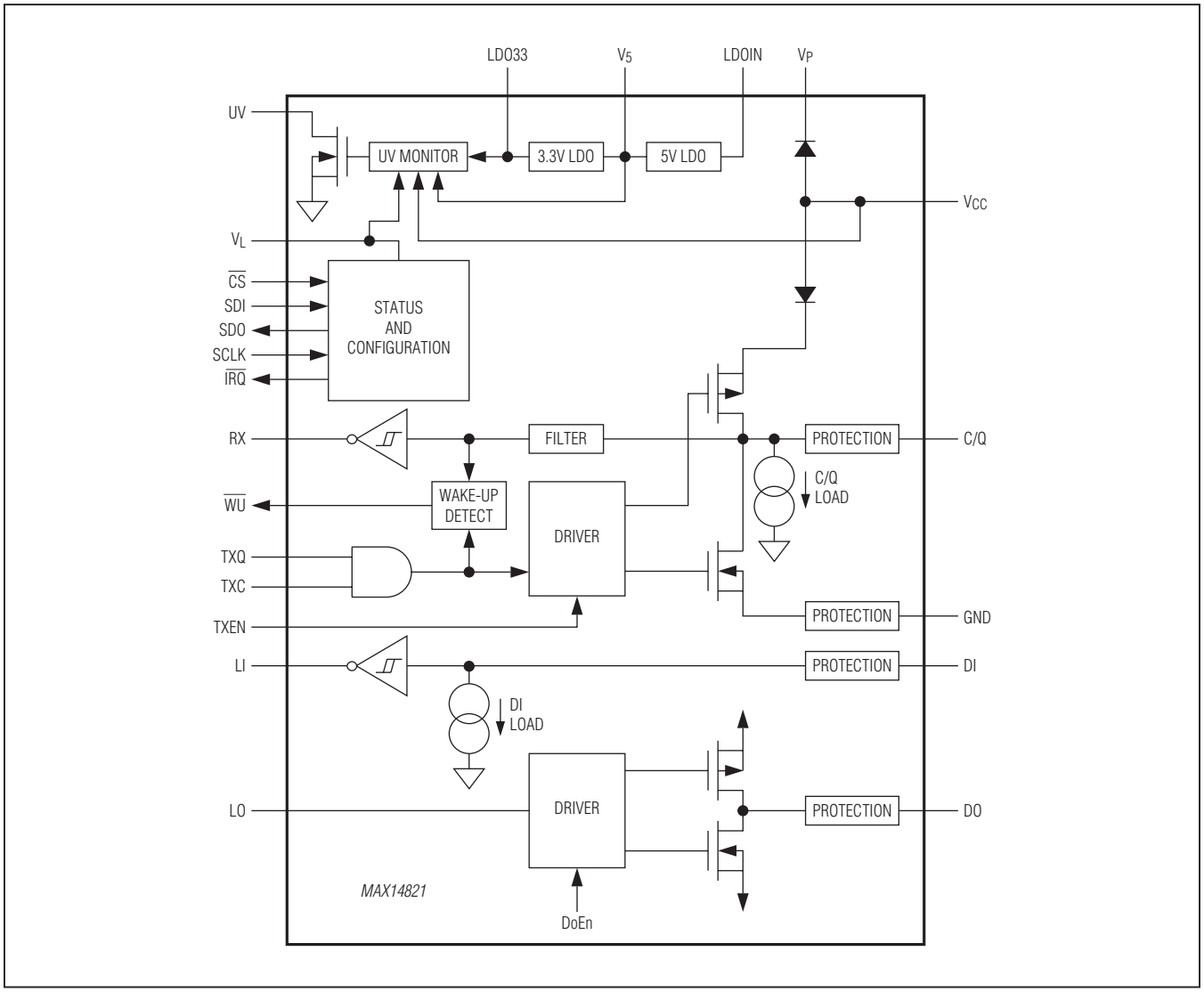
Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} ..... -40V to +40V
V_P (I_{VP} < 50mA) ..... the higher of -0.3V and (V_{CC} - 1V) to +40V
LDOIN ..... -0.3V to +40V
V_5 ..... -0.3V to the lesser of (V_{LDOIN} + 0.3V) and +6V
LDO33 ..... -0.3V to the lesser of (V_5 + 0.3V) and +6V
V_L ..... -0.3V to +6V
DI ..... -40V to +40V
C/Q, DO ..... MIN: the higher of -40V and (V_{CC} - 40V)
MAX: the lesser of +40V and (V_{CC} + 40V)
Logic Inputs
TXC, TXQ, TXEN, LO, $\overline{CS}$, SDI, SCLK ... -0.3V to (V_L + 0.3V)
Logic Outputs
RX, $\overline{WU}$, LI, SDO, $\overline{IRQ}$ ..... -0.3V to (V_L + 0.3V)
UV ..... -0.3V to +6V
Continuous Current Into Any Logic Pin Q50mA
Continuous Power Dissipation
TQFN (derate 27.8mW/°C above +70°C) 2222mW
WLP (derate 22.7mW/°C above +70°C) 1816mW
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (TQFN only; soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 24 TQFN	
Package Code	T2444+4
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

PACKAGE TYPE: 25 WLP	
Package Code	W252A2+1
Outline Number	**21-0191**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	44°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	For driver operation	9		36	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 24V, C/Q as input, no load on V5 or LDO33, LDOIN not connected to VP, V_{LDOIN} = 24V		1	2.5	mA
V_{CC} Undervoltage-Lockout Threshold	V_{CCUVLO}	V_{CC} falling	6	7.4	9	V
V_{CC} Undervoltage-Lockout Threshold Hysteresis	V_{CCUVLO_HYST}			200		mV
V_5 Supply Current	I_{5_IN}	LDOIN shorted to V_5, external 5V applied to V_5, no switching, LDO33 disabled		3		mA
V_5 Undervoltage-Lockout Threshold	V_{5UVLO}	V_5 falling		2.0		V
V_L Logic-Level Supply Voltage	V_L		2.3		5.5	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND			5	µA
V_L Undervoltage Threshold	V_{LUVLO}	V_L falling	0.65	0.95	1.30	V
5V LDO (V_5)						
LDOIN Input Voltage Range	V_{LDOIN}		7		36	V
LDOIN Supply Current	I_{LDOIN}	V_{LDOIN} = 24V, C/Q is configured as an input, no load on V_5 or LDO33		2.5	5	mA
V_5 Output Voltage Range	V_5	No load on V_5, 7V ≤ V_{LDOIN} ≤ 36V	4.75	5.00	5.25	V
V_5 Load Regulation		1mA < I_{LOAD} < 10mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5		0.8		%
		1mA < I_{LOAD} < 30mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5, 10Ω–1µF compensation network added to V_5		0.8		
3.3V LDO (LDO33)						
LDO33 Output Voltage	V_{LDO33}	No load on LDO33	3.1	3.3	3.5	V
LDO33 Undervoltage-Lockout Threshold	$V_{LDO33UVLO}$	V_{LDO33} falling		2.4		V
LDO33 Load Regulation		1mA < I_{LOAD} < 20mA, V_{LDOIN} = 7V		0.25		%
24V INTERFACE						
C/Q Driver Output-Voltage High	$V_{OH\_C/Q}$	C/Q high-side enabled, $I_{C/Q}$ = -100mA, 9V ≤ V_{CC} ≤ 36V	V_{CC} - 3	V_{CC} – 1.3		V
C/Q Driver Output-Voltage Low	$V_{OL\_C/Q}$	C/Q low-side enabled, $I_{C/Q}$ = +100mA, 9V ≤ V_{CC} ≤ 36V		1.4	3	V
C/Q Driver Source Current Limit	$I_{OH\_C/Q}$	C/Q high-side enabled, $V_{C/Q}$ < (V_{CC} - 3V), 9V ≤ V_{CC} ≤ 36V	+100	+140	+190	mA
C/Q Driver Sink Current Limit	$I_{OL\_C/Q}$	C/Q low-side enabled, $V_{C/Q}$ > 3V, 9V ≤ V_{CC} ≤ 36V	-190	-140	-100	mA

DC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DO Driver Output-Voltage High	V_{OH_DO}	DO high-side enabled, I_{DO} = +100mA, 9V ≤ V_{CC} ≤ 36V		V_{CC} - 3	V_{CC} - 1.6		V
DO Driver Output-Voltage Low	V_{OL_DO}	DO low-side enabled, I_{DO} = -100mA, 9V ≤ V_{CC} P 36V			1.6	3	V
DO Driver Source Current Limit	I_{OH_DO}	DO high-side enabled, V_{DO} < (V_{CC} - 3V)		+100	+135	+190	mA
DO Driver Sink Current Limit	I_{OL_DO}	DO high-side enabled, V_{DO} > 3V		-190	-135	-100	mA
C/Q, DI Input Voltage Range	V_{IN}	For valid RX, LI		-1.0		V_{CC} + 1.0	V
C/Q Input Threshold High	$V_{IH\_C/Q}$	C/Q driver disabled		10.5		13.0	V
C/Q Input Threshold Low	$V_{IL\_C/Q}$	C/Q driver disabled		8.0		11.5	V
C/Q Input Hysteresis	$V_{HYS\_C/Q}$	C/Q driver disabled		1.0			V
DI Input Threshold High	V_{IH_DI}			6.8		8	V
DI Input Threshold Low	V_{IL_DI}			5.2		6.4	V
DI Input Hysteresis	V_{HYS_DI}			1			V
C/Q Weak Pulldown Current	$I_{PDC/Q}$	C/Q driver disabled, $V_{C/Q}$ = (V_{CC} - 1V)		100		400	µA
DO Weak Pulldown Current	I_{PDDO}	DO driver disabled, V_{CC} = 36V, V_{DO} = (V_{CC} - 1V)		40		120	µA
DI Weak Pulldown Current	I_{PDDI}	DI load disabled, VCC = 36V, V_{DI} = (V_{CC} - 1V)		50		300	µA
C/Q Input Capacitance	$C_{C/Q}$	C/Q driver disabled			40		pF
DO Input Capacitance	C_{DO}	DO driver disabled			40		pF
DI Input Capacitance	C_{DI}				20		pF
C/Q, DI CURRENT SINK							
C/Q Load Current	$I_{LLM\_C/Q}$	C/Q load enabled (C/QLoad = 1)	0V ≤ $V_{C/Q}$ ≤ 5V	0		9	mA
			5V ≤ $V_{C/Q}$	5	6.6	9	
DI Load Current	I_{LLM_DI}	DI load enabled (DiLoad = 1)	0V ≤ V_{DI} ≤ 5V	0		9	mA
			9V ≤ V_{DI}	6	7.5	9	
LOGIC INPUTS (TXC, TXQ, TXEN, LO, $\overline{CS}$, SDI, SCLK)							
Logic-Input Voltage Low	V_{IL}			0.3 x V_L			V
Logic -Input Voltage High	V_{IH}					0.7 x V_L	V
Logic-Input Leakage Current	I_{LEAK}	Logic input = GND or V_L		-1		+1	µA
Logic-Input Capacitance	C_{IN}				5		pF

DC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS (RX, $\overline{WU}$, LI, UV, SDO, $\overline{IRQ}$)						
Logic-Output Voltage Low	VOL	I_{OUT} = -5mA			0.4	V
Logic-Output Voltage High	V_{OHRX}, V_{OHWU}, V_{OHLI}, V_{OHSDO}, V_{OHIRQ}	I_{OUT} = 5mA (Note 2)	V_L - 0.6			V
SDO Leakage Current	I_{LK_SDO}	SDO disabled, SDO = GND or V_L	-1		+1	µA
THERMAL SHUTDOWN						
Thermal-Warning Threshold		Die temperature rising, OTemp bit is set		+115		°C
Thermal-Warning Threshold Hysteresis		Die temperature falling, OTemp bit is cleared		20		°C
Thermal-Shutdown Threshold		Die temperature rising		+150		°C
Thermal-Shutdown Hysteresis				20		°C

AC Electrical Characteristics

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q, DO, DI INTERFACES							
Data Rate	DR	HiSlew = 1		4.8		230.4	kbps
		HiSlew = 0		4.8		38.4	
DRIVER (C/Q, DO)							
Driver Low-to-High Propagation Delay	t_{PDLH}	Push-pull or high-side (PNP) configuration, Figure 1	HiSlew = 1		0.5	2	µs
			HiSlew = 0		1.6	5	
Driver High-to-Low Propagation Delay	t_{PDHL}	Push-pull or low-side (NPN) configuration, Figure 1	HiSlew = 1		0.5	2	µs
			HiSlew = 0		1.6	5	
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$			0.1	2	µs
Driver Rise Time	t_{RISE}	Push-pull or high-side (PNP) configuration, Figure 1	HiSlew = 1		0.4	1.7	µs
			HiSlew = 0		1.5	4	
Driver Fall Time	t_{FALL}	Push-pull or low-side (NPN) configuration, Figure 1	HiSlew = 1		0.4	1.7	µs
			HiSlew = 0		1.4	4	
Driver Enable Time High	t_{ENH}	Push-pull or high-side (PNP) configuration, Figure 3	HiSlew = 1		0.3	1	µs
			HiSlew = 0		0.8	7	
Driver Enable Time Low	t_{ENL}	Push-pull or low-side (NPN) configuration, Figure 2	HiSlew = 1		0.3	1	µs
			HiSlew = 0		0.9	7	

AC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Disable Time High	t_{DISH}	Push-pull or high-side (PNP) configuration, Figure 2 (Note 3)	HiSlew = 1		1.6	3	µs
			HiSlew = 0		1.6	3	
Driver Disable Time Low	t_{DISL}	Push-pull or low-side (NPN) configuration, Figure 3 (Note 3)	HiSlew = 1		0.1	3	µs
			HiSlew = 0		0.1	3	
RECEIVER (C/Q, DI) (Figure 4)							
Receiver Low-to-High Propagation Delay	t_{PRLH}	RxFilter = 1			0.2	2	µs
		RxFilter = 0			0.4	2	
Receiver High-to-Low Propagation Delay	t_{PRHL}	RxFilter = 1			0.3	2	µs
		RxFilter = 0			0.5	2	
WAKE-UP DETECTION (Figure 5)							
Wake-Up Input Minimum Pulse Width	t_{WUMIN}			30	40	50	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}			120	140	160	µs
WU Output Low Time	t_{WUL}	Valid wake-up condition on C/Q		120	190	260	µs
SPI TIMING ($\overline{CS}$, SCLK, SDI, SDO) (Figure 6)							
SCLK Clock Period	t_{CH+CL}			83.3			ns
SCLK Pulse-Width High	t_{CH}			41.65			ns
SCLK Pulse-Width Low	t_{CL}			41.65			ns
CS Fall to SCLK Rise Time	t_{CSS}			20			ns
SCLK Rise to CS Rise Hold Time	t_{CSH}			20			ns
SDI Hold Time	t_{DH}			10			ns
SDI Setup Time	t_{DS}			10			ns
Output Data Propagation Delay	t_{DO}					36	ns
SDO Rise and Fall Times	t_{FT}					20	ns
Minimum CS Pulse	t_{CSW}			76.8			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: UV is an open-drain output. Connect UV to a voltage less than 5.5V through an external pullup resistor.

Note 3: Disable time measurements are load dependent.

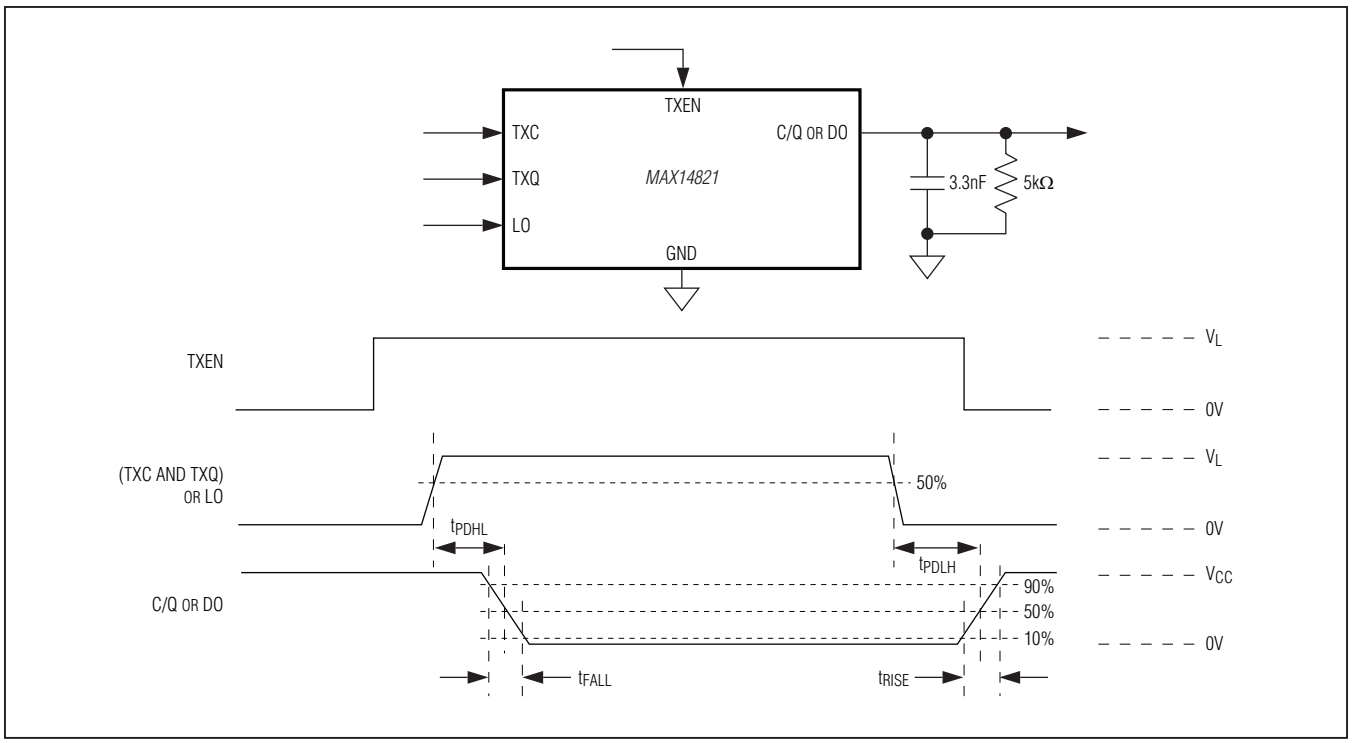


Figure 1. C/Q and LO Driver Propagation Delays and Rise/Fall Times

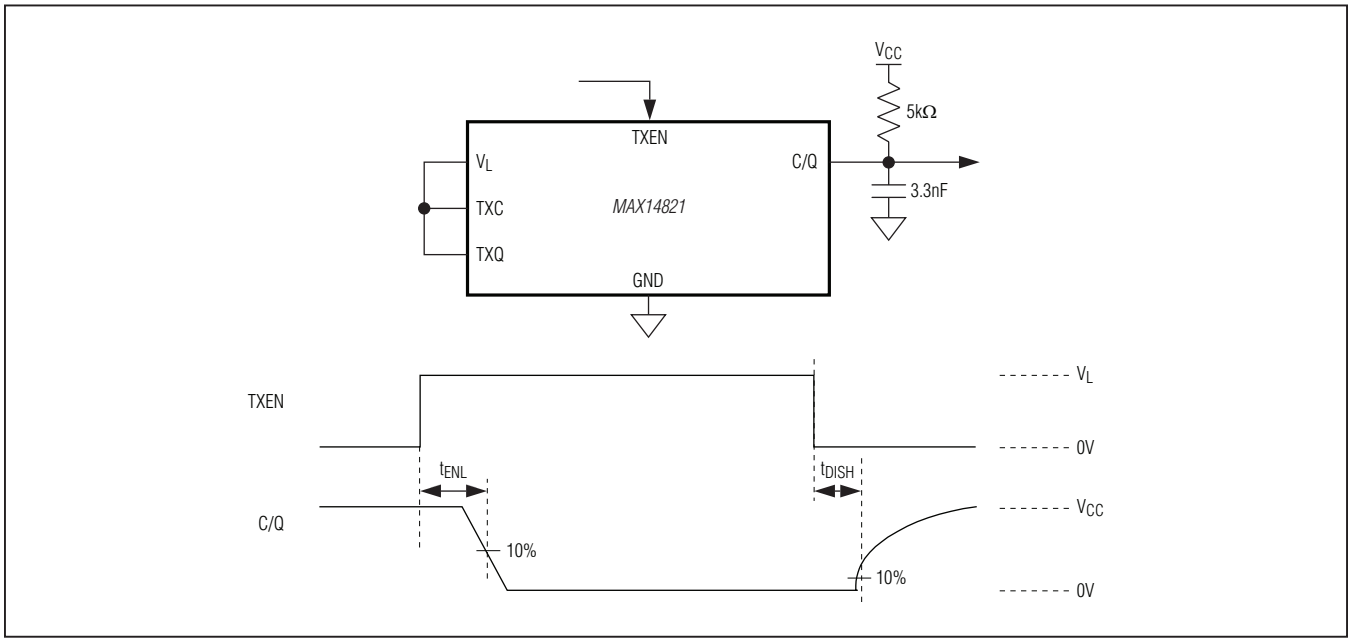


Figure 2. C/Q Driver Enable Low and Disable High Timing with External Pullup Resistor

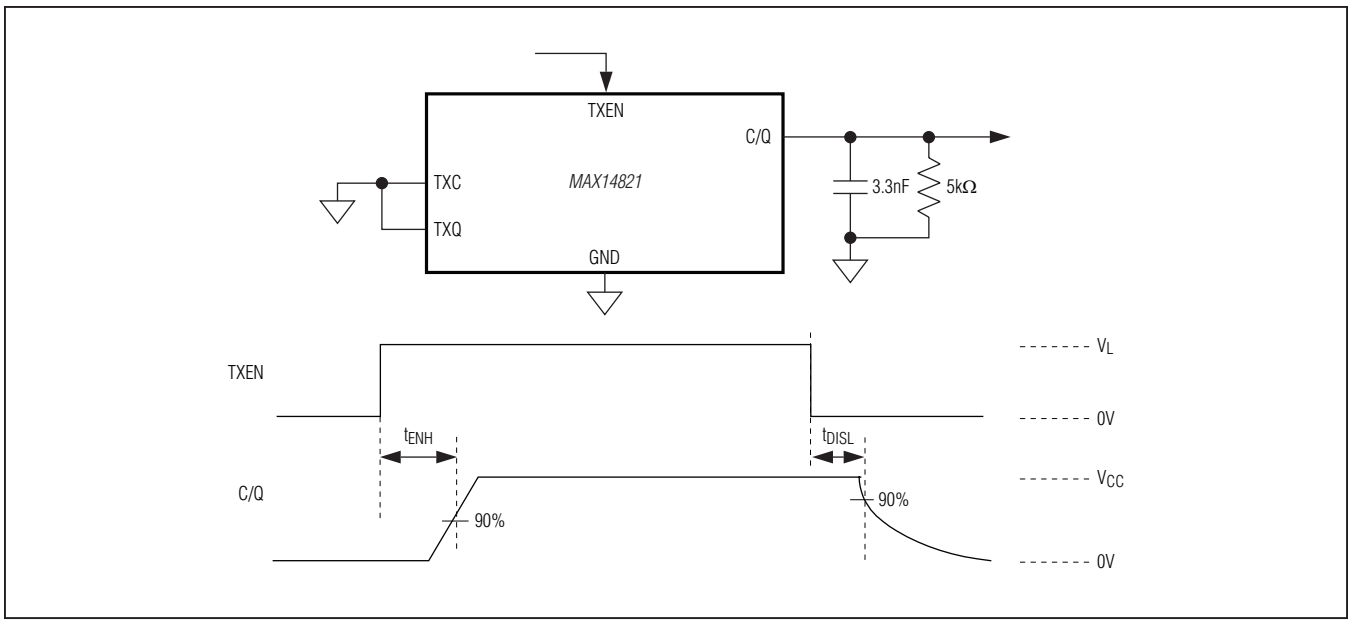


Figure 3. C/Q Driver Enable High and Disable Low Timing

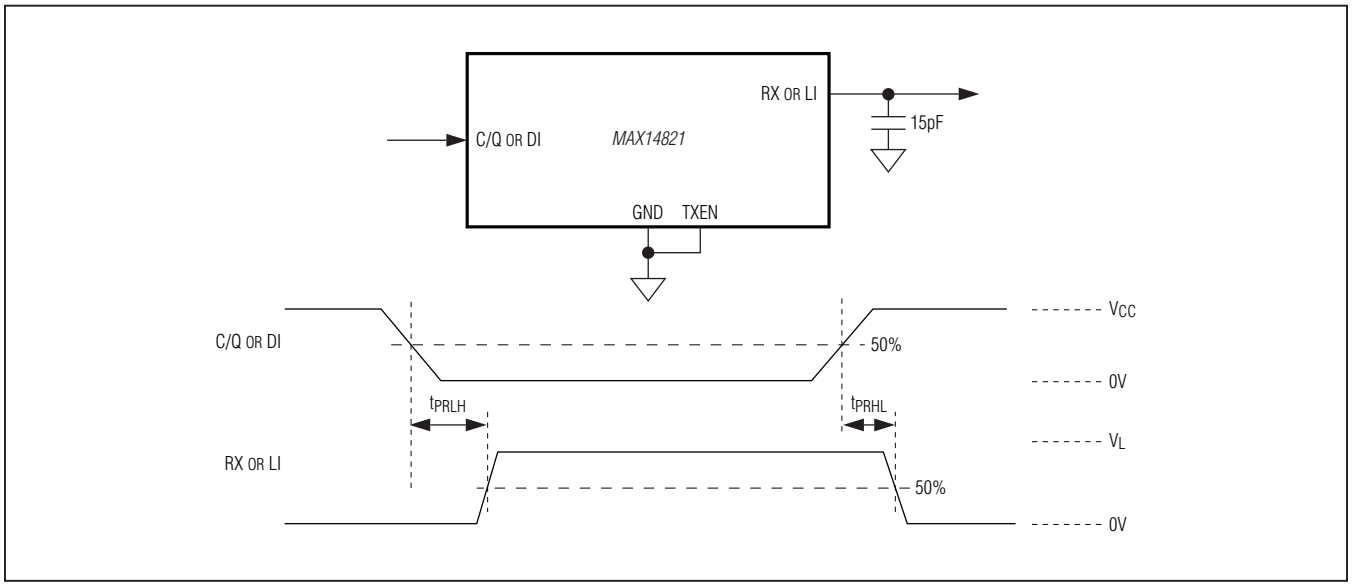
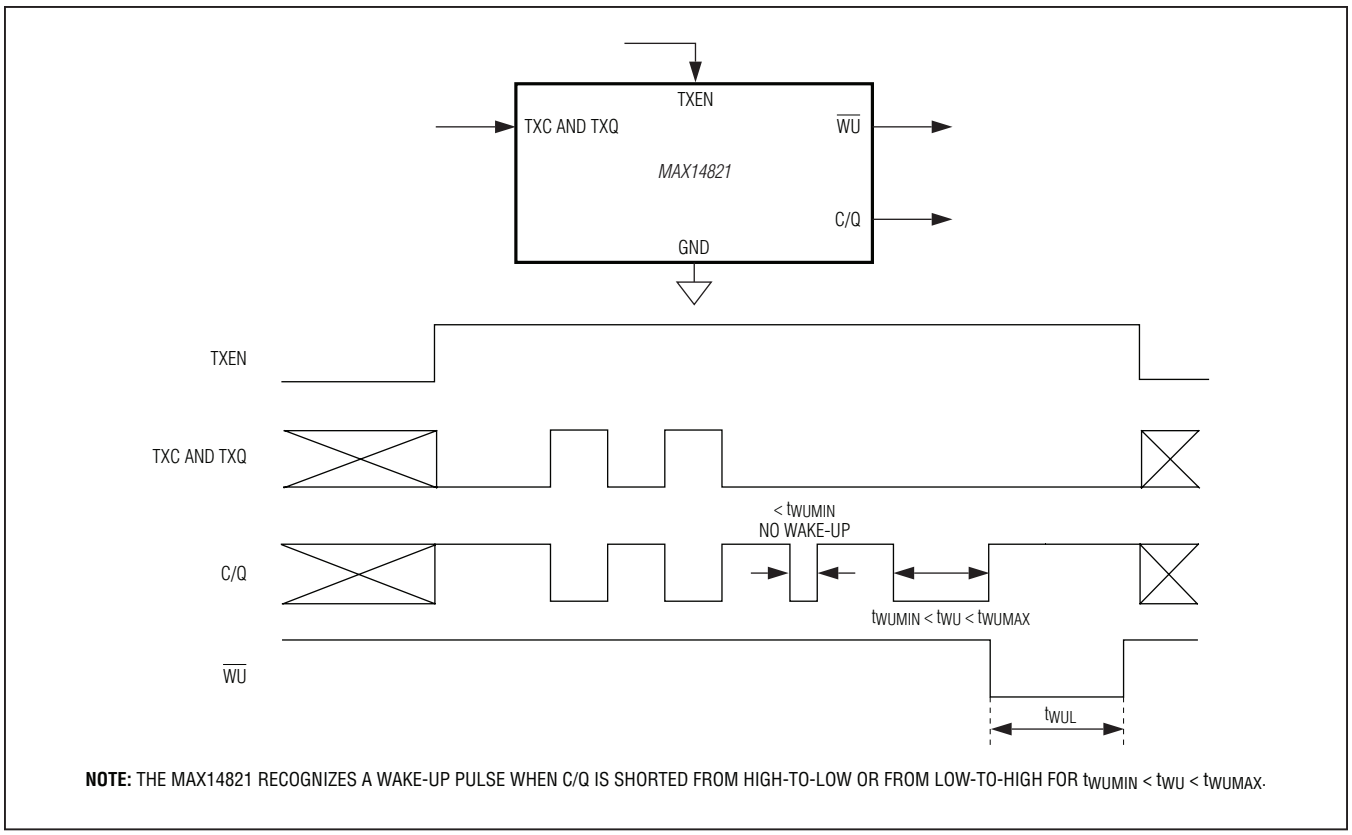


Figure 4. C/Q and DI Receiver Propagation Delays



NOTE: THE MAX14821 RECOGNIZES A WAKE-UP PULSE WHEN C/Q IS SHORTED FROM HIGH-TO-LOW OR FROM LOW-TO-HIGH FOR $t_{WUMIN} < t_{WU} < t_{WUMAX}$.

Figure 5. Wake-Up Detection Timing

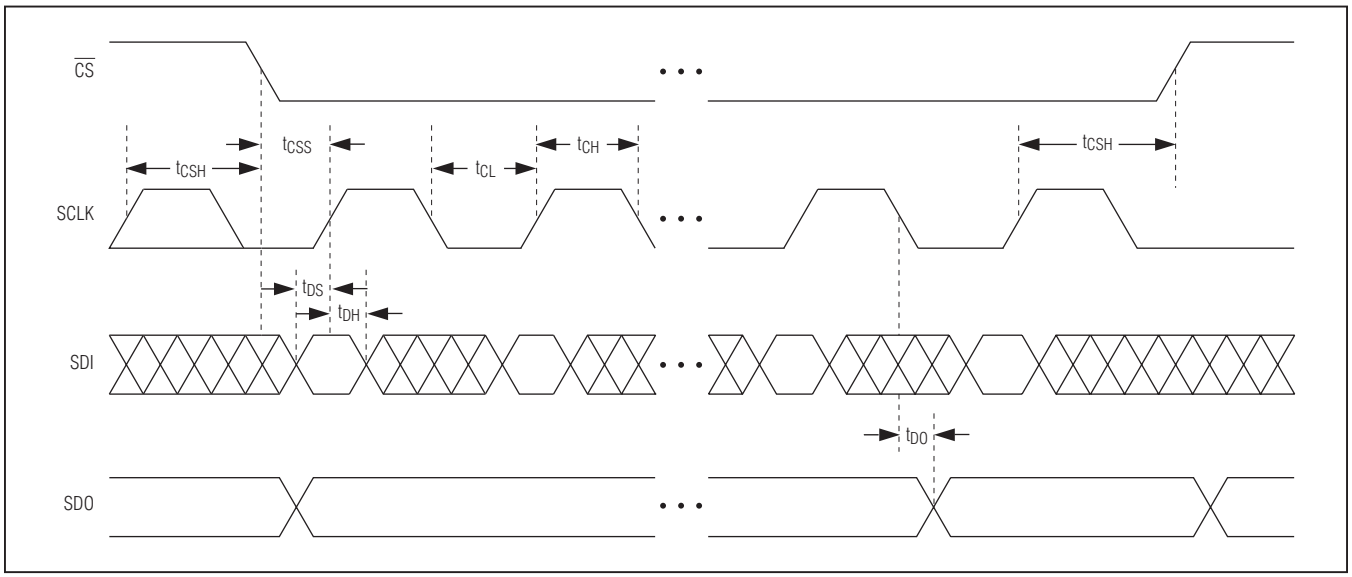
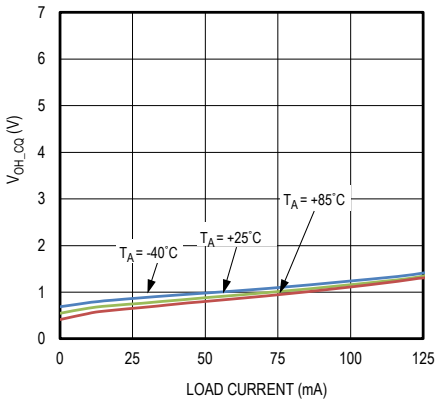


Figure 6. SPI Timing Diagram

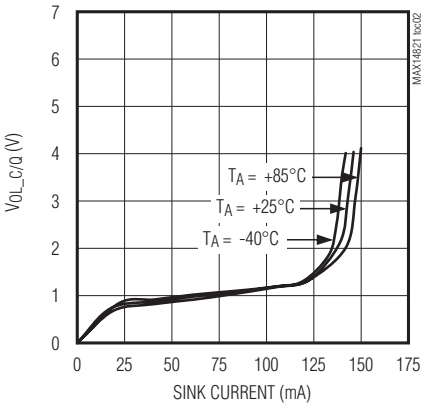
Typical Operating Characteristics

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

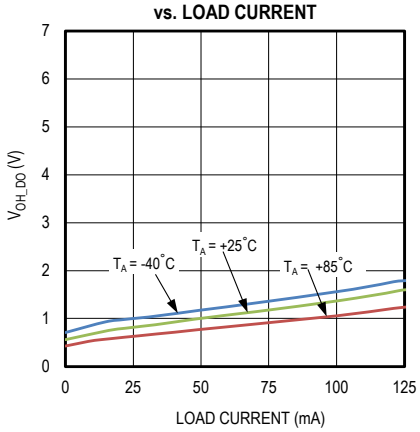
C/Q DRIVER OUTPUT HIGH vs. LOAD CURRENT



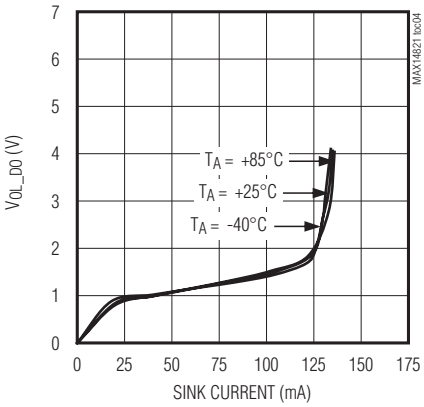
C/Q DRIVER OUTPUT LOW vs. SINK CURRENT



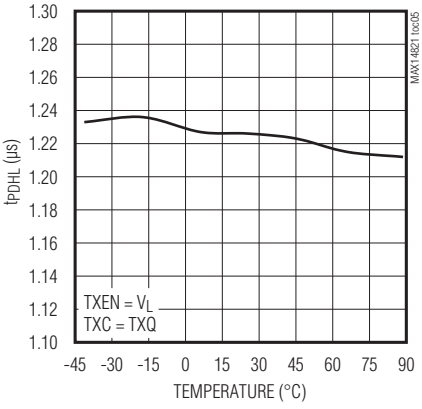
DO DRIVER OUTPUT HIGH vs. LOAD CURRENT



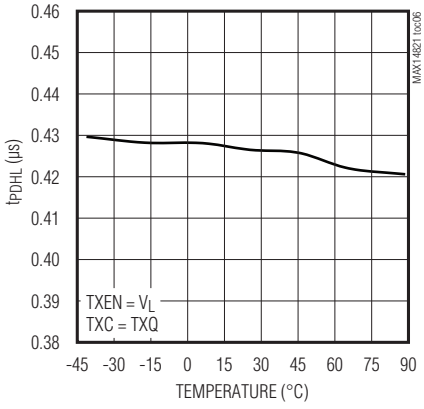
DO DRIVER OUTPUT LOW vs. SINK CURRENT



C/Q DRIVER PROPAGATION DELAY vs. TEMPERATURE (HiSlew = 0)



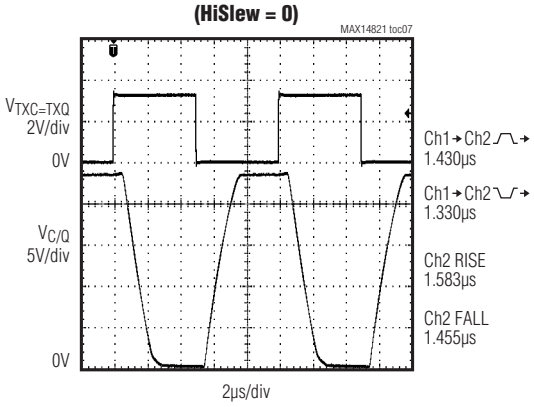
C/Q DRIVER PROPAGATION DELAY vs. TEMPERATURE (HiSlew = 1)



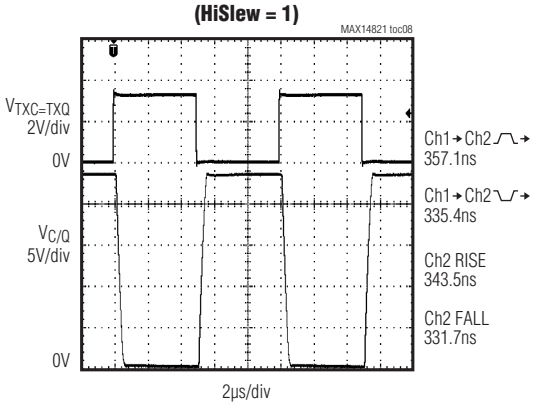
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

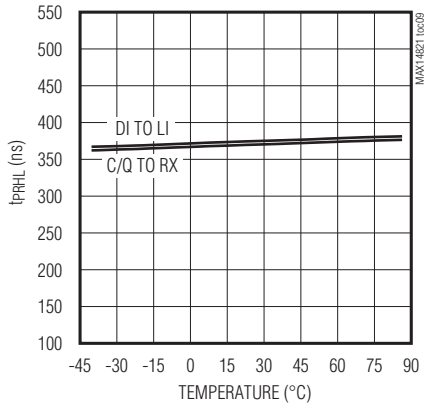
C/Q DRIVER OUTPUT SWITCHING (HiSlew = 0)



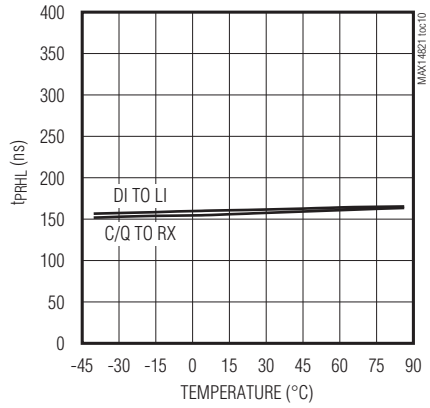
C/Q DRIVER OUTPUT SWITCHING (HiSlew = 1)



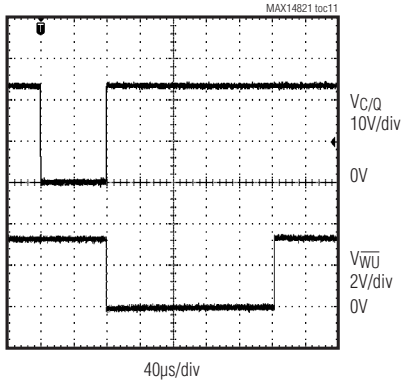
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (RxFilter = 0)



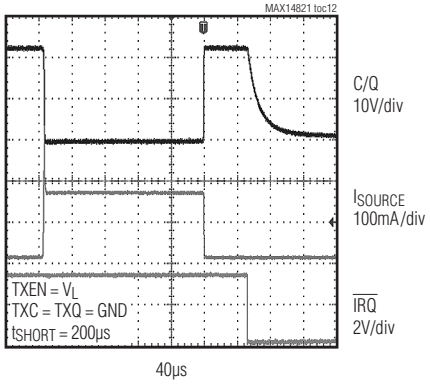
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (RxFilter = 1)



WAKE-UP DETECTION



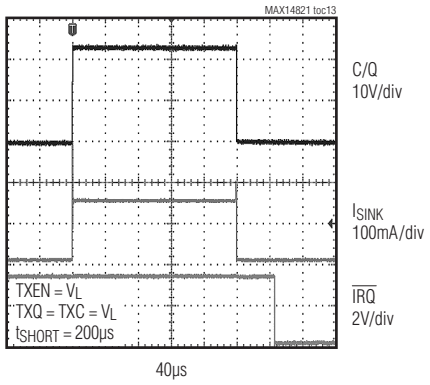
C/Q SHORT-CIRCUIT PROTECTION



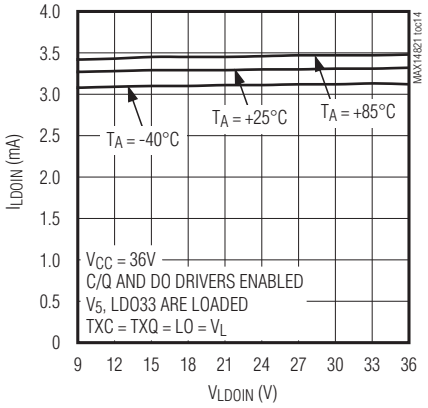
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

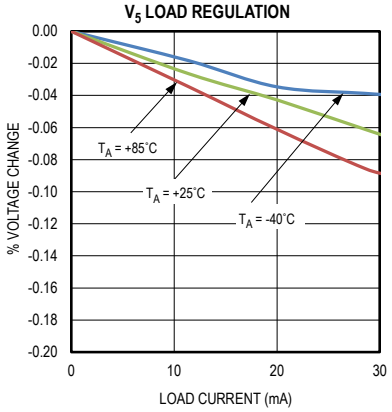
C/Q SHORT-CIRCUIT PROTECTION



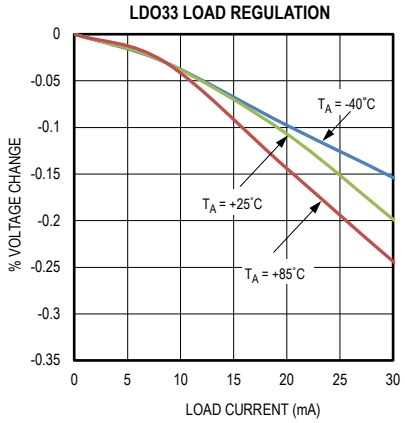
LDOIN SUPPLY CURRENT vs. LDOIN VOLTAGE



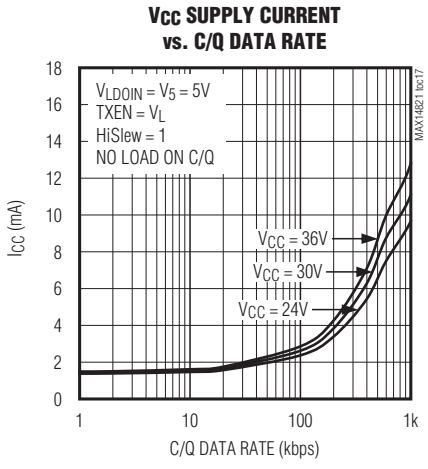
V_5 LOAD REGULATION



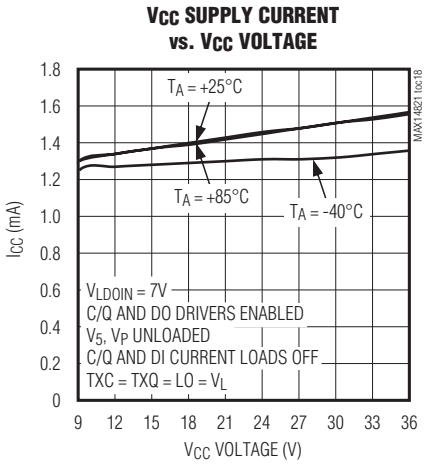
LDO33 LOAD REGULATION



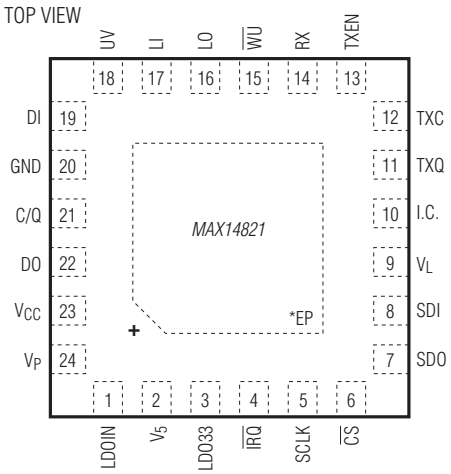
V_{CC} SUPPLY CURRENT vs. C/Q DATA RATE



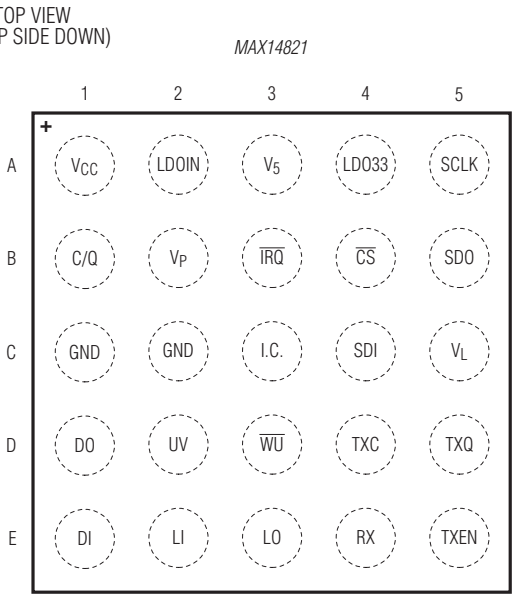
V_{CC} SUPPLY CURRENT vs. V_{CC} VOLTAGE



Pin/Bump Configurations



TQFN



WLP

*CONNECT EXPOSED PAD TO GND.

Pin/Bump Descriptions

PIN		NAME	FUNCTION
TQFN-EP	WLP		
1	A2	LDOIN	5V Linear Regulator Input. Bypass LDOIN to GND with a 1µF ceramic capacitor.
2	A3	V_5	5V Power-Supply Input and 5V Linear Regulator Output. Bypass V_5 to GND with a 0.1µF ceramic capacitor for 10mA load capability. Add the recommended compensation network to increase the source capability to 30mA. See the 5V and 3.3V Linear Regulators section for more information.
3	A4	LDO33	3.3V Linear Regulator Output. Bypass LDO33 to GND with a 1µF ceramic capacitor.
4	B3	IRQ	Active-Low Interrupt Request Output. $\overline{IRQ}$ is a push-pull output referenced to V_L.
5	A5	SCLK	SPI Clock Input
6	B4	$\overline{CS}$	Active-Low SPI Chip-Select Input
7	B5	SDO	SPI Serial-Data Output
8	C4	SDI	SPI Serial-Data Input
9	C5	V_L	Logic-Level Supply Input. V_L defines the logic levels on all the logic inputs and outputs. Bypass V_L to GND with a 0.1µF ceramic capacitor.
10	C3	I.C.	Internally Connected. Connect to V_L or leave unconnected.

Pin/Bump Descriptions (continued)

PIN		NAME	FUNCTION
TQFN-EP	WLP		
11	D5	TXQ	Transmit Level Input. The logic on the C/Q output is the inverse logic level of the signals on the TXC and TXQ inputs. TXQ is ANDed with TXC. Drive TXQ high if not in use.
12	D4	TXC	Transmit Communication Input. The logic on the C/Q output is the inverse logic level of the signals on the TXC and TXQ inputs. TXC is ANDed with TXQ. Drive TXC high if not in use.
13	E5	TXEN	Transmitter Enable. Drive TXEN high to enable the C/Q transmitter. TXEN is referenced to VL.
14	E4	RX	Receiver Output. RX is the inverse logic level of C/Q. RX is always high when the RxDis bit in the CQConfig register is set to 1.
15	D3	$\overline{WU}$	Active-Low Wake-Up Output. $\overline{WU}$ is a push-pull output referenced to V_L. $\overline{WU}$ pulses low for 190µs (typ) when a valid wake-up pulse is detected on the C/Q line.
16	E3	LO	Logic Input of the DO Output. LO is the logic input that drives DO. LO is referenced to V_L.
17	E2	LI	Logic Output of the 24V DI Logic Input. LI is the inverse logic of DI. LI is referenced to V_L.
18	D2	UV	Open-Drain Undervoltage Indicator Output. In case of an undervoltage, the UV open-drain transistor is off.
19	E1	DI	24V Logic-Level Digital Input
20	C1, C2	GND	Ground
21	B1	C/Q	SIO/IO-Link Data Input/Output. Drive TXEN high to enable the C/Q driver. The logic on the C/Q output is the inverse logic level of the signals on the TXC and TXQ inputs. RX is the logic inverse of C/Q. The C/Q driver output level can be set by the TXC/TXQ inputs or programmed by the Q bit. The level on C/Q can be read by the RX ouput or the $\overline{Q}$Lvl bit.
22	D1	DO	24V Logic-Level Digital Output. DO is the inverse logic level of the LO input and can be digitally controlled through the DIOConfig register.
23	A1	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
24	B2	V_P	Protected 24V Supply Output. V_P is one diode drop below V_{CC}. V_P is reverse-polarity protected and can be used as a 24V protected supply to the sensor or actuator electronics.
—	—	EP	Exposed Pad (TQFN Only). Connect EP to GND.

Detailed Description

The MAX14821 is a sensor/actuator transceiver designed for IO-Link device applications supporting all the specified IO-Link data rates. In IO-Link applications, the device acts as the physical layer interface to a microcontroller running the data-link layer protocol. The device contains an additional 24V digital input and an additional 24V digital output. Two internal linear regulators generate common sensor and actuator power requirements: 5V and 3.3V.

The device detects IO-Link wake-up conditions on the C/Q line and generates a wake-up signal on the $\overline{WU}$ output. The C/Q and DO drivers are independently configurable to any one of three driver output types: push-pull, high-side (PNP), or low-side (NPN).

The C/Q and DI inputs have selectable current sinks that can be enabled for use in actuators where the master requires a Type 2 load. The device is configured and monitored through an SPI interface. Extensive alarms are available through SPI.

24V Interface

The device features an IO-transceiver interface capable of operating with voltages up to 36V. This is the 24V interface and includes the C/Q input/output, the logic-level digital output (DO), and the logic-level digital input (DI).

Configurable Drivers

The device features selectable push-pull, high-side (PNP), or low-side (NPN) switching drivers at C/Q and DO.

Set the C/Q_N/P and C/Q_PP bits in the CQConfig register to select the driver mode for the C/Q driver. When configured as a push-pull output, C/Q switches between V_P and ground. Set the C/Q_PP bit to 1 to select push-pull operation at C/Q. Set the C/Q_PP bit to 0 to configure the C/Q output for open-drain operation. The C/Q_N/P bit selects NPN or PNP operation when C/Q is configured as an open-drain output.

Set the DoN/P and DoPP bits in the DIOConfig register to select the driver mode for the DO output. When configured as a push-pull output, DO switches between V_{CC} and ground. Set the DoPP bit to 1 for push-pull operation. The DoN/P bit selects NPN or PNP operation when DO is configured as an open-drain output. Set the DoPP bit to 0 to select high-side or low-side operation at DO.

C/Q Driver and Receiver

The TXEN input enables the C/Q driver. Drive TXEN high to enable the C/Q driver. Drive TXEN low to disable the driver.

The C/Q driver is specified to supply up to 100mA DC load current.

The HiSlew bit increases the slew rate of the C/Q and DO driver outputs. Set HiSlew to 1 for data rates of 230kbps or higher. Set HiSlew to 0 to reduce both the C/Q and DO driver slew rates to reduce EMI emission and reflections.

The C/Q receiver is always on. Disable the RX output through the RxDis bit in the CQConfig register. Set the RxDis bit to 1 to set the RX output high. Set the RxDis bit to 0 for normal receive operation.

The C/Q receiver has an analog lowpass filter to reduce high-frequency noise present on the line. Set the RxFilter bit in the CQConfig register to 0 to set the filter corner frequency to 500kHz (typ). Set the RxFilter bit to 1 to set the corner frequency of the filter to 1MHz (typ). Noise filters are present on both the C/Q and DI receivers and are controlled simultaneously by the RxFilter bit.

C/Q Fault Detection

The device registers a C/Q fault condition under either of two conditions:

1) When it detects a short circuit for longer than 140µs (typ). A short condition exists when the C/Q driver's load current exceeds the 140mA (typ) current limit.
2) When it detects a voltage level error at the C/Q output. A voltage level error occurs when the C/Q driver is configured for open-drain operation (NPN or PNP), the driver is turned off, and the C/Q voltage is not pulled to exceed the C/Q receiver's threshold levels (< 8V or > 13V) by the external supply.

When a C/QFault error occurs, the C/QFault and C/QFaultInt bits are set, $\overline{IRQ}$ asserts, and the driver is turned off 240µs (typ) after the start of the fault condition.

When a short-circuit event occurs on C/Q, the driver enters autoretry mode. In autoretry mode the device periodically checks whether the short is still present and attempts to correct the driver output. Autoretry attempts last for 240µs (typ) and occur every 26ms (typ).

DO Fault Detection

The device registers a DoFault event when a short circuit is present at the DO output for 440µs. A short condition exists when the load current on the DO driver exceeds the 135mA (typ) DO current limit. When a short-circuit condition is detected, the DO driver enters autoretry mode. In autoretry mode the device periodically checks whether the error is still present. Autoretry attempts last for 440µs (typ) and occur every 26ms (typ). When a DoFault error is detected, the DoFault and DoFaultInt bits are set, $\overline{IRQ}$ asserts, and the driver is turned off 440µs (typ) after the start of the DO faults.

Reverse-Polarity Protection

The device is protected against reverse-polarity connections on V_{CC}, C/Q, DO, DI, and GND. Any combination of these pins can be connected to DC voltages up to 40V (max). A short to 40V results in a current flow of less than 500µA.

Ensure that the maximum voltage between any of these pins does not exceed 40V.

5V and 3.3V Linear Regulators

The device includes two internal regulators to generate 5V (V_5) and 3.3V (LDO33). LDO5 is specified for 10mA total external load current (i.e., LDO33 + V_5) when bypassed with a 0.1µF capacitor to ground. Add the compensation network shown in Figure 7 to draw up to 30mA of total external load current from the 5V LDO. LDO33 is specified at 20mA. The input of V_5, LDOIN, can be powered from V_P, the protected 24V supply output, or to another voltage in the 7V to 36V range.

If the external circuits that are powered by the linear regulators require an input bypass capacitance larger than 100nF for 5V or 1µF for 3.3V, a compensation network must be added on V5 and/or LDO33. The compensation network consists of a 10Ω series resistor and a capacitor equal to the value required by the external circuit, as shown in Figure 8. The capacitors C33* and C5* in Figure 8 represent the capacitance required by the external circuits. Figure 8 does not show any protection diodes for simplicity.

When the internal 5V LDO is not used, V_5 becomes the supply input for the internal analog and digital functions and thus has to be supplied externally so that the MAX14820 operates normally. The 5V LDO can be disabled by connecting LDOIN to V_5. Apply an external voltage of 4.75V to 5.25V to V_5 when the LDO is disabled.

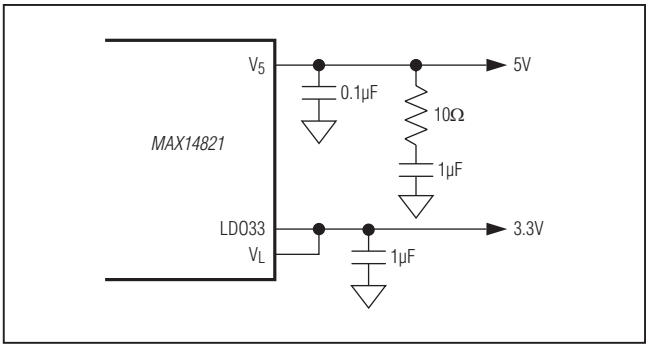


Figure 7. V_5 Compensation Network

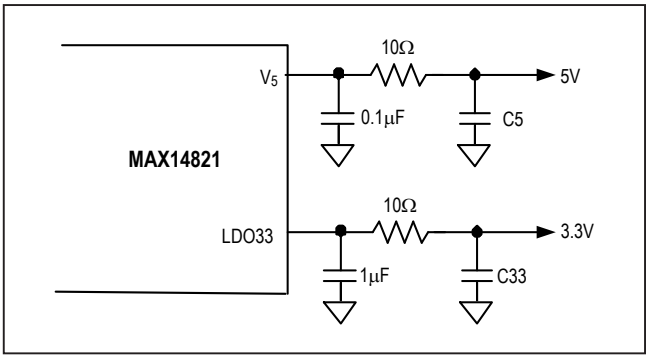


Figure 8. Larger Bypass Capacitance for Powering External Circuits

Use the LDO33Dis bit in the Mode register to disable LDO33. See the *Mode Register [R1, R0] = [1,1]* section for more information. V_5 and LDO33 are not protected against short circuits.

Power-Up

The C/Q and DO driver outputs and the UV output are high impedance when V_{CC}, V_5, V_L, and/or LDO33 voltages are below their respective undervoltage thresholds during power-up. UV goes low and the drivers are enabled when all these voltages exceed their respective undervoltage-lockout thresholds.

The drivers are automatically disabled if V_{CC}, V_5, or V_L falls below its UVLO threshold.

Undervoltage Detection

The device monitors V_{CC}, V_5, V_L, and optionally LDO33 for undervoltage conditions. UV is high impedance when any monitored voltage falls below its UVLO threshold.

V_{CC}, V_5, and V_L undervoltage detection cannot be disabled. When V_{CC} falls below the V_{CCUVLO} threshold, the UV24

and UV24Int bits are set, UV asserts high, and $\overline{IRQ}$ asserts low.

The SPI register contents are unchanged while V_5 is present, regardless of the state of V_{CC} and LDO33. The SPI interface is not accessible and $\overline{IRQ}$ is not available when UV is asserted due to a V_5 or V_L undervoltage event.

When the internal 3.3V LDO regulator voltage (V_{LDO33}) falls below the LDO33 undervoltage-lockout threshold, the UV33Int bit in the Status register is set and $\overline{IRQ}$ asserts. UV asserts if the UV33En bit in the Mode register is set to 1.

The UV output deasserts once the undervoltage condition is removed; however, bits in the Status register and the $\overline{IRQ}$ output are not cleared until the Status register has been read.

Wake-Up Detection

The device detects an IO-Link wake-up condition on the C/Q line in push-pull, high-side (PNP), or low-side (NPN) operation modes. A wake-up condition is detected when the C/Q output is shorted for 80µs (typ). $\overline{WU}$ pulses low for 190µs (typ) when the device detects a wake-up pulse on C/Q (Figure 5).

Set the WuIntEn bit in the Mode register to set the WuInt bit in the Status register and generate an interrupt on $\overline{IRQ}$ when a wake-up pulse is detected. WuInt is set and $\overline{IRQ}$ asserts immediately after C/Q is released when WuIntEn = 1.

Thermal Protection and Considerations

The internal LDOs and drivers can generate more power than the package for the device can safely dissipate. Ensure that the driver LDO loading is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{C/Q} + P_{DO} + P_5 + P_{LDO33} + P_Q + P_{CLCQ} + P_{CLDI}$$

where $P_{C/Q}$ is the power generated in the C/Q driver, P_{DO} is the power dissipated by the DO driver, P_5 and P_{LDO33} are the power generated by the LDOs, P_Q is the quiescent power generated by the device, and P_{CLCQ} and P_{CLDI} are the power generated in the C/Q and DI current sinks.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mΩ) due to the C/Q driver:

$$P_{C/Q} = [I_{C/Q}(max)] \times [0.5 + 7 \times I_{C/Q}(max)]$$

Calculate the internal power dissipation of the DO driver using the following equation:

$$P_{DO} = [I_{DO}(max)] \times [0.5 + 7 \times I_{DO}(max)]$$

Calculate the power dissipation in the 5V LDO, V_5, using the following equation:

$$P_5 = (V_{LDOIN} - V_5) \times I_5$$

where I_5 includes the I_{LDO33} current sourced from LDO33.

Calculate the power dissipated in the 3.3V LDO, LDO33, using the following equation:

$$P_{LDO33} = 1.7V \times I_{LDO33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_Q = I_{CC}(max) \times V_{CC}(max)$$

If the current sinks are enabled, calculate their associated power dissipation as:

$$P_{CLCQ} = I_{LLM\_C/Q}(max) \times V_{C/Q}(max)$$

$$P_{CLDI} = I_{LLM\_DI}(max) \times V_{DI}(max)$$

Overtemperature Warning

Bits in the Status and Mode registers are set when the temperature of the device exceeds +115°C (typ). The OTempInt bit in the Status register is set and $\overline{IRQ}$ asserts when the OTemp bit in the Mode register is set. Read the Status register to clear the OTempInt bit and $\overline{IRQ}$.

The OTemp bit is cleared when the die temperature falls to +95°C.

The device continues to operate normally unless the die temperature reaches the +150°C thermal shutdown threshold, when the device enters thermal shutdown.

Thermal Shutdown

When the die temperature rises above the +150°C (typ) thermal shutdown threshold, the C/Q and DO drivers and the C/Q and DI current loads are automatically turned off. The internal 3.3V and 5V LDOs remain on during thermal shutdown, if enabled. If the internal or external V_5 supply remains on during thermal shutdown (which is always true in case of the internal V_5 regulator), the register contents are maintained and SPI communication is available.

When the die temperature falls below the thermal shutdown threshold plus hysteresis, the C/Q and DO drivers and C/Q and DI current sinks turn on automatically.

Table 1. Register Summary

REGISTER	R1	R0	D7	D6	D5	D4	D3	D2	D1	D0
Status	0	0	WuInt	DoFaultInt	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
CQConfig	0	1	RxFilter	HiSlew	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	C/QLoad
DIOConfig	1	0	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	LiDis	DiLoad
Mode	1	1	RST	WuIntEn	DoFault	C/QFault	UV24	OTemp	UV33En	LDO33Dis

R1/R0 = Register address.

Status Register [R1, R0] = [0,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	WuInt	DoFaultInt	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	X	X	0	0	0	0
Reset Upon Read	Yes	Yes	No	No	Yes	Yes	Yes	Yes

X = Unknown. These bits are dependent on the DI logic and C/Q inputs.

The Status register reflects the logic levels of C/Q and DI and shows the source of interrupts that cause an $\overline{IRQ}$ hardware interrupt. The $\overline{IRQ}$ interrupt is asserted when an alarm condition (OTemp, UV33Int, UV24, C/QFault, DoFault, WuInt) is detected. All bits in the Status register are read-only. The interrupt bits return to the default state after the Status register is read. If a C/Q or DO fault condition persists, the associated interrupt bits are immediately set after the Status register is read.

BIT	NAME	DESCRIPTION
D7	WuInt	**Wake-Up Interrupt Request.** WuInt is set when an IO-Link wake-up request pulse is detected on C/Q and the WuIntEn bit in the Mode register is set. $\overline{IRQ}$ asserts when WuInt is set to 1. Read the Status register to clear the WuInt bit and deassert $\overline{IRQ}$.
D6	DoFaultInt	**DO Fault Interrupt.** DoFaultInt interrupt bit and DoFault bit (in the Mode register) are set when a fault condition occurs on the DO driver output. The device registers a fault condition when a short circuit or voltage fault is detected on DO (see the *DO Fault Detection* section for more information). $\overline{IRQ}$ asserts when DoFaultInt is 1. Read the Status register to clear the DoFaultInt bit and deassert $\overline{IRQ}$.
D5	DiLvl	**DI Logic Level.** The DiLvl bit mirrors the current logic level at the DI input. It is the inverse of the LI output and is always active regardless of the state of the LiDis bit (Table 2). DiLvl does not affect $\overline{IRQ}$. DiLvl is not changed when the Status register is read.

BIT	NAME	DESCRIPTION
D4	$\overline{Q}$Lvl	**C/Q Logic Level.** The $\overline{Q}$Lvl bit is the inverse of the logic level at C/Q. $\overline{Q}$Lvl is 1 when the C/Q input level is low (< 8V) and is 0 when the C/Q logic level is high (> 13V) (Table 3). $\overline{Q}$Lvl remains active when the C/Q receiver is disabled (RxDis = 1). $\overline{Q}$Lvl does not affect $\overline{IRQ}$. $\overline{Q}$Lvl is not changed when the Status register is read.
D3	C/QFaultInt	**C/Q Fault Interrupt.** The C/QFaultInt interrupt bit and C/QFault bit (in the Mode register) are set when a short circuit or voltage fault occurs on the C/Q driver output (see the *C/Q Fault Detection* section for more information). $\overline{IRQ}$ asserts when C/QFault is 1. Read the Status register to clear the C/QFaultInt bit and deassert $\overline{IRQ}$.
D2	UV33Int	**Internal 3.3V LDO (LDO33) Undervoltage Warning.** Both the UV33Int interrupt bit and the UV33En bit (in the Mode register) are set when V_{LDO33} falls below the 2.4V LDO33 undervoltage threshold. If UV33En is set in the Mode register, $\overline{IRQ}$ asserts low when the UV33Int bit is 1. Read the Status register to clear the UV33Int bit and deassert $\overline{IRQ}$. Set the UV33En bit to 1 in the Mode register to enable undervoltage monitoring for UV33Int. When enabled, UV asserts high when the UV33Int bit is 1. UV deasserts when V_{LDO33} rises above the LDO33 undervoltage threshold.
D1	UV24Int	**V_{CC} Undervoltage Interrupt.** The UV24Int interrupt bit and the UV24 bit (in the Mode register) are set when the V_{CC} voltage falls below the 7.4V undervoltage threshold. $\overline{IRQ}$ asserts low when the UV24Int bit is 1. Read the Status register to clear the UV24Int bit and deassert $\overline{IRQ}$. V_{CC} undervoltage detection cannot be disabled.
D0	OTempInt	**Overtemperature Warning.** The OTempInt interrupt bit and the OTemp bit (in the Mode register) are set when a high-temperature condition is detected by the device. OTemp is set when the temperature of the die exceeds +115°C (typ). OTempInt is set and $\overline{IRQ}$ asserts when the OTemp bit is 1. The OTempInt bit is cleared and $\overline{IRQ}$ deasserts when the Status register is read. Once cleared, OTempInt is not reset if the die temperature remains above the thermal warning threshold and does not fall below +95°C.

Table 2. DiLvl and LI Output

V_{DI} (V)	DiLvl BIT	LI OUTPUT
< 5.2	0	High
> 8	1	Low

Table 3. $\overline{Q}$Lvl and RX Output

$V_{C/Q}$ (V)	$\overline{Q}$Lvl BIT	RX OUTPUT
< 8	1	High
>13	0	Low

CQConfig Register [R1, R0] = [0,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RxFilter	HiSlew	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	C/QLoad
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0

Use the CQConfig register to control the C/Q receiver and driver parameters. All bits in the CQConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	RxFilter	C/Q and DI Receiver Filter Control. The C/Q and DI receivers have analog lowpass filters to reduce high-frequency noise on the receiver inputs. Set the RxFilter bit to 0 to set the filter corner frequency to 500kHz. Set the RxFilter bit to 1 to set the filter corner frequency to 1MHz (this setting is used for high-speed COM3 operation). Noise filters on C/Q and DI are controlled simultaneously by the RxFilter bit.
D6	HiSlew	Slew-Rate Control. The HiSlew bit increases the slew rate for the C/Q and DO drivers and is used for high-speed COM3 (230kbps) data rates. Set HiSlew to 0 for COM1 and COM2 operation.
D5	C/Q_N/P	C/Q Driver NPN/PNP Mode. The C/Q_N/P bit selects between low-side (NPN) and high-side (PNP) modes when the C/Q driver is configured as an open-drain output (C/Q_PP = 0). Set C/Q_N/P to 1 to configure the driver for low-side (NPN) operation. Set C/Q_N/P to 0 for high-side (PNP) operation.
D4	C/Q_PP	C/Q Driver Push-Pull Operation. Set C/Q_PP to 1 to enable push-pull operation on the C/Q driver. The C/Q output is open-drain when C/Q_PP is 0.
D3	C/QDEn	C/Q Driver Enable/Disable. Set the C/QDEn bit to 1 to enable the C/Q driver. Set C/QDEn to 0 for hardware (TXEN) control. See Table 4.
D2	Q	C/Q Driver Output Logic. The Q bit can be used to program the C/Q output driver through software. The C/Q driver must be enabled and TXC = TXQ must be high to control the C/Q driver through the Q bit (Figure 8). C/Q has the same logic polarity as the Q bit. Set the Q bit to 0 to control the C/Q driver with TXC and TXQ. The C/Q driver output state depends on the C/Q_PP and C/Q_N/P bits as shown in Table 5. Note that Table 5 assumes that the C/Q driver is enabled (TXEN = V_L or C/QDEn = 1).
D1	RxDis	C/Q Receiver Enable/Disable. Set the RxDis bit to 1 to disable the C/Q receiver. The RX output is high when RxDis is 1.
D0	C/QLoad	C/Q Current Sink Enable. Set the C/QLoad bit to 1 to enable the internal current sink at C/Q.

Table 4. C/QDEn and TXEN C/Q Driver Control

C/QDEn	TXEN	C/Q DRIVER
0	Low	Disabled
X	High	Enabled
1	X	Enabled

X = Don't care.

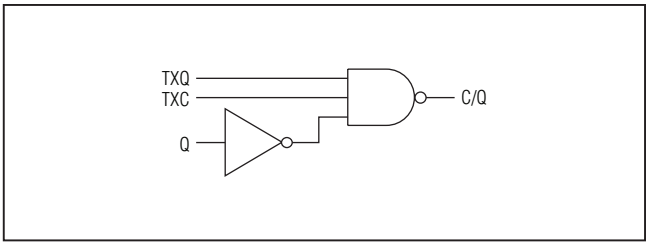


Figure 9. Equivalent C/Q Logic

Table 5. C/Q Driver Output State

TXC AND TXQ (SEE NOTE)	Q	C/Q_PP	C/Q_N/P	C/Q CONFIGURATION	C/Q STATE
High	1	0	0	PNP, open-drain	On, C/Q is high
High	0	0	0	PNP, open-drain	Off, C/Q is high impedance
High	1	0	1	NPN, open-drain	Off, C/Q is high impedance
High	0	0	1	NPN, open-drain	On, C/Q is low
High	1	1	X	Push-pull	High
High	0	1	X	Push-pull	Low

Note: TXC and TXQ = V_L.

X = Don't care.

DIOConfig Register [R1, R0] = [1,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	LiDis	DiLoad
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0

Use the DIOConfig register to control the DI and DO interfaces. All bits in the DIOConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	DoInv	DO Output Polarity. Set the DoInv bit to 1 to invert the logic of the DO output. This bit also works in conjunction with the DoAv (Table 6). DO tracks the TXC and TXQ inputs with the opposite polarity when both the DoAv and DoInv bits are set.
D6	DoAv	DO Antivalent Operation. Set the DoAv bit to 1 to enable antivalent output operation on DO. DO tracks the TXC and TXQ inputs (and the Q bit) when DoAv is 1 (Table 6). The LO input and the DoBit are ignored when the DoAv bit is 1.
D5	DoN/P	DO Driver NPN/PNP Operation. The DoN/P bit selects between low-side (NPN) and high-side (PNP) modes when the DO driver is configured as an open-drain output (DoPP = 0). Set DoN/P to 1 to configure the driver for low-side (NPN) operation. Set DoN/P to 0 for high-side (PNP) operation.
D4	DoPP	DO Driver Push-Pull Operation. Set the DoPP bit to 1 to configure the DO driver output for push-pull operation. DO is an open-drain output when DoPP is 0.
D3	DoEn	DO Driver Enable/Disable. Set the DoEn bit to 1 to enable the DO driver. The DO driver is high impedance with a weak pulldown when DoEn is 0.
D2	DoBit	DO Driver Output Logic. The DoBit bit can be used to program the DO output driver through software. Drive LO high to activate DoBit programming (Figure 9). The DO output state is given in Table 7. Note that Table 7 assumes that the DoInv bit is 0.
D1	LiDis	LI Output Enable/Disable. Set the LiDis bit to 1 to disable the LI output. The LI output is low when LiDis is 1.
D0	DiLoad	DI Current Sink Enable. Set the DiLoad bit to 1 to enable the internal current sink at the DI input.

Table 6. DoAv and DoInv Operation

DoAv	DoInv	TXC AND TXQ (NOTE 1)	LO (NOTE 1)	DO (NOTE 2)	C/Q (NOTE 2)
0	0	Low	Low	High	High
0	0	Low	High	Low	High
0	0	High	Low	High	Low
0	0	High	High	Low	Low
0	1	Low	Low	Low	High
0	1	Low	High	High	High
0	1	High	Low	Low	Low
0	1	High	High	High	Low
1	0	Low	Low	Low	High
1	0	Low	High	Low	High
1	0	High	Low	High	Low
1	0	High	High	High	Low
1	1	Low	Low	High	High
1	1	Low	High	High	High
1	1	High	Low	Low	Low
1	1	High	High	Low	Low

Note 1: Low is when V_{TXC}, V_{TXQ}, OR V_{LO} = 0V; high is when V_{TXC}, V_{TXQ}, or V_{LO} = V_L.

Note 2: Low is when C/Q or DO < 8V; high is when C/Q or DO >13V.

Table 7. DO Output Programmed by DoBit

LO	DoBit	DoPP	DoN/P	DO CONFIGURATION	DO STATE
High	0	1	X	Push-pull	Low
High	1	1	X	Push-pull	High
High	0	0	0	PNP	Off, DO is high impedance
High	1	0	0	PNP	On, DO is high
High	0	0	1	NPN	On, DO is low
High	1	0	1	NPN	Off, DO is high impedance
Low	X	X	X	See Table 6	See Table 6

X = Don't care.

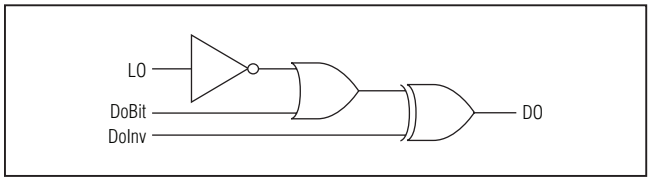


Figure 10. Equivalent DO Logic

Mode Register [R1, R0] = [1,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST	WuIntEn	DoFault	C/QFault	UV24	OTemp	UV33En	LDO33Dis
Read/Write	R/W	R/W	R	R	R	R	R/W	R/W
POR State	0	0	0	0	0	0	0	0

Use the Mode register to reset the MAX14821 and manage the 3.3V LDO. The Mode register has bits that represent the current status of fault conditions. When writing to the Mode register, the contents of the fault indication bits (bits 2 to 5) do not change.

BIT	NAME	DESCRIPTION
D7	RST	**Register Reset.** Set RST to 1 to reset all registers to their default power-up state. Then set RST to 0 for normal operation. The Status register is cleared and $\overline{IRQ}$ deasserts (if asserted) when RST = 1. Interrupts are not generated while RST = 1.
D6	WuIntEn	**Wake-Up Interrupt Enable.** Set WuIntEn to 1 to enable wake-up interrupt generation. When WuIntEn is set, the WuInt bit in the Status register is set and $\overline{IRQ}$ asserts when a valid wake-up condition is detected. The C/Q driver must be enabled for wake-up detection. The state of WuIntEn does not affect the $\overline{WU}$ output. See the *Wake-Up Detection* section for more information. When the IO-Link device is in IO-Link communication mode, the WuInt bit should be set to 0, so that interrupts are not generated for false wake-up events.
D5	DoFault	**DO Fault Status.** The DoFault bit is set when a short circuit or voltage fault occurs at the DO driver output (see the *DO Fault Detection* section for more information). The DoFault and DoFaultInt bits are both set when a fault occurs on DO. DoFault is cleared when the fault is removed.
D4	C/QFault	**C/Q Fault Status.** The C/QFault bit is set when a short circuit or voltage fault occurs at the C/Q driver output (see the *C/Q Fault Detection* section for more information). The C/QFault and C/QFaultInt bits are both set when a fault occurs on C/Q. C/QFault is cleared when the fault is removed.
D3	UV24	**V_{CC} Undervoltage Condition.** Both the UV24 and the UV24Int bits are set when V_{CC} falls below V_{CCUVLO}. UV24 is cleared when V_{CC} rises above the V_{CC} threshold. V_5 must be present for V_{CC} undervoltage monitoring.
D2	OTemp	**Temperature Warning.** The OTemp bit is set when a high-temperature condition occurs on the device. Both the OTempInt interrupt in the Status register and the OTemp bit are set when the junction temperature of the die rises to above +115°C (typ). The OTemp bit is cleared when the junction temperature falls below +95°C (typ).
D1	UV33En	**LDO33 UV Enable.** Set the UV33En bit to 1 to assert the UV output when LDO33 voltage falls below the 2.4V (typ) undervoltage-lockout threshold. The UV33En bit does not affect the UV33Int bit in the Status register; $\overline{IRQ}$ asserts when V_{LDO33} falls below $V_{LDO33UVLO}$ regardless of the state of UV33En.
D0	LDO33Dis	**LDO33 Enable/Disable.** Set LDO33Dis to 1 to disable the 3.3V linear regulator (LDO33).

Register Functionality

The device has four 8-bit-wide registers for configuration and monitoring (Table 1).

SPI Interface

The device communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs—clock (SCLK), chip select ($\overline{CS}$), and data in (SDI)—and one output, data out (SDO). The maximum SPI clock rate for the device is 12MHz. The SPI interface complies with clock polarity CPOL = 0 and clock phase CPHA = 0 (see Figure 11 and Figure 12).

The SPI interface is not available when V_5 or V_L are not present.

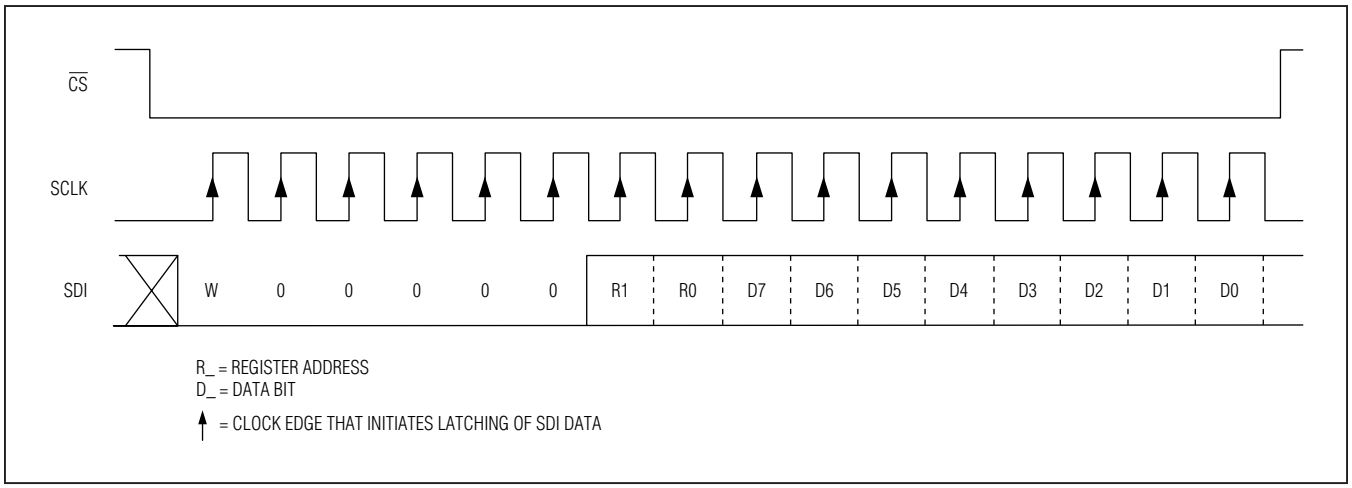


Figure 11. SPI Write Cycle

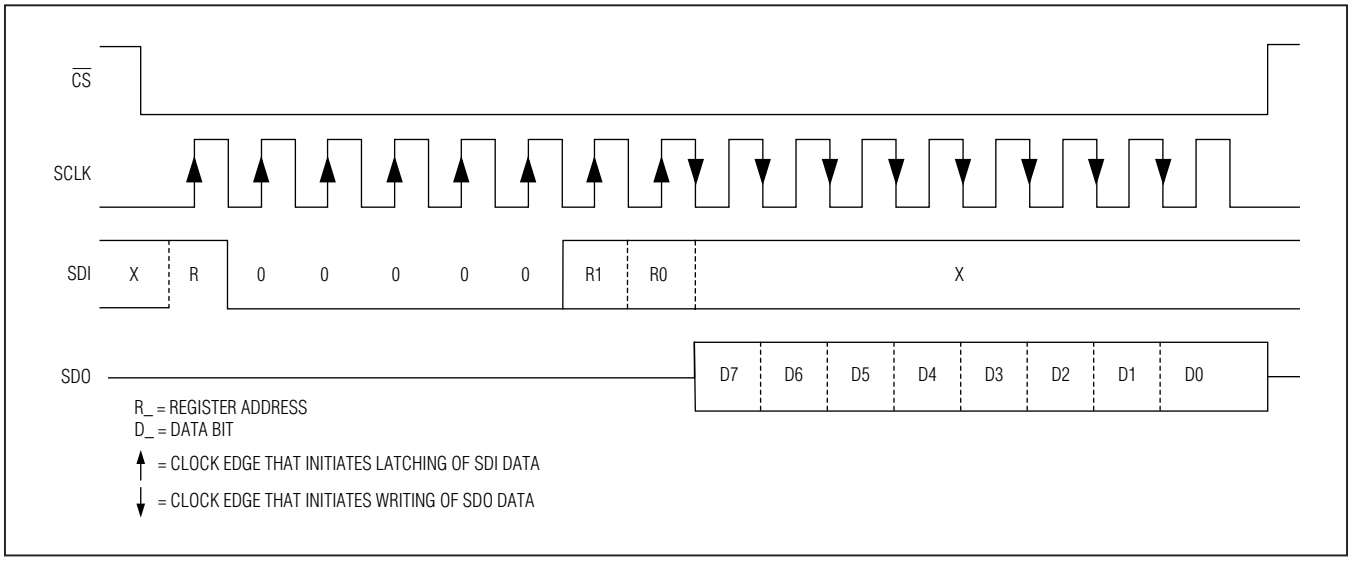


Figure 12. SPI Read Cycle

Applications Information

UART Interfacing

The logic levels of the microcontroller interface I/Os (TXC, TXQ, TXEN, and RX) are defined by V_L.

The device can be interfaced to microcontrollers where the on-board UART TX output cannot be programmed as a logic output (GPO). In this case, connect the TX output of the UART to the TXC input for IO-Link communication and connect a separate GPO output on the microcontroller to TXQ for standard IO (SIO) mode operation (Figure 13). As the TXQ and TXC inputs are internally logically ANDed, the unused input (TXC or TXQ) must be held high while the other is in operation.

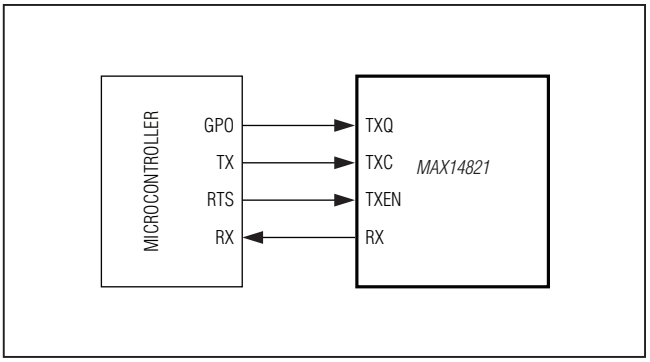


Figure 13. UART Interface

Transient Protection

Inductive load switching, surges, and bursts create high transient voltages. C/Q, DO, and DI should be protected against high overvoltage and undervoltage transients. Positive voltage transients on C/Q, DO, and DI must be limited to +55V relative to GND and negative voltage transients must be limited to -55V (relative to V_{CC}) on DO and C/Q and to -55V (relative to GND) on DI. Figure 14 shows suitable protection using TVS diodes to meet both the IEC 61000-4-2 ESD and, ±2kV IEC 61000-4-4 burst and ±1kV/500Ω surge testing. Connect the TVS diodes as close to the MAX14821 pins as possible.

The device has to be protected against transients that occur during hot-plugging of the L+ sensor supply (V_{CC} input). This is achieved by placing a 10Ω resistor with 1µF capacitor before LDOIN and connecting an RC between the sensor supply input and the V_{CC} pin, as shown in Figure 14. The RC time constant of the filter on V_{CC} should be larger or equal to 0.8µs. In case that V_L is supplied by V_5 and the bypass capacitor on V_5 is 100nF, the 10Ω resistor in series with LDOIN is not needed.

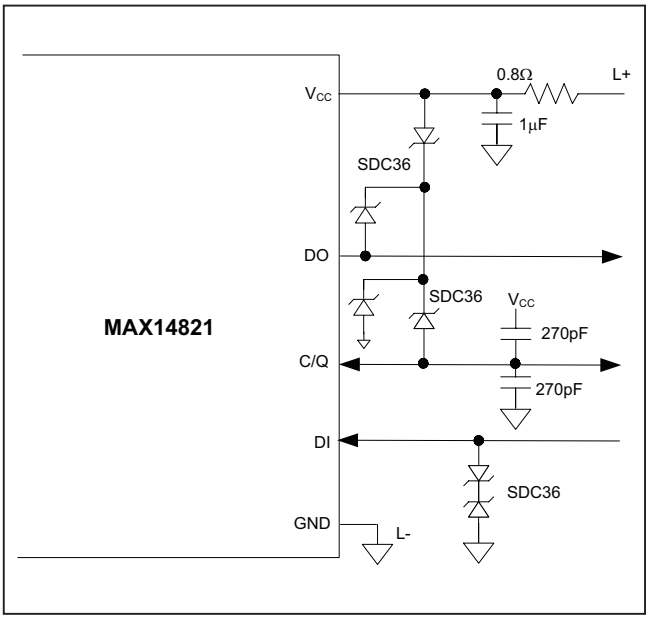


Figure 14. MAX14821 Operating Circuit with TVS Protection

Optional External Powering

The MAX14821 requires the V_{CC}, V_5, and V_L pins be supplied for the device to operate normally. The V_5 supply can be derived from the internal 5V regulator or from an external 5V regulator.

V_L is the logic supply, which sets the logic levels of the microcontroller interface. The logic and SPI interface are operational when the V_5 and V_L are present, even if V_{CC} is not present.

The LDO33 supply is not required by the device and is provided as a 3.3V regulator output for optional powering of external devices, like a microcontroller.

The V_P output provides a reverse-polarity-protected voltage one diode drop below V_{CC} and can be used for supplying external circuitry, like power supplies. The current drawn from V_P cannot exceed 50mA. Be aware that capacitance on V_P can cause transient currents at power-up equal to C x dV_{CC}/dt.

In order to reduce power dissipated in the device, an reverse protection diode can be used to power the external circuitry, instead of using V_P, as shown in Figure 15.

V_5 is typically powered by the internal 5V regulator, but can alternatively be powered by an external 5V regulator. When powering V_5 externally, connect LDOIN to V_5.

(Figure 15). This configuration disables operation of the internal 5V regulator and reduces the on-chip power consumption.

When an external 5V regulator is used to power V_5, the V_5 bypass capacitance is determined by that regulator, and is not limited to 100nF.

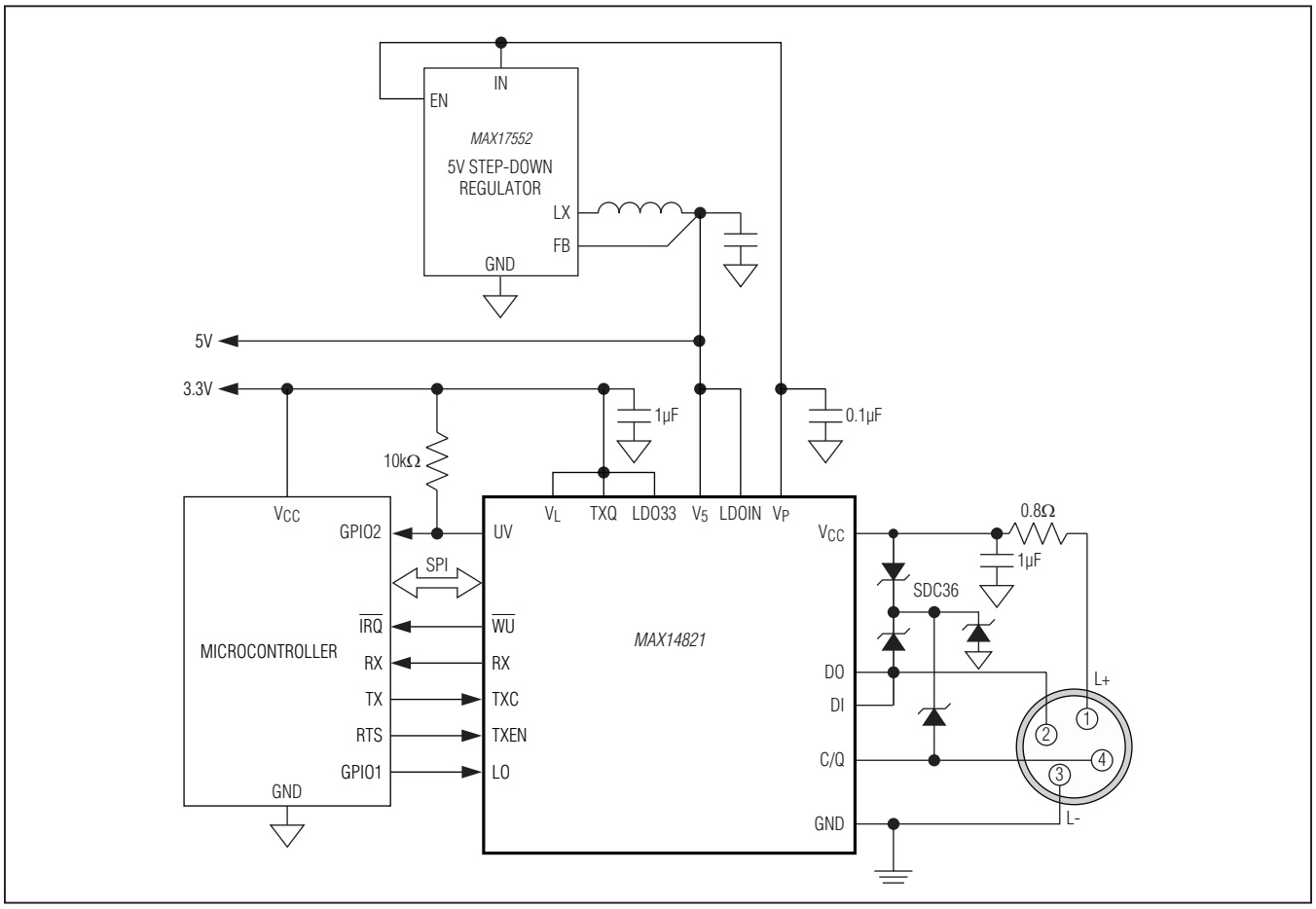


Figure 15. Using an Optional External Supply to Power the MAX14821

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14821ETG+	-40°C to +85°C	24 TQFN-EP*
MAX14821EWA+**	-40°C to +85°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS