19-6331; Rev 0; 5/12

MAX14850PMB1 Peripheral Module

General Description

The MAX14850PMB1 peripheral module utilizes the MAX14850 digital isolator to isolate another SPI- or UART-based module from any host system that utilizes Pmod™-compatible expansion ports configurable for either a UART or SPI interface. This peripheral module is first plugged into the host Pmod port. Another UART- or SPI-based module plugged into the 12-pin Pmod-compatible connector on this peripheral module is galvanically isolated from the host and referenced to a secondary power supply connected to this peripheral module.

The IC is a 6-channel digital isolator utilizing Maxim's proprietary process technology, whose monolithic design provides a compact and low-cost transfer of digital signals between circuits with different power domains. Of the six total channels, the four unidirectional channels are each capable of DC to 50Mbps, with two of the four channels passing data across the isolation barrier in each direction. The two bidirectional channels are open drain and each is capable of data rates from DC to 2Mbps.

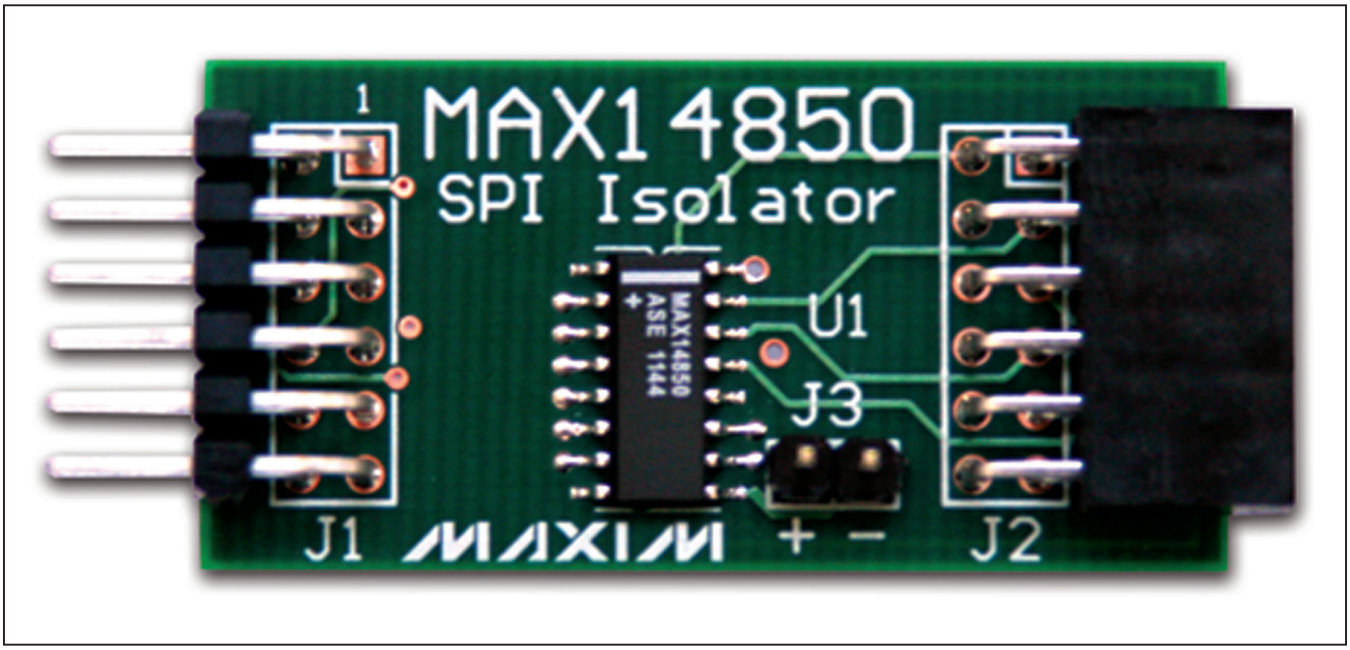
Refer to the MAX14850 IC data sheet for detailed information regarding operation of the IC.

Features

- **Isolates SPI- or UART-Based Pmod-Compatible Modules from the Host System**
- **Data Rates from 2Mbps to 20Mbps or Greater, Depending on Configuration**
- **2-Pin Header to Connect External Voltage for Isolated Module**
- **600V_{RMS} Isolation for 60s**
- **Isolates Four SPI or UART Signals and Two Control Signals**
- **Short-Circuit Protection on Unidirectional Outputs**
- **12-Pin Pmod-Compatible Male Connector to Host**
- **12-Pin Pmod-Compatible Female Connection for Module to be Isolated**
- **RoHS Compliant**
- **Proven PCB Layout**
- **Fully Assembled and Tested**

Ordering Information appears at end of data sheet.

MAX14850PMB1 Peripheral Module



Pmod is a trademark of Digilent Inc.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	2	0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104KA01D
C3	1	1µF ±10%, 10V X7R ceramic capacitor (0603) TDK C1608X7R1A105K
J1	1	12-pin (2 x 6) right-angle male header
J2	1	12-pin (2 x 6) right-angle female header
J3	1	2-pin straight male header
R1–R6	6	150Ω ±5% resistors (0603)
R7–R10	4	4.7kΩ ±5% resistors (0603)
U1	1	6-channel digital isolator (16 SO) Maxim MAX14850ASE+
—	1	PCB: EPCB14850PM1

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX14850PMB1 when contacting these component suppliers.*

Detailed Description

UART Interface

The MAX14850PMB1 peripheral module can interface to the host by plugging directly into a Pmod-compatible port (configured for SPI or UART) through connector J1. See Table 1.

Connector J2 provides the galvanically isolated connection to another peripheral module. Note that even though the pinout numbering is different than J1, the signals from the top row of pins on J1 are passed through to the top row of pins on J2. See Table 2.

Connector J3 provides power from the 2nd power domain to the isolated side of the IC and the isolated Pmod.

Software and FPGA Code

Example software and drivers are available that execute directly without modification on several FPGA development boards that support an integrated or synthesized microprocessor. These boards include the Digilent Nexys 3, Avnet LX9, and Avnet ZEDBoard, although other platforms can be added over time. Maxim provides complete Xilinx ISE projects containing HDL, Platform Studio, and SDK projects. In addition, a synthesized bit stream, ready for FPGA download, is provided for the demonstration application.

The software project (for the SDK) contains several source files intended to accelerate customer evaluation and design. These include a base application (maximModules.c) that demonstrates module functionality, and uses an API interface (maximDeviceSpecific Utilities.c) to set and access Maxim device functions within a specific module.

The source code is written in standard ANSI C format, and all API documentation including theory/operation, register description, and function prototypes are documented in the API interface file (maximDeviceSpecificUtilities.h & .c).

The complete software kit is available for download at **www.maxim-ic.com**. Quick start instructions are also available as a separate document.

Table 1. Connector J1 (with SPI/UART Peripheral Attached to J2)

PIN	SIGNAL	DESCRIPTION
1	SS_CTS	Serial select/clear to send
2	MOSI_TXD	Master-out slave input/host transmit
3	MISO_RXD	Master-in slave output/host receive
4	SCK_RTS	Serial clock/ready to send
5	GND	Ground
6	VCC	Power supply
7	SPAREIN	Spare input from Pmod to host
8	N.C.	Not connected
9	N.C.	Not connected
10	SPAREIO	Spare input/output
11	GND	Ground
12	VCC	Power supply

Table 2. Connector J2

PIN	SIGNAL	DESCRIPTION
1	O_SPAREIN	Spare input from Pmod to host
2	N.C.	Not connected
3	N.C.	Not connected
4	O_SPAREIO	Spare input/output
5	O_GND	Ground from 2nd power domain (supplied through J3)
6	O_VCC	Power from 2nd power domain (supplied through J3)
7	O_SS_CTS	Serial select/clear to send
8	O_MOSI_TXD	Master-out slave input/host transmit
9	O_MISO_RXD	Master-in slave output/host receive
10	O_SCK_RTS	Serial clock/ready to send
11	O_GND	Ground from 2nd power domain (supplied through J3)
12	O_VCC	Power from 2nd power domain (supplied through J3)

Table 3. Connector J3

PIN	SIGNAL	DESCRIPTION
1	O_VCC	VCC for the 2nd power domain (up to 600V_{RMS} separation)
2	O_GND	Ground for the 2nd power domain

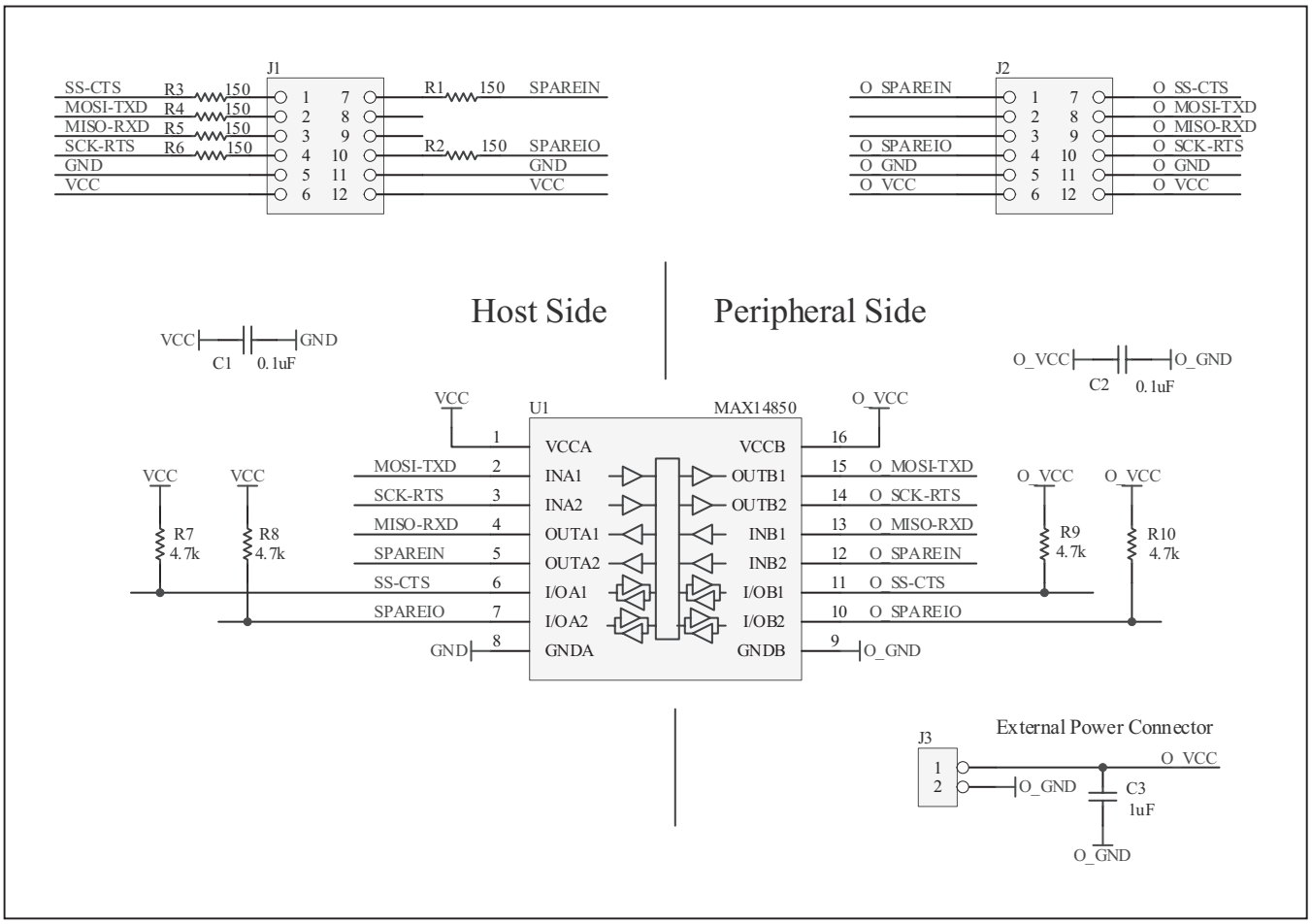


Figure 1. MAX14850PMB1 Peripheral Module Schematic

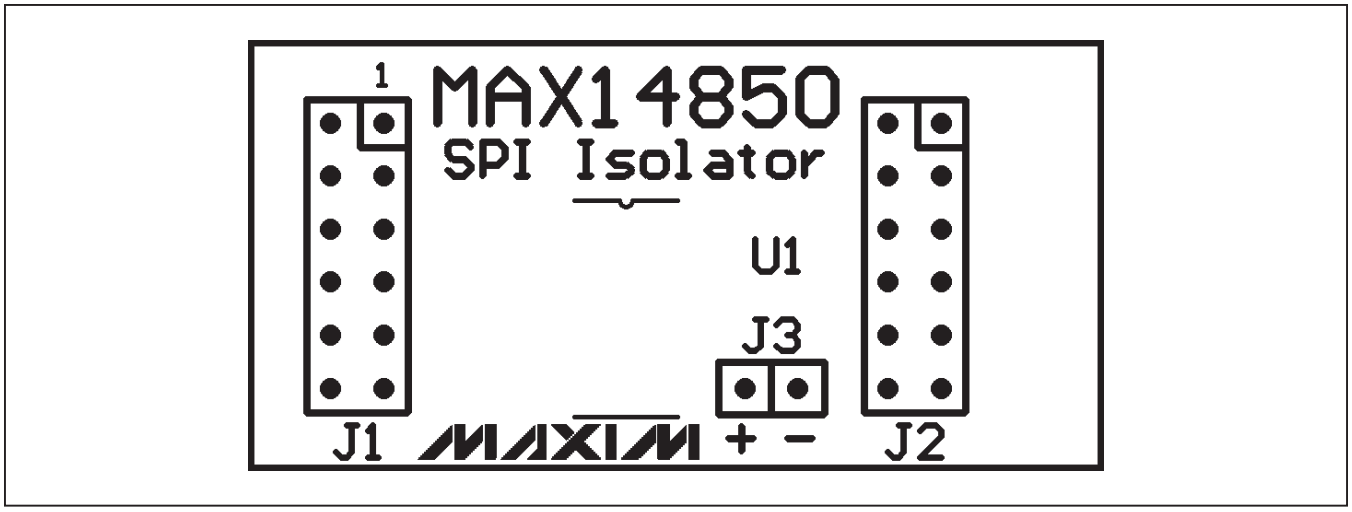


Figure 2. MAX14850PMB1 Peripheral Module Component Placement Guide—Component Side

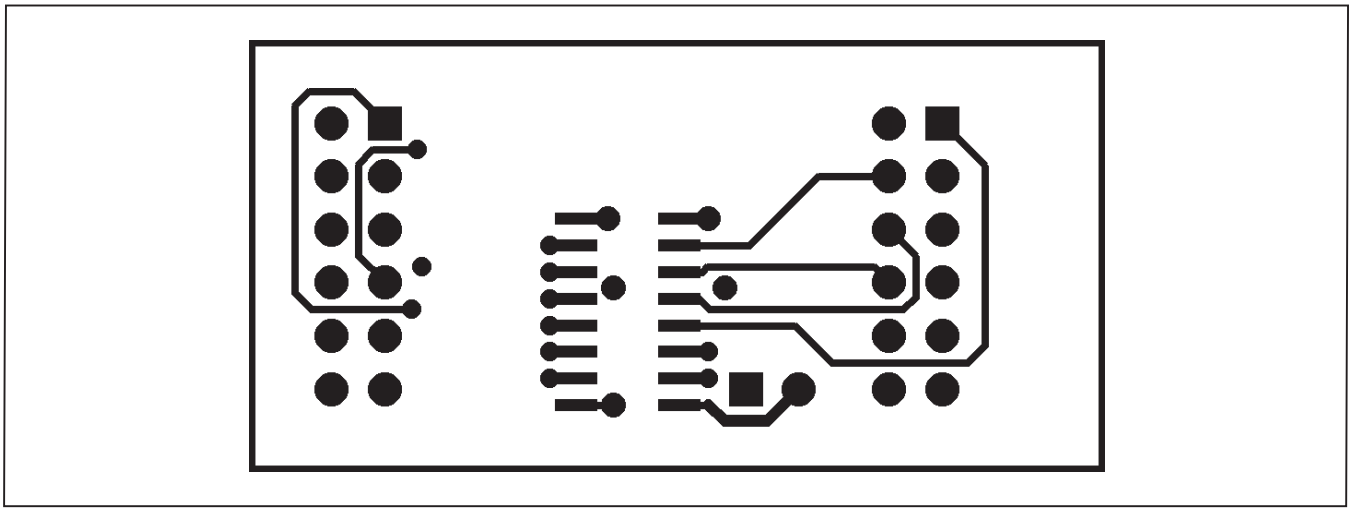


Figure 3. MAX14850PMB1 Peripheral Module PCB Layout—Component Side

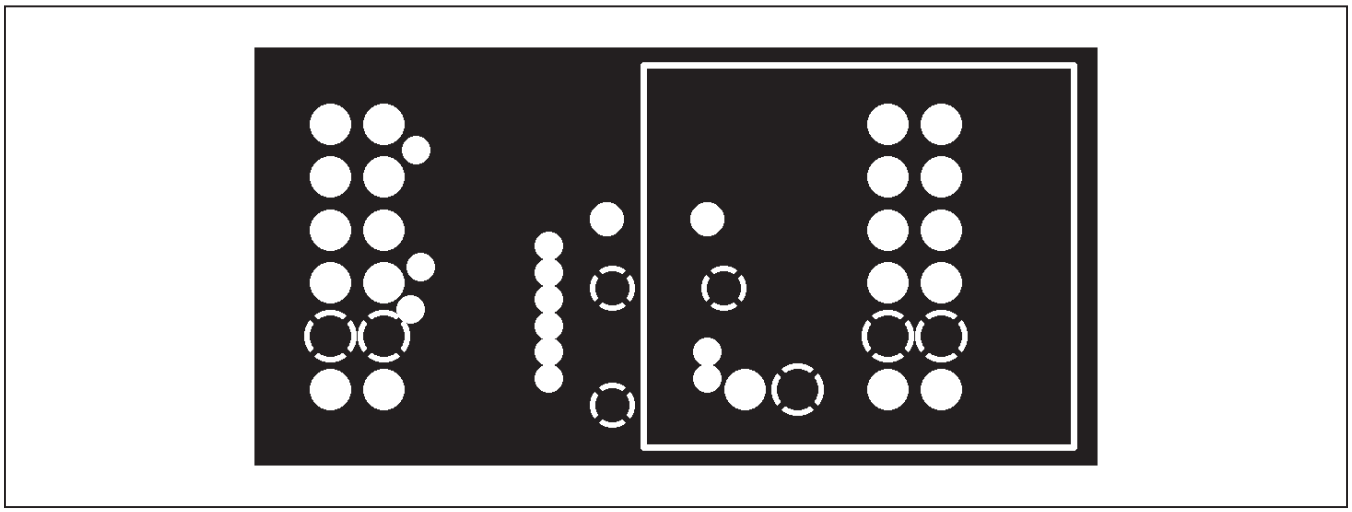


Figure 4. MAX14850PMB1 Peripheral Module PCB Layout—Inner Layer 1 (Ground)

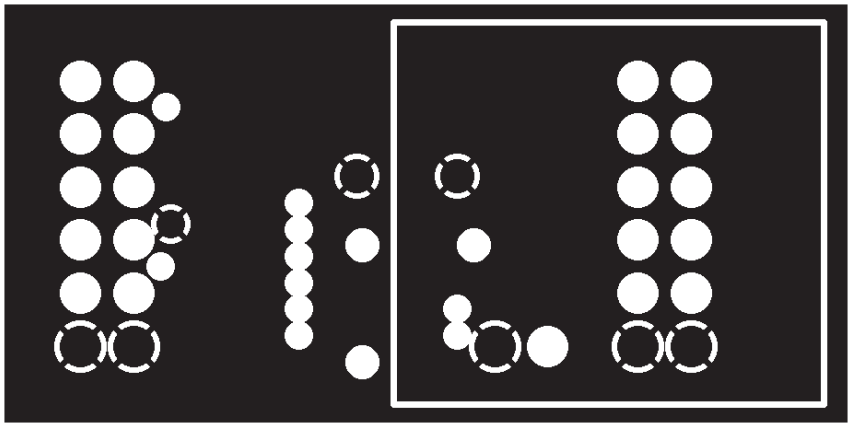


Figure 5. MAX14850PMB1 Peripheral Module PCB Layout—Inner Layer 2 (Power)

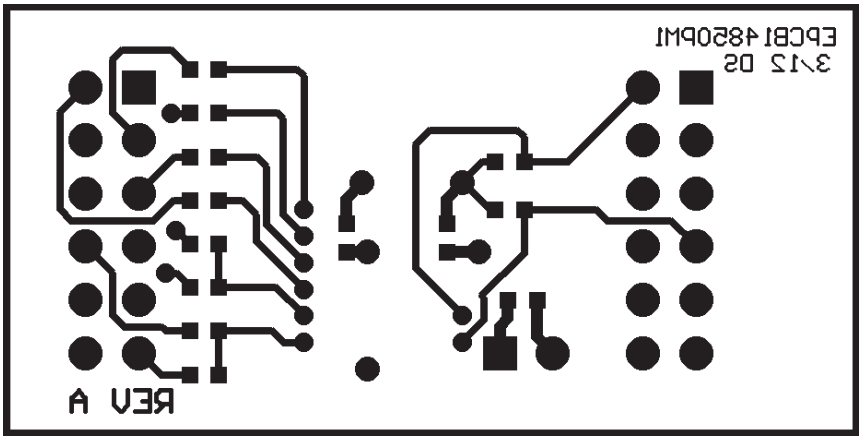


Figure 6. MAX14850PMB1 Peripheral Module PCB Layout—Solder Side

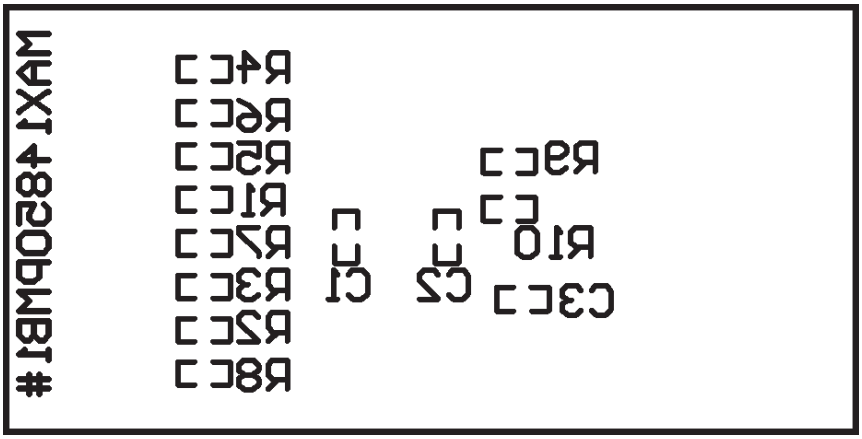


Figure 7. MAX14850PMB1 Peripheral Module Component Placement Guide—Solder Side

Ordering Information

PART	TYPE
MAX14850PMB1#	Peripheral Module

#Denotes RoHS compliant.