MAX14986

Dual 6GT/s SAS/SATA Redriver with Equalization and Extended Temperature Operation

General Description

The MAX14986 dual-channel redriver is designed to redrive one full lane of SAS or SATA signals up to 6.0GT/s (gigatransfers per second) and operates from a single +3.3V supply.

The MAX14986 features independent input equalization and output preemphasis. It enhances signal integrity at the receiver by equalizing the signal at the input and establishing preemphasis at the output of the device. SAS and SATA OOB (out-of-band) signaling is supported using high-speed amplitude detection on the inputs and squelch on the corresponding outputs. Inputs and outputs are all internally 50Ω terminated and must be AC-coupled to the SAS/SATA controller IC and SAS/SATA device.

The MAX14986 is available in a small 28-pin, 3.5mm x 5.5mm TQFN package with flow-through traces for ease of layout. This device is specified over the -40°C to +85°C extended operating temperature range.

Applications

- Industrial/Embedded PCs
- Computer on Modules
- Carrier Boards
- Test Equipment
- Rack Server Industrial PCs
- Medical Equipment

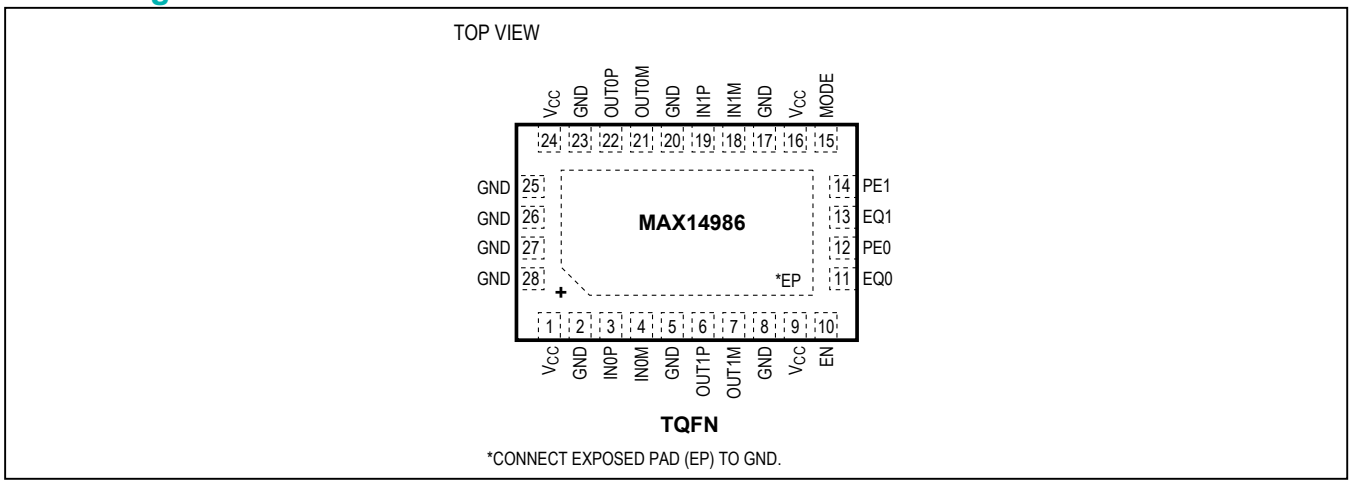
Benefits and Features

- High-Performance Solution Designed to Overcome Lossy Channels
  - 3dB of Independent (per Channel) Selectable Input EQ and Output Preemphasis
  - Compensates Up to 30in of Channel Losses with Deterministic Jitter: $23ps_{P-P}$ (max); Random Jitter: $1.5ps_{RMS}$ (max)
  - 8dB (typ) of Return Loss Up to 3.0GHz
- Designed to Reliably Operate in Harsh Environments
  - Industrial Temperature Rated: -40°C to +85°C
  - ±2.5kV Human Body Model (HBM) ESD Protection on All Pins
  - Housed in a Flow-Through (3.5mm x 5.5mm, 28-Pin) TQFN Package for Resistance to Vibration/Shocks
- Ease of Design and Layout
  - Single 3.3V Operation
  - Internal Input/Output 50Ω Termination Resistors on All Pins
  - Flow-Through Pinout

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14986.related.

Pin Configuration



Absolute Maximum Ratings

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
All Other Pins ..... -0.3V to (V_{CC} + 0.3V
Continuous Current (PE_, EQ_, MODE) ..... ±15mA
Peak Current (for 10kHz, 1% duty cycle)
(IN__, OUT__) ..... ±100A

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C) 2286mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Junction Temperature ..... +15°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JC}) ..... 2.7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 35°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, C_{COUPLE} = 12nF, R_L = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V_{CC}		3.0		3.6	V
Operating Supply Current	I_{CC}	EQ_ = PE_ = GND		140	175	mA
		EQ_ = PE_ = V_{CC}		175	220	
Standby Supply Current	I_{STBY}	EN = GND		16	20	mA
Input Termination	R_{RX-SE}	Single-ended to V_{CC}	42.5		57.5	Ω
Output Termination	R_{TX-SE}	Single-ended to V_{CC}	42.5		57.5	Ω
AC PERFORMANCE						
Differential Input Return Loss (Note 3)	S_{DD11}	0.1GHz ≤ f ≤ 0.3GHz	-10			dB
		0.3GHz ≤ f ≤ 3.0GHz	-7.9			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Common-Mode Input Return Loss (Note 3)	S_{CC11}	0.1GHz ≤ f ≤ 0.3GHz	-6			dB
		0.3GHz ≤ f ≤ 3.0GHz	-5			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Differential Output Return Loss (Note 3)	S_{DD22}	0.1GHz ≤ f ≤ 0.3GHz	-10			dB
		0.3GHz ≤ f ≤ 3.0GHz	-7.9			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Common-Mode Output Return Loss (Note 3)	S_{CC22}	0.1GHz ≤ f ≤ 0.3GHz	-6			dB
		0.3GHz ≤ f ≤ 3.0GHz	-4			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Differential Input Voltage	$V_{IN-DIFF}$	SAS 1.5, 3.0, or 6.0GT/s MODE = GND	275		1600	mV_{P-P}
		SATA 1.5, 3.0, or 6.0GT/s MODE = V_{CC}	225		1600	
Input Equalization	EQ	EQ_ = V_{CC} (Note 4)		3		dB
Differential Output Voltage	$V_{OUT-DIFF}$	f = 750MHz, PE_ = GND	750		1200	mV_{P-P}

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{COUPLE} = 12nF, R_L = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Preemphasis	PE	PE_ = V_{CC}, Figure 1		3		dB
Propagation Delay	t_{PD}	PE_ = EQ_ = GND		300		ps
Output Transition Time	T_{TX-RF}	PE_ = GND, 20% to 80%	30			ps
Differential Output Skew Same Pair	T_{SK}			10		ps
Deterministic Jitter	T_{DJ}	K28.5 pattern, 6.0GT/s, PE_ = EQ_ = GND (Note 3)			23	ps_{P-P}
Random Jitter	T_{RJ}	D10.2 pattern, 6.0GT/s, PE_ = EQ_ = GND			1.5	ps_{RMS}
OOB Squelch Threshold	$V_{SQ-DIFF}$	MODE = GND, f = 0.75GHz	120		220	mV_{P-P}
		MODE = V_{CC}, f = 0.75GHz	75		200	
OOB Squelch Entry Time	$T_{OOB,SQ}$	f = 0.75GHz (Note 3)			5	ns
OOB Squelch Exit Time	$T_{OOB,EX}$	f = 0.75GHz (Note 3)			9	ns
OOB Differential Offset Delta	$\Delta V_{OOB,DIFF}$	Difference between OOB and active-mode output offset	-50		+50	mV
OOB Common-Mode Offset Delta	$\Delta V_{OOB,CM}$	Difference between OOB and active-mode output common-mode voltage	-30		+30	mV
OOB Output Disable	$V_{OOB,OUT}$	OOB disabled output level			30	mV_{P-P}
CONTROL LOGIC INPUTS						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.6	V
Input Logic Hysteresis	V_{HYST}			75		mV
Input Leakage Current	I_{IN}	V_{CC} = +3.3V, V_{IN} = +0.5V or +1.5V	-50		+50	µA

Note 2: All devices are 100% production tested at T_A= +85°C. All temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

Note 4: EQ (input equalization) as employed in this device refers to the equivalent of adding preemphasis before the input. For example, input EQ of 3dB would show the same waveform as output PE of 3dB (see Figure 1).

Timing Diagram

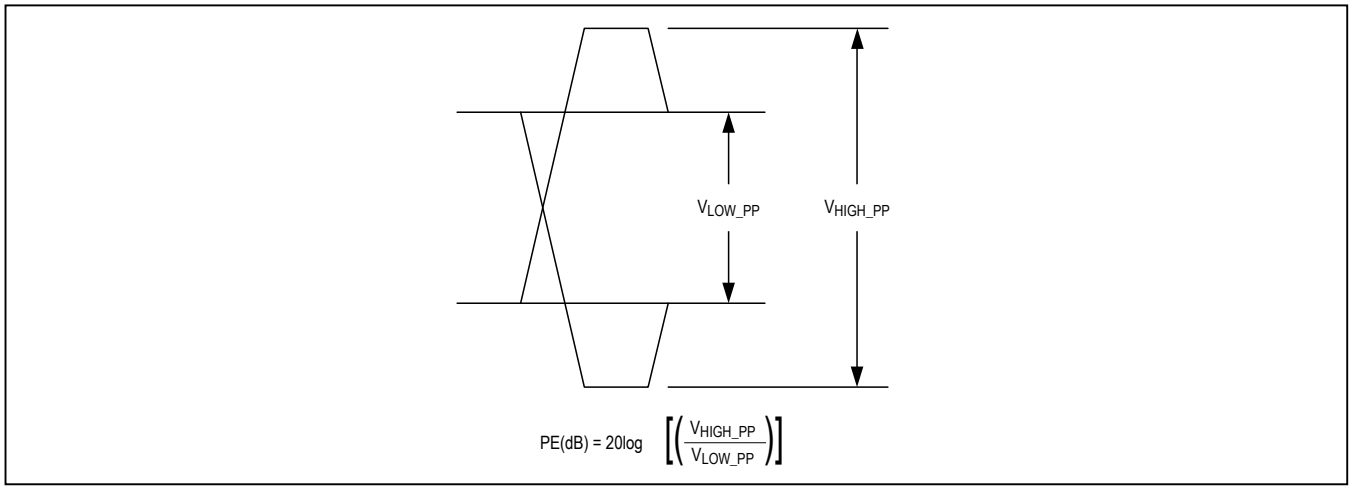
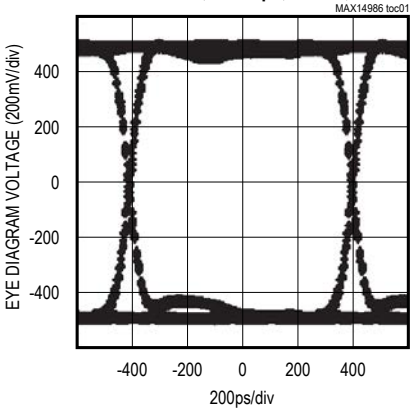


Figure 1. Output Preemphasis

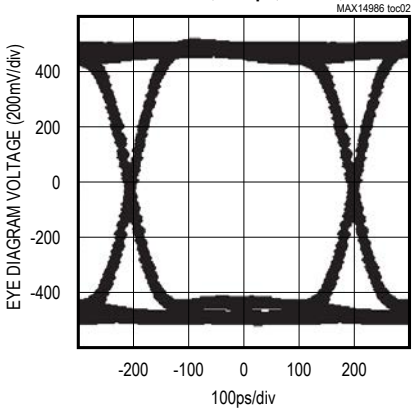
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

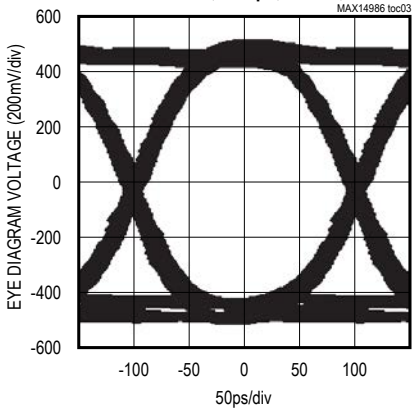
V_{IN} = 275mV$_{P-P}$, 1.5Gbps, PE = 0, EQ = 0



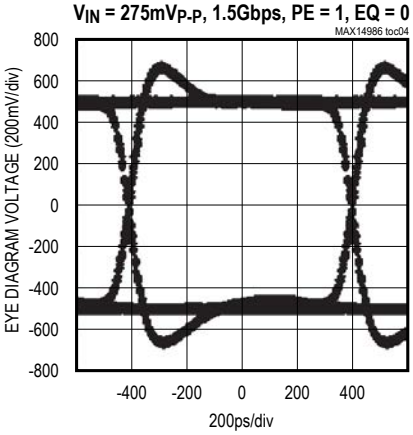
V_{IN} = 275mV$_{P-P}$, 3Gbps, PE = 0, EQ = 0



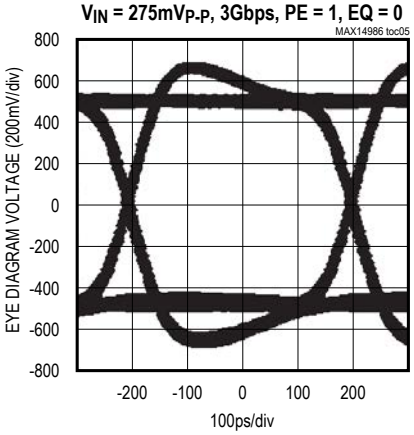
V_{IN} = 275mV$_{P-P}$, 6Gbps, PE = 0, EQ = 0



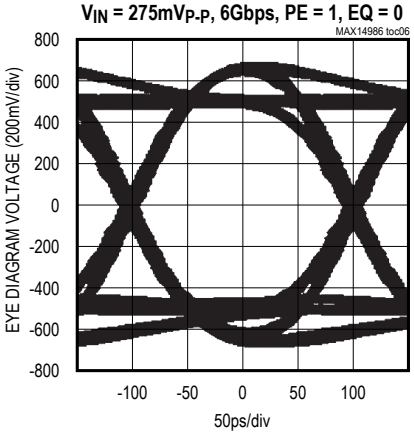
V_{IN} = 275mV$_{P-P}$, 1.5Gbps, PE = 1, EQ = 0



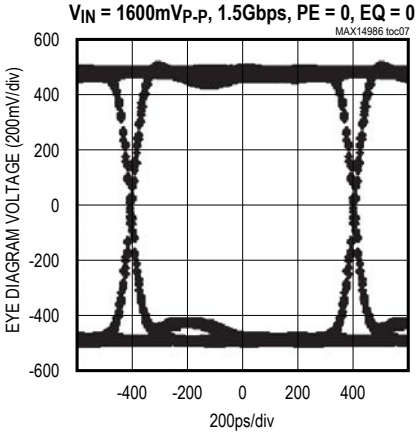
V_{IN} = 275mV$_{P-P}$, 3Gbps, PE = 1, EQ = 0



V_{IN} = 275mV$_{P-P}$, 6Gbps, PE = 1, EQ = 0



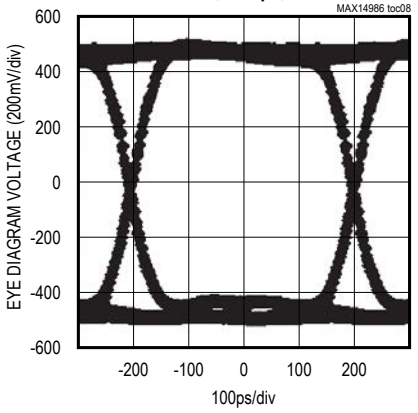
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, PE = 0, EQ = 0



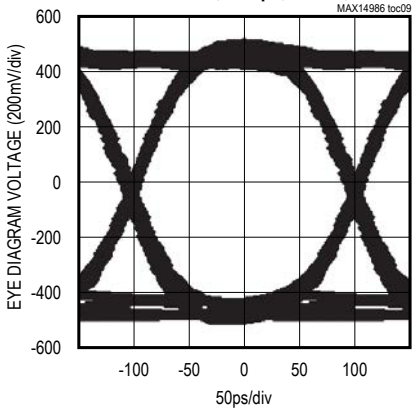
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

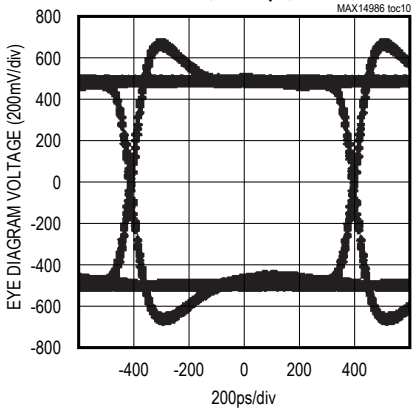
V_{IN} = 1600mV$_{P-P}$, 3Gbps, PE = 0, EQ = 0



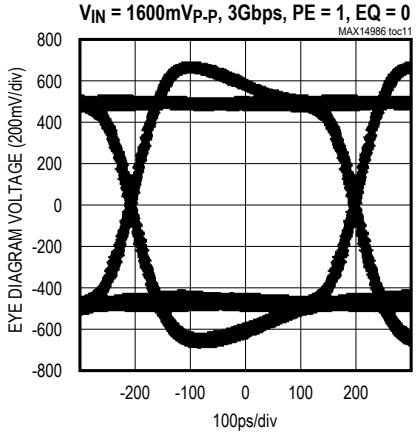
V_{IN} = 1600mV$_{P-P}$, 6Gbps, PE = 0, EQ = 0



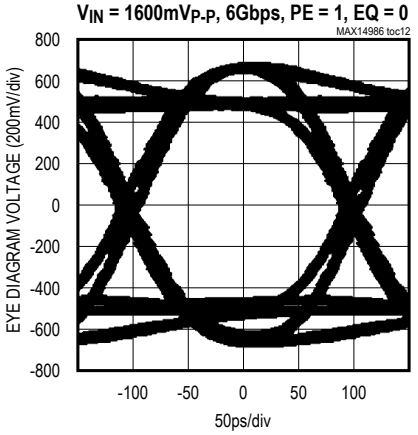
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, PE = 1, EQ = 0



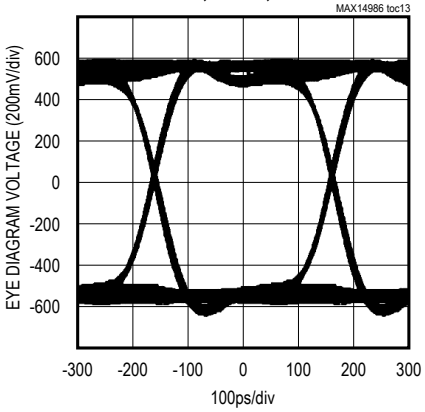
V_{IN} = 1600mV$_{P-P}$, 3Gbps, PE = 1, EQ = 0



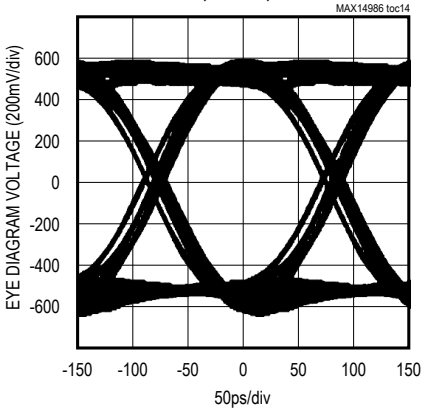
V_{IN} = 1600mV$_{P-P}$, 6Gbps, PE = 1, EQ = 0



V_{IN} = 500mV$_{P-P}$ WITH 20in FR4 STRIPLINE, 3GT/s, PE = 0, EQ = 0



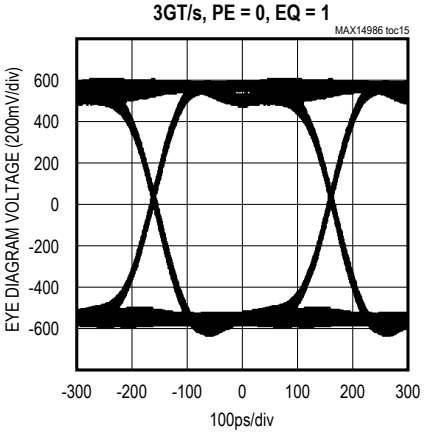
V_{IN} = 500mV$_{P-P}$ WITH 20in FR4 STRIPLINE, 6GT/s, PE = 0, EQ = 0



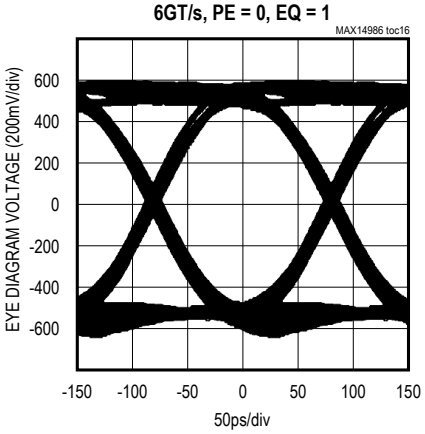
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

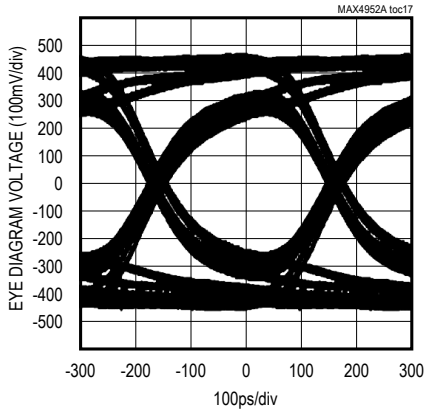
V_{IN} = 500mV$_{P-P}$ WITH 20in FR4 STRIPLINE, 3GT/s, PE = 0, EQ = 1



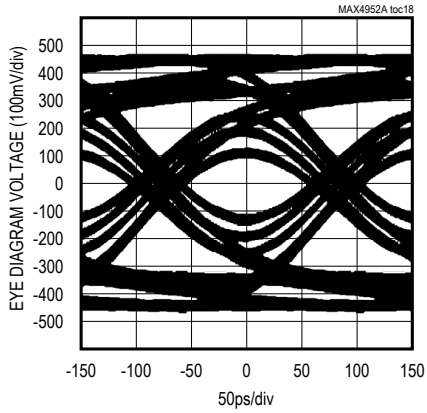
V_{IN} = 500mV$_{P-P}$ WITH 20in FR4 STRIPLINE, 6GT/s, PE = 0, EQ = 1



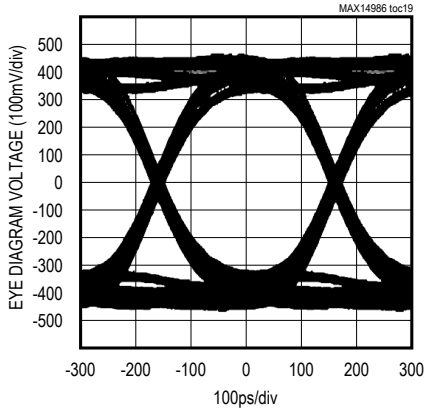
V_{IN} = 275mV$_{P-P}$, 3GT/s, PE = 0, EQ = 0, OUTPUT AFTER 20in FR4 STRIPLINE



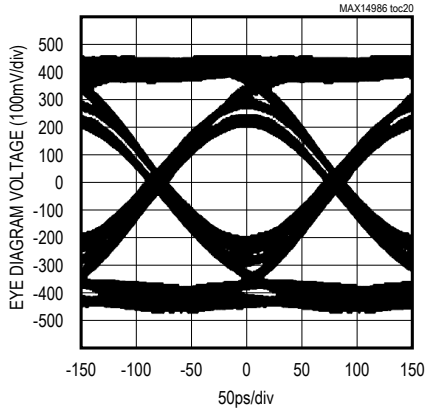
V_{IN} = 275mV$_{P-P}$, 6GT/s, PE = 0, EQ = 0, OUTPUT AFTER 20in FR4 STRIPLINE



V_{IN} = 275mV$_{P-P}$, 3GT/s, PE = 1, EQ = 0, OUTPUT AFTER 20in FR4 STRIPLINE



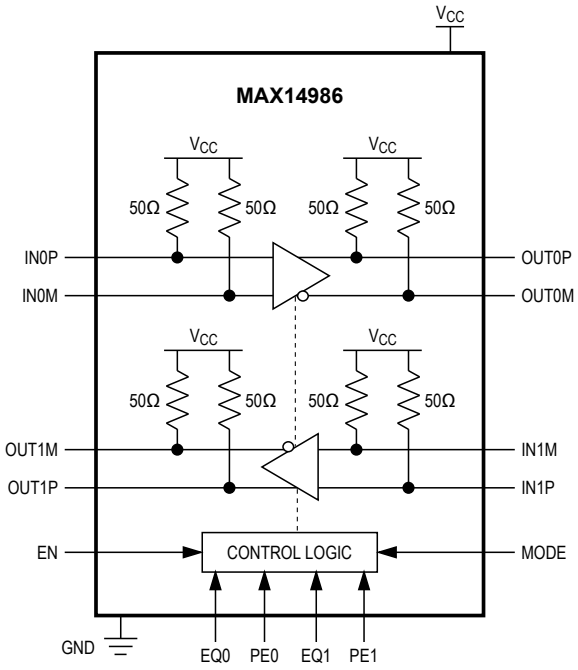
V_{IN} = 275mV$_{P-P}$, 6GT/s, PE = 1, EQ = 0, OUTPUT AFTER 20in FR4 STRIPLINE



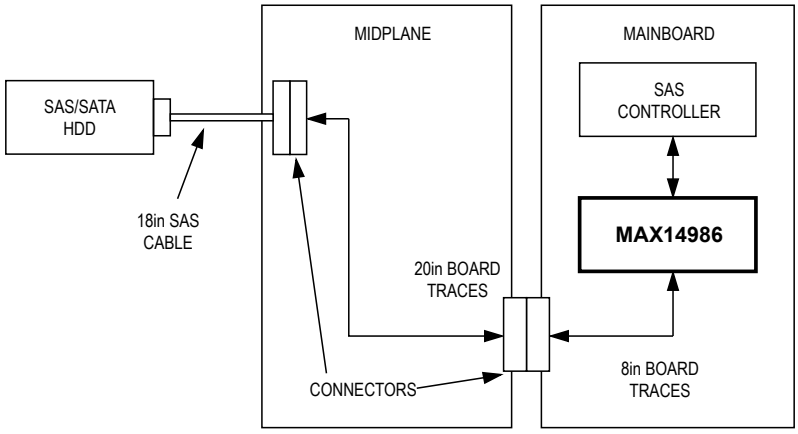
Pin Description

PIN	NAME	FUNCTION
1, 9, 16, 24	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} to GND with 2.2µF and 0.01µF capacitors in parallel as close as possible to the device, recommended on each V_{CC} pin.
2, 5, 8, 17, 20, 23, 25–28	GND	Ground
3	IN0P	Noninverting Input 0
4	IN0M	Inverting Input 0
6	OUT1P	Noninverting Output 1
7	OUT1M	Inverting Output 1
10	EN	Active-High Enable Input. Drive EN low to put device in standby mode. Drive EN high for normal operation. EN is internally pulled down.
11	EQ0	Channel 0 Input Equalizer Logic Input. EQ0 is internally pulled down.
12	PE0	Channel 0 Output Preemphasis Logic Input. PE0 is internally pulled down.
13	EQ1	Channel 1 Input Equalizer Logic Input. EQ1 is internally pulled down.
14	PE1	Channel 1 Output Preemphasis Logic Input. PE1 is internally pulled down.
15	MODE	OOB Threshold Logic Input. MODE is internally pulled down.
18	IN1M	Inverting Input 1
19	IN1P	Noninverting Input 1
21	OUT0M	Inverting Output 0
22	OUT0P	Noninverting Output 0
—	EP	Exposed Pad. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation. Do not use EP as the sole ground connection.

Functional Diagram



Typical Application Circuit



Detailed Description

The MAX14986 consists of two identical redrivers with input equalization and output preemphasis useful for SAS or SATA signals up to 6.0GT/s.

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V_{CC} (see the *Functional Diagram*) and must be AC-coupled using 12nF (max) capacitors to the SAS/SATA controller IC and SAS/SATA device for proper operation.

Enable Input (EN)

The MAX14986 features an active-high enable input (EN). EN has an internal pulldown resistor of 70kΩ (typ). When EN is driven low or left unconnected, the MAX14986 enters low-power standby mode and the redrivers are disabled. Drive EN high for normal operation.

Out-of-Band Threshold Selector (MODE)

The MAX14986 provides full OOB signal support through high-speed amplitude detection circuitry. OOB differential input signals less than the internal OOB threshold ($V_{SQ-DIFF}$) are detected as off and not passed to the output. This prevents the system from responding to unwanted noise. OOB differential input signals higher than $V_{SQ-DIFF}$ are detected as on and passed to the output, allowing OOB signals to transmit through the MAX14986. The logic level of the MODE input sets $V_{SQ-DIFF}$ for either SAS or SATA OOB signals (see Table 1). MODE has an internal pulldown resistor of 70kΩ (typ).

Table 1. Out-of-Band Logic Threshold (MODE)

MODE	OOB MODE
0	SAS
1	SATA

Input Equalization (EQ0, EQ1)

The MAX14986 features control logic inputs (EQ0, EQ1) to enable input equalization on either channel, providing 3dB of boost (see Note 4 in the *Electrical Characteristics* table). Drive EQ0 or EQ1 high to enable input equalization on channel 0 or channel 1. Drive EQ0 or EQ1 low to disable input equalization on channel 0 or channel 1 (see Table 2). EQ0 and EQ1 have internal pulldown resistors of 70kΩ (typ).

Output Preemphasis (PE0, PE1)

The MAX14986 features control logic inputs (PE0, PE1) to enable output preemphasis on either channel, providing 3dB of boost. The MAX14986 uses true preemphasis, so the transition signal is increased after a changing bit, thus increasing the total energy content of the signal when employed. Drive PE0 or PE1 high to enable output preemphasis on channel 0 or channel 1. Drive PE0 or PE1 low to disable output preemphasis on channel 0 or channel 1 (see Table 3). PE0 and PE1 have internal pulldown resistors of 70kΩ (typ).

Table 2. Input Equalization (EQ0, EQ1)

EQ1	EQ0	CHANNEL 1 (dB)	CHANNEL 0 (dB)
0	0	0	0
0	1	0	3 (typ)
1	0	3 (typ)	0
1	1	3 (typ)	3 (typ)

Table 3. Output Preemphasis (PE0, PE1)

PE1	PE0	CHANNEL 1 (dB)	CHANNEL 0 (dB)
0	0	0	0
0	1	0	3 (typ)
1	0	3 (typ)	0
1	1	3 (typ)	3 (typ)

Applications Information

Exposed Pad Package

The exposed pad, 28-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX14986 must be soldered to GND for proper thermal and electrical performance. For more information on exposed pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages.*

Layout

Use controlled-impedance transmission lines to interface with high-speed inputs and outputs of the MAX14986. Place power-supply 2.2µF and 0.01µF bypass capacitors as close as possible to V_{CC}, recommended on each V_{CC} pin.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying signals, especially if the signal is not current limited.

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14986ETI+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN	T283555+1	**21-0184**	**90-0123**