



# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

**MAX15018/MAX15019**

## General Description

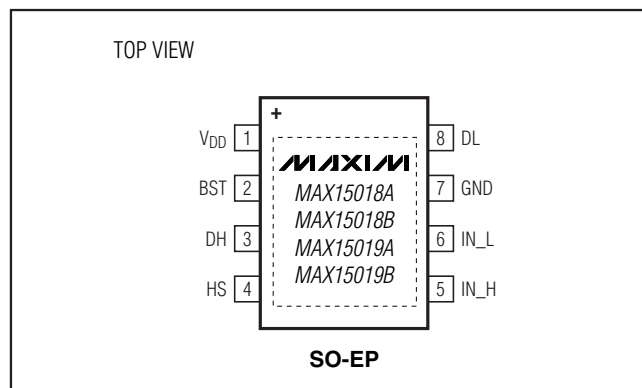
The MAX15018A/MAX15018B/MAX15019A/MAX15019B high-frequency, 125V half-bridge, n-channel MOSFET drivers drive high- and low-side MOSFETs in high-voltage applications. These drivers are independently controlled, and their 35ns (typ) propagation delay, from input to output, are matched to within 2ns (typ). The high-voltage operation with very low and matched propagation delay between drivers, and high source-/sink-current capabilities in a thermally enhanced package make these devices suitable for high-power, high-frequency telecom power converters. The 125V maximum input voltage provides plenty of margin over the 100V input transient requirement of telecom standards. A reliable on-chip bootstrap diode connected between  $V_{DD}$  and BST eliminates the need for an external discrete diode.

The MAX15018A/MAX15019A both offer noninverting drivers. The MAX15018B/MAX15019B offer a noninverting high-side driver and an inverting low-side driver (see the *Selector Guide*.) The MAX15018\_ feature CMOS ( $V_{DD}/2$ ) logic inputs. The MAX15019\_ feature TTL-logic inputs. The drivers are available in the industry-standard 8-pin SO footprint and pin configuration with a thermally enhanced 8-pin SO package. All devices operate over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  automotive temperature range.

## Applications

Telecom Power Supplies  
Synchronous Buck DC-to-DC Converters  
Half-Bridge, Full-Bridge, and Two-Switch Forward Converters  
Power-Supply Modules  
Motor Control

## Pin Configuration



## Features

- ◆ HIP2100IB/HIP2101IB Pin Compatible (MAX15018A/MAX15019A)
- ◆ Up to 125V  $V_{IN}$  Operation
- ◆ 8V to 12.6V  $V_{DD}$  Input Supply Range
- ◆ 3A Peak Source and Sink Current
- ◆ 35ns Propagation Delay
- ◆ Guaranteed 8ns or Less Propagation Delay Matching Between High- and Low-Side Drivers
- ◆ Both Noninverting/Noninverting and Noninverting/Inverting Logic-Input Versions Available
- ◆ Up to 15V Logic Inputs, Independent of  $V_{DD}$  Supply Voltage
- ◆ Low 8pF Input Capacitance
- ◆ Available in CMOS ( $V_{DD}/2$ ) or TTL Logic-Level Inputs with Hysteresis
- ◆ Available in a Space-Saving, Thermally Enhanced 8-Pin SO-EP Package

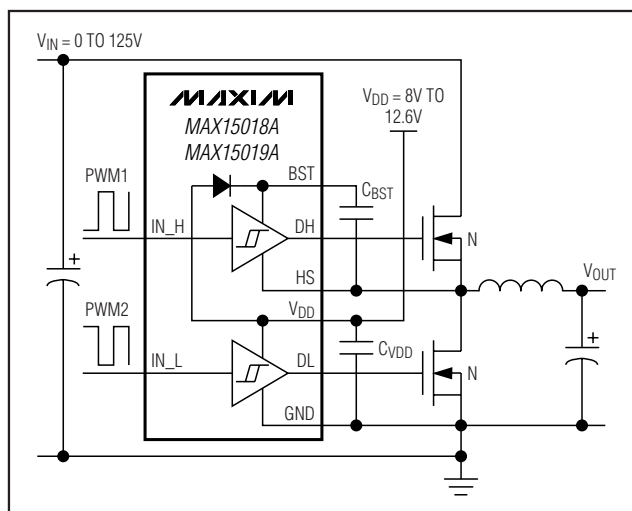
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15018AASA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 SO-EP*
MAX15018BASA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 SO-EP*
MAX15019AASA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 SO-EP*
MAX15019BASA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 SO-EP*

+ Denotes a lead-free/RoHS-compliant package.

\*EP = Exposed pad. Internally connected to GND.

## Typical Operating Circuit



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## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND	-0.3V to +15V
IN_H, IN_L to GND	-0.3V to +15V
DL to GND	-0.3V to (V <sub>DD</sub> + 0.3V)
DH to HS	-0.3V to (V <sub>DD</sub> + 0.3V)
BST to HS	-0.3V to +15V
HS to GND (repetitive transient)	-5V to +130V
HS dv/dt to GND	.50V/ns

Continuous Power Dissipation (T <sub>A</sub> = +70°C) Single and Multilayer Board 8-Pin SO-EP (derate 23.8mW/°C above +70°C)*	1.904W
θ <sub>JC</sub>	6°C/W
Operating Temperature	-40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

\*As per JEDEC Standard 51 (Single-Layer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = V<sub>BST</sub> = 8V to 12.6V, V<sub>HS</sub> = V<sub>GND</sub> = 0V, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>DD</sub> = V<sub>BST</sub> = 12V and T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Operating Supply Voltage	V <sub>DD</sub>		8.0		12.6	V
V <sub>DD</sub> Quiescent Supply Current	I <sub>DDQ</sub>	IN_H and IN_L are unconnected (no switching)	MAX15018A/ MAX15018B	65	130	μA
			MAX15019A/ MAX15019B	95	190	
V <sub>DD</sub> Operating Supply Current	I <sub>DDO</sub>	f <sub>sw</sub> = 500kHz, V <sub>DD</sub> = 12V, no capacitive load		2.75	3.75	mA
BST Quiescent Supply Current	I <sub>BSTQ</sub>	IN_H and IN_L are unconnected (no switching)		95	190	μA
BST Operating Supply Current	I <sub>BSTO</sub>	f <sub>sw</sub> = 500kHz, V <sub>BST</sub> - V <sub>HS</sub> = 12V, no capacitive load		2.75	3.75	mA
UVLO (V <sub>DD</sub> to GND)	V <sub>DD_UVLO</sub>	V <sub>DD</sub> rising	6.5	7.3	8	V
UVLO (BST to HS)	V <sub>BST_UVLO</sub>	V <sub>BST</sub> rising	6.2	6.9	7.6	V
UVLO Hysteresis				0.5		V
<b>LOGIC INPUT</b>						
Input-Logic High	V <sub>IH</sub>	MAX15018A/MAX15018B (CMOS)	0.67 x V <sub>DD</sub>			V
		MAX15019A/MAX15019B (TTL)	2			
Input-Logic Low	V <sub>IL</sub>	MAX15018A/MAX15018B (CMOS)		0.33 x V <sub>DD</sub>		V
		MAX15019A/MAX15019B (TTL)		0.8		
Logic-Input Hysteresis	V <sub>HYS</sub>	MAX15018A/MAX15018B (CMOS)	1.65			V
		MAX15019A/MAX15019B (TTL)	0.4			

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = V_{BST} = 8V$  to  $12.6V$ ,  $V_{HS} = V_{GND} = 0V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD} = V_{BST} = 12V$  and  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic-Input Current	$I_{IN\_}$	IN_H = IN_L = GND (MAX15018A/MAX15019A)		-1		+1	$\mu A$
		IN_H = GND, IN_L = $V_{DD}$ (MAX15018B/MAX15019B)					
Input Resistance	$R_{IN\_}$	IN_L to GND (MAX15018A/MAX15019A)			5001		$k\Omega$
		IN_L to $V_{DD}$ (MAX15018B/MAX15019B)					
		IN_H to GND					
Input Capacitance	$C_{IN\_}$				8		$pF$
<b>HIGH-SIDE GATE DRIVER</b>							
HS Maximum Voltage	$V_{HS\_MAX}$			125			V
BST Maximum Voltage	$V_{BST\_MAX}$			140			V
Driver Output Resistance	$R_{ON\_HP}$	$(V_{BST} - V_{HS}) = 12V$ , $I_{DH} = 100mA$ (sourcing)	$T_A = +25^\circ C$	1.75	2.4	$\Omega$	
			$T_A = +125^\circ C$	2.3	3.0		
	$R_{ON\_HN}$	$(V_{BST} - V_{HS}) = 12V$ , $I_{DH} = 100mA$ (sinking)	$T_A = +25^\circ C$	1.1	1.75		
			$T_A = +125^\circ C$	1.6	2.25		
Power-Off Pulldown Clamp Voltage		$V_{BST} = 0V$ or unconnected, $I_{DH} = 1mA$ (sinking)		0.88	1.2		V
Peak Output Current	$I_{PK\_HP}$	$V_{DH} = 0V$		3			A
	$I_{PK\_HN}$	$V_{DH} = 12V$		3			
<b>LOW-SIDE GATE DRIVER</b>							
Driver Output Resistance	$R_{ON\_LP}$	$V_{DD} = 12V$ , $I_{DL} = 100mA$ (sourcing)	$T_A = +25^\circ C$	1.75	2.4	$\Omega$	
			$T_A = +125^\circ C$	2.3	3.0		
	$R_{ON\_LN}$	$V_{DD} = 12V$ , $I_{DL} = 100mA$ (sinking)	$T_A = +25^\circ C$	1.1	1.75		
			$T_A = +125^\circ C$	1.6	2.25		
Power-Off Pulldown Clamp Voltage		$V_{DD} = 0V$ or unconnected, $I_{DL} = 1mA$ (sinking)		0.88	1.2		V
Peak Output Current	$I_{PK\_LP}$	$V_{DL} = 0V$		3			A
	$I_{PK\_LN}$	$V_{DL} = 12V$		3			
<b>INTERNAL BOOTSTRAP DIODE</b>							
Forward Voltage Drop	$V_F$	$I_{BST} = 100mA$		0.9	1.1		V
Turn-On and Turn-Off Time	$t_{RR}$	$I_{BST} = 100mA$		40			ns

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = V_{BST} = 8V$  to  $12.6V$ ,  $V_{HS} = V_{GND} = 0V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD} = V_{BST} = 12V$  and  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>SWITCHING CHARACTERISTICS FOR HIGH- AND LOW-SIDE DRIVERS (<math>V_{DD} = V_{BST} = +12V</math>)</b>							
Rise Time	$t_R$	No $C_L$		1		ns	
		$C_L = 1000pF$		5			
		$C_L = 5000pF$		25			
		$C_L = 10,000pF$		50			
Fall Time	$t_F$	No $C_L$		1		ns	
		$C_L = 1000pF$		5			
		$C_L = 5000pF$		20			
		$C_L = 10,000pF$		40			
Turn-On Propagation Delay Time	$t_{D\_ON}$	Figure 1, $C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	33	60	ns	
			MAX15019A/ MAX15019B (TTL)	36	66		
Turn-Off Propagation Delay Time	$t_{D\_OFF}$	Figure 1, $C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	30	55	ns	
			MAX15019A/ MAX15019B (TTL)	36	66		
Delay Matching Between High-Side Turn-On to Low-Side Turn-On	$t_{MATCH1}$	$C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	1	5	ns	
			MAX15019A/ MAX15019B (TTL)	1	6		
Delay Matching Between High-Side Turn-Off to Low-Side Turn-Off	$t_{MATCH2}$	$C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	1	5	ns	
			MAX15019A/ MAX15019B (TTL)	1	6		
Delay Matching Between High-Side Turn-Off to Low-Side Turn-On	$t_{MATCH3}$	$C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	2	8	ns	
			MAX15019A/ MAX15019B (TTL)	1	6		
Delay Matching Between High-Side Turn-On to Low-Side Turn-Off	$t_{MATCH4}$	$C_L = 1000pF$ (Note 2)	MAX15018A/ MAX15018B (CMOS)	2	8	ns	
			MAX15019A/ MAX15019B (TTL)	1	6		
Minimum Input Pulse Width for Output Change	$t_{PW}$			20			ns

**Note 1:** All devices are 100% production tested at  $T_A = T_J = +125^\circ C$ . Limits over temperature are guaranteed by design and characterization.

**Note 2:** Guaranteed by design, not production tested.

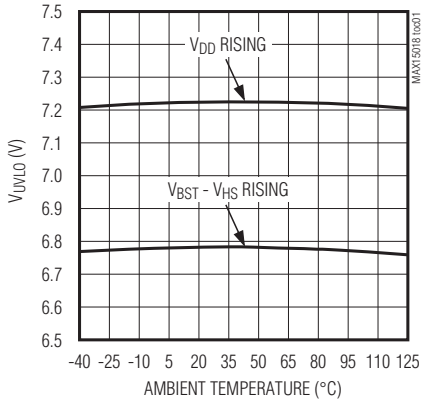
# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## Typical Operating Characteristics

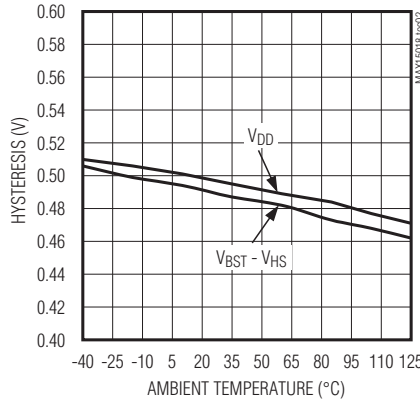
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

MAX15018/MAX15019

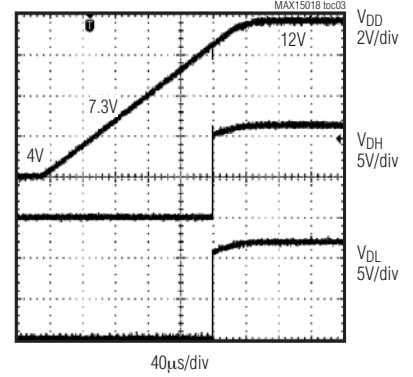
**V<sub>DD</sub> AND BST UNDERVOLTAGE LOCKOUT vs. TEMPERATURE**



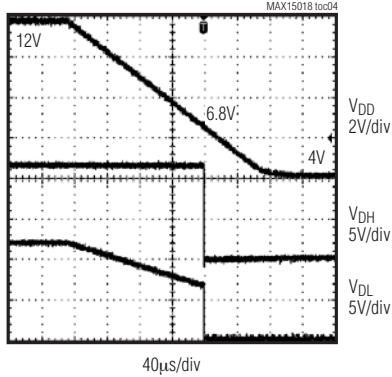
**V<sub>DD</sub> AND BST UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE**



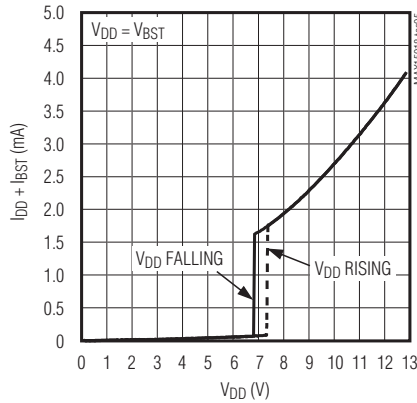
**UNDERVOLTAGE LOCKOUT RESPONSE (V<sub>DD</sub> RISING)**



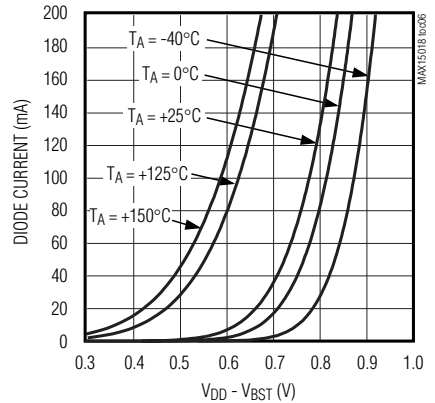
**UNDERVOLTAGE LOCKOUT RESPONSE (V<sub>DD</sub> FALLING)**



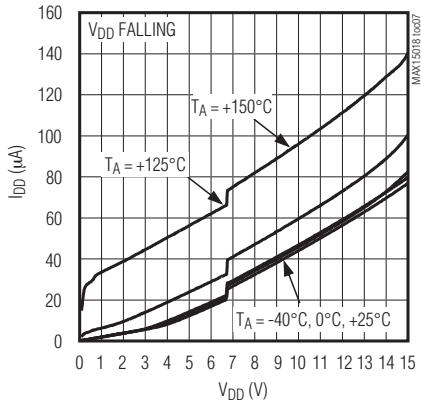
**MAX15018A I<sub>DD</sub> + I<sub>BST</sub> CURRENT vs. V<sub>DD</sub> (250kHz SWITCHING)**



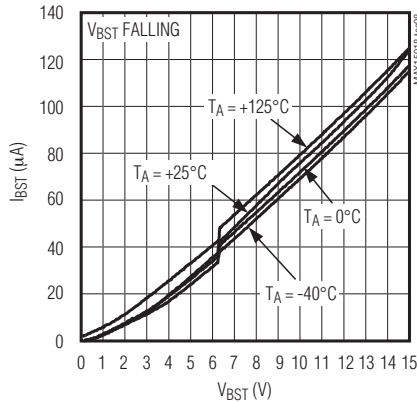
**INTERNAL BOOTSTRAP DIODE I-V CHARACTERISTICS**



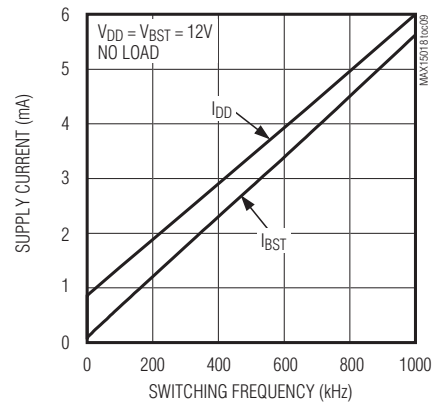
**MAX15018A V<sub>DD</sub> QUIESCENT CURRENT vs. V<sub>DD</sub> (NO SWITCHING)**



**MAX15018A BST QUIESCENT CURRENT vs. V<sub>BST</sub> (NO SWITCHING)**



**MAX15018A I<sub>DD</sub> AND I<sub>BST</sub> vs. SWITCHING FREQUENCY**

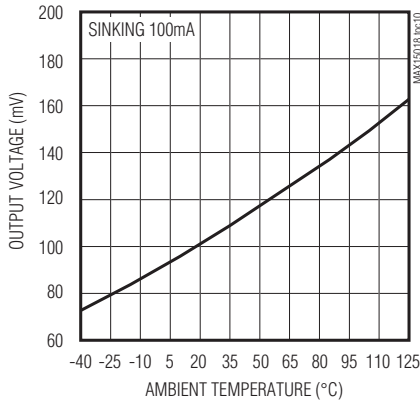


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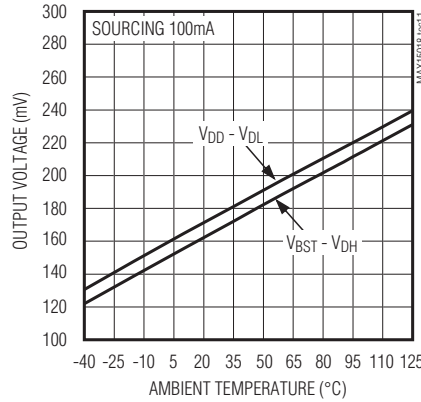
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

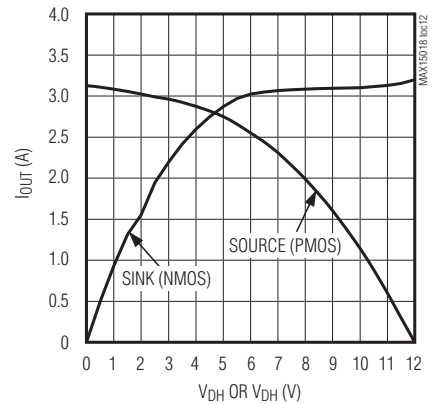
**DH OR DL OUTPUT LOW VOLTAGE vs. TEMPERATURE**



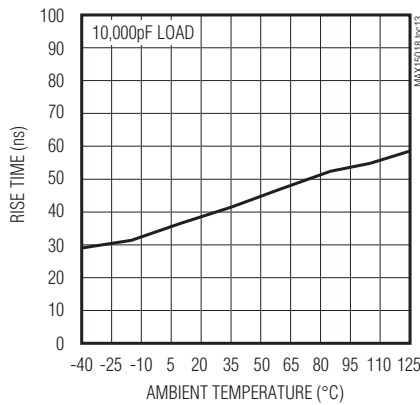
**DH AND DL OUTPUT HIGH VOLTAGE vs. TEMPERATURE**



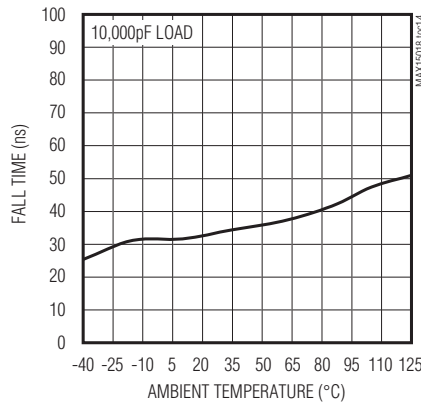
**PEAK OUTPUT CURRENT vs. OUTPUT VOLTAGE**



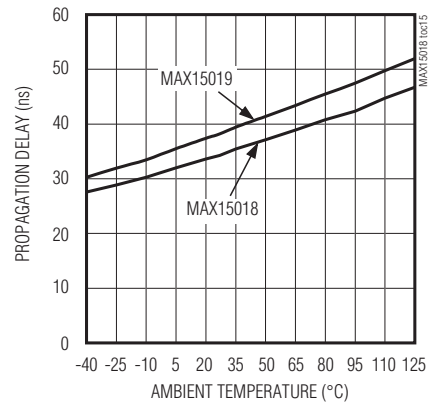
**DH OR DL OUTPUT RISE TIME vs. TEMPERATURE**



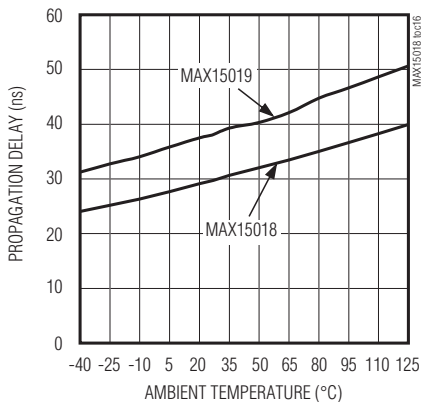
**DH OR DL OUTPUT FALL TIME vs. TEMPERATURE**



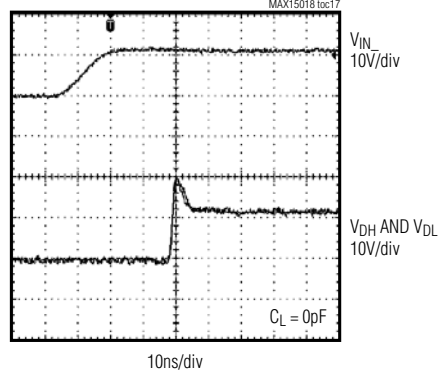
**DH OR DL RISING PROPAGATION DELAY vs. TEMPERATURE**



**DH OR DL FALLING PROPAGATION DELAY vs. TEMPERATURE**



**DELAY MATCHING (DH AND DL RISING)**

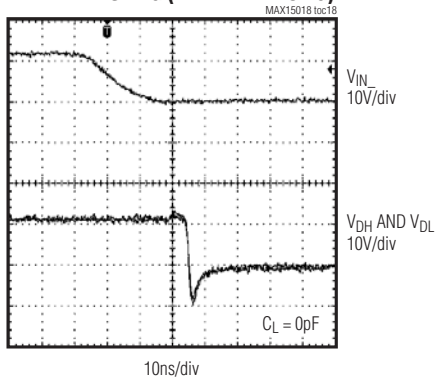


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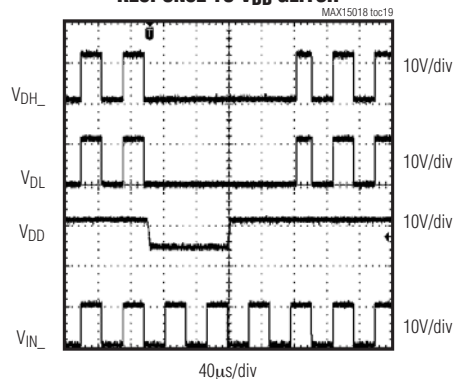
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

**DELAY MATCHING (DH AND DL RISING)**



**RESPONSE TO  $V_{DD}$  GLITCH**



MAX15018/MAX15019

## Pin Description

PIN	NAME	FUNCTION
1	$V_{DD}$	Input Supply Voltage. Valid supply voltage ranges from 8V to 12.6V. Bypass $V_{DD}$ to GND with a parallel combination of 0.1µF and 1µF ceramic capacitors as close to the IC as possible.
2	BST	Boost Flying Capacitor Connection. Connect a 0.22µF ceramic capacitor from BST to HS as close to the IC as possible for the high-side MOSFET driver supply.
3	DH	High-Side Gate Driver Output. Driver output for the high-side MOSFET gate.
4	HS	Source Connection for High-Side MOSFET. Also serves as the return for the high-side driver.
5	IN_H	High-Side Noninverting Logic Input
6	IN_L	Low-Side Noninverting (MAX15018A/MAX15019A) or Low-Side Inverting (MAX15018B/MAX15019B) Input
7	GND	Ground. Use GND as a return path to the DL driver output and the IN_H, IN_L inputs. Must be connected to ground.
8	DL	Low-Side Gate Driver Output. Driver output for the low-side MOSFET gate.
—	EP	Exposed Pad. Internally connected to GND. Externally connect the exposed pad to a large ground plane to aid in heat dissipation. Grounding EP does not substitute the requirement to connect GND to ground.

# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## Detailed Description

The MAX15018A/MAX15018B/MAX15019A/MAX15019B half-bridge, n-channel MOSFET drivers control high- and low-side MOSFETs in high-voltage, high peak-current applications and offer a high 125V voltage range that allows ample margin above the 100V transient specification of telecom standards. These drivers operate with an IC supply voltage of 8V to 12.6V, and consume only 2.75mA of supply current during typical switching operations. The MAX15018\_/MAX15019\_ provide 3A (typ) sink/source peak current per output and are capable of operating with large capacitive loads and with switching frequencies near 1MHz.

These drivers are intended to be used to drive the high-side MOSFET without requiring an isolation device such as an optocoupler or a drive transformer. The high-side driver is controlled by a TTL/CMOS logic signal referenced to ground and is powered by a bootstrap circuit formed by an integrated diode and an external capacitor. Undervoltage lockout (UVLO) protection is provided for both the high- and low-side driver supplies (BST and V<sub>DD</sub>) and includes a UVLO hysteresis of 0.5V (typ).

The drivers are independently controlled and feature exceptionally fast switching times, very short propagation delays (35ns typ), and matched propagation delay-times (2ns typ) between drivers, making them ideally suited for high-frequency applications. Internal logic circuitry prevents shoot-through during output state changes and minimizes package power dissipation.

These devices are available with CMOS (V<sub>DD</sub>/2) or TTL logic-level inputs. The MAX15018A/MAX15018B accept CMOS input logic levels, while the MAX15019A/MAX15019B accept TTL input logic levels. For both versions, the logic inputs are protected against voltage spikes up to +15V, regardless of V<sub>DD</sub>. See the *Driver Logic Inputs (IN\_H, IN\_L)* section.

The MAX15018\_/MAX15019\_ are available with both high-side and low-side noninverting logic inputs or with noninverting high-side and inverting low-side logic inputs. See the *Functional Diagrams* and *Selector Guide*. The MAX15018A and MAX15019A are pin-for-pin replacements for the HIP2100IB and HIP2101IB, respectively.

The MAX15018\_/MAX15019\_ are available in a space-saving, high-power, 8-pin SO-EP package that can dissipate up to 1.95W at +70°C. All devices operate over the -40°C to +125°C automotive temperature range.

## Undervoltage Lockout

Both the high- and low-side drivers feature separate UVLO protection that monitors each driver's input supply voltage (BST and V<sub>DD</sub>). The low-side driver UVLO threshold (V<sub>DD\_UVLO</sub>) is referenced to GND and pulls both driver outputs low when V<sub>DD</sub> falls below 7.3V (typ). The high-side driver UVLO threshold (V<sub>BST\_UVLO</sub>) is referenced to HS, and only pulls DH low when V<sub>BST</sub> falls below 6.9V (typ) with respect to HS. After the IC is first energized, and once V<sub>DD</sub> rises above its UVLO threshold, DL starts switching and either follows the IN\_L logic input (MAX15018A/MAX15019A) or is inverted with reference to the IN\_L logic input (MAX15018B/MAX15019B). At this time, the bootstrap capacitor is not charged, and DH does not switch since the BST-to-HS voltage is below V<sub>BST\_UVLO</sub>. Within a short time following engagement of low-side switching, C<sub>BST</sub> charges through V<sub>DD</sub> and causes V<sub>BST</sub> to exceed V<sub>BST\_UVLO</sub>. DH then starts switching and follows IN\_H. For synchronous buck and half-bridge converter topologies, the bootstrap capacitor can charge up in one cycle. Normal operation then begins in a few microseconds after the BST-to-HS voltage exceeds V<sub>BST\_UVLO</sub>. In the two-switch forward topology, C<sub>BST</sub> takes more time (a few hundred microseconds) to charge and increase its voltage above V<sub>BST\_UVLO</sub>. The typical hysteresis for both UVLO thresholds is 0.5V. The bootstrap capacitor value should be selected carefully to avoid oscillations during turn-on and turn-off at the DH output. Choose a capacitor value 20 times greater than the total gate capacitance of the MOSFET. Use a low ESR-type X7R dielectric ceramic capacitor at BST (typically a 0.1μF ceramic is adequate) and a parallel combination of 1μF and 0.1μF ceramic capacitors from V<sub>DD</sub> to GND. The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of C<sub>BST</sub>, I<sub>BST</sub> (190μA, max), and V<sub>BST\_UVLO</sub>.



# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

MAX15018/MAX15019

## Output Driver

The MAX15018\_/MAX15019\_ drivers contain low on-resistance p-channel and n-channel devices in a totem pole configuration for the driver output stage. This allows for rapid turn-on and turn-off of high gate-charge ( $Q_g$ ) external switching MOSFETs.

The drivers exhibit low drain-to-source resistance ( $R_{DS\_ON}$ ), which decreases for higher values of  $V_{DD}$  and for lower operating temperatures. Lower  $R_{DS\_ON}$  means higher source and sink currents from the IC, and results in faster switching speeds, since the external MOSFET gate capacitance will charge and discharge at a quicker rate. The peak source and sink current provided by the drivers is typically 3A.

Propagation delay from the logic inputs to the driver outputs is matched to within 8ns (max) between the low-side and high-side drivers. Turn-on and turn-off propagation delays are typically 35ns and 36ns. See Figure 1. The internal drivers also contain break-before-make logic to eliminate shoot-through conditions that would cause unnecessarily high operating supply currents, efficiency reduction, and voltage spikes at  $V_{DD}$ .

Voltage at DL is approximately equal to  $V_{DD}$  when in a high state, and zero when in a low state. Voltage from

DH to HS is approximately equal to  $V_{DD}$  minus the diode drop of the integrated bootstrap diode when in a high state, and zero when in a low state. The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of the bootstrap capacitor ( $C_{BST}$ ),  $I_{BST}$  (190 $\mu$ A max), and  $V_{BST\_UVLO}$ .

## Integrated Bootstrap Diode

An integrated diode between  $V_{DD}$  and BST is used in conjunction with an external bootstrap capacitor ( $C_{BST}$ ) to provide the voltage required to turn on the high-side MOSFET (see the *Typical Operating Circuit*). The internal diode charges the bootstrap capacitor from  $V_{DD}$  when the low-side switch is on, and isolates  $V_{DD}$  when HS is pulled high when the high-side driver turns on. The internal bootstrap diode has a typical forward voltage drop of 0.9V and has a 40ns (typ) turn-off/on time. The turn-off time (reverse recovery time) depends on the reverse-recovery current and can be as low as 10ns. If a lower diode voltage-drop between  $V_{DD}$  and BST is needed, connect an external Schottky diode between  $V_{DD}$  and BST.

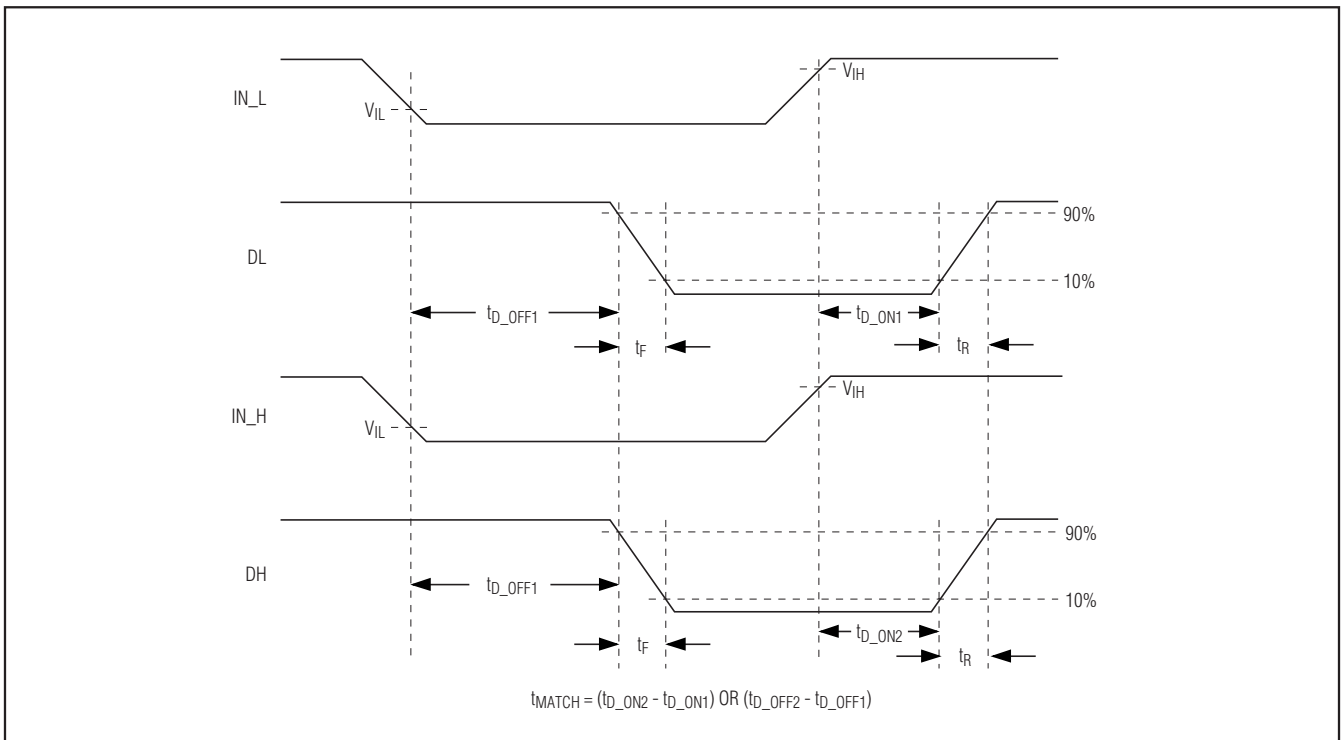


Figure 1. Timing Characteristics of Logic Inputs (MAX15018A/MAX15019A)

# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## Bootstrap Capacitor

The bootstrap capacitor is used to ensure adequate charge is available to switch the high-side MOSFET. This capacitor is charged from  $V_{DD}$  through the internal bootstrap diode when the low-side MOSFET is on. The bootstrap capacitor value should be selected carefully to avoid oscillations during turn-on and turn-off at the DH output. Choose a capacitor value approximately 20 times greater than the total gate capacitance of the MOSFET being switched. Use a low-ESR, X7R-type dielectric ceramic capacitor (typically a 0.1 $\mu$ F ceramic is adequate). The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of  $C_{BST}$ ,  $I_{BST}$  (190 $\mu$ A max), and  $V_{BST\_UVLO}$ . Note that the bootstrap capacitor requires time to charge up to  $V_{DD}$ , according to the time constant of the charging loop through the lower MOSFET (see the *Typical Operating Circuit*). Ensure that the lower MOSFET is on for at least the minimum time required to charge  $C_{BST}$ .

## Driver Logic Inputs (IN\_H, IN\_L)

The MAX15018\_ are CMOS ( $V_{DD}/2$ ) logic-input drivers, and the MAX15019\_ are TTL-compatible logic-input drivers. The required logic-input levels are independent of  $V_{DD}$ . For example, the IC can be powered by a 10V supply while the logic inputs are provided from 12V CMOS logic. Additionally, the logic inputs are protected against voltage spikes up to 15V, regardless of  $V_{DD}$  voltage. The TTL and CMOS logic inputs have 400mV and 1.6V hysteresis, respectively, to avoid double pulsing during signal transition. The logic inputs are high-impedance pins (500k $\Omega$  typ) and should not be left unconnected to ensure the input logic state is at a known level. With the logic inputs unconnected, the DH and DL outputs pull low as  $V_{DD}$  rises up above the UVLO threshold. The PWM output from the controller must assume a proper state while powering up the device.

## Applications Information

### Supply Bypassing and Grounding

Careful attention is required when choosing the bypassing and grounding scheme of the MAX15018\_/MAX15019\_. Peak supply and output currents may

exceed 6A when both drivers are simultaneously driving large external capacitive loads in phase. Supply drops and ground shifts create forms of negative feedback for inverting topologies and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the  $V_{DD}$ , DH, DL, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX15018\_/MAX15019\_ with any capacitive load. Place one or more 0.1 $\mu$ F ceramic capacitors in parallel from  $V_{DD}$  to GND as close as possible to the device to bypass the input supply. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFETs as close as possible to the MAX15018\_/MAX15019\_ to reduce trace length and further minimize board inductance and AC path resistance.

### Power Dissipation

Power dissipation in the MAX15018\_/MAX15019\_ is primarily due to power loss in the internal boost diode and the internal nMOS and pMOS FETS. For capacitive loads, the total power dissipation for the device is:

$$P_D = (C_L \times V_{DD}^2 \times f_{SW}) + (I_{VDDO} + I_{BSTO}) \times V_{DD}$$

where  $C_L$  is the combined capacitive load at DH and DL,  $V_{DD}$  is the supply voltage, and  $f_{SW}$  is the switching frequency of the IC.  $P_D$  includes the power dissipated in the internal bootstrap diode ( $P_{DIODE}$ ). The internal power dissipation reduces by  $P_{DIODE}$ , if an external bootstrap Schottky diode is used. The power dissipation in the internal boost diode (when driving a capacitive load) will be the charge through the diode per switching period multiplied by the maximum diode forward voltage drop ( $V_F = 1V$ ) as given in the following equation.

$$P_{DIODE} = C_{DH} \times (V_{DD} - 1) \times f_{SW} \times V_F$$

where  $C_{DH}$  is the capacitive load at DH,  $V_{DD}$  is the supply voltage,  $f_{SW}$  is the switching frequency of the converter,  $V_F$  is the maximum diode forward voltage drop.

The total power dissipation when using the internal boost diode will be  $P_D$  and, when using an external Schottky diode, will be  $P_D - P_{DIODE}$ . The total power dissipated in the device must be kept below the maximum of 1.95W for the 8-pin SO with exposed pad at  $T_A = +70^\circ\text{C}$  ambient.

# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

MAX15018/MAX15019

## Layout Information

The MAX15018\_/MAX15019\_ drivers source and sink large currents to create very fast rise and fall edges at the gates of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PCB layout guidelines when designing with the MAX15018\_/MAX15019\_:

- It is important that the  $V_{DD}$  voltage (with respect to ground) or BST voltage (with respect to HS) does not exceed 15V. Voltage spikes higher than 15V from  $V_{DD}$  to GND or from BST to HS can damage the device. Place one or more low-ESL 0.1 $\mu$ F decoupling ceramic capacitors from  $V_{DD}$  to GND and from BST to HS as close as possible to the part. The ceramic decoupling capacitors should be at least 20 times the gate capacitance being driven.
- There are two AC current loops formed between the IC and the gate of the MOSFET being driven. The

MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from the MOSFET driver output (DL or DH) to the MOSFET gate, to the MOSFET source, and to the return terminal of the MOSFET driver (either GND or HS). When the gate of the MOSFET is being pulled high, the active current loop is from the MOSFET driver output, (DL or DH), to the MOSFET gate, to the MOSFET source, to the return terminal of the drivers decoupling capacitor, to the positive terminal of the decoupling capacitor, and to the supply connection of the MOSFET driver. The decoupling capacitor will be either  $C_{BST}$  for the high-side MOSFET or the  $V_{DD}$  decoupling capacitor for the low-side MOSFET. Care must be taken to minimize the physical distance and the impedance of these AC current paths.

- Solder the exposed pad of the 8-pin SO-EP package to a large copper plane to achieve the rated power dissipation.

## Typical Application Circuits

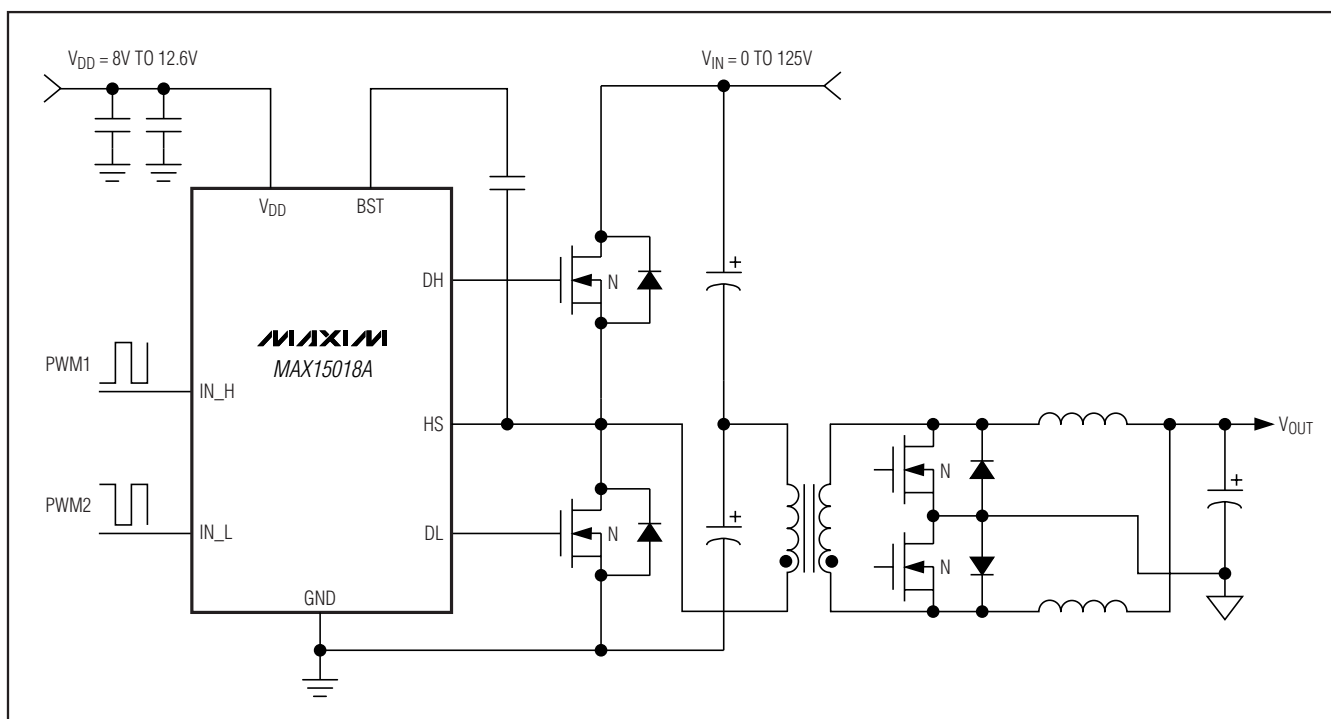


Figure 2. Half-Bridge Converter Application with Secondary-Side Synchronous Rectification

# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## Typical Application Circuits (continued)

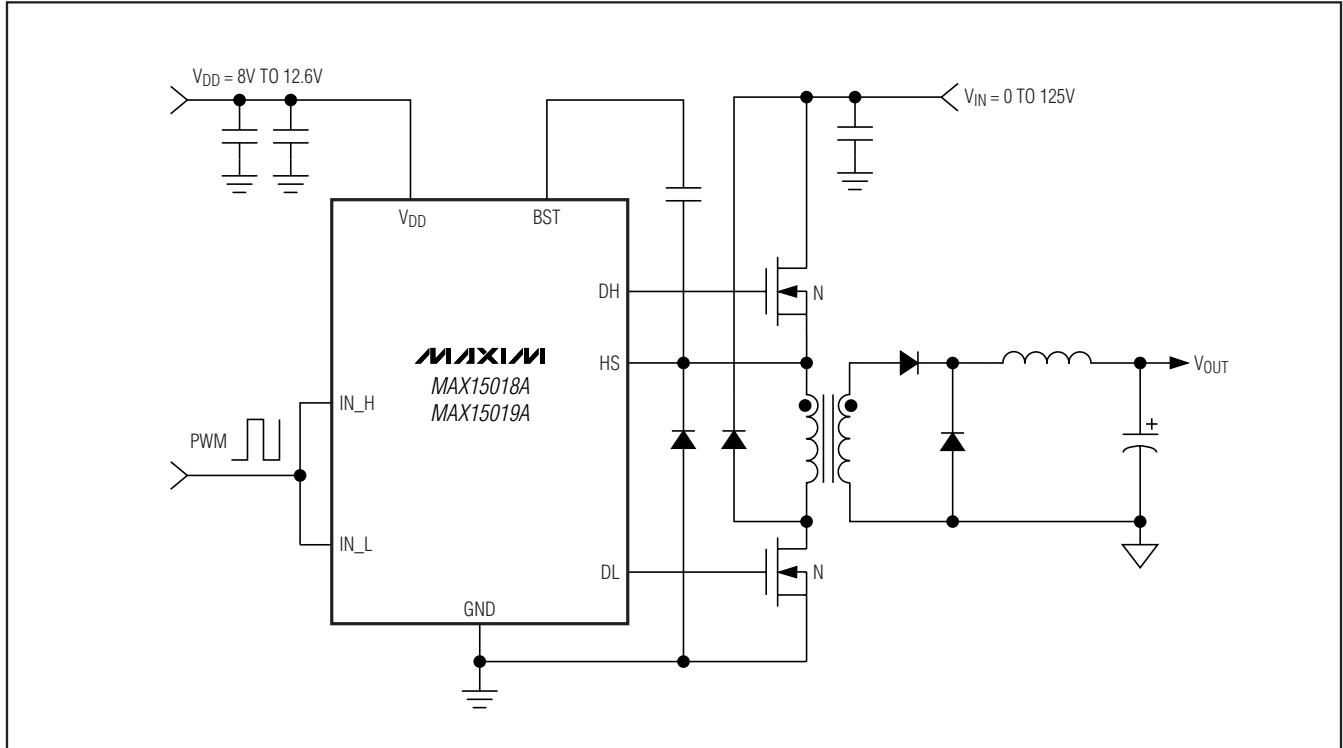
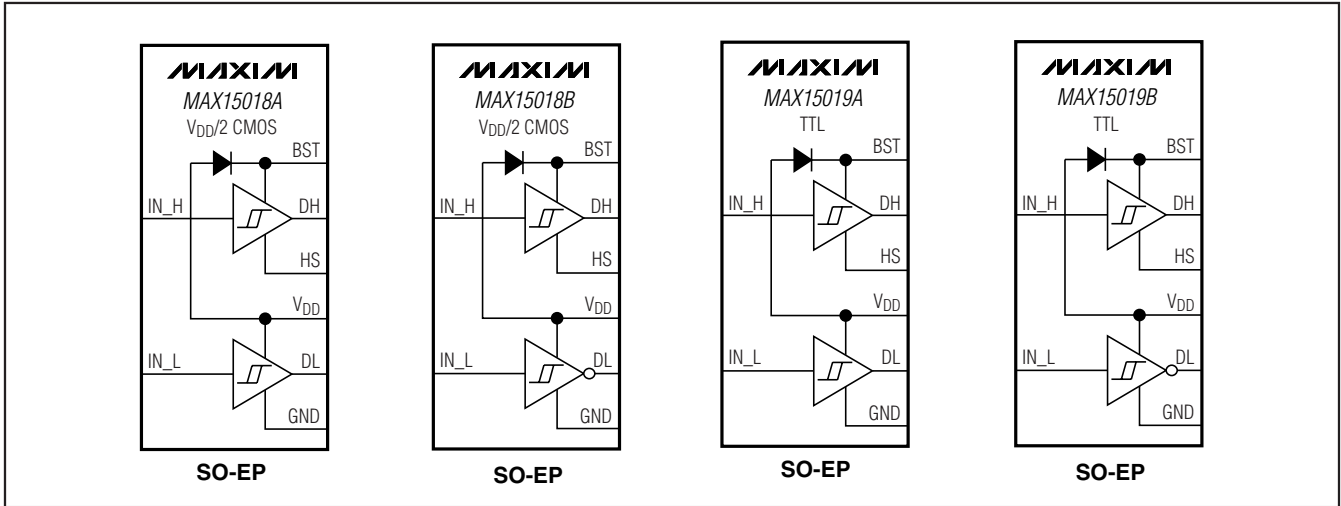


Figure 3. Two-Switch Forward Application

# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## Functional Diagrams

MAX15018/MAX15019



## Selector Guide

PART	HIGH-SIDE DRIVER	LOW-SIDE DRIVER	LOGIC LEVEL	PIN COMPATIBLE
MAX15018AASA+	Noninverting	Noninverting	CMOS ( $V_{DD}/2$ )	HIP 2100IB
MAX15018BASA+	Noninverting	Inverting	CMOS ( $V_{DD}/2$ )	—
MAX15019AASA+	Noninverting	Noninverting	TTL	HIP 2101IB
MAX15019BASA+	Noninverting	Inverting	TTL	—

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8E-14	<a href="#">21-0111</a>