MAX15059

76V, 300mW Boost Converter and Current Monitor for APD Bias Applications

General Description

The MAX15059 constant-frequency pulse-width modulating (PWM) step-up DC-DC converter features an internal switch and a high-side current monitor with high-speed adjustable current limiting. This device is capable of generating output voltages up to 76V (300mW for the MAX15059A and 200mW for the MAX15059B) and provides current monitoring up to 4mA. The MAX15059 operates from 2.8V to 5.5V.

The constant-frequency (400kHz) current-mode PWM architecture provides low-noise-output voltage that is easy to filter. A high-voltage internal power MOSFET allows this device to boost output voltages up to 76V. Internal soft-start circuitry limits the input current when the boost converter starts. The MAX15059 features a shutdown mode to save power.

The MAX15059 includes a current monitor with more than three decades of dynamic range and monitors current ranging from 500nA to 4mA with high accuracy. Resistor-adjustable current limiting protects the APD from optical power transients. A clamp diode protects the monitor's output from overvoltage conditions. Other protection features include cycle-by-cycle current limiting of the boost converter switch, undervoltage lockout (UVLO), and thermal shutdown if the die temperature reaches +125°C.

The MAX15059 is available in a thermally enhanced, lead-free, 16-pin TQFN-EP package and operates over the -40°C to +125°C temperature range.

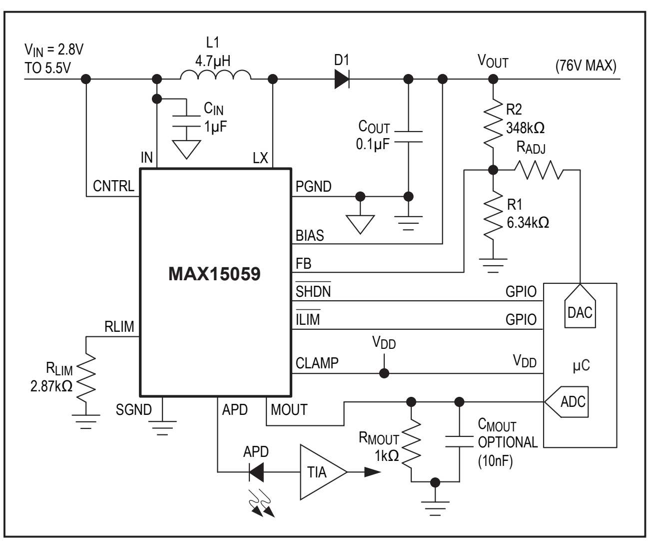
Features

- Input Voltage Range: +2.8V to +5.5V
- Wide Output-Voltage Range from (V_{IN} + 5V) to 76V
- Internal 1Ω (typ) 80V MOSFET
- Boost Converter Output Power: 300mW
- 200mW Version Available for Smaller Inductor
- Accurate ±5% (1:1 and 5:1) High-Side Current Monitor
- Resistor-Adjustable Ultra-Fast APD Current Limit (1µs Response Time)
- Open-Drain Current-Limit Indicator Flag
- 400kHz Fixed-Switching Frequency
- Constant PWM Frequency Provides Easy Filtering in Low-Noise Applications
- Internal Soft-Start
- 2µA (max) Shutdown Current
- -40°C to +125°C Temperature Range
- Small, Thermally Enhanced, 3mm x 3mm, Lead-Free, 16-Pin TQFN-EP Package

Applications

- Avalanche Photodiode Biasing and Monitoring
- PIN Diode Bias Supply
- Low-Noise Varactor Diode Bias Supply
- FBON Modules
- GPON Modules

Typical Operating Circuit



Ordering Information

PART	MAXIMUM POWER (mW)	I_{APD}: I_{MOUT}	PIN-PACKAGE
MAX15059AETE+	300	1:1	16 TQFN-EP*
MAX15059BETE+	200	5:1	16 TQFN-EP*
MAX15059AATE+	300	1:1	16 TQFN-EP*
MAX15059BATE+	200	5:1	16 TQFN-EP*

Note: *The MAX15059AATE+ and MAX15059BATE+ operate over the -40°C to +125°C temperature range. The MAX15059EATE+ and MAX15059BETE+ operate over the -40°C to +85°C temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Absolute Maximum Ratings

IN, $\overline{SHDN}$, FB, $\overline{ILIM}$, RLIM, CNTRL to SGND.........-0.3V to +6V
LX to PGND..-0.3V to +80V
BIAS to SGND..-0.3V to +79V
APD, CLAMP to SGND ....-0.3V to (V_{BIAS} + 0.3V)
PGND to SGND...-0.3V to +0.3V
MOUT to SGND ....-0.3V to (V_{CLAMP} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN-EP
(derate 20.8mW/°C above +70°C) 1666.7mW

Operating Temperature Range
MAX15059AETE, MAX15059BETE .... -40°C to +85°C
MAX15059AATE, MAX15059BATE............. -40°C to +125°C
Operating Temperature Range.......................... -40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})................7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = $V_{\overline{SHDN}}$ = V_{CNTRL}= 3.3V. C_{IN} = 1µF, V_{PGND} = V_{SGND} = 0V, V_{BIAS} = 40V. LX = APD = CLAMP = $\overline{ILIM}$ = unconnected, V_{MOUT} = 0V, T_A = -40°C to +85°C for the MAX15059AETE+ and MAX15059BETE+ and T_A = -40°C to +125°C for the MAX15059AATE+ and MAX15059BATE+, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Supply Voltage Range	V_{IN}			2.8		5.5	V
Supply Current	I_{SUPPLY}	V_{FB} = 1.4V, no switching	T_A = -40°C to +85°C		0.6	1.2	mA
			T_A = +125°C			1.35	
Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising		2.475	2.6	2.775	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}				200		mV
Shutdown Current	I_{SHDN}	$V_{\overline{SHDN}}$ = 0V			0.003	2	µA
Shutdown BIAS Current	I_{BIAS_SHDN}	V_{BIAS} = 3.3V, $V_{\overline{SHDN}}$ = 0V			9	20	µA
BOOST CONVERTER							
Output-Voltage Adjustment Range				V_{IN} + 5		76	V
Switching Frequency	f_{SW}	V_{IN} = 5V		380	400	420	kHz
Maximum Duty Cycle	D_{CLK}	V_{IN} = 2.8V		88	90	92	%
FB Set-Point Voltage	V_{FB_SET}			1.205	1.23	1.255	V
FB Input-Bias Current	I_{FB}	V_{FB} = V_{FB_SET}, T_A = +25°C		100		500	nA
Internal Switch On-Resistance	R_{ON}	I_{LX} = 100mA, V_{IN} = 2.8V	T_A = -40°C to +85°C		1	2	Ω
			T_A = +125°C			2.25	
Peak Switch Current Limit	I_{LIM_LX}	MAX15059A		1.1	1.2	1.3	A
		MAX15059B		0.825	0.9	0.975	
Peak Current-Limit Response					100		ns

Electrical Characteristics (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = V_{CNTRL}= 3.3V. C_{IN} = 1µF, V_{PGND} = V_{SGND} = 0V, V_{BIAS} = 40V. LX = APD = CLAMP = $\overline{ILIM}$ = unconnected, V_{MOUT} = 0V, T_A = -40°C to +85°C for the MAX15059AETE+ and MAX15059BETE+ and T_A = -40°C to +125°C for the MAX15059AATE+ and MAX15059BATE+, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Leakage Current		V_{LX} = 76V, T_A = +25°C				1	µA
Line Regulation		2.8V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 4.5mA			0.01		%
Load Regulation		0 ≤ I_{LOAD} ≤ 4.5mA			0.05		%
Soft-Start Duration					8		ms
Soft-Start Steps					32		Steps
CONTROL INPUT (CNTRL)							
Maximum Control Input Voltage Range		FB set point is controlled to V_{CNTRL}			1.2		V
CNTRL-to-REF Transition Threshold		V_{FB} = V_{REF} above this voltage			1.3		V
CNTRL Input-Bias Current		V_{CNTRL} = V_{FB_SET}, T_A = +25°C				500	nA
CURRENT MONITOR							
Bias Voltage Range	V_{BIAS}			10		76	V
Bias Quiescent Current	I_{BIAS}	I_{APD} = 500nA	MAX15059A		150	250	µA
			MAX15059B		150	250	
		I_{APD} = 2mA	MAX15059A		4	6	mA
			MAX15059B		3	4	
Voltage Drop	V_{DROP}	I_{APD} = 2mA, V_{DROP} = V_{BIAS} - V_{APD}			2.7	3.5	V
Dynamic Output Resistance at MOUT	R_{MOUT}	R_{MOUT} = $\Delta V_{MOUT}/\Delta I_{MOUT}$, I_{APD} = 2.5mA	MAX15059A		5		GΩ
APD Current-Step Response		Step load on I_{APD} = 20µA to 1mA			25		ns
MOUT Output Leakage		APD is unconnected, T_A = +25°C			1	300	nA
Output Clamp Voltage	V_{MOUT} - V_{CLAMP}	Forward diode current = 500µA		0.4	0.7	0.95	V
MOUT Voltage Range	V_{MOUT}	10V ≤ V_{BIAS} ≤ 76V, 0 ≤ I_{APD} ≤ 1mA, CLAMP is unconnected		V_{BIAS} - 2.7			V
Current Gain	I_{MOUT}/I_{APD}	I_{APD} = 500nA	MAX15059A	0. 95	1	1.1	mA/mA
			MAX15059B	0.19	0.2	0.22	
		I_{APD} = 2mA	MAX15059A	0.965	1	1.035	
			MAX15059B	0.193	0.2	0.207	
Power-Supply Rejection Ratio	PSRR	$(\Delta I_{MOUT}/I_{MOUT})/\Delta V_{BIAS}$, V_{BIAS} = 10V to 76V and I_{APD} = 5µA to 1mA (Note 3)	MAX15059A	20	300	610	ppm/V
			MAX15059B	20	300	700	
APD Input Current Limit	I_{LIM_APD}	T_A = -40°C to +85°C		4	4.6	5.2	mA
		T_A = +125°C		3.85		5.2	
Current-Limit Adjustment Range		9.75kΩ ≥ R_{LIM} ≥ 0	T_A = -40°C to +85°C	0.9		5.2	mA
			T_A = +125°C	0.89		5.2	
Power-Up Settling Time	t_S	I_{MOUT} settles to within 0.1%, 10nF connected from APD to ground	I_{APD} = 500nA		7.5		ms
			I_{APD} = 2.5mA		90		µs

Electrical Characteristics (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = V_{CNTRL}= 3.3V. C_{IN} = 1µF, V_{PGND} = V_{SGND} = 0V, V_{BIAS} = 40V. LX = APD = CLAMP = $\overline{ILIM}$ = unconnected, V_{MOUT} = 0V, T_A = -40°C to +85°C for the MAX15059AETE+ and MAX15059BETE+ and T_A = -40°C to +125°C for the MAX15059AATE+ and MAX15059BATE+, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

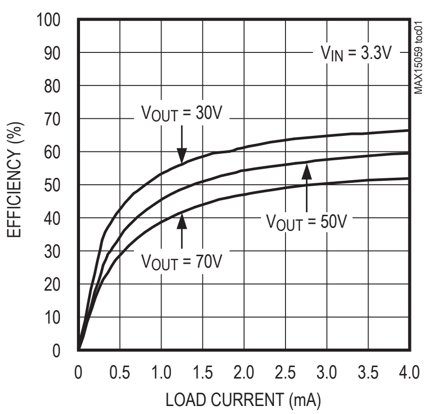
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC I/O						
$\overline{SHDN}$ Input Voltage Low	V_{IL}				0.8	V
$\overline{SHDN}$ Input Voltage High	V_{IH}		2.1			V
$\overline{ILIM}$ Output Voltage Low	V_{OL}	I_{LIM} = 2mA			0.1	V
$\overline{ILIM}$ Output Leakage Current	I_{OH}	T_A = +25°C			1	µA
THERMAL PROTECTION						
Thermal-Shutdown Temperature		Temperature rising		+150		°C
Thermal-Shutdown Hysteresis				15		°C

Note 2: All MIN/MAX parameters are tested at T_A = +25°C. Limits overtemperature are guaranteed by design.
Note 3: Guaranteed by design and not production tested.

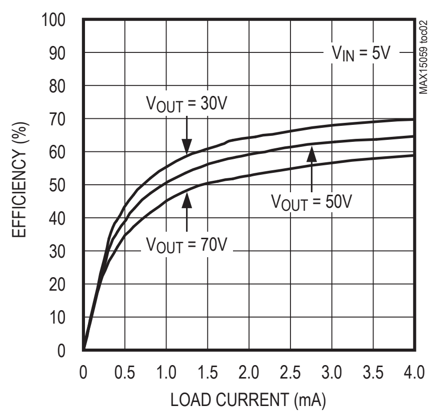
Typical Operating Characteristics

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

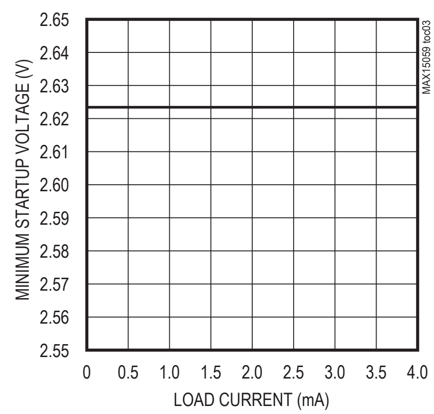
EFFICIENCY vs. LOAD CURRENT



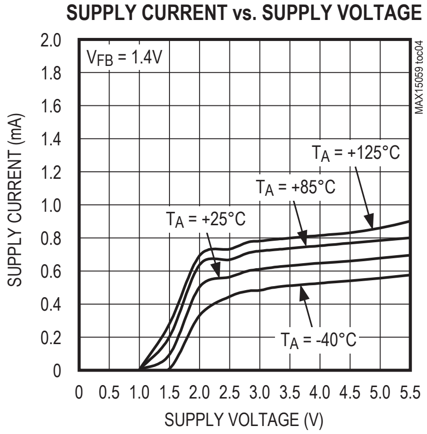
EFFICIENCY vs. LOAD CURRENT



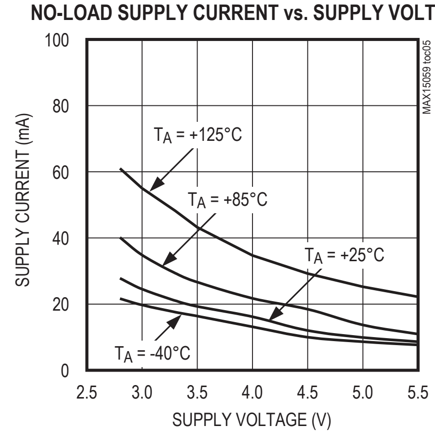
MINIMUM STARTUP VOLTAGE vs. LOAD CURRENT



SUPPLY CURRENT vs. SUPPLY VOLTAGE



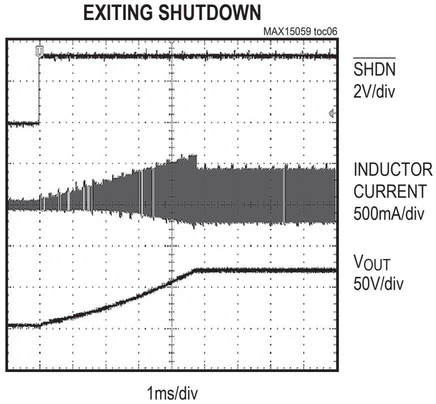
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



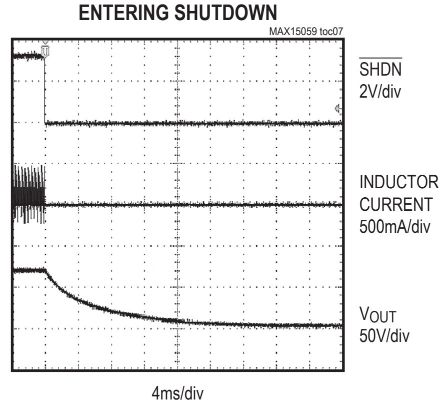
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

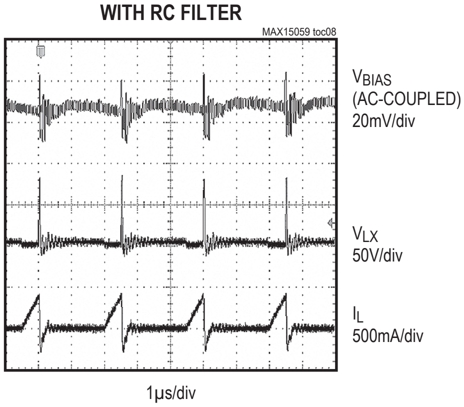
EXITING SHUTDOWN



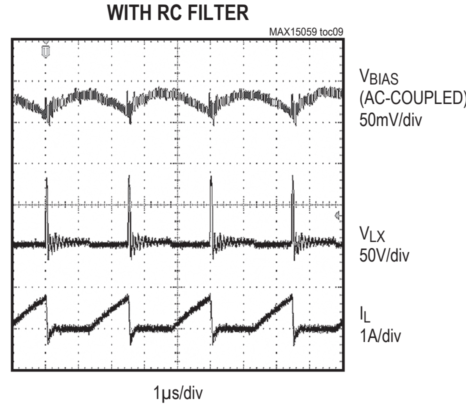
ENTERING SHUTDOWN



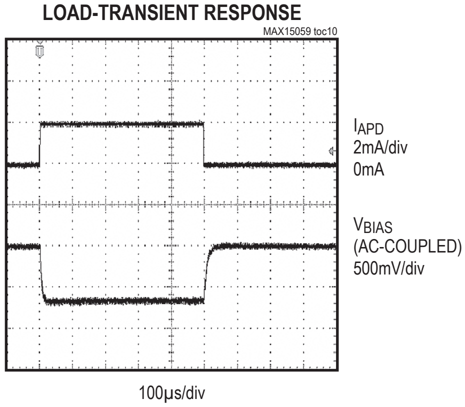
LIGHT-LOAD SWITCHING WAVEFORMS WITH RC FILTER



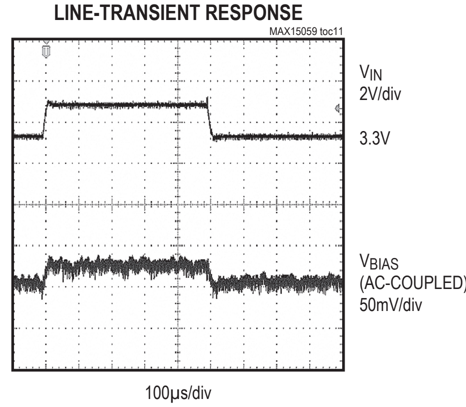
HEAVY-LOAD SWITCHING WAVEFORMS WITH RC FILTER



LOAD-TRANSIENT RESPONSE



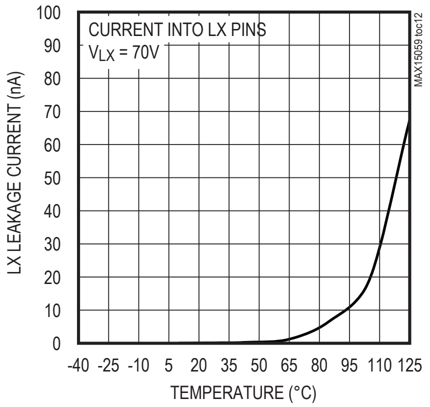
LINE-TRANSIENT RESPONSE



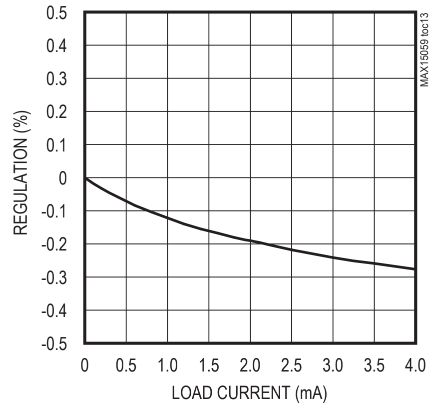
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

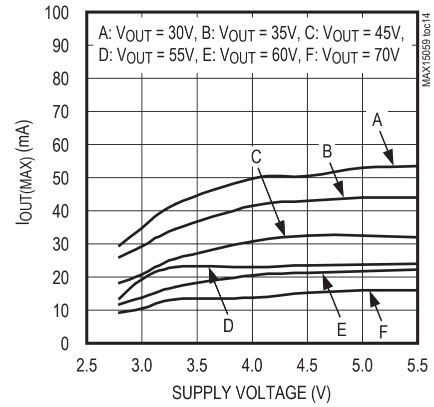
LX LEAKAGE CURRENT vs. TEMPERATURE



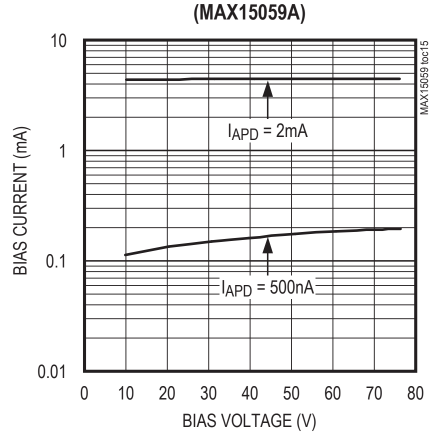
LOAD REGULATION



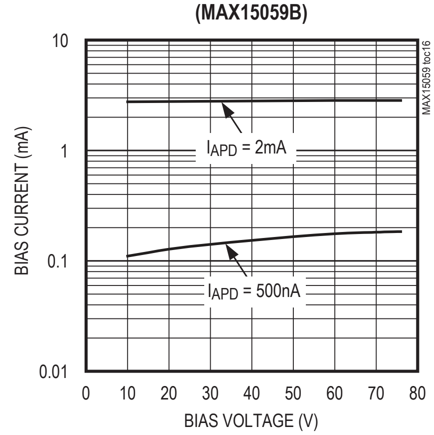
MAXIMUM LOAD CURRENT vs. SUPPLY VOLTAGE



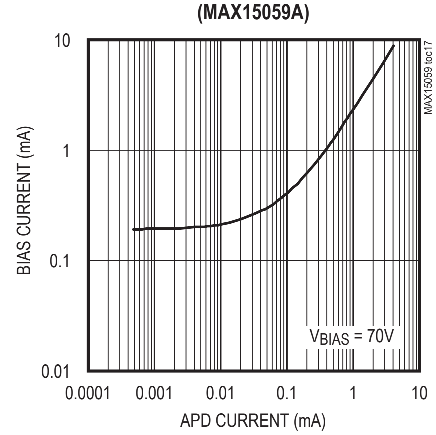
BIAS CURRENT vs. BIAS VOLTAGE (MAX15059A)



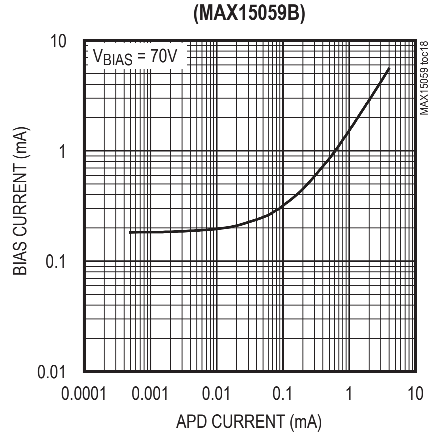
BIAS CURRENT vs. BIAS VOLTAGE (MAX15059B)



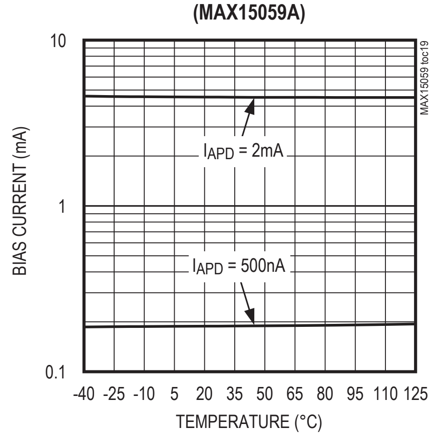
BIAS CURRENT vs. APD CURRENT (MAX15059A)



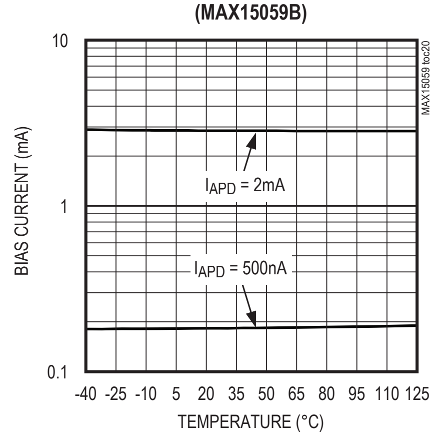
BIAS CURRENT vs. APD CURRENT (MAX15059B)



BIAS CURRENT vs. TEMPERATURE (MAX15059A)



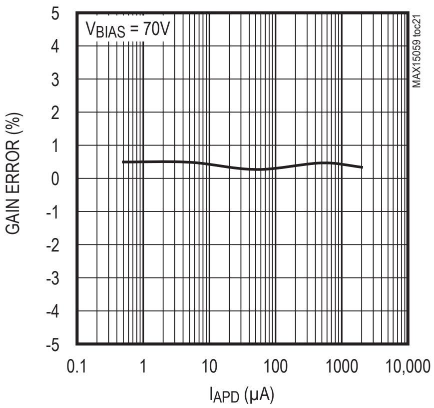
BIAS CURRENT vs. TEMPERATURE (MAX15059B)



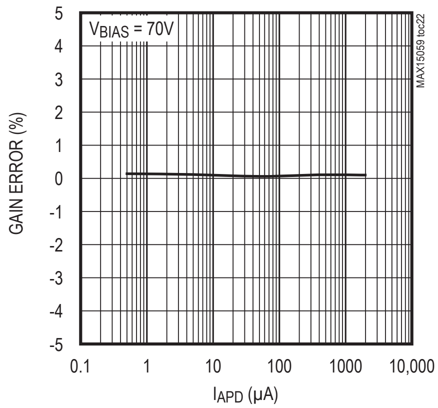
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

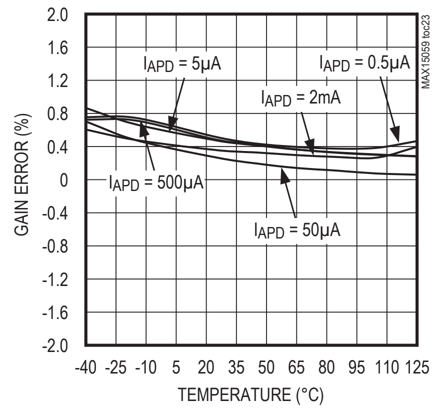
GAIN ERROR vs. APD CURRENT (MAX15059A)



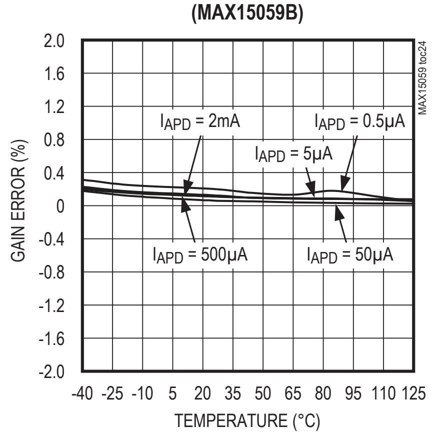
GAIN ERROR vs. APD CURRENT (MAX15059B)



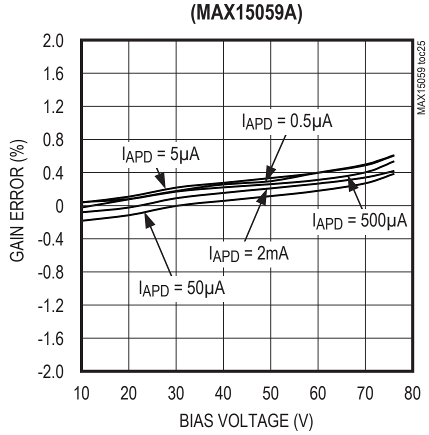
GAIN ERROR vs. TEMPERATURE (MAX15059A)



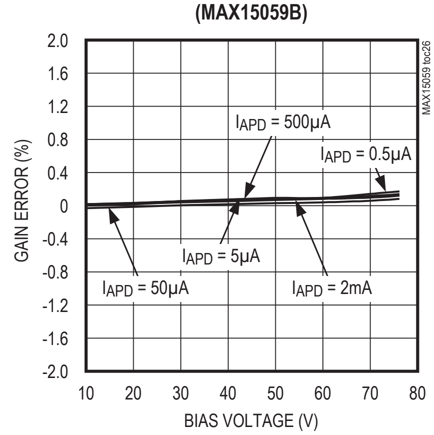
GAIN ERROR vs. TEMPERATURE (MAX15059B)



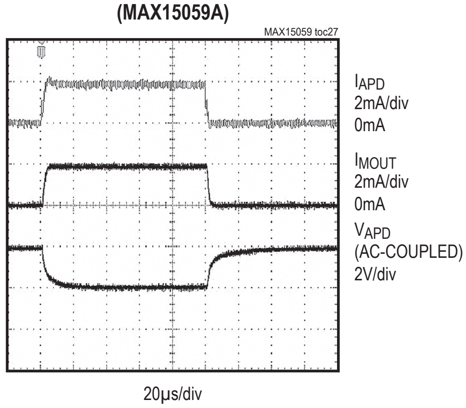
GAIN ERROR vs. BIAS VOLTAGE (MAX15059A)



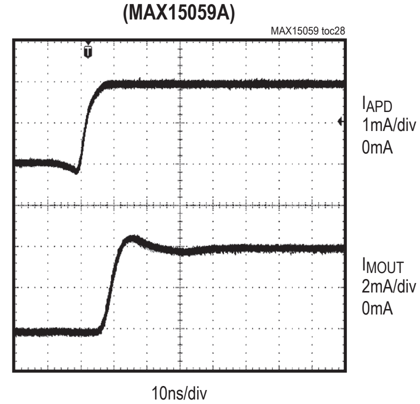
GAIN ERROR vs. BIAS VOLTAGE (MAX15059B)



APD TRANSIENT RESPONSE (MAX15059A)



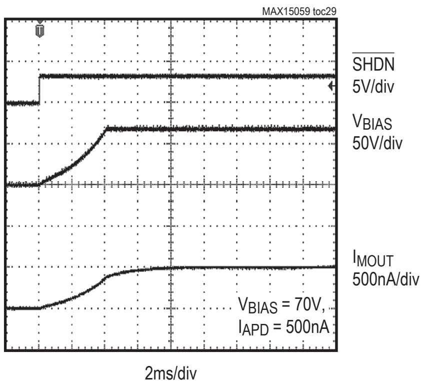
APD TRANSIENT RESPONSE (MAX15059A)



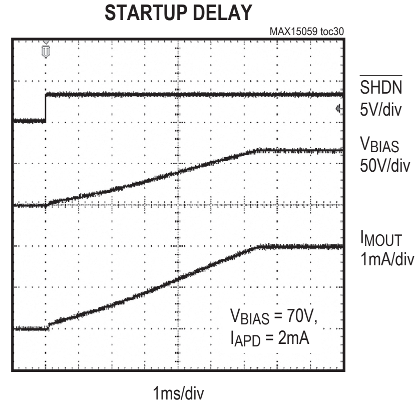
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

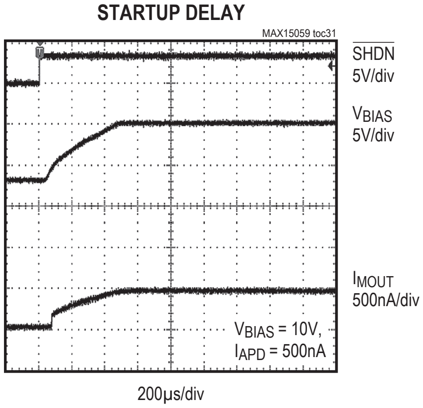
STARTUP DELAY



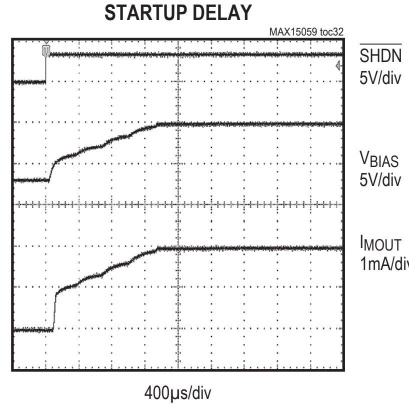
STARTUP DELAY



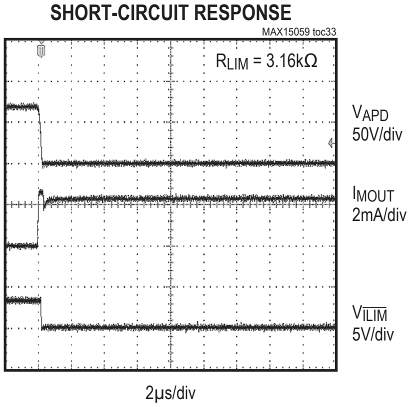
STARTUP DELAY



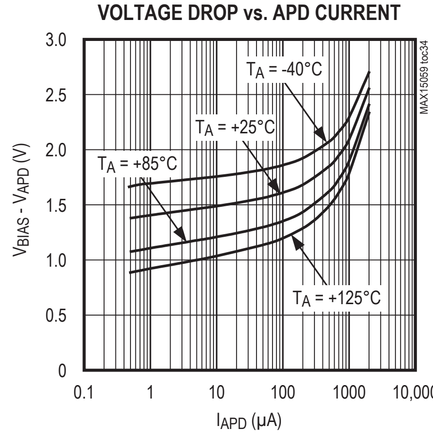
STARTUP DELAY



SHORT-CIRCUIT RESPONSE



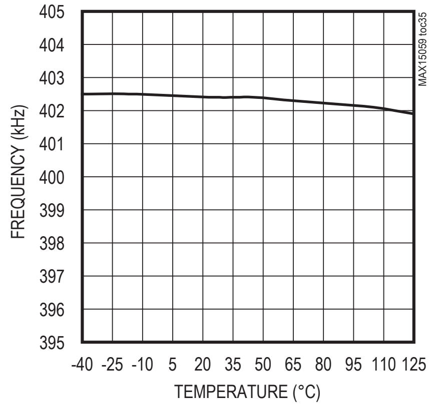
VOLTAGE DROP vs. APD CURRENT



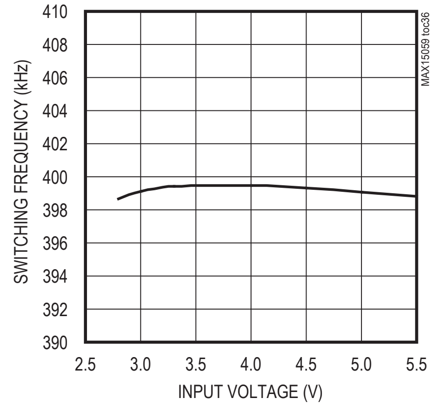
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25°C, unless otherwise noted.)

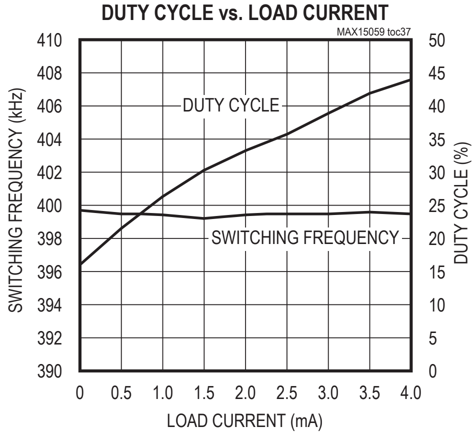
SWITCHING FREQUENCY vs. TEMPERATURE



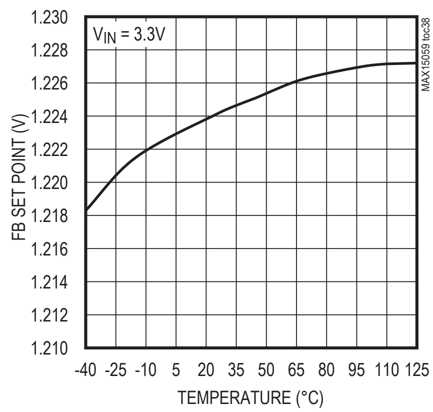
SWITCHING FREQUENCY vs. INPUT VOLTAGE



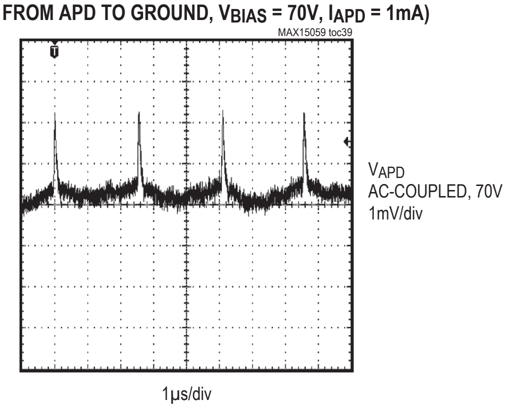
SWITCHING FREQUENCY AND DUTY CYCLE vs. LOAD CURRENT



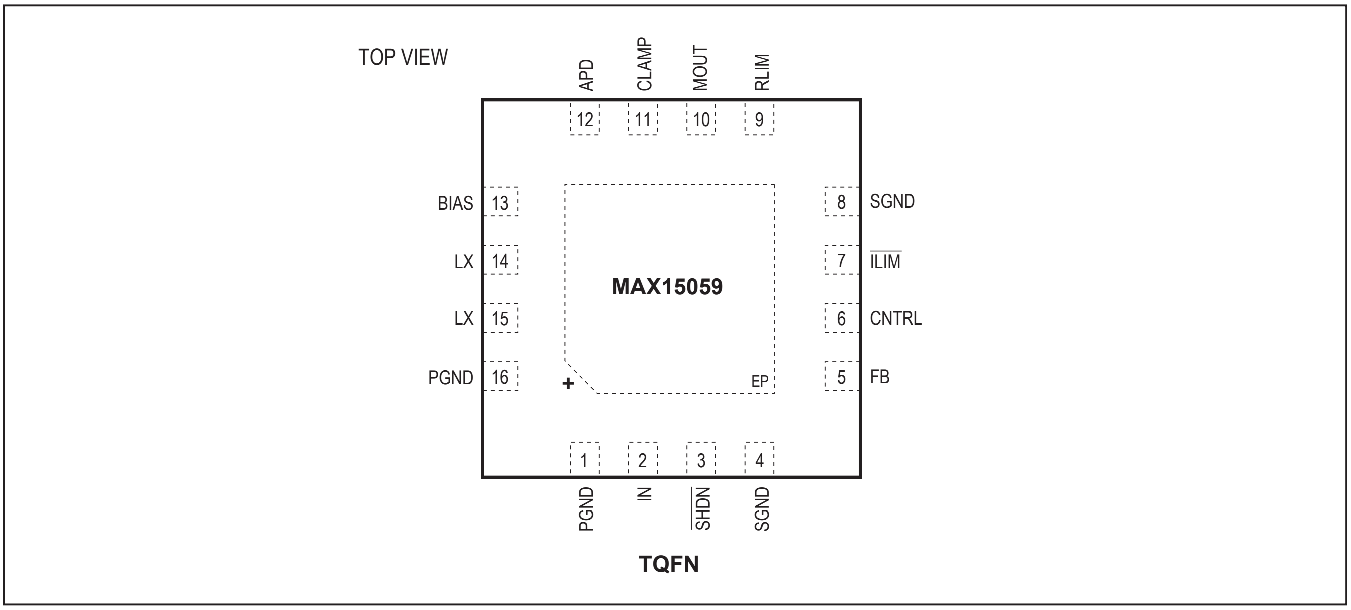
FB SET POINT vs. TEMPERATURE



APD OUTPUT RIPPLE VOLTAGE
(0.1µF FROM APD TO GROUND, V_{BIAS} = 70V, I_{APD} = 1mA)



Pin Configuration



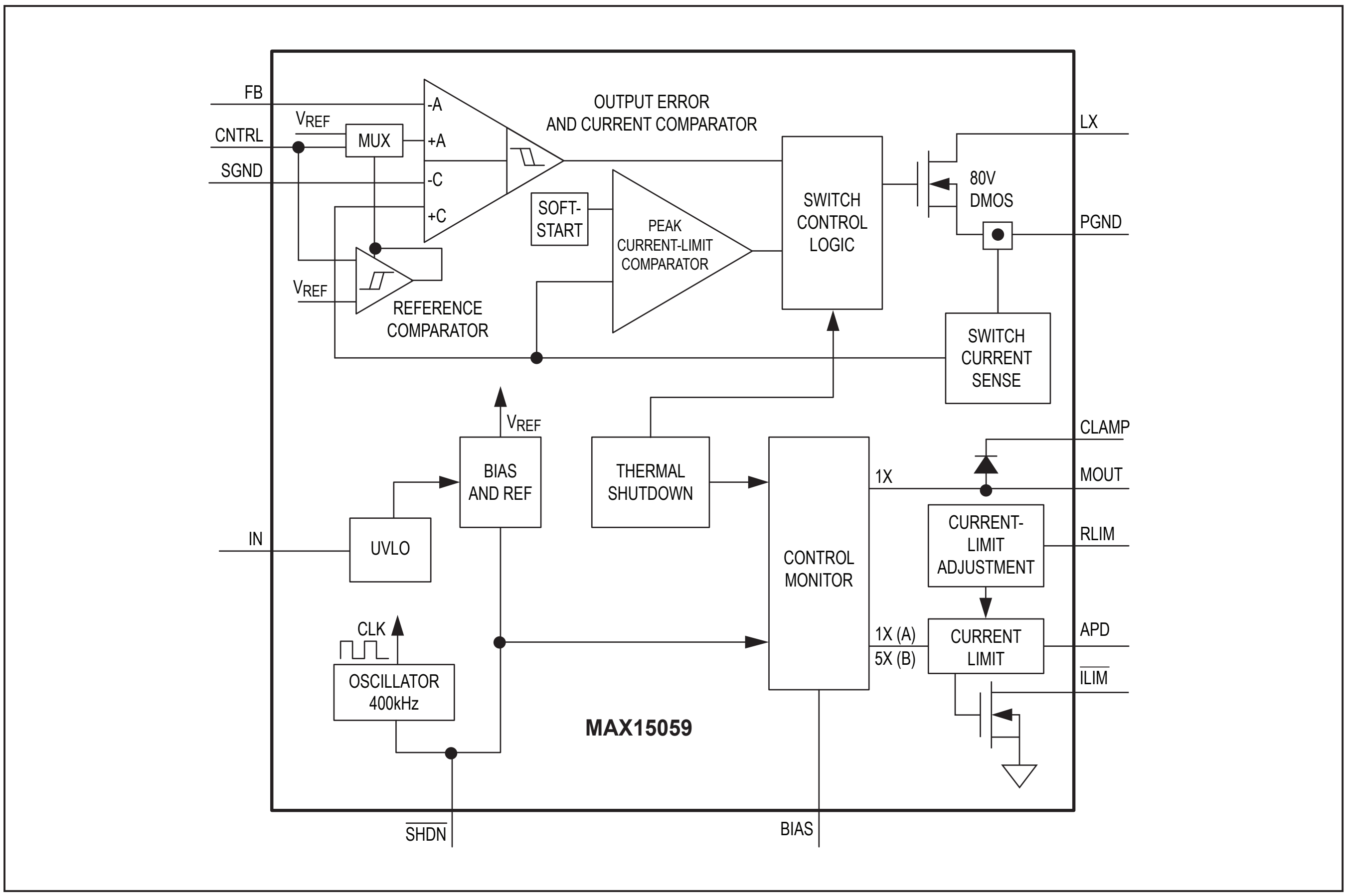
Pin Description

PIN	NAME	FUNCTION
1, 16	PGND	Power Ground. Connect the negative terminals of the input and output capacitors to PGND. Connect PGND externally to SGND at a single point, typically at the return terminal of the output capacitor.
2	IN	Input-Supply Voltage. Bypass IN to PGND with a ceramic capacitor of 1µF minimum value.
3	$\overline{\text{SHDN}}$	Active-Low Shutdown Control Input. Apply a logic-low voltage to $\overline{\text{SHDN}}$ to shut down the device. Connect $\overline{\text{SHDN}}$ to IN for normal operation. Ensure that $V_{\overline{SHDN}}$ is not greater than the input voltage, V_{IN}. $\overline{\text{SHDN}}$ is internally pulled low. The converter is disabled when $\overline{\text{SHDN}}$ is left unconnected.
4, 8	SGND	Signal Ground. Connect directly to the local ground plane. Connect SGND to PGND at a single point, typically near the return terminal of the output capacitor.
5	FB	Feedback Regulation Input. Connect FB to the center tap of a resistive voltage-divider from the boost output to SGND to set the output voltage. The FB voltage regulates to 1.23V (typ) when V_{CNTRL} is above 1.3V (typ) and to V_{CNTRL} when V_{CNTRL} is below 1.2V (typ).
6	CNTRL	Control Input for Boost Converter Output-Voltage Programmability. CNTRL allows the feedback set-point voltage to be set externally by CNTRL when V_{CNTRL} is less than 1.2V. Pull CNTRL above 1.3V (typ) to use the internal 1.23V (typ) feedback set-point voltage.
7	$\overline{\text{ILIM}}$	Open-Drain Current-Limit Indicator. $\overline{\text{ILIM}}$ asserts low when the APD current limit has been exceeded.
9	RLIM	Current-Limit Resistor Connection. Connect a resistor from RLIM to SGND to program the APD current-limit threshold. When RLIM is connected to SGND, the current limit is set to 4.6mA.
10	MOUT	Current-Monitor Output. For the MAX15059A, MOUT sources a current equal to I_{APD}. For the MAX15059B, MOUT sources a current equal to 1/5 of I_{APD}.
11	CLAMP	Clamp Voltage Input. CLAMP is the external potential used for voltage clamping of MOUT.

Pin Description (continued)

PIN	NAME	FUNCTION
12	APD	Reference Current Output. APD provides the source current to the cathode of the photodiode.
13	BIAS	Bias-Voltage Input. Connect BIAS to the boost converter output (V_{OUT}) either directly or through a lowpass filter for ripple attenuation. BIAS provides the voltage bias for the current monitor and is the current source for APD.
14, 15	LX	Drain of Internal 80V n-Channel DMOS. Connect inductor to LX. Minimize the trace area at LX to reduce switching-noise emission.
—	EP	Exposed Pad. Connect to a large copper plane at the SGND and PGND potential to improve thermal dissipation. Do not use as the only ground connection.

Functional Diagram



Detailed Description

The MAX15059 constant-frequency, current-mode, PWM boost converters are intended for low-voltage systems that require a locally generated high voltage. This device is capable of generating a low-noise, high output voltage required for PIN and varactor diode biasing. The MAX15059 operates from +2.8V to +5.5V.

The MAX15059 operates in discontinuous mode in order to reduce the switching noise caused by reverse recovery charge of the rectifier diode and eliminates the need for external compensation components. Other continuous-mode boost converters generate large voltage spikes at the output when the LX switch turns on because there is a conduction path between the output, diode, and switch to ground during the time needed for the diode to turn off and reverse its bias voltage. To reduce the output noise even further, the LX switch turns off by taking 10ns typically to transition from on to off. As a consequence, the positive slew rate of the LX node is reduced and the current from the inductor does not “force” the output voltage as hard as would be the case if the LX switch were to turn off faster.

The constant-frequency (400kHz) PWM architecture generates an output voltage ripple that is easy to filter. An 80V lateral DMOS device used as the internal power switch is ideal for boost converters with output voltages up to 76V. The MAX15059 can also be used in other topologies where the PWM switch is grounded, like SEPIC and flyback converters.

The MAX15059 includes a versatile current monitor intended for monitoring the APD, PIN, or varactor diode DC current in fiber and other applications. The MAX15059 features more than three decades of dynamic current ranging from 500nA to 4mA and provides an output current accurately proportional to the APD current at MOUT. MOUT output accuracy is ±10% from 500nA to 1mA and ±5% from 1mA to 2mA.

The MAX15059 also features a shutdown logic input to disable the device and reduce its standby current to 2μA (max).

Fixed-Frequency PWM Controller

The heart of the MAX15059 current-mode PWM controller is a BiCMOS multi-input comparator that simultaneously processes the output-error signal and switch current signal. The main PWM comparator uses direct summing, lacking a traditional error amplifier and its associated phase shift. The direct summing configuration approaches ideal cycle-by-cycle control over the output voltage since there is no conventional error amplifier in the feedback path.

This device operates in PWM mode using a fixed-frequency, current-mode operation. The current-mode frequency loop regulates the peak inductor current as a function of the output-voltage error signal.

The current-mode PWM controller is intended for DCM operation. No internal slope compensation is added to the current signal.

Current Limit

The current limit of the current monitor is programmable from 1mA to 4.6mA (typ). Connect RLIM to SGND to get a default current-limit threshold of 4.6mA or connect a resistor from RLIM to SGND to program the current-limit threshold below the default setting of 4.6mA. Calculate the value of the external resistor, R_{LIM}, for a given current limit, I_{LIM}, using the following equation:

$$R_{LIM}\,(k\Omega) = \left[\left(\frac{1.23V}{I_{LIM}\,(mA)}\right) x\,10 - 2.67(k\Omega)\right]$$

Clamping the Monitor Output Voltage (MOUT)

CLAMP provides a means for diode clamping the voltage at MOUT; thus, V_{MOUT} is limited to (V_{CLAMP} + 0.6V). CLAMP can be connected to either an external supply or BIAS. Leave CLAMP unconnected if voltage clamping is not required.

Shutdown

The MAX15059 features an active-low shutdown input ($\overline{SHDN}$). Pull $\overline{SHDN}$ low or leave it unconnected to enter shutdown. During shutdown, the supply current drops to 2μA (max). The output remains connected to the input through the inductor and output rectifier, holding the output voltage to one diode drop below IN when the MAX15059 is in shutdown. Connect $\overline{SHDN}$ to IN for always-on operation.

Adjusting the Feedback Set-Point/Reference Voltage

Apply a voltage to the CNTRL input to set the feedback set-point reference voltage, V_{REF} (see the *Functional Diagram*). For V_{CNTRL} > 1.3V, the internal 1.23V (typ) reference voltage is used as the feedback set point and for V_{CNTRL} < 1.2V, the CNTRL voltage is used as the reference voltage (V_{FB} set equal to V_{CNTRL}).

Design Procedure

Setting the Output Voltage

Set the MAX15059 output voltage by connecting a resistive divider from the output to FB to SGND (Figure 1). Select R_1 (FB to SGND resistor) between 5kΩ and 10kΩ. Calculate R_2 (V_{OUT} to FB resistor) using the following equation:

$$R_2 = R_1\left[\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right]$$

where V_{OUT} can range from (V_{IN} + 5V) to 76V. Apply a voltage to the CNTRL input to set the feedback set-point reference voltage, V_{REF} (see the *Functional Diagram*). For V_{CNTRL} > 1.3V, the internal 1.23V (typ) reference voltage is used as the feedback set point and for V_{CNTRL} < 1.2V, $V_{REF} = V_{CNTRL}$. See the *Adjusting the Feedback Set-Point/Reference Voltage* section for more information on adjusting the feedback reference voltage, V_{REF}.

Determining Peak Inductor Current

If the boost converter remains in the discontinuous mode of operation, then the approximate peak inductor current, I_{LPEAK} (in A), is represented by the formula below:

$$I_{LPEAK} = \sqrt{\frac{2 \times t_S \times (V_{OUT} - V_{IN\_MIN}) \times I_{OUT\_MAX}}{\eta \times L}}$$

where t_S is the switching period in µs, V_{OUT} is the output voltage in volts, V_{IN_MIN} is the minimum input voltage in volts, I_{OUT_MAX} is the maximum output current in amps, L is the inductor value in µH, and η is the efficiency of the boost converter (see the *Typical Operating Characteristics*).

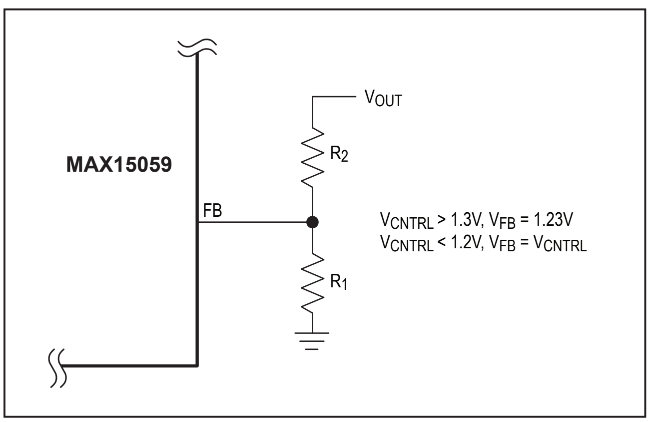


Figure 1. Adjustable Output Voltage

Determining the Inductor Value

Three key inductor parameters must be specified for operation with the MAX15059: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). In general, the inductor should have a saturation current rating greater than the maximum peak switch current-limit value (I_{LIM_LX} = 1.3A). DCR should be low for reasonable efficiency.

Use the following formula to calculate the lower bound of the inductor value at different output voltages and output currents. This is the minimum inductance value for discontinuous mode operation for supplying full 300mW of output power:

$$L_{MIN}[\mu H] = \frac{2 \times t_S \times I_{OUT} \times (V_{OUT} - V_{IN\_MIN})}{\eta \times I_{LIM\_LX}^2}$$

where V_{IN_MIN}, V_{OUT} (both in volts), and I_{OUT} (in amps) are typical values (so that efficiency is optimum for typical conditions), t_S (in µs) is the period, η is the efficiency, and I_{LIM_LX} is the peak switch current in amps (see the *Electrical Characteristics* table).

Calculate the optimum value of L ($L_{OPTIMUM}$) to ensure the full output power without reaching the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) using the following formula:

$$L_{OPTIMUM}[\mu H] = \frac{L_{MAX}[\mu H]}{2.25}$$

where:

$$L_{MAX}[\mu H] = \frac{V_{IN\_MIN}^2 (V_{OUT} - V_{IN\_MIN}) \times t_S \times \eta}{2 \times I_{OUT} \times V_{OUT}^2}$$

For a design in which V_{IN} = 3.3V, V_{OUT} = 70V, I_{OUT} = 3mA, η = 45%, I_{LIM_LX} = 1.2A, and t_S = 2.5µs: L_{MAX} = 27µH and L_{MIN} = 1.5µH.

For a worse-case scenario in which V_{IN} = 2.8V, V_{OUT} = 70V, I_{OUT} = 4mA, η = 43%, I_{LIM_LX} = 1.2A, and t_S = 2.5µs: L_{MAX} = 15µH and L_{MIN} = 2.2µH.

The choice of 4.7µH is reasonable given the worst-case scenario above. In general, the higher the inductance, the lower the switching noise. Load regulation is also better with higher inductance.

Diode Selection

The MAX15059's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward-voltage drop. Ensure that the diode's peak current rating is greater than the peak inductor current. Also, the diode breakdown voltage must be greater than V_{OUT}.

Output Filter Capacitor Selection

For most applications, use a small output capacitor of 0.1µF or greater. To achieve low output ripple, a capacitor with low ESR, low ESL, and high capacitance value should be selected. If tantalum or electrolytic capacitors are used to achieve high capacitance values, always add a smaller ceramic capacitor in parallel to bypass the high-frequency components of the diode current. The higher ESR and ESL of electrolytic capacitors increase the output ripple and peak-to-peak transient voltage. Assuming the contribution from the ESR and capacitor discharge equals 50% (proportions may vary), calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$C_{OUT}\,[\mu F] = \frac{I_{OUT}}{0.5 \times \Delta V_{OUT}}\left[t_S - \frac{I_{LPEAK} \times L_{OPTIMUM}}{(V_{OUT} - V_{IN\_MIN})}\right]$$

$$ESR[m\Omega] = \frac{0.5 \times \Delta V_{OUT}}{I_{OUT}}$$

For very-low-output-ripple applications, the output of the boost converter can be followed by an RC filter to further reduce the ripple. Figure 2 shows a 100Ω, 0.1µF (R_F C_F) filter used to reduce the switching output ripple to $1mV_{P-P}$ with a 0.1mA load or $1mV_{P-P}$ with a 4mA load. The output voltage regulation resistive divider must remain connected to the diode/output capacitor node.

Use X7R ceramic capacitors for more stability over the full temperature range.

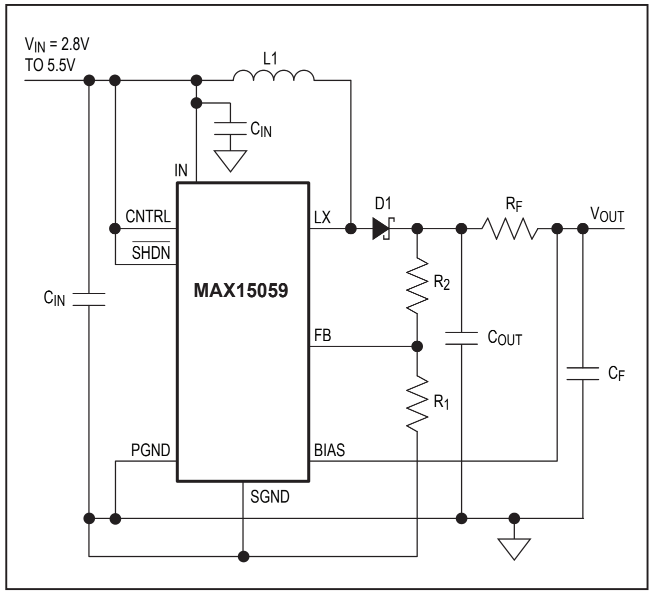


Figure 2. Typical Operating Circuit with RC Filter

Input-Capacitor Selection

Bypass IN to PGND with a 1µF (min) ceramic capacitor. Depending on the supply source impedance, higher values may be needed. Make sure that the input capacitors are close enough to the IC to provide adequate decoupling at IN as well. If the layout cannot achieve this, add another 0.1µF ceramic capacitor between IN and PGND in the immediate vicinity of the IC. Bulk aluminum electrolytic capacitors may be needed to avoid chattering at low-input voltage. In case of aluminum electrolytic capacitors, calculate the capacitor value and ESR of the input capacitor using the following equations:

$$C_{IN}\,[\mu F] = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN} \times 0.5 \times \Delta V_{IN}}\left[t_S - \frac{I_{LPEAK} \times L_{OPTIMUM} \times V_{OUT}}{V_{IN\_MIN}(V_{OUT} - V_{IN\_MIN})}\right]$$

$$ESR[m\Omega] = \frac{0.5 \times \Delta V_{IN} \times \eta \times V_{IN\_MIN}}{V_{OUT} \times I_{OUT}}$$

Applications Information

Using APD or PIN Photodiodes in Fiber Applications

When using the MAX15059 to monitor APD or PIN photodiode currents in fiber applications, several issues must be addressed. In applications where the photodiode must be fully depleted, keep track of voltages budgeted for each component with respect to the available supply voltage(s). The current monitors require as much as 3.5V between BIAS and APD, which must be considered part of the overall voltage budget.

Additional voltage margin can be created if a negative supply is used in place of a ground connection, as long as the overall voltage drop experienced by the MAX15059 is less than or equal to 76V. For this type of application, the MAX15059 is suggested so the output can be referenced to “true” ground and not the negative supply. The MAX15059’s output current can be referenced as desired with either a resistor to ground or a transimpedance amplifier. Take care to ensure that output voltage excursions do not interfere with the required margin between BIAS and MOUT. In many fiber applications, MOUT is connected directly to an ADC that operates from a supply voltage that is less than the voltage at BIAS. Connecting the MAX15059’s clamping diode output, CLAMP, to the ADC power supply helps avoid damage to the ADC. Without this protection, voltages can develop at MOUT that might destroy the ADC. This protection is less critical when MOUT is connected directly to subsequent transimpedance amplifiers (linear or logarithmic) that have low-impedance, near-ground-referenced inputs. If a transimpedance amp is used on the low side of the photodiode, its voltage drop must also be considered. Leakage from the clamping diode is most often insignificant over nominal operating conditions, but grows with temperature.

To maintain low levels of wideband noise, lowpass filtering the output signal is suggested in applications where only DC measurements are required. Connect the filter capacitor at MOUT. Determining the required filtering components is straightforward, as the MAX15059 exhibits a very high output impedance of 5GΩ.

In some applications where pilot tones are used to identify specific fiber channels, higher bandwidths are desired at MOUT to detect these tones. Consider the minimum and maximum currents to be detected; if the minimum current is too small, insufficient bandwidth could result, while too high a current could result in excessive noise across the desired bandwidth.

Layout Considerations

Careful PCB layout is critical to achieve low switching losses and clean and stable operation. Protect sensitive analog grounds by using a star ground configuration. Connect SGND and PGND together close to the device at the return terminal of the output bypass capacitor. Do not connect them together anywhere else. Keep all PCB traces as short as possible to reduce stray capacitance, trace resistance, and radiated noise. Ensure that the feedback connection to FB is short and direct. Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for SGND as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors. Refer to the MAX15059 Evaluation Kit data sheet for a layout example.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633-4	21-0136	90-0031