Click here for production status of specific part numbers.

MAX15095/MAX15095A/ MAX15095D

2.7V to 18V, 6.6A Integrated Hot-Swap/ Electronic Circuit Breaker

General Description

The MAX15095 family of devices is an integrated solution for hot-swap applications requiring the safe insertion and removal of circuit line cards from a live backplane. They can also be used as electronics circuit breakers for hard drives, solid-state drives, and fans. The devices integrate a hot-swap controller (10.6mΩ typ) power MOSFET, and an electronic circuit-breaker protection in a single package.

The devices are designed for protection of 2.7V to 18V supply voltages. These devices implement a foldback current limit during startup to control inrush current, lowering di/dt and keeping the MOSFET operating under safe operating area (SOA) conditions. After the startup cycle is complete, on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, and immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The devices are factory calibrated to deliver accurate overcurrent protection with ±10% accuracy. During a fault condition, PG goes low and the devices can latch off (MAX15095) or automatic retry (MAX15095A); the output can also be discharged after a fault event (MAX15095D).

The devices feature an IN-to-OUT short-circuit detection before startup. The devices provide a power-MOSFET GATE pin to program the slew rate during startup by adding an external capacitor. The devices have an undervoltage/overvoltage input pin (UVOV) that can detect an undervoltage/overvoltage fault and disconnect the IN from the OUT. Additional features include internal overtemperature protection and a power-good output (PG).

The devices are available in a 12-pin, 2.5mm x 2.5mm FC2QFN package and are rated over a -40°C to +105°C extended temperature range.

Benefits and Features

- Integration Reduces Solution Size for Blade Servers and Other Space-Constrained Designs
  - Integrated 10.6mΩ (typ) Internal Power MOSFET
  - Programmable Overvoltage Protection and Undervoltage-Lockout Threshold
  - Drive-Present Signal Input ($\overline{\text{PRSNT}}$ pin)
  - Thermal Protection
- Flexibility Enables Use in Many Unique Designs
  - 2.7V to 18V Operating Voltage Range
  - Programmable Inrush-Current Control under SOA Operation
  - Adjustable Circuit-Breaker Current/Current-Limit Threshold
  - Programmable Slew-Rate Control
  - Variable-Speed Circuit-Breaker Response
  - Latchoff (MAX15095) or Automatic Retry (MAX15095A) Options
- Safety Features Ensure Accurate, Robust Protection
  - 6.6A (max) Load-Current Capability
  - ±10% Circuit-Breaker Threshold Accuracy
  - IN-to-OUT Short-Circuit Detection
  - Open-Drain PG Output
  - Output Discharge after a Fault Event (MAX15095D Only)
  - Programmable Additional Delay (2µs max) to Fast-Comparator Response Time
  - Enable Input (EN)

Applications

- Blade Servers
- Server I/O Cards
- RAID Systems
- Disk Drive Power
- Storage Applications
- Industrial Applications

***Ordering Information* appears at end of data sheet.**

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19-100266; Rev 4; 7/19

maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +20V
IN to GND.....-0.3V to +20V
PG, $\overline{PRSNT}$ to GND.....-0.3V to +20V
OUT to GND.....-0.3V to (V_{IN} + 0.3V)
GATE to OUT .....-0.3V to +6V
EN, UVOV to GND .....-0.3V to +6V
TIMER, CB to GND .....-0.3V to (V_{REG} + 0.3V)
REG to GND.....-0.3V to min (+6V, (V_{CC} + 0.3V))

Continuous Power Dissipation (T_A = +70°C)
derate 13.8mW/°C above 70°C.....1.105W
Operating Temperature Range..... -40°C to +105°C
Junction Temperature..... 150°C
Storage Temperature Range..... -60°C to +150°C
Soldering Temperature (reflow)..... 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 12-PIN FC2QFN	
Package Code	F122A2F-1
Outline Number	**21-100198**
Land Pattern Number	**90-100073**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θJ_A)	72.4°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 10.5kΩ, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{CC} Operating Range	V_{CC}		2.7		18	V
IN Operating Range	V_{IN}		2.7		18	V
V_{CC} Supply Current	I_{CC}	Enable		0.58	0.9	mA
		Disable		0.590		
IN Supply Current	I_{IN}	R_{CB} = 41.67kΩ, no load		3.3	3.9	mA
		R_{CB} = 10KΩ, no load		1.3	1.8	
V_{CC} Default Undervoltage Lockout	V_{UVLO}	V_{CC} rising	2.35	2.5	2.65	V
V_{CC} Default Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}			0.1		V
REG Regulator Voltage	V_{REG}	No load, V_{CC} > 4V	3	3.3	3.6	V

Electrical Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 10.5kΩ, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UV Turn-On Threshold	V_{UV_TH}	V_{UVOV} rising		0.536	0.55	0.564	V
UV Turn-On Threshold Hysteresis	V_{UV_HYS}	V_{UVOV} falling			50		mV
OV Turn-On Threshold	V_{OV_TH}	V_{UVOV} rising		1.199	1.23	1.261	V
OV Turn-On Threshold Hysteresis	V_{OV_HYS}	V_{UVOV} falling			50		mV
OVUV Input Leakage Current	I_{LEAK}	V_{UVOV} = V_{EN} = 0V to 5.5V		-1		+1	µA
CURRENT LIMIT							
Circuit-Breaker Accuracy (Note 2)	I_{CB_TH}	V_{IN} = 12V	R_{CB} = 41.2kΩ	6	6.6	7.2	A
			R_{CB} = 10.5kΩ	1.2	1.43	1.66	
		V_{IN} = 3.3V, T_A = 85°C (Note 3, 4)	R_{CB} = 46.4kΩ	7.0	7.7	8.4	
Circuit-Breaker Accuracy Deviation (Note 4)		R_{CB} = 10.5kΩ to 21.5kΩ, compared to nominal current-limit value, V_{IN} = V_{CC} = 2.7V to 12V		-16		+16	%
		R_{CB} = 21.5kΩ to 41.2kΩ, compared to nominal current-limit value		-10		+10	
Slow-Comparator Response Time (Note 5)	t_{SCD}	0.6% overcurrent			2.7		ms
		30% overcurrent			200		µs
CB Source Current	I_{THCB_NORM}	In power-on mode			12		µA
Maximum Current Limit During Startup	I_{LIM}	(see Figure 2)			0.5 x I_{CB_TH}		A
Fast-Comparator Threshold	I_{FC_TH}				1.5 x I_{CB_TH}		A
Fast-Comparator Response Time	t_{FCD}				200		ns
Additional Delay Time by TIMER	t_{AFCD}	R_{TIMER} = open			2		µs
Minimum CB Voltage Reference During Foldback (Note 6)	V_{THCB_MIN}	V_{IN} - V_{OUT} > 10V, R_{CB} = 41.2kΩ			60		mV
Maximum CB Voltage Reference During Foldback (Note 6)	V_{THCB_MAX}	V_{IN} - V_{OUT} < 2V, R_{CB} = 41.2kΩ			250		mV
TIMING							
Startup Maximum Time Duration	t_{SU}			43	52	61	ms
Autoretry Delay Time	$t_{RESTART}$	MAX15095A and MAX15095D only			3.4		s
Output Short Detection at Startup	t_{SHORT}			10.4	13.2	15.6	ms
MOSFET							
Total On-Resistance	R_{ON}	T_A = +25°C, I_{OUT} = 0.5A			10.6	14.3	mΩ
		T_A = -40°C to +105°C, I_{OUT} = 0.5A				18	
		T_A = +70°C, V_{IN} = 3.3V, I_{OUT} = 4A (Note 4)				18	
GATE Charge Current	I_{GATE}			4.8	5.9	7.1	µA

Electrical Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 10.5kΩ, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS						
PG Output Low Voltage	V_{OL}	Low-impedance state, I_{PG} = +5mA			0.4	V
PG Output High-Leakage Current	I_{OH}	High-impedance state, V_{PG} = 16V			1	µA
DISCHARGE						
Discharge Current After PG Deasserted	$I_{DISCHARGE}$	V_{OUT} < 7.1V (MAX15095D only)	50	100	160	mA
		V_{OUT} ≥ 7.1V to 18V (MAX15095D only)		710mW/V_{OUT}		
PG THRESHOLD						
PG Threshold	V_{PG}	V_{IN} = 12V		0.9 x V_{IN}		V
PG Assertion Delay	t_{PG}	From V_{OUT} > V_{PG} and V_{GATE} - V_{OUT} > 3V	12	16	20	ms
OUT-to-IN Short-Circuit Detection Threshold	V_{IOSHT}	Measured at V_{OUT}		0.9 x V_{IN}		V
OUT Preload Threshold	V_{PL}	Measured at V_{OUT}		0.5 x V_{IN}		V
INPUTS						
Input Logic Threshold EN	V_{EN_TH}	Rising	0.95	1	1.05	V
Threshold Hysteresis EN	$V_{EN\_TH\_HYS}$	Falling		50		mV
Input Logic Threshold $\overline{PRSNT}$	$V_{\overline{PRSNT}\_TH}$	Falling	0.92	0.97	1.02	V
Threshold Hysteresis $\overline{PRSNT}$	$V_{\overline{PRSNT}\_TH\_HYS}$	Rising		50		mV
EN Bias Current	I_{EN_BIAS}	V_{EN} = 0 or 5.5V			1	µA
$\overline{PRSNT}$ Input Bias Current	$I_{\overline{PRSNT}\_BIAS}$	$V_{\overline{PRSNT}}$ = 0 or 18V			1	µA
EN Deglitch Time	t_{EN_DEG}			100		µs
$\overline{PRSNT}$ High-to-Low Deglitch Time	$t_{\overline{PRSNT}\_DEG}$			400		µs
THERMAL SHUTDOWN						
Thermal Shutdown	TSD	T_J rising		145		°C
Thermal Shutdown Hysteresis		T_J falling		125		°C

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: 41.2kΩ is the maximum allowed external resistance value to be connected at the CB pin to GND for safe operation over the full 2.7V to 18V V_{IN} range. The parameter specified at R_{CB} = 41.2kΩ is guaranteed by bench characterization and correlation, with respect to the tested parameter at R_{CB} = 10.5kΩ. The formula that describes the relationship between R_{CB} and the circuit-breaker current threshold is: I_{CB} = (R_{CB}/5920) - (V_{IN}/33).

Note 3: The CB resistance can be increased to 46.4kΩ if V_{IN} is between 2.7V and 3.6V, with operating current of 6.6A for no longer than 500ms. Do not exceed 6A continuous current.

Note 4: Guaranteed by design and not production tested.

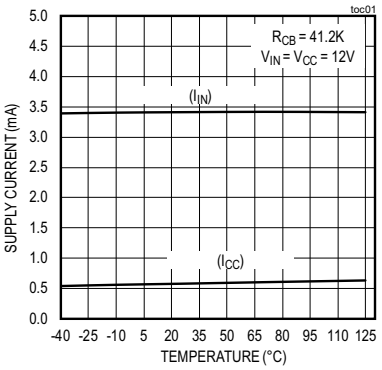
Note 5: The current-limit slow-comparator response time is weighed against the amount of overcurrent so the higher the overcurrent condition, the faster the response time.

Note 6: Foldback is active during the startup phase so the internal power MOSFET operates within SOA.

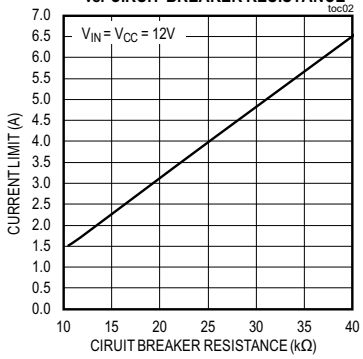
Typical Operating Characteristics

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 10.5kΩ, and T_A = +25°C.)

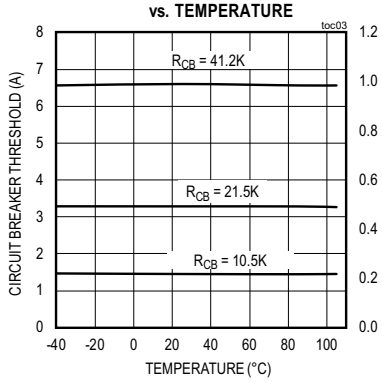
SUPPLY CURRENT vs. TEMPERATURE



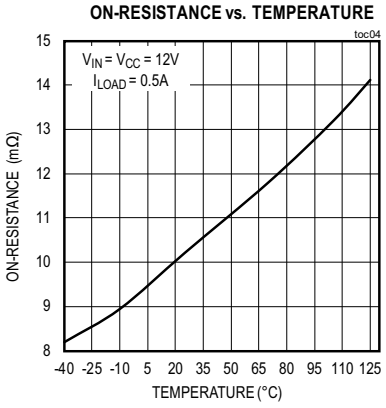
CIRUIT-BREAKER THRESHOLD vs. CIRUIT-BREAKER RESISTANCE



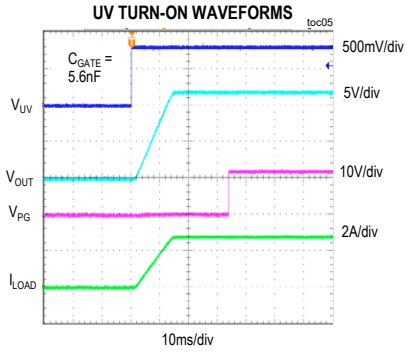
CIRUIT-BREAKER THRESHOLD vs. TEMPERATURE



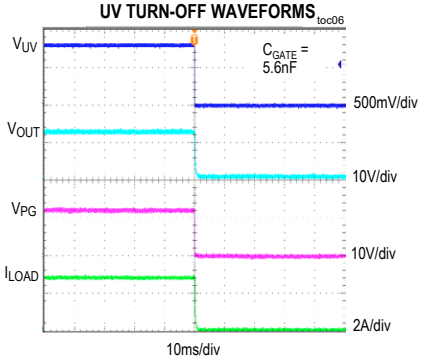
ON-RESISTANCE vs. TEMPERATURE



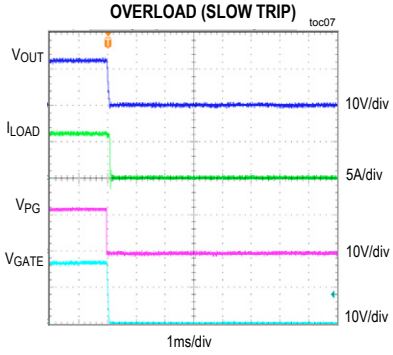
UV TURN-ON WAVEFORMS



UV TURN-OFF WAVEFORMS



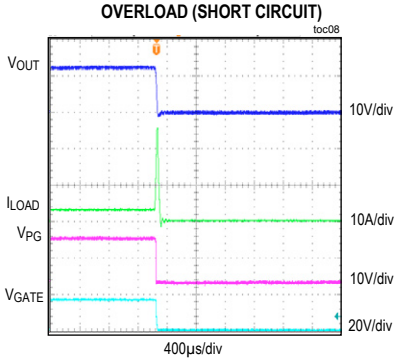
FAULT-SHUTDOWN WAVEFORMS OVERLOAD (SLOW TRIP)



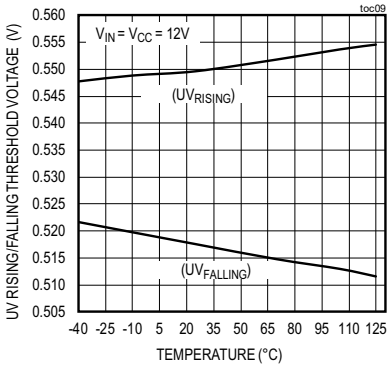
Typical Operating Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 10.5kΩ, and T_A = +25°C.)

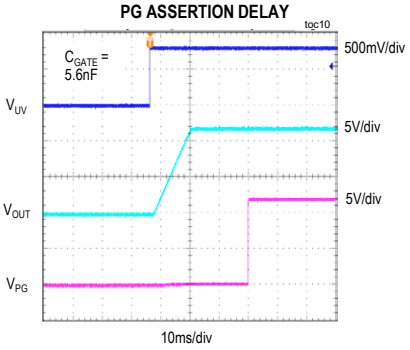
FAULT-SHUTDOWN WAVEFORMS
OVERLOAD (SHORT CIRCUIT)



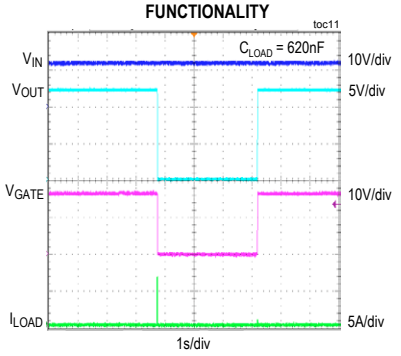
UV RISING/FALLING THRESHOLD
vs. TEMPERATURE



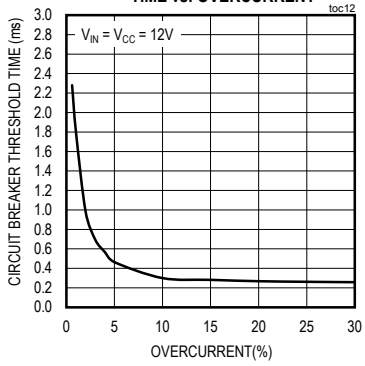
PG ASSERTION DELAY



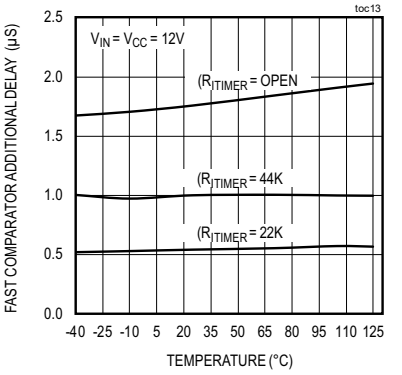
AUTORETRY
FUNCTIONALITY



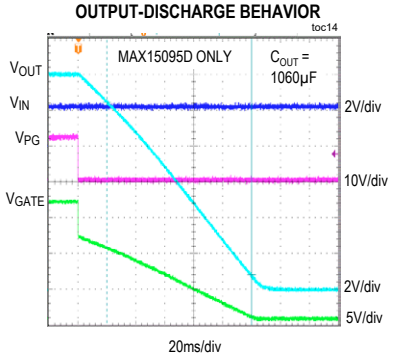
CIRCUIT-BREAKER THRESHOLD
TIME vs. OVERCURRENT



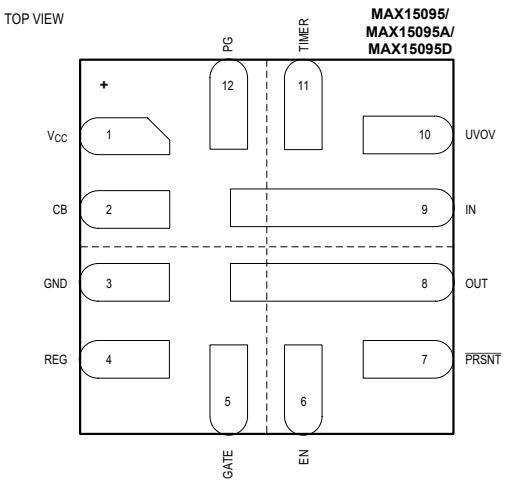
FAST COMPARATOR ADDTIONAL DELAY
vs. TEMPERATURE



OUTPUT-DISCHARGE BEHAVIOR



Pin Configuration

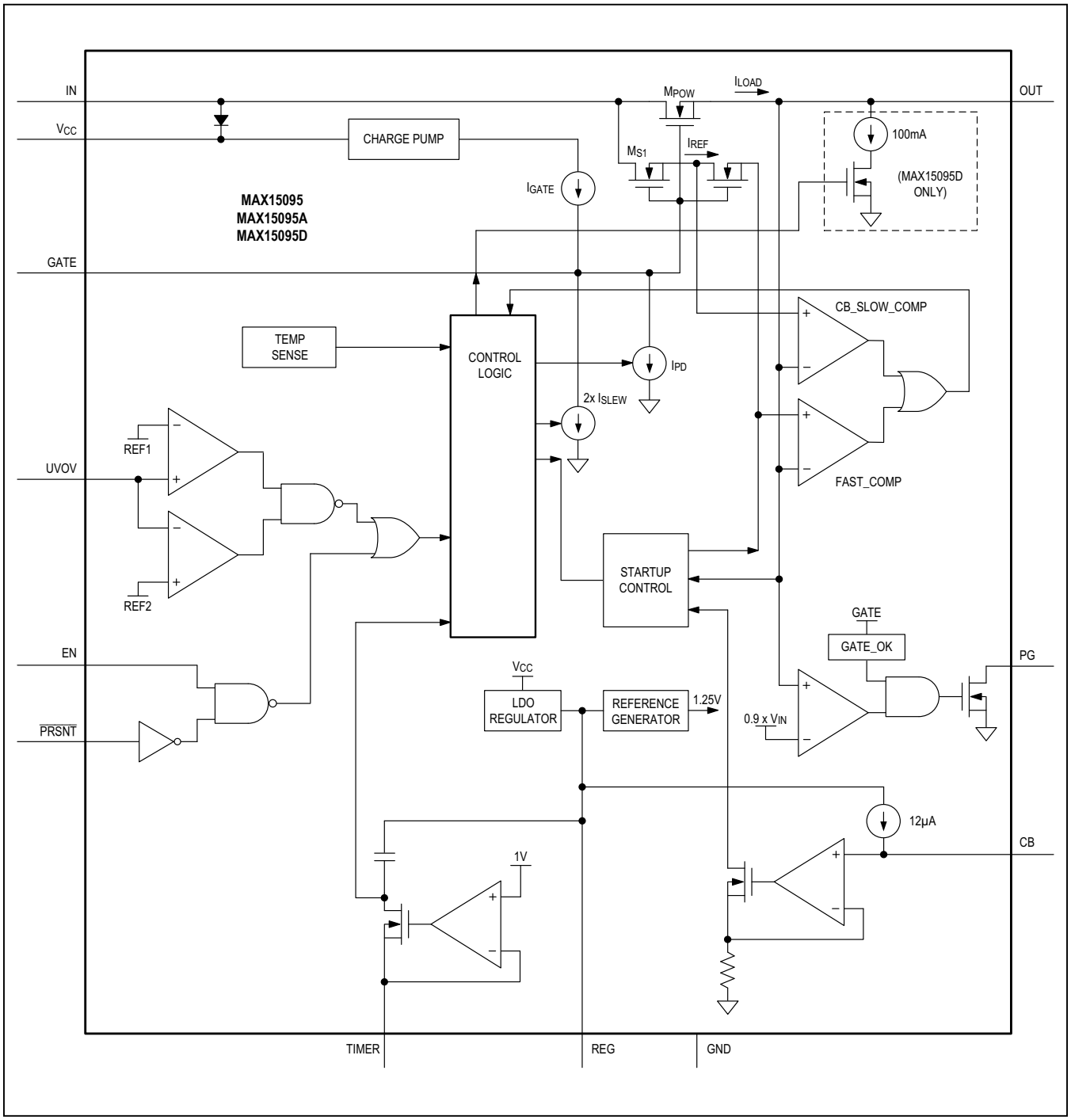


12-Pin FC2QFN

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power-Supply Input. Connect V_{CC} to a voltage between 2.7V and 18V. Connect a Schottky diode (or 10Ω resistor) from IN to V_{CC}, and a 1µF bypass capacitor to GND to guarantee full operation in the event V_{IN} collapses during a strong short from OUT to GND.
2	CB	Current-Limit Threshold Set. Connect a resistor from CB to GND to set the circuit-breaker threshold. Having the CB pin connected to GND sets the circuit- breaker threshold at 0A.
3	GND	Ground
4	REG	Internal Regulator Output. Bypass to ground with a 1µF capacitor. Do not power external circuitry using the REG output.
5	GATE	Gate of Internal MOSFET. During startup, a 5.9µA (typ) current is sourced to enhance the internal MOSFET with a 10V/ms slew rate. Connect an external capacitance from GATE to GND to reduce the output slew rate during startup.
6	EN	Active-High Enable Comparator Input. Pulling EN high enables the output if $\overline{PRSNT}$ is held low.
7	$\overline{PRSNT}$	Active-Low Present-Detect Logic Input. Pulling $\overline{PRSNT}$ to GND enables the output if EN is high.
8	OUT	Load Output. Source of the internal power MOSFET.
9	IN	Supply Voltage Input. IN is connected to the drain of the internal 10.6mΩ (typ) MOSFET. Bypass IN with a transient voltage-suppressor diode to GND for clamping inductive kick transients in the case of fast output short circuit to GND.
10	UVOV	Undervoltage and Overvoltage Threshold Pin. UVOV sets the under/overvoltage threshold.
11	TIMER	Timing Input. Connect a resistor from TIMER to GND to program the maximum time the part is allowed to remain in current limit. See the *TIMER* section. If TIMER is not connected, the parasitic capacitance between TIMER and GND must be less than 10pF.
12	PG	Power-Good Output. PG is an open-drain output. Connect to an external pullup resistor to make it an active-high output. PG pulls low until the internal power MOSFET is fully enhanced.

Block Diagram



Timing Diagram

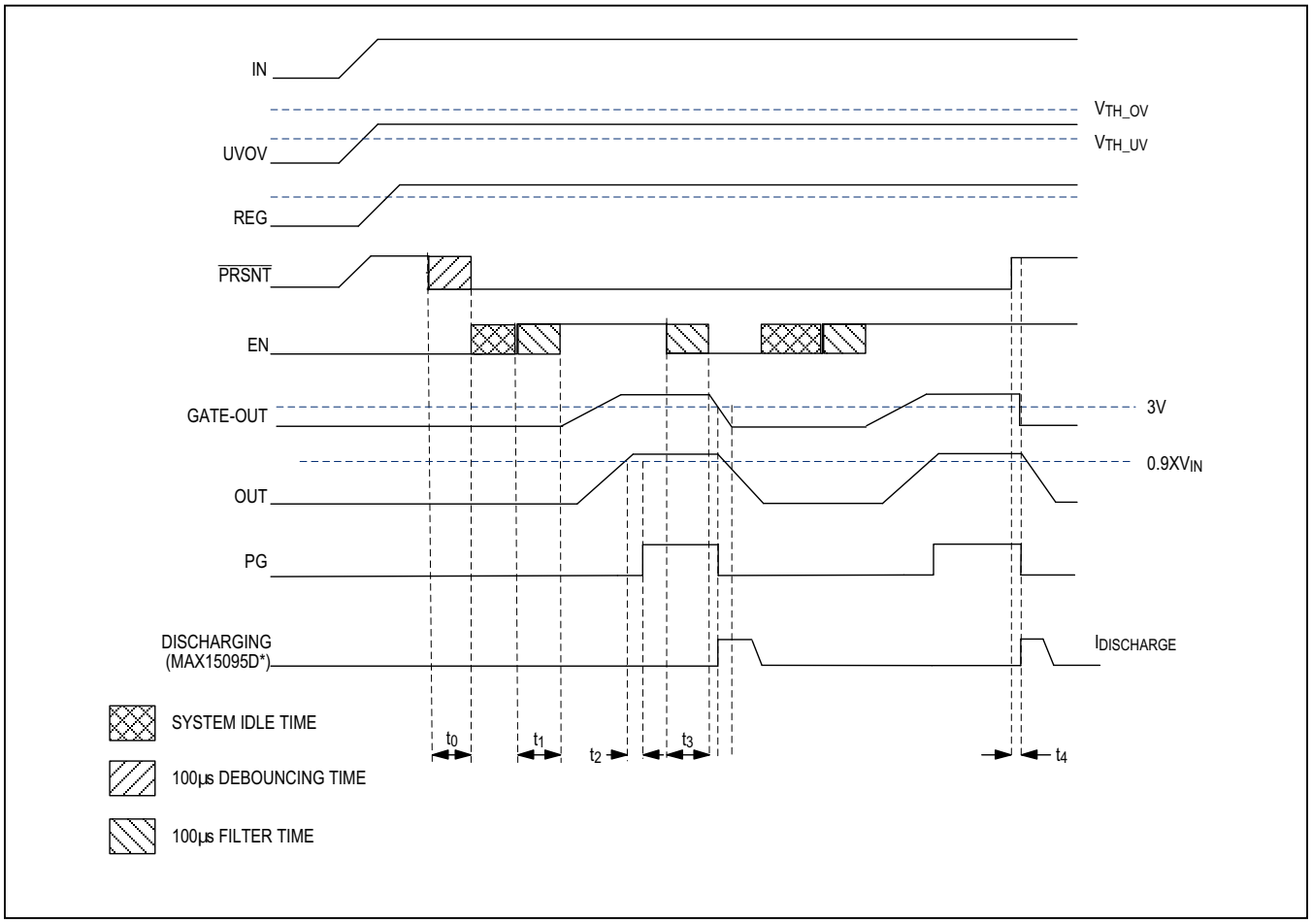


Table 1. Timing

TIMING PARAMETER	MIN	TYP	MAX	UNITS
t_0	—	400	—	µs
t_1	—	100	—	µs
t_2	12	16	20	ms
t_3	—	100	—	µs
t_4	—	0.5	—	µs

Detailed Description

Enable Logic and Undervoltage/ Overvoltage-Lockout Threshold

The supply output can become active only after all the following events have occurred:

- IN is within the UVOV window
- V_{CC} is above its UVLO threshold
- EN meets its enable threshold for more than 100µs
- $\overline{PRSNT}$ is low for more than 400µs

The MAX15095 family of devices enables the outputs as shown in Table 1. The devices are ready to drive the output when the V_{CC} supply rises above the V_{UVLO} threshold. The devices turn on the output when V_{CC} > V_{UVLO}, V_{UVOV} is higher than 0.55V (V_{UV_TH}) and less than 1.23V (V_{OV_TH}). The devices turn off the output when V_{UVOV} falls below (0.55V - V_{UV_HYS}) or V_{UVOV} rises above 1.23V. An external resistive divider (as shown in Figure 1) from IN to UVOV and ground provide the flexibility to select the undervoltage/overvoltage-lockout threshold to the desired value. Set the UVOV threshold using the following equations:

$$UVP = 0.55(R1 + R2) / R2$$

$$OVP = 1.23(R1 + R2) / R2$$

Startup

Once the devices' output is enabled, the device provides controlled application of power to the load. The voltage at OUT begins to rise at approximately 10V/ms default until the programmed circuit-breaker current level is reached, while the devices actively limit the inrush current at the circuit-breaker setting. An external capacitance connected to the GATE pin allows the user to program the slew rate to a value lower than the default. The inrush current can be programmed by appropriate selection of R_{CB}. During startup, a foldback current limit is active to protect the internal MOSFET to operate within a safe operating area. (Figure 2).

Table 2. Output-Enable Truth Table

POWER SUPPLY	PRECISION ANALOG INPUT		OUT
V_{CC} UVLO	UVP	OVP	
V_{CC} > V_{UVLO}	V_{UVOV} > V_{UV_TH}	V_{UVOV} < V_{OV_TH}	On
V_{CC} < V_{UVLO}	X	X	Off
X	V_{UVOV} < (V_{UV_TH} - V_{UV_HYS})	X	Off
X	X	V_{UVOV} > V_{OV_TH}	Off

X = Don't care.
V_{UV_TH} = 0.55V (typ).
V_{OV_TH} = 1.23V (typ).

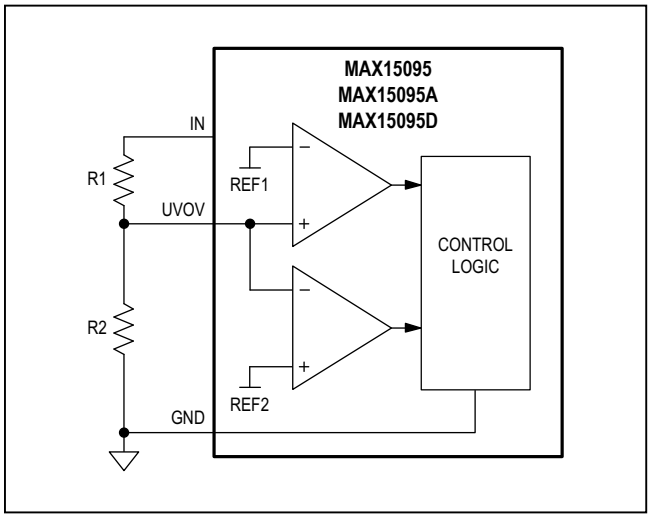


Figure 1. Undervoltage/Overvoltage Threshold Setting

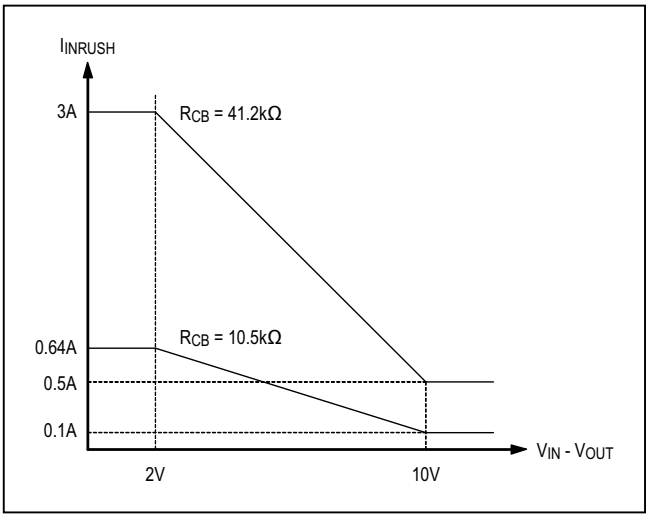


Figure 2. Startup Inrush Current Foldback Characteristics

An internal 52ms (typ) timer starts counting when the device enters a startup phase. The devices complete the startup phase and enter normal operation mode if the voltage at OUT rises above the preload threshold (0.9 x V_{IN}) and (V_{GATE} - V_{OUT}) > 3V. An open-drain power-good output (PG) goes high impedance 16ms after the startup successfully completes. The thermal-protection circuit is always active and the internal MOSFET is immediately turned off so a thermal-shutdown threshold condition can be reached.

If the startup is not successful because the output is shorted or the load is too high (OUT voltage < 1V), the devices turn off the hot-swap switch after the output short detection at startup t_{SHORT} (13.2ms) elapses.

VariableSpeed/BiLevel-Fault Protection

VariableSpeed/BiLevel-fault protection incorporates comparators with different thresholds and response times to monitor the load current (Figure 3). Protection is provided in normal operation (after the startup period has expired) by discharging the MOSFET gate in response to a fault condition. During a fault condition, the MAX15095A enters an autoretry mode while the MAX15095 latches off (see the *Autoretry and Latchoff-Fault Management* section).

Enable Input (EN)

The devices allow for enabling the MOSFET in an active-high configuration. When all other enabling conditions are verified and the EN pin is at a logic-high level, the MOSFET is enabled. Similarly, when the EN pin is at a logic-low level, the MOSFET is disabled.

Charge Pump

An integrated charge pump provides the gate-drive voltage for the internal power MOSFET. The charge pump generates the proper gate-drive voltage above V_{IN} to fully enhance the internal power MOSFET and guarantee low R_{ON} operation during normal-state condition.

During startup, the internal charge pump drives the GATE of the MOSFET with a fixed 5.9µA current to enhance the internal MOSFET with 10V/ms (typ) slew rate. To reduce the output slew rate during startup below 10V/ms, connect an external capacitor (C_{GATE}) from GATE to GND. The value of C_{GATE} is determined according to the equation:

$$C_{GATE} = I_{GATE} \times (t_{ON}/V_{OUT})$$

where I_{GATE} is 5.9µA (typ), t_{ON} is the desired output ramp-up time, and V_{OUT} is the final output voltage.

The slew rate of the OUT pin during startup is controlled by I_{GATE}/C_{GATE} under light-load conditions, but under heavier load, the foldback current limit and the external capacitive load will determine the actual slew rate.

$$(\Delta V_{OUT}/\Delta t) = (I_{LIM} - I_{LOAD})/C_{LOAD}$$

where I_{LIM} represents the voltage-dependent foldback current limit. See Electrical Characteristics.table and Figure 3. The load current is subtracted from I_{LIM}, because any current consumed by the load does not help charge the output capacitance.

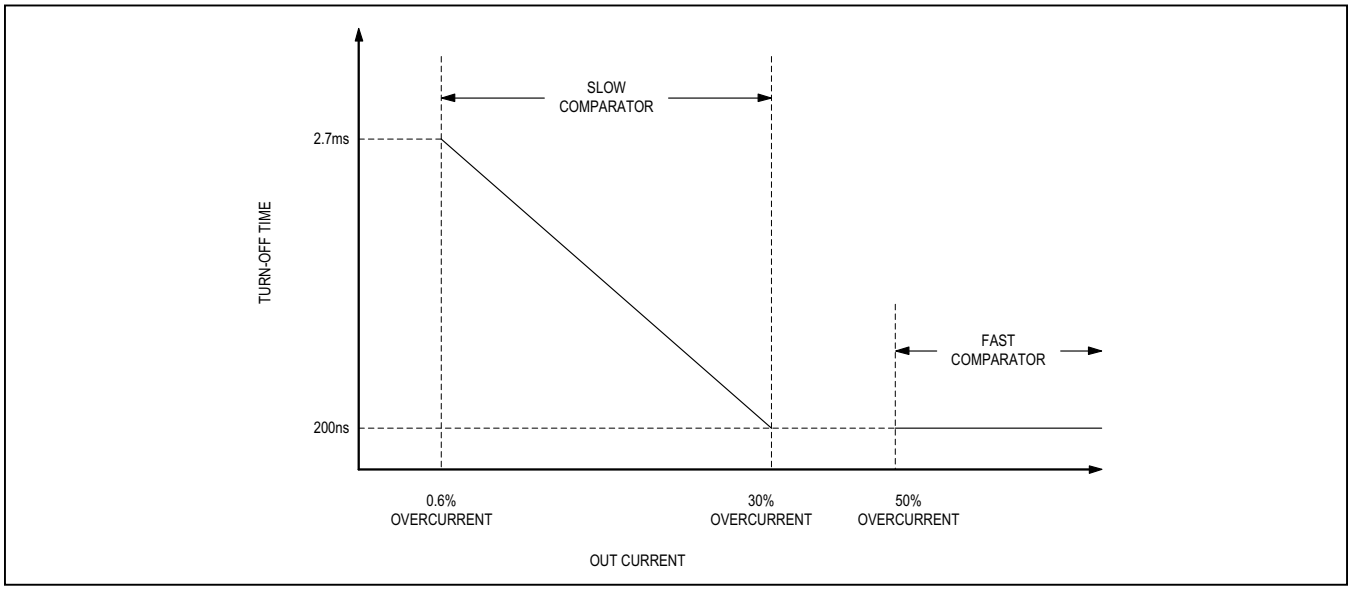


Figure 3. VariableSpeed/BiLevel Response

Circuit-Breaker Comparator and Current Limit

The current through the internal power MOSFET is compared to a circuit-breaker threshold. An external resistor between CB and ground sets this threshold according to the following formula:

$$I_{CB}\ (A) = (R_{CB} / 5920) - (V_{IN} / 33)$$

where R_{CB} is the resistor between CB and ground.

The circuit-breaker comparator is designed so that the load current can exceed the threshold for some amount of time before tripping. The time delay varies inversely with the overdrive above the threshold. The greater the overcurrent condition, the faster the response time, allowing the devices to tolerate load transients and noise near the circuit-breaker threshold. The operating current should not be allowed to exceed 6.6A for longer than 500ms. The maximum allowed external resistor value is 46.4kΩ.

The devices also feature catastrophic short-circuit protection. During normal operation, if OUT is shorted directly to ground, a fast protection circuit forces the gate of the internal MOSFET to discharge quickly and disconnect the output from the input.

Autoretry and Latchoff-Fault Management

During a fault condition, the devices turn off the internal MOSFET, disconnecting the output from the input. The MAX15095A enters an autoretry mode and restarts after $t_{RESTART}$ (3.4s typ) time delay elapses.

The MAX15095 latches off and remains off until the enable logic is cycled off and on after a certain delay. The delay prevents the latchoff device from restarting and operating with an unsafe power-dissipation duty cycle. See the *Timing Diagram* and Table 1 for delay values.

Latchoff Reset

The latchoff could be reset if any one of the following happens:

- V_{CC} is below its UVLO threshold
- EN is disabled for longer than 100µs
- UV is triggered
- $\overline{PRSNT}$ goes above its threshold
- OV is triggered

Power-Good (PG) Delay

The devices feature an open-drain, power-good output that asserts after t_{PG} delay, indicating that OUT voltage has reached (0.9 x V_{IN}) voltage and (V_{GATE} - V_{OUT}) > 3V.

REG

The devices include a linear regulator that outputs 3.3V at REG. REG provides power to the internal circuit blocks of the devices and must not be loaded externally (except a resistor > 50kΩ connected from REG to EN). REG requires a 1µF capacitor to ground for proper operation.

Output Discharging

The discharge FET is active when the output is disabled or under fault event. In this event, the hot-swap is off and the output is on the way down. The discharging is triggered after the main FET has completely turned off.

The maximum output capacitance is approximately 1000µF. The voltage could be up to 18V. Ideally, it discharges the output capacitor in constant-power mode (710mW typ) to ensure the voltage rail is below 0.3V within 2s or less.

TIMER

Connect a resistor from the TIMER pin to the GND pin to program the fast-trip response time. This time is the sum of the internal fast-comparator propagation delay (less than 200ns typ) plus an additional delay set by the external resistor connected from TIMER to ground. Choosing different resistance values, it is possible to change the value of additional delay. If the TIMER pin is connected to REG, the total response time is less than 200ns (typ).

Additional delay is disabled also during the startup phase or after a short-circuit event (V_{OUT} < 90% V_{IN}). Be careful about additional delay settings related to a short event.

Additional delay can be calculated using the following formula:

$$Additional\_Delay\ (\mu s) = R_{TIMER}\ (k\Omega) \times 22.9E^{-03}$$

Maximum additional delay time is set to 2µs. Table 3 provides additional delay settings.

Table 3. Additional Delay Settings

OPTION	R_{TIMER} (kΩ)	RESPONSE TIME (µs)
1	Open	2
2	86.6	2
3	43.2	1
4	21.5	0.5
5	11	0.25
6	0	0.050

Thermal Protection

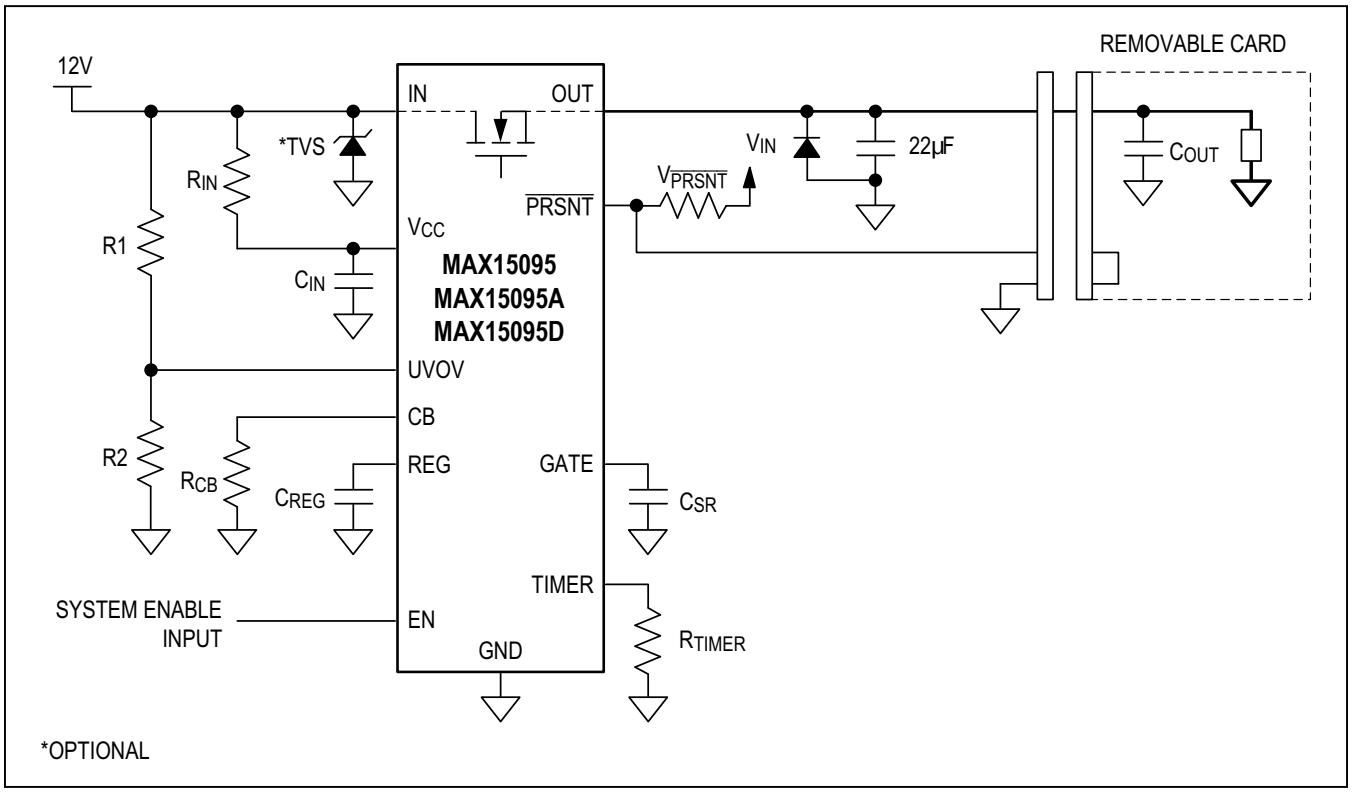
The devices enter a thermal shutdown mode in the event of overheating caused by excessive power dissipation or high ambient temperature. When the junction temperature exceeds T_J = 145°C (typ), the internal thermal protection circuitry turns off the internal power MOSFET. The devices recover from thermal shutdown mode once the junction temperature drops by 20°C (typ).

IN-to-OUT Short-Circuit Protection

At startup, after all the input conditions are satisfied (UV, OV, V_{UVLO}), the devices immediately check for IN-to-OUT short-circuit faults. If V_{OUT} is greater than 90% of V_{IN}, the internal MOSFET cannot be turned on, then the MAX15095A autoretries in $t_{RESTART}$ (3.4s typ), while the MAX15095 latches off.

If V_{OUT} is in the range from 50% to 90% of V_{IN}, then the internal MOSFET still cannot be turned on after t_{SU} time elapses. The MAX15095A autoretries in $t_{RESTART}$, while the MAX15095 latches off.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE (°C)	PIN-PACKAGE	FAULT MANAGEMENT
MAX15095GFC+	-40 to +105	12 FC2QFN	Latchoff
MAX15095AGFC+	-40 to +105	12 FC2QFN	Autoretry
MAX15095DGFC+	-40 to +105	12 FC2QFN	Autoretry

+Denotes a lead (Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS