Click here for production status of specific part numbers.

MAX16919

500mA–3A Automotive Hi-Speed USB Protector with USB Host-Charger Port Detection

General Description

The MAX16919 provides high-ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The device supports both Hi-Speed USB (480Mbps) and full-speed USB (12Mbps) operation. In addition, the device includes integrated circuitry to enable fast-charging for consumer devices adhering to the Hi-Speed USB host-charger port-detection protocol.

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. The device is capable of a short-to-battery condition of up to +18V. Short-to-GND and overcurrent protection are also provided on the HVBUS output to protect the internal BUS power rail from overcurrent faults.

The device features high-ESD protection to ±15kV Air Gap method and ±8kV Contact method on all protected HVBUS, HVD+, and HVD- outputs.

The device features two low 4.0Ω on-resistance Hi-Speed USB switches and a current-limited low-voltage 22mΩ BUS switch, and provides an integrated high-voltage external power-switch controller. The BUS switch can start up into large capacitive noncompliant USB loads. The device also features an enable input, a fault output, and an integrated host-charger port-detection circuit adhering to the USB 2.0 battery charging specification.

The device is available in a 16-pin QSOP package, and operates over -40°C to +105°C temperature range.

Features

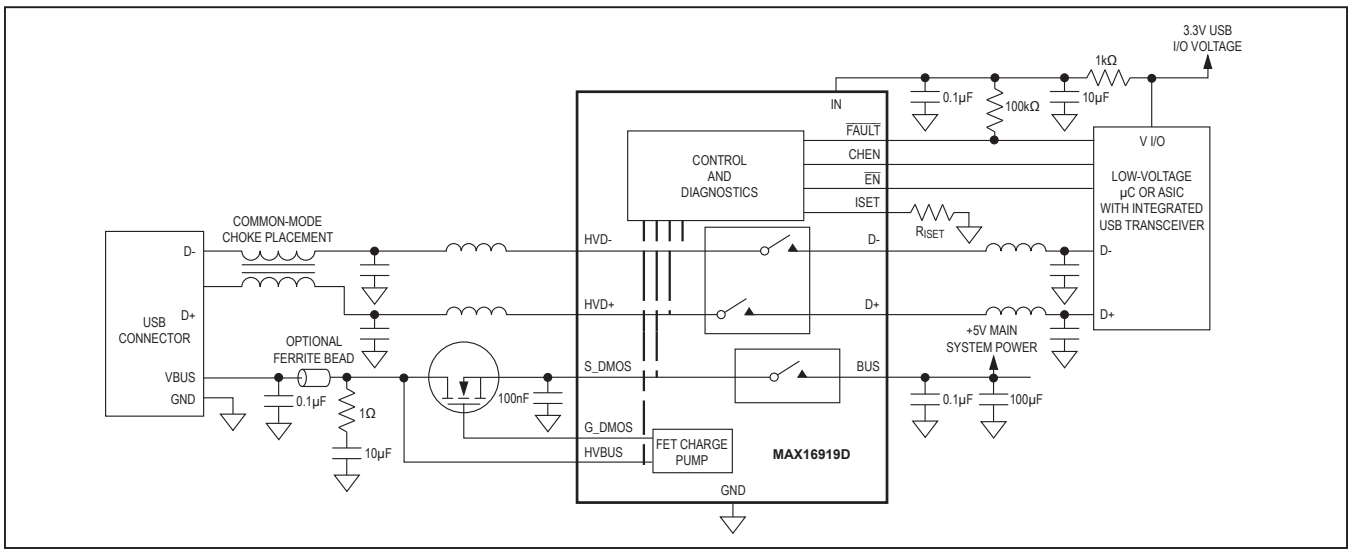
- Two 4.0Ω (typ) R_{ON} USB 2.0 Data Switches
- Current-Limited 22mΩ (typ) BUS Switch with High-Capacitive Load Capability
- 480Mbps or 12Mbps USB 2.0 Operation
- Short-to-Battery and Short-to-GND Protection on Protected HVBUS Output
- Short-to-Battery and Short-to-HVBUS Protection on Protected HVD+ and HVD- Outputs
- 20ms Fault-Blanking Timeout Period
- Integrated Overcurrent and Short-Circuit Autoretry
- Integrated USB Host-Charger Port-Detection Circuitry
- High ESD Protection (HVD+, HVD-, HVBUS)
  - ±15kV Human Body Model
  - ±15kV IEC 61000-4-2 Air Gap
  - ±8kV IEC 61000-4-2 Contact
- 16-Pin (3.90mm x 4.94mm) QSOP Package
- -40°C to +105°C Operating Temperature Range
- AEC-Q100 Qualified

Applications

- Automotive USB Protection

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

IN, BUS, ISET, S_DMOS, D+, D- to GND.....-0.3V to +6V
D+, D- to IN.....+0.3V
EN, $\overline{EN}$, $\overline{FAULT}$, CHEN to GND.....-0.3V to +6V
HVD+, HVD-, HVBUS to GND.....-0.3V to +18V
G_DMOS to GND.....-0.3V to +16V
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.5mW/°C above +70°C).....761mW
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....105°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
BUS Power-Supply Range	V_{BUS}		4.75		5.25	V
IN Power-Supply Range	V_{IN}		3.0		3.6	V
IN Overvoltage Lockout	V_{OVLO}	V_{IN} rising		4.0		V
BUS Input Current	I_{BUS}	Supply for internal blocks, V_{CHEN} = 0V			800	µA
IN Input Current	I_{IN}	V_{CHEN} = V_{IN}			320	µA
CHARGE PUMP						
Unloaded Output Voltage	V_{OCHP}	Referenced to V_{BUS}, internal discharge path 2MΩ to GND	8.0		10.5	V
Output Impedance	R_{OCHP}				50	kΩ
Output DC Current	I_{OCHP}	V_{G_DMOS} - V_{BUS} ≥ 7V	20			µA
D+/D- ANALOG USB SWITCHES						
Analog Signal Range		Guaranteed by R_{ON} measurement (Note 2)	0		3.6	V
Protection Trip Threshold	V_{OV_HVD}		3.7	3.85		V
Protection Response Time	t_{FP_D}	V_{IN} = 4.0V, $V_{HVD\_}$ = 3.3V to 4.3V step, R_L = 15kΩ on D_, delay to $V_{D\_}$ < 3V		6		µs
Overvoltage Blanking Timeout Period	t_{B,OV_D}	From overvoltage condition to $\overline{FAULT}$ asserted		20		ms
On-Resistance	R_{ON}	V_{BUS} = 5V, I_L = 40mA, 0V ≤ $V_{D\_}$ ≤ 3.6V		4.0	8	Ω

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L= ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance Match Between Channels	ΔR_{ON}	V_{BUS} = 5V, I_L = 40mA, $V_{D\_}$ = 1.5V or 3.0V		0.03	0.2	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{BUS} = 5V, I_L = 40mA, $V_{D\_}$ = 0V or 0.4V		0.02		Ω
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	$V_{HVD\_}$ = 18V, $V_{D\_}$ = 0V, T_A = +25°C	-200		200	µA
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{D\_}$ = V_{IN} or 0V, device enabled, T_A = +25°C	-7		+7	µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD\_}$ = 18V, $V_{D\_}$ = 0V, T_A = +25°C	-1		+1	µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance 50Ω, Figure 5		450		MHz
Crosstalk	V_{CT}	R_L = 50Ω, f = 480MHz		-30		dB
On-Capacitance	C_{ON}	f = 1MHz		15		pF
Rise-Time Propagation Delay	t_{PLH}	R_S = R_L = 50Ω		200		ps
Fall-Time Propagation Delay	t_{PHL}	R_S = R_L = 50Ω		200		ps
Output Skew Between Switches	$t_{SK(O)}$	Skew between D+ and D- switch, R_L = 50Ω		50		ps
Output Skew Same Switch	$t_{SK(P)}$	Skew between opposite transitions in same switch, R_L = 50Ω		50		ps
BUS POWER SWITCH						
HVBUS Protection Trip Threshold Absolute	$V_{OV\_BUS, ABS}$	HVBUS rising	5.3	5.5		V
HVBUS Protection Trip Threshold Relative	$V_{OV\_BUS, REL}$	HVBUS rising		V_{BUS} + 0.10		V
Voltage Protection Response Time	t_{FP_BUS}	HVBUS rising		0.3		µs
Overvoltage Fault Blanking Timeout Period	t_{B,OV_BUS}	From overvoltage condition to $\overline{FAULT}$ asserted		20		ms
BUS Undervoltage Lockout	V_{UVLO}	V_{BUS} falling	3.5	3.85	4.2	V
BUS Undervoltage Protection	V_{UV_BUS}	V_{BUS} falling, switch turned off (with R_L = 50Ω on S_DMOS measured when S_DMOS goes low)	4.30	4.45	4.60	V
BUS Undervoltage Protection Response Time	t_{F_BUS}	V_{BUS} falling from 5V with slew rate of 0.5V/µs, switch turned off (with R_L = 50Ω on S_DMOS measured when S_DMOS goes low)		1		µs
BUS Undervoltage Protection Fault Blanking Timeout Period	t_{B,UV_BUS}	From undervoltage condition to $\overline{FAULT}$ asserted		20		ms
On-Resistance	R_{ON}			22	40	mΩ

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Forward-Current Limit	I_{LIM}	R_{ISET} = 51kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	0.52	0.67	0.80	A
		R_{ISET} = 26.4kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	1.18	1.36	1.5	
		R_{ISET} = 15.5kΩ, V_{BUS} - V_{S_DMOS} = 0.5V	2.08	2.37	2.68	
		R_{ISET} = 10.0kΩ, V_{BUS} - V_{S_DMOS} = 0.5V (Note 3)	3.12	3.63	4.28	
Short-Circuit Peak Current Limit	$I_{LIM,SC}$	I_{OUT} pulsing, R_{ISET} = 51kΩ, V_{S_DMOS} = 0V		0.91		APK
		I_{OUT} pulsing, R_{ISET} = 26.4kΩ, V_{S_DMOS} = 0V		1.8		APK
		I_{OUT} pulsing, R_{ISET} = 15.5kΩ, V_{S_DMOS} = 0V		3.0		APK
		I_{OUT} pulsing, R_{ISET} = 10.0kΩ, V_{S_DMOS} = 0V		4.5		APK
Short-Circuit Detect Threshold	V_{SC}	Measured on S_DMOS (Note 4)		1		V
Voltage at ISET	V_{ISET}		1.18	1.24	1.30	V
ISET Short-Detection Threshold	$I_{ISET,SC}$	Switch turned off when current at I_{SET} exceeds value	180	300		µA
Continuous Current-Limit Fault Blanking Timeout Period	$t_{B,ILIM}$	From continuous current-limit condition to $\overline{FAULT}$ asserted	10	20	35	ms
HVBUS Turn-On Delay	t_{ON}	R_{OUT} = 44Ω, C_{OUT} = 4.7µF (from 0% to 10% of V_{OUT})		1.0	3	ms
HVBUS Output Rise Time	t_{RISE}	R_{OUT} = 44Ω, C_{OUT} = 4.7µF (from 10% to 90% of V_{OUT})		0.7	3	ms
HVBUS Turn-Off Delay	t_{OFF}	R_{OUT} = 44Ω, C_{OUT} = 4.7µF (from 100% to 90% of V_{OUT})		0.9	4	ms
HVBUS Output Fall Time	t_{FALL}	R_{OUT} = 44Ω, C_{OUT} = 4.7µF (from 90% to 10% of V_{OUT})		1.5	4	ms
HVBUS Autoreset Current	I_{RETRY}	In latched-off state, V_{HVBUS} = 0V		25		mA
HVBUS Autoreset Threshold	V_{RETRY}	In latched-off state, HVBUS rising		0.5		V
HVBUS Autoreset Blanking Time	$t_{B,RETRY}$	In latched-off state, V_{HVBUS} > 0.5V		20		ms
Off-Leakage Current	I_{LKG_HVBUS}	V_{HVBUS} = 18V, V_{BUS} = 4.75V		230	400	µA
S_DMOS Off-Leakage Current		V_{BUS} = 5.25V, V_{S_DMOS} = 0V, T_A = +25°C	-10		+10	µA
THERMAL PROTECTION						
Thermal Shutdown				+160		°C
Thermal Shutdown Hysteresis				20		°C
$\overline{FAULT}$ OUTPUT						
$\overline{FAULT}$ Output Low Voltage	V_{OL}	I_{SINK} = 500µA			0.5	V
$\overline{FAULT}$ Output High Leakage		T_A = +25°C			1	µA

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = 3.3V, T_J = T_A = -40°C to +105°C, R_L= ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or V_{EN} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN/$\overline{EN}$ INPUT						
Input Logic-High	V_{IH}		1.6			V
Input Logic-Low	V_{IL}				0.5	V
Input Current	$I_{\overline{EN}}$	$V_{\overline{EN}}$ = 0V (MAX16919D), internal 2MΩ pullup to V_{IN}		-1.65		µA
Input Current	I_{EN}	V_{EN} = 3.3V (MAX16919B), internal 2MΩ pulldown to GND		1.65		µA
CHEN INPUT						
Input Current	I_{CHEN}	V_{CHEN} = 3.3V, internal 2MΩ pulldown to GND		1.65		µA
Input Logic-High	$V_{IH,CHEN}$		1.6			V
Input Logic-Low	$V_{IL,CHEN}$				0.5	V
USB 2.0 CHARGING SPEC, D+/D-/CHEN						
Input Logic-High	$V_{IH,U}$		2.0			V
Input Logic-Low	$V_{IL,U}$				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	100	150	µA
Data-Detect Voltage High	V_{DAT_REFH}		0.4			V
Data-Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data-Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data Source Voltage	V_{DAT_SRC}		0.5		0.7	V
Data Source Load Current	I_{DAT_SRC}				200	µA
ESD PROTECTION FOR ALL INPUTS AND OUTPUTS EXCEPT HVD+, HVD-, AND HVBUS						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION FOR HVD+, HVD-, HVBUS						
ESD Protection Level	V_{ESD}	Human Body Model		±15		kV
		IEC 61000-4-2 Air Gap Discharge		±15		
		IEC 61000-4-2 Contact Discharge		±8		

Note 2: Design guaranteed by ATE characterization. Limits are not production tested.
Note 3: Design guaranteed by bench characterization. Limits are not production tested.
Note 4: Short-circuit detect threshold is the output voltage at which the device transitions from short-circuit current limit to continuous current limit.

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

Timing Diagrams/Test Circuits

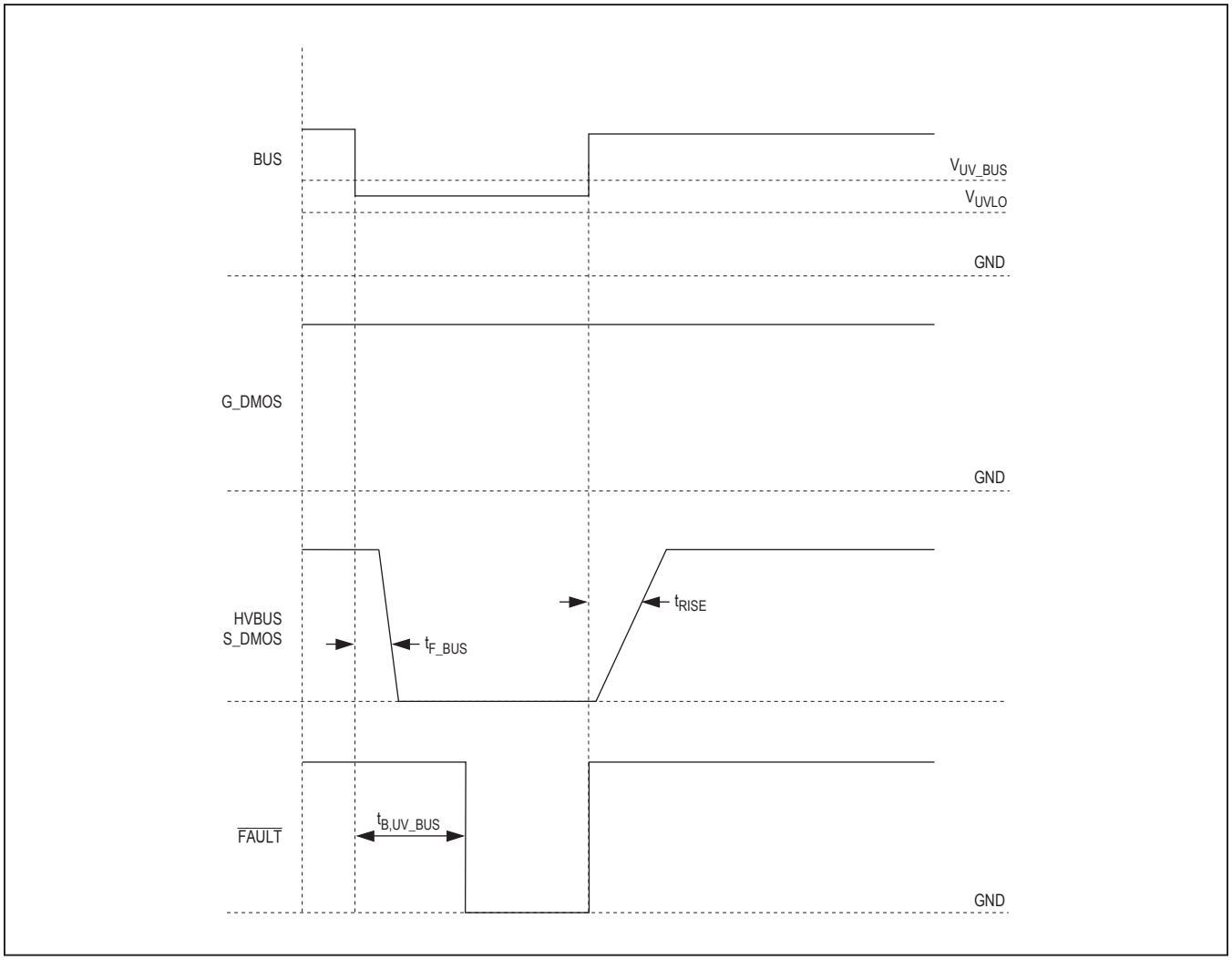


Figure 1. Timing Diagram for Undervoltage Event on BUS

Timing Diagrams/Test Circuits (continued)

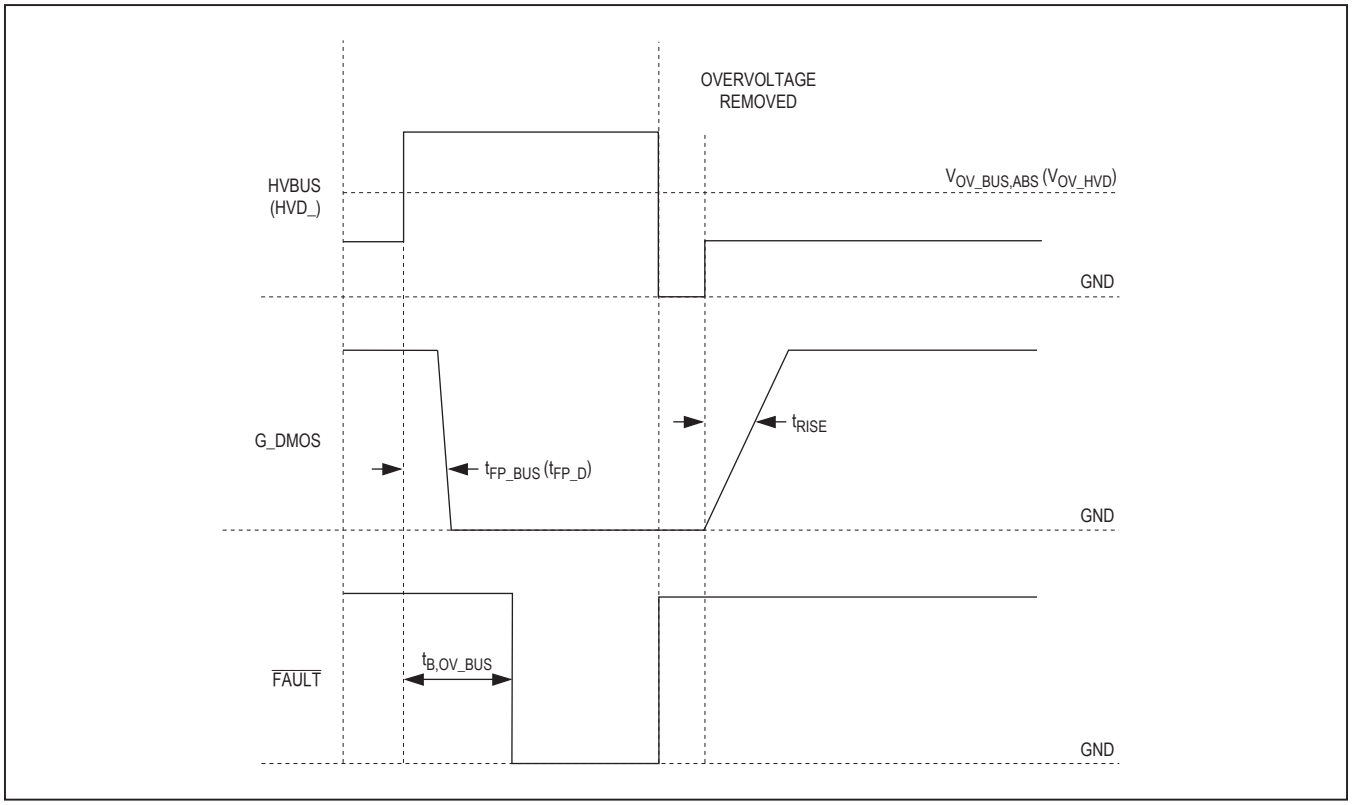


Figure 2. Timing Diagram for Overvoltage Protection on HVBUS, HVD+, and HVD-

Timing Diagrams/Test Circuits (continued)

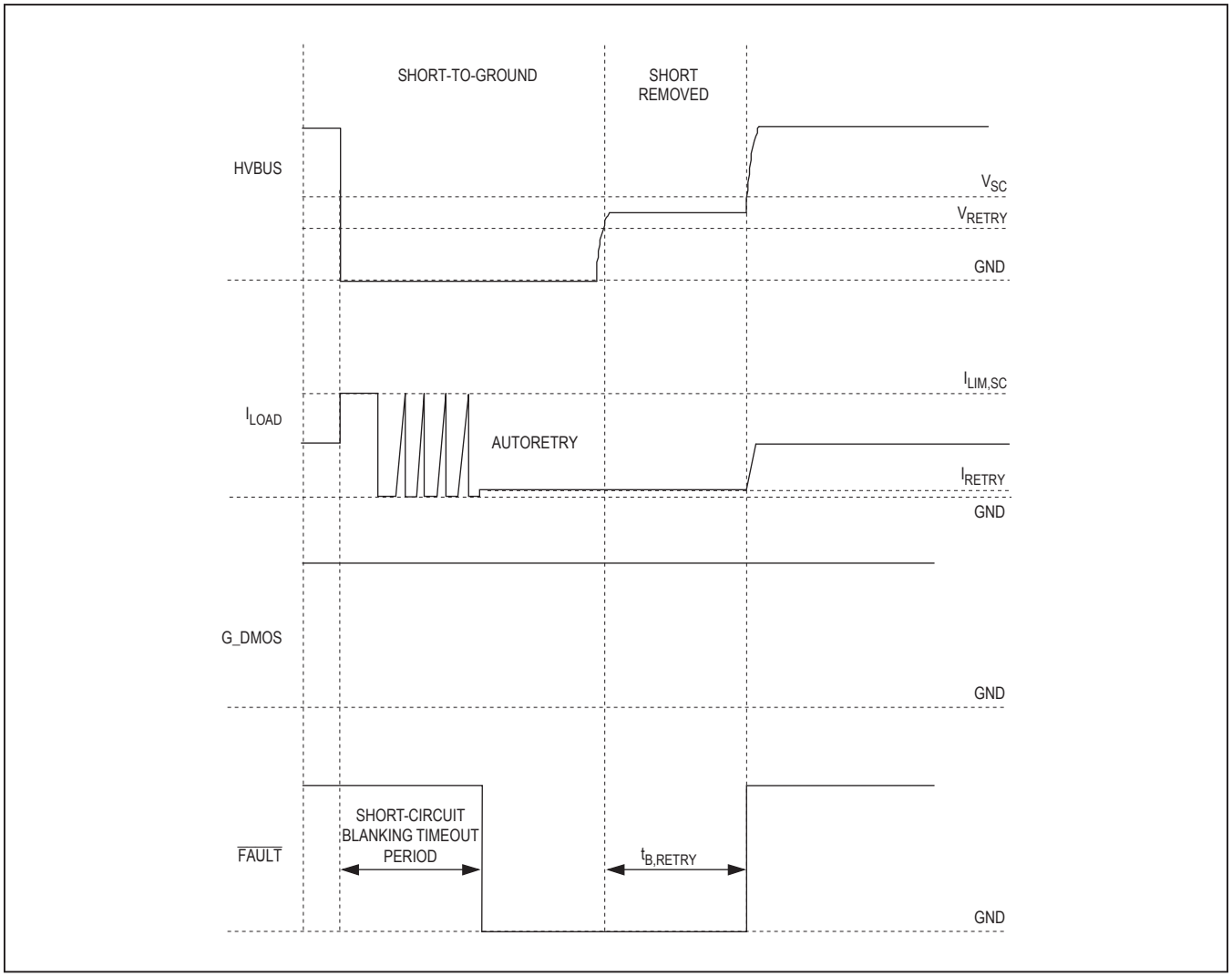


Figure 3. Timing Diagram for Short-to-Ground Protection

Timing Diagrams/Test Circuits (continued)

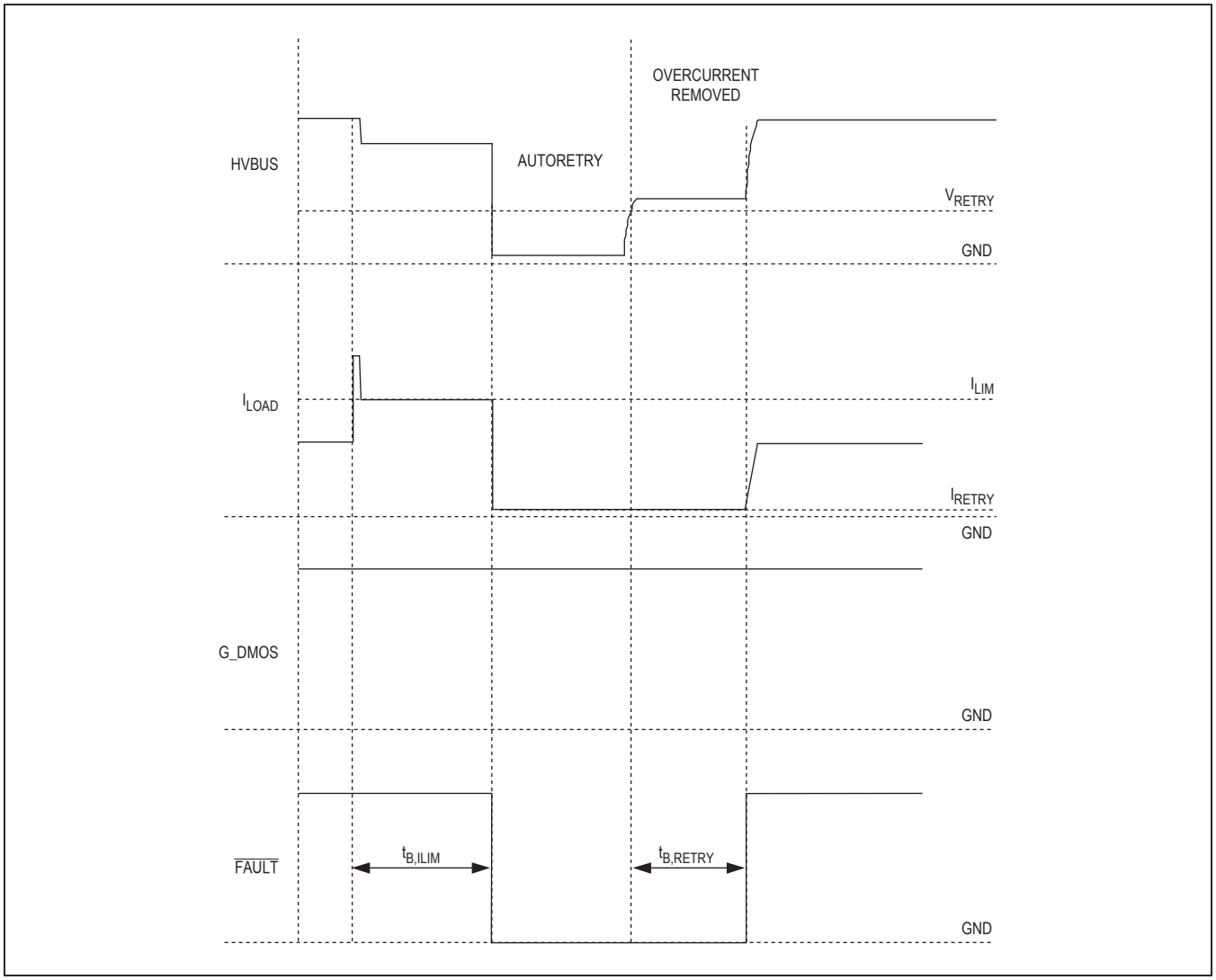


Figure 4. Timing Diagram for Overcurrent Protection

Timing Diagrams/Test Circuits (continued)

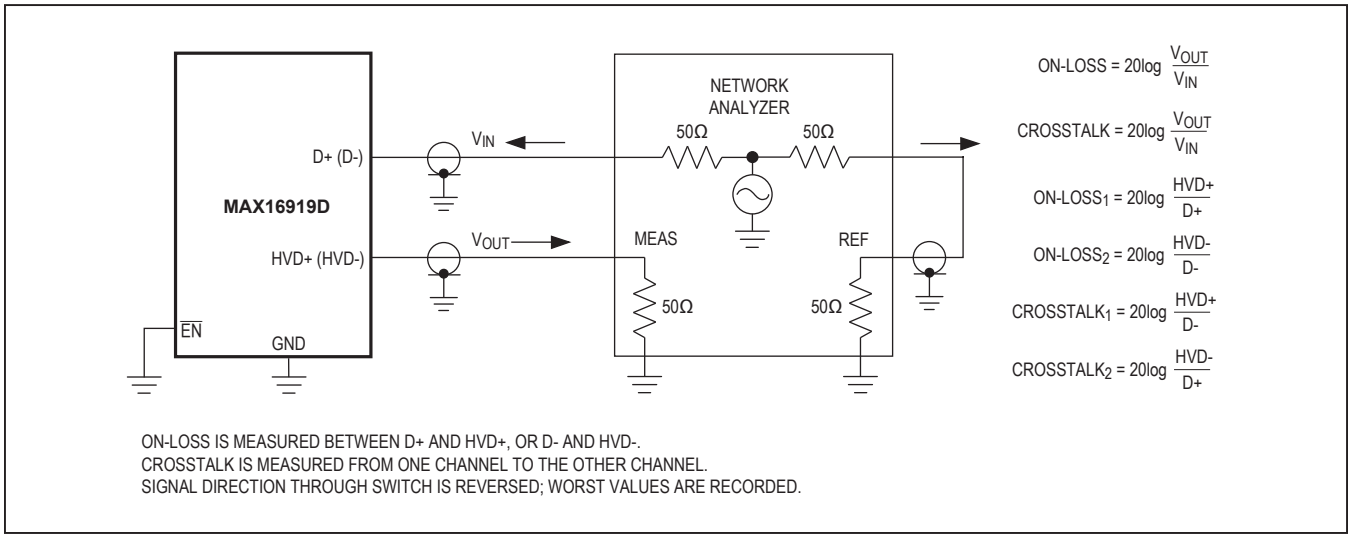


Figure 5. On-Channel -3dB Bandwidth and Crosstalk

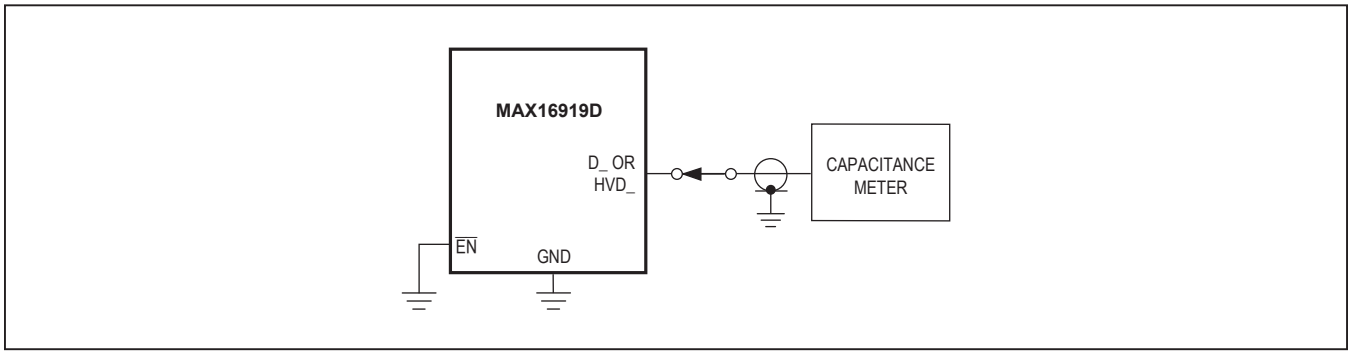


Figure 6. On-Capacitance

Timing Diagrams/Test Circuits (continued)

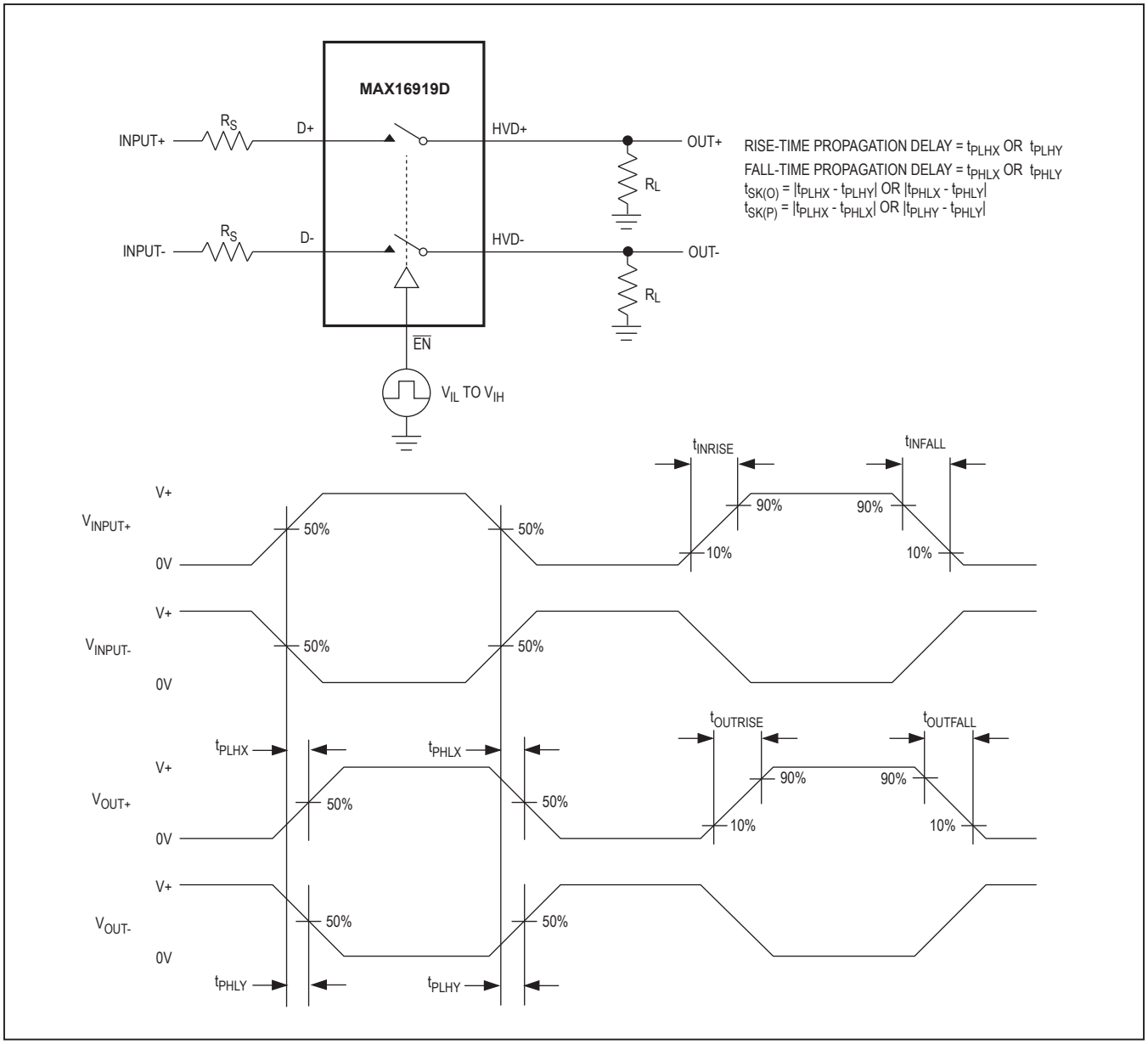
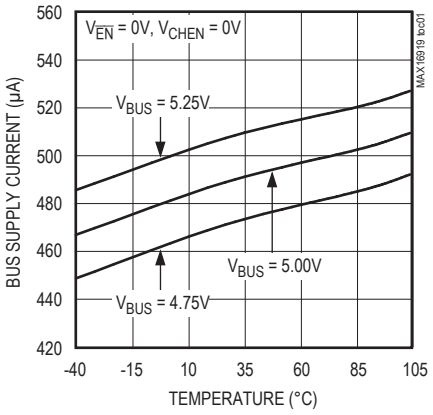


Figure 7. Propagation Delay and Output Skew

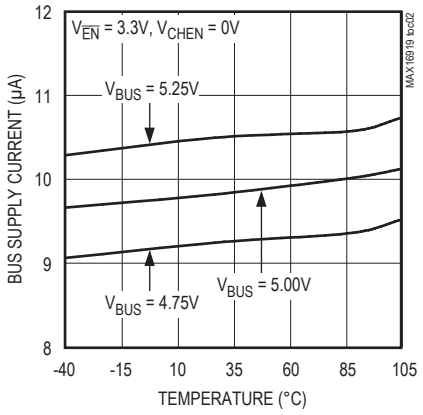
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

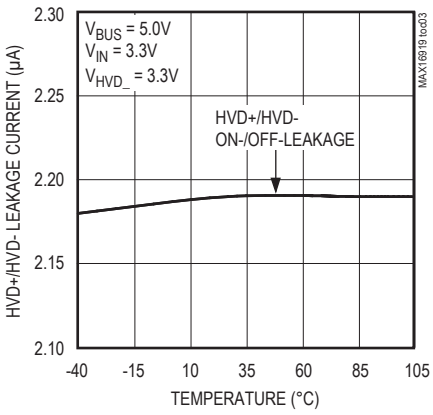
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = GND)



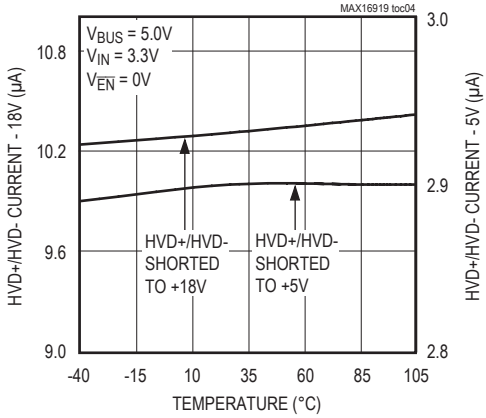
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = IN)



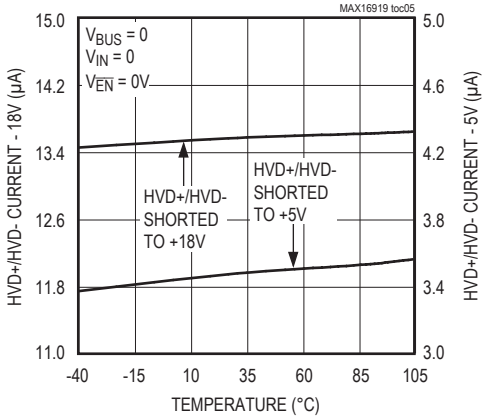
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



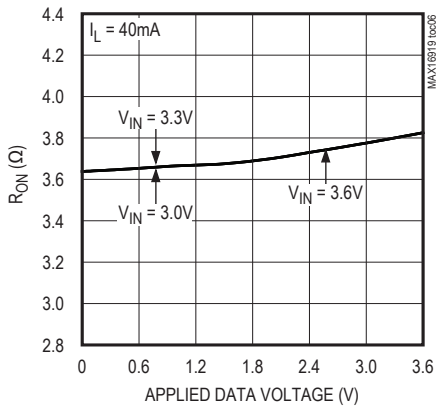
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



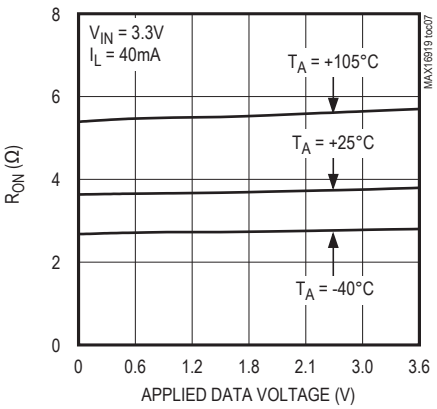
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



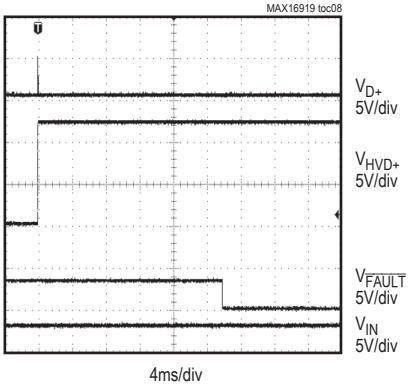
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



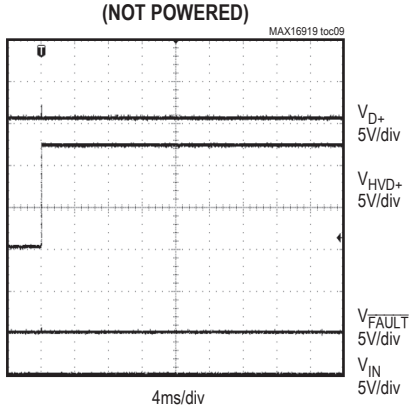
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

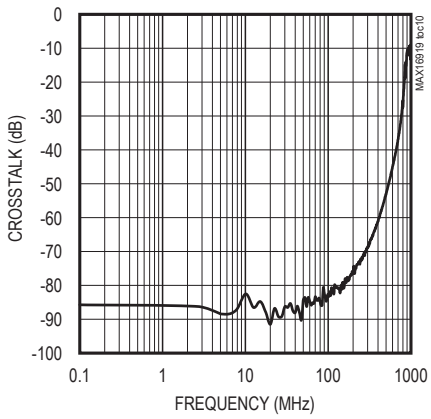
SHORT-TO-BATTERY TURN-OFF RESPONSE



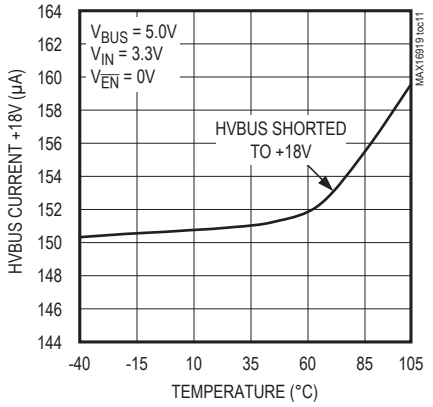
SHORT-TO-BATTERY TURN-OFF RESPONSE (NOT POWERED)



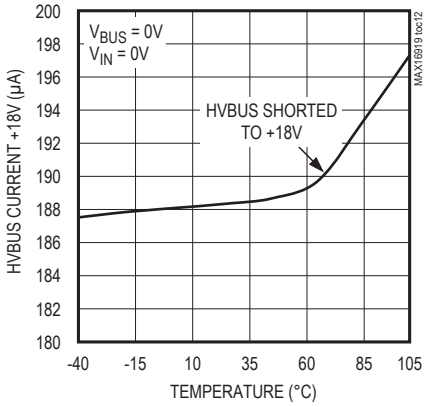
CROSSTALK



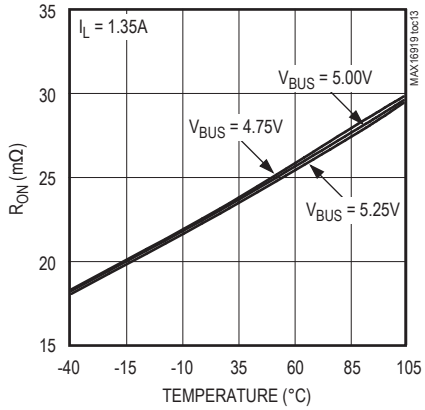
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



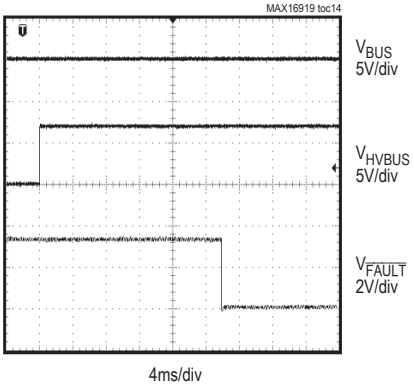
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



BUS R_{ON} vs. TEMPERATURE



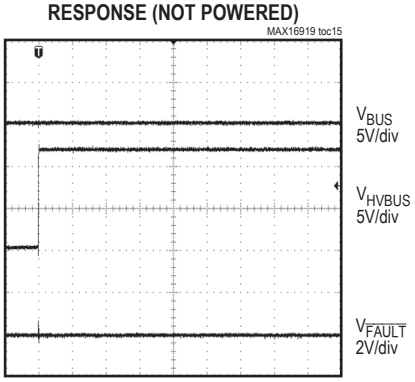
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



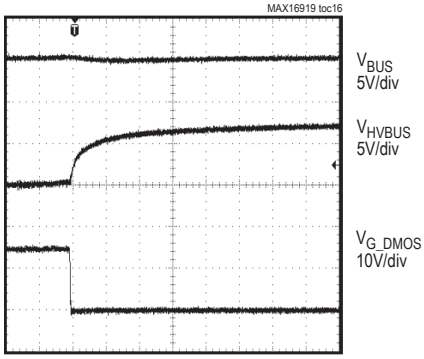
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

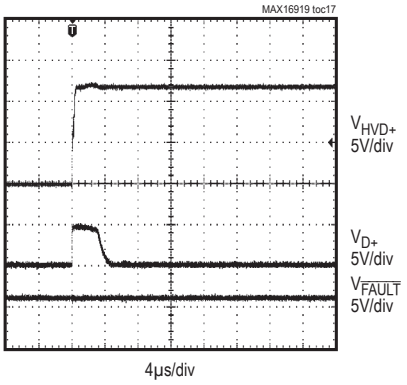
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE (NOT POWERED)



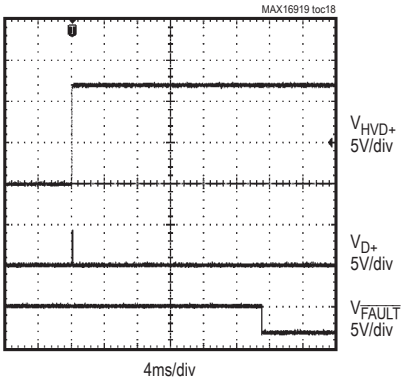
HVBUS SHORT-TO-BATTERY TURN-OFF G_DMOS RESPONSE



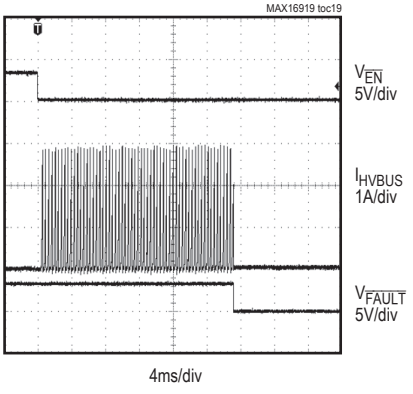
HVD+/HVD- SHORT-TO-BATTERY TURN-OFF RESPONSE



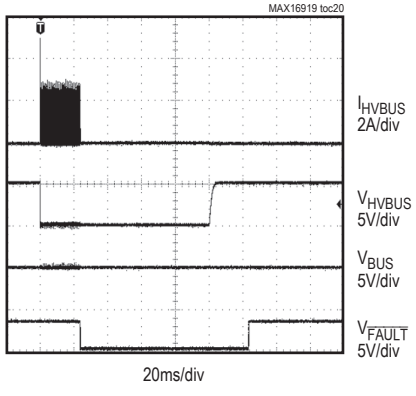
HVD+/HVD- SHORT-TO-BATTERY TURN-OFF RESPONSE



DEVICE ENABLED INTO SHORT-TO-GROUND



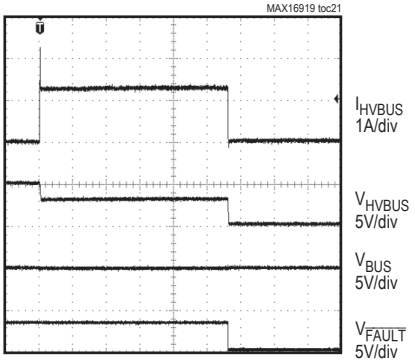
HVBUS SHORT-CIRCUIT AUTORETRY RESPONSE



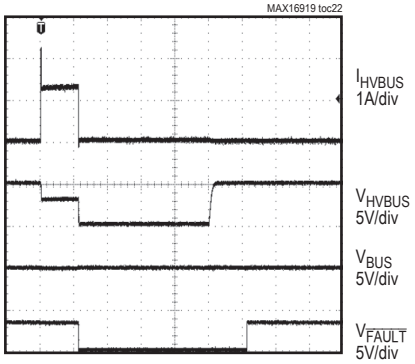
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

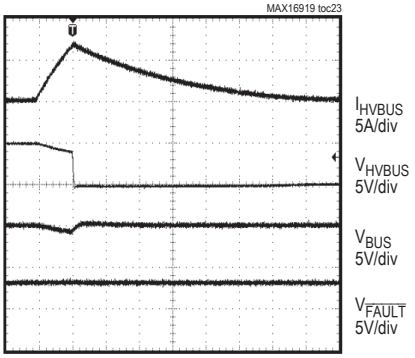
HVBUS OVERCURRENT RESPONSE



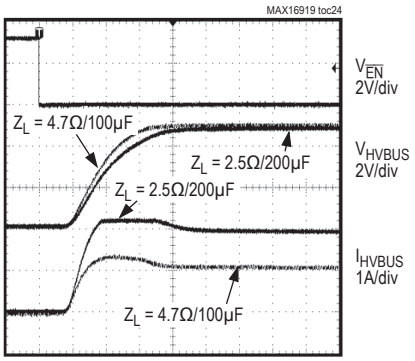
HVBUS OVERCURRENT AUTORETRY RESPONSE



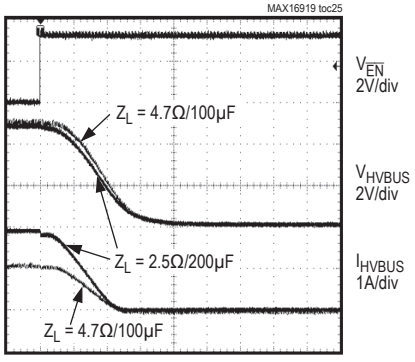
SHORT-TO-GROUND INRUSH



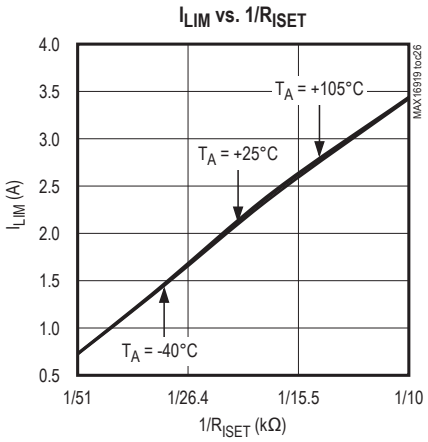
INRUSH CURRENT $\overline{EN}$ ON RESPONSE WITH RC LOAD



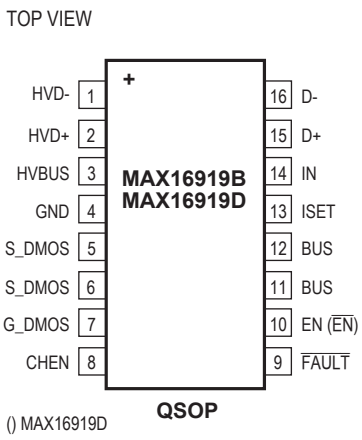
DISCHARGE CURRENT $\overline{EN}$ OFF RESPONSE WITH RC LOAD



I_{LIM} vs. $1/R_{ISET}$



Pin Configuration



Pin Description

PIN		NAME	FUNCTION
MAX16919B	MAX16919D		
1	1	HVD-	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- directly to USB connector D-.
2	2	HVD+	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ directly to USB connector D+.
3	3	HVBUS	High-Voltage Bus and DMOS Drain Connect. Connect to the drain of an external n-channel DMOS and to the USB connector BUS.
4	4	GND	Ground
5, 6	5, 6	S_DMOS	DMOS Source Input. Connect to the source of an external n-channel DMOS. Connect both S_DMOS pins together and bypass S_DMOS to GND with a 100nF ceramic capacitor placed close to the S_DMOS pin.
7	7	G_DMOS	DMOS Gate-Drive Output. Connect to the gate of an external n-channel DMOS.
8	8	CHEN	Charger-Detect Enable. Connect CHEN to a microprocessor I/O. Drive CHEN high to enable USB host-charger port detection.
9	9	$\overline{\text{FAULT}}$	Active-Low Open-Drain Fault Indicator Output
10	—	EN	Active-High Enable Input. Connect EN to a microprocessor I/O. Drive EN high to enable the device.
—	10	$\overline{\text{EN}}$	Active-Low Enable Input. Connect $\overline{\text{EN}}$ to a microprocessor I/O. Drive $\overline{\text{EN}}$ low to enable the device.
11, 12	11, 12	BUS	USB Power Supply. Connect BUS to +5V USB supply. Connect both BUS inputs together for proper operation. Bypass BUS to GND with 0.1µF and 100µF ceramic capacitors.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX16919B	MAX16919D		
13	13	ISET	Forward-Current Limit Set. Set the forward-current limit of the power switch using a resistor to GND. See the *Forward-Current Limit* section.
14	14	IN	Logic Power-Supply Input. The supply voltage range is from +3.0V to +3.6V. Place a 1kΩ resistor between logic supply and IN. Bypass IN to GND with 0.1µF and 10µF ceramic capacitors.
15	15	D+	USB Differential Data D+ Input. Connect D+ to low-voltage USB transceiver D+.
16	16	D-	USB Differential Data D- Input. Connect D- to low-voltage USB transceiver D-.

Detailed Description

The MAX16919 provides high-ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The device supports both Hi-Speed USB (480Mbps) and full-speed USB (12Mbps) operation. In addition, the device includes integrated circuitry to enable fast-charging for consumer devices adhering to the Hi-Speed USB host-charger port-detection protocol.

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. The device is capable of a short-to-battery condition of up to +18V. Short-to-GND and overcurrent protection are also provided on the HVBUS output to protect the internal BUS power rail from overcurrent faults.

The device features high-ESD protection to ±15kV Air Gap method and ±8kV Contact method on all protected HVBUS, HVD+, and HVD- outputs.

The device features two low 4.0Ω on-resistance Hi-Speed USB switches and a current-limited low-voltage 22mΩ BUS switch, and provides an integrated high-voltage external power-switch controller. The device also features an enable input, a fault output, and an integrated host-charger port-detection circuit adhering to the USB 2.0 battery charging specification.

D+ and D- Protection

D+/D- protection consists of ESD and OVP (overvoltage protection) for both 12Mbps and 480Mbps USB transceiver applications. ESD protection is ±15kV (Air Gap method) and ±8kV (Contact method) per IEC 61000-4-2. OVP protection up to 18V is provided for short-to-battery conditions in the vehicle harness to prevent damaging the low voltage USB transceiver. This is accomplished with an extremely low-capacitance high-voltage FET in series with the D+ or D- path. Overcurrent short-to-GND protection for D+ and D- is provided by the upstream USB transceiver.

BUS Protection

Power to the USB connector is provided through an externally controlled high-voltage FET and an internal, current-limited protected FET. The design can withstand short-to-battery conditions of up to 18V, short-to-ground, and can withstand the ±15kV (Air Gap method)/±8kV (Contact method) ESD requirement. The internal FET has an adjustable current limit from 500mA up to 3A.

The HVBUS short-to-battery protection is done with an external power FET. The gate of this FET is driven by an internal charge pump that generates a minimum 7V gate-source voltage.

All overvoltage protection switches are guaranteed to be off when power is not applied to the device.

Fault Conditions

Table 1 summarizes the conditions that generate a fault and actions taken by the device.

Fault Output ($\overline{FAULT}$)

The device features an active-low, open-drain fault output. $\overline{FAULT}$ goes low when there is a fault condition. Fault detection includes short-to-battery, short-to-GND, or overcurrent on HVBUS, overvoltage on HVD+ or HVD-, overheating in the device, and a low R_{ISET} value. Connect a 100kΩ pullup resistor from $\overline{FAULT}$ to IN.

Table 1. Fault Conditions

EVENT	CONDITION	ACTION TAKEN
Overvoltage on the Data Lines (High-Voltage Side)	V_{HVD+} or V_{HVD-} > 3.85V	The device immediately shuts off the external power switch and the USB data switches. The fault indicator asserts when the overvoltage condition persists for more than 20ms.
Overvoltage on IN	V_{IN} > 4.0V	The device immediately shuts off the external power switch and the USB data switches. The fault indicator asserts when the overvoltage condition persists for more than 20ms.
Overvoltage on the High-Voltage Bus	V_{HVBUS} > (V_{BUS} + 0.1V) or 5.5V	The device immediately shuts off the external power switch and the USB data switches. The fault indicator asserts when the overvoltage condition persists for more than 20ms.
Shorting the High-Voltage Bus to Ground	V_{HVBUS} < 1V	When HVBUS falls below 1V, the device produces a pulsed current with a peak value of 1.2 x I_{LIM} (forward-current limit). The fault indicator asserts when the short condition persists for more than 20ms and the device enters autoreset mode. In autoreset mode, the device reduces the bus current to 25mA. When the short condition is removed (i.e., V_{HVBUS} rises and remains above 0.5V for 20ms), the fault indicator deasserts and the gate driver slowly turns on the power switch.
Overcurrent on the High-Voltage Bus	V_{HVBUS} > 1V	The device detects an overcurrent when the high-voltage bus current exceeds the foward-current limit (I_{LIM}), but the bus voltage remains above 1V. Upon detecting an overcurrent condition, the device regulates the current at I_{LIM}. The fault indicator asserts when the condition persists for more than 20ms and the device enters into autoreset mode. In autoreset mode, the device reduces the bus current to 25mA. When the over-current condition is removed (i.e., V_{HVBUS} rises and remains above 0.5V for 20ms), the fault indicator deasserts and the gate driver slowly turns on the power switch.
Undervoltage on BUS	V_{BUS} < 4.45V	The device immediately shuts off the internal current-limited switch. The fault indicator asserts when undervoltage condition (3.85V < V_{BUS} < 4.45V) persists for more than 20ms.
	V_{BUS} < 3.85V	The device immediately shuts off the internal current-limited switch, USB data switches, and digital logic circuitry.
Overheating	T_J > +160°C	The device immediately shuts off the external power switch, internal current-limited switch, and the USB data switches. The fault indicator asserts immediately when the junction temperature exceeds +160°C. The device has a thermal hysteresis of 20°C. The fault indicator deasserts when the junction temperature falls below +140°C.
R_{ISET} Value Too Low	I_{ISET} > 300µA	The device immediately shuts off the external power switch and the USB data switches. The fault indicator asserts immediately when ISET sources more than 300µA (typ).

Enable Input (EN/$\overline{EN}$)

The device features active-high or active-low enable logic (see the *Ordering Information* table). While V_{CHEN} = 0V, drive EN ($\overline{EN}$) high (low) for normal operation and to enable the protection switches. This allows BUS power, D+, and D- USB signals to pass through the device. Drive EN/($\overline{EN}$) low (high) to disable the device and to turn off the power and USB data switches.

CHEN Input

When the MAX16919 is active (EN = 1, $\overline{EN}$ = 0), use CHEN to enable the device's internal USB host-charger port-detection circuitry (Figure 8). The device's internal charge-detect circuitry allows the peripheral device attached to it to determine if it is connected to a USB port capable of supplying greater than the typical 500mA. If detected, the peripheral device enables its internal battery charger to enter fast-charge mode and begins charging above 500mA at its maximum capable current. EN ($\overline{EN}$) should only be inactivated at the same time as CHEN or when CHEN is already inactive.

Connect CHEN to an I/O port on the host system microprocessor that has access to the USB transceiver. This is needed to place the device into one of its three operating modes: disabled, USB Hi-Speed (HS) mode, and USB low-speed (LS)/full-speed (FS) mode with host-charger port detection.

Disabled Mode

This is the lowest power mode for the device. In this mode, both the USB BUS power, HVD+ to D+ and HVD- to D-, data paths are disabled.

USB Low-Speed/Full-Speed (LS/FS) Mode with Host-Charger Port Detection

After a USB-compliant portable device detects VBUS, it is allowed to check if the host device is a host charger by applying a voltage to HVD+ and checking the voltage on HVD-. At this time, it is assumed that HVD+ and HVD- are logic-low, which means that the voltage is less than 0.8V and CHEN is logic-high. Then the port-detection circuit is enabled and switch 1 is on (Figure 8).

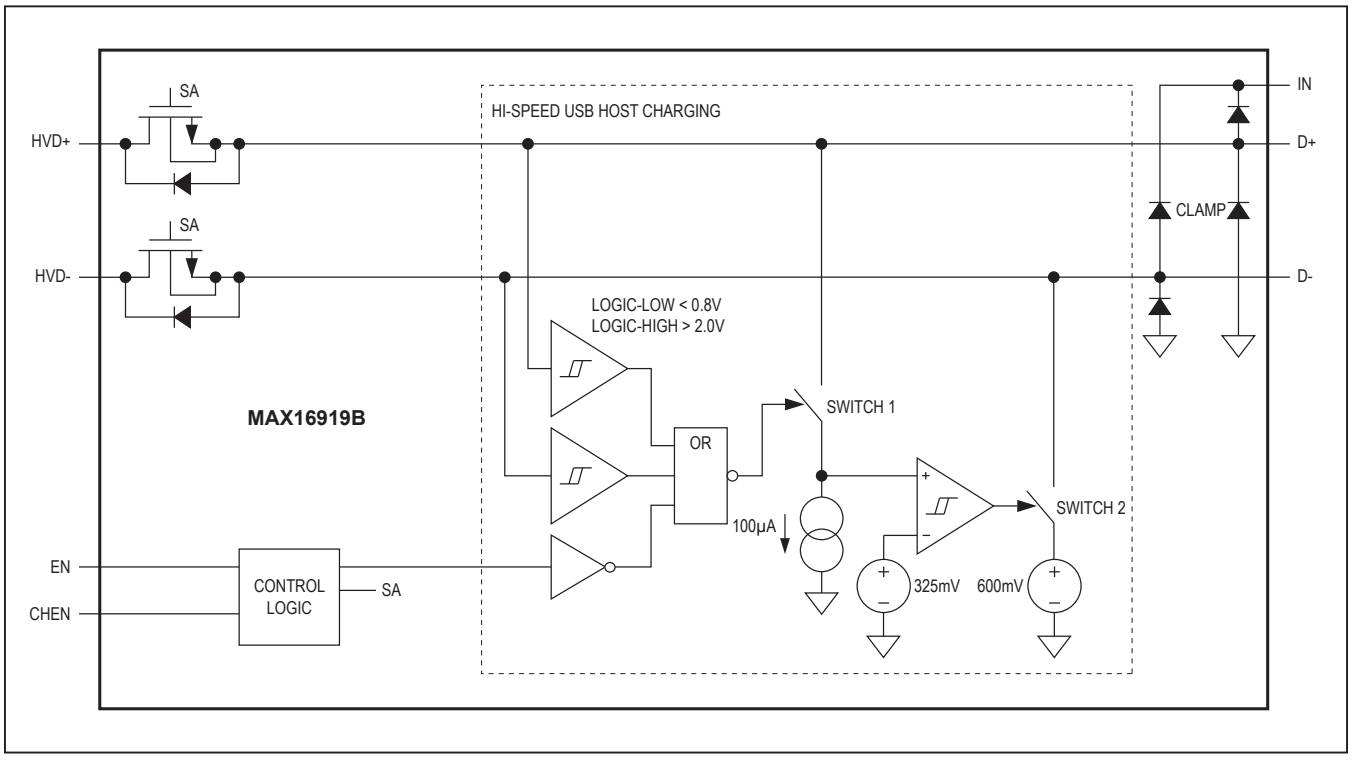


Figure 8. Host-Charger Port-Detection Circuit

The portable device drives HVD+ to 0.6V (typ). The comparator closes switch 2 and the D- line is then driven to 0.6V (typ). The portable device can now detect that it is connected to a USB host charger.

When a full-speed (FS) device connects, it pulls the D+ line logic-high to a voltage greater than 2V. Then switch 1 opens, the positive input of the comparator is forced to zero, and switch 2 is also opened. Because D- is low, the portable device detects that it is connected to a host charger.

When a low-speed (LS) device connects, it pulls the D- line logic-high (after it has stopped driving HVD+ to 0.6V). Because D+ stays low, the portable device detects that it is connected to a host charger.

When the portable device has connected in low-speed or full-speed mode, either D+ or D- is logic-high upon enumeration, which disables the charger-detect circuit. A delay is implemented that closes switch 1 after HVD+ and HVD- are logic-low longer than 100µs. This ensures that switch 1 stays off when the logic-high states of D+ and D- do not overlap.

If a Hi-Speed-capable device connects to the port and CHEN is logic-high, it can detect that it is connected to a host charger. Upon enumeration, and before entering Hi-Speed mode, the host system microprocessor must query the USB transceiver to determine if Hi-Speed mode is needed. If so, it must drive the CHEN input low to disable the port-detection circuit and enter USB Hi-Speed mode. The host system microprocessor must also query the USB transceiver to detect when the Hi-Speed portable device is disconnected or no longer in Hi-Speed mode. Once detected it must drive the CHEN input high to re-enable the port-detection circuit for the next connection sequence. This is needed as the Hi-Speed differential logic levels on HVD+ and HVD- are below 500mV.

USB Hi-Speed (HS) Mode

USB Hi-Speed (HS) mode provides true pass-through operation for USB Hi-Speed (480Mbps) data signals and disables the USB host-charger port-detection circuitry. Place the device into this mode when the USB transceiver requests to enter Hi-Speed mode.

Applications Information

Foward-Current Limit

The device allows the current limit of the power switch to be set by a resistor. As shown in the forward-current limit specification of the *Electrical Characteristics* table, the typical current limit can vary by ±20% to ±25%. Assume variation of ±25% for forward-current limit between 500mA and 1A. For current limit above 1A, assume ±20% variation. The maximum expected current in the application determines the worst-case minimum current limit value to be set. It is recommended to have an additional 5% margin to prevent triggering the current limit at the maximum expected current limit in the application. To find the correct value for R_{ISET}, modify the desired current limit value for the application ($I_{LIM,MIN}$) with a factor 1.33 (> 1A) to 1.43 (< 1A), which corresponds to the above mentioned variations including 5% margin:

$$I_{LIM,TYP} = \text{factor} \times I_{LIM,MIN}$$

The resistor value is then calculated as:

$$R_{ISET} = 35{,}650/I_{LIM,TYP}$$

Examples for R_{ISET} are given in the *Electrical Characteristics* table and correspond to 0.5A, 1.2A, 2.1A, and 3.1A maximum current in the application.

The device accommodates a forward current-limit range of 500mA to 3A. The short-circuit peak current limit is set 20% higher than the forward-current limit.

Selecting the External n-Channel DMOS Device

The external power DMOS device must be a 20V V_{GS} type. The charge pump generates at least 7V V_{GS}, which guarantees low R_{ON} for nonlogic-level devices.

Power-Supply Bypass Capacitor

Bypass HVBUS to GND with a 0.1µF ceramic capacitor as close as possible to the USB connector to provide ±15kV (HBM) ESD protection. Parasitic inductance and capacitance due to long wire lengths between the load and HVBUS form an LC tank circuit, which can cause overshoots that violate absolute maximum ratings.

Ferrite beads to reduce EMI should be placed between the 0.1µF ceramic connector capacitor and HVBUS node. Connect a 1Ω resistor in series with a 10µF capacitor on the HVBUS node to GND to avoid overshoots on HVBUS. Bypass BUS to GND with minimum 100µF, low-ESR ceramic capacitor to avoid large droops on BUS when hot-plugging discharged capacitors on HVBUS. Bypass BUS to GND with a 0.1µF capacitor.

Bypass IN to GND with 0.1µF and 10µF ceramic capacitors. Place a 1kΩ resistor between the logic supply and IN node to ensure optimal ESD performance.

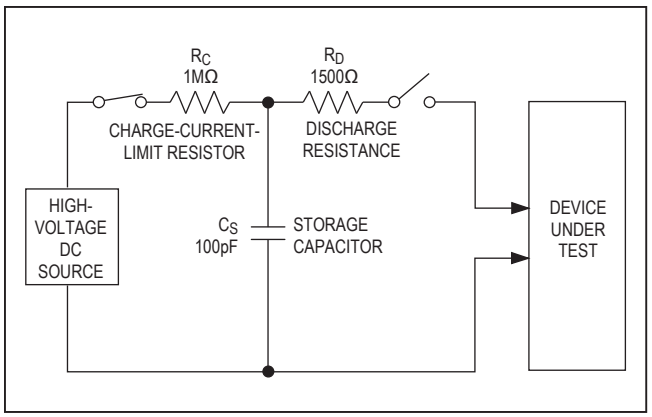


Figure 9. Human Body ESD Test Model

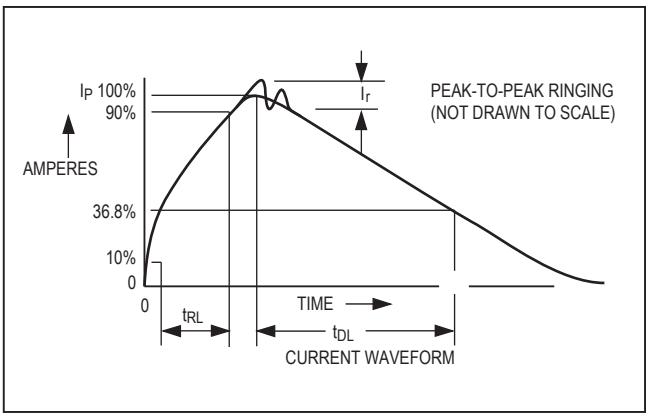


Figure 10. Human Body Current Waveform

Wire Length

The wire length between USB peripheral and the HVBUS, HVD+, and HVD- each should be in the 0.5m to 5m range for proper operation, which corresponds to approximately 650nH to 6.5mH inductance. A minimum wire length is needed for limiting the current slew rate for the short-to-battery and short-to-ground events.

Layout of USB Data Line Traces

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance matched traces of equal lengths. Insert tuning peaking inductors and capacitors on both the HVD_ and D_ pins to tune out parasitic capacitance. The values are layout dependent. Contact Maxim Applications for assistance.

±15kV ESD Protection

Maxim devices incorporate ESD-protection structures to protect against electrostatic discharges encountered during handling and assembly. The device provides additional protection against static electricity. Maxim's state-of-the-art structures protect against ESD of ±15kV on HVD+, HVD-, and HVBUS. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the device continues to work without latchup. Other solutions can latchup and require the power to be cycled to remove latchup. The device is characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±15kV using the IEC 61000-4-2 Air Gap method
3) ±8kV using the IEC 61000-4-2 Contact Discharge method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 9 shows the Human Body Model, and Figure 10 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

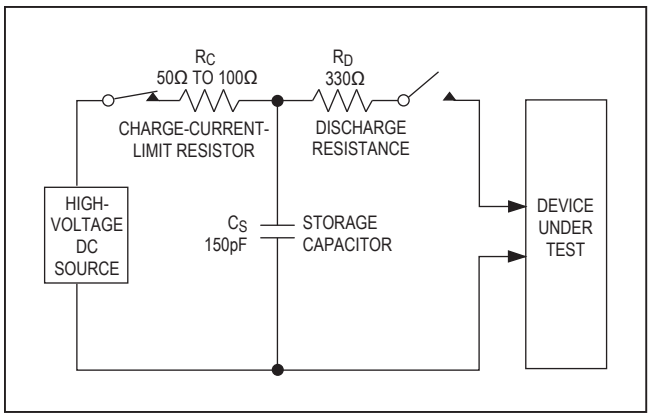


Figure 11. IEC 61000-4-2 ESD Test Model

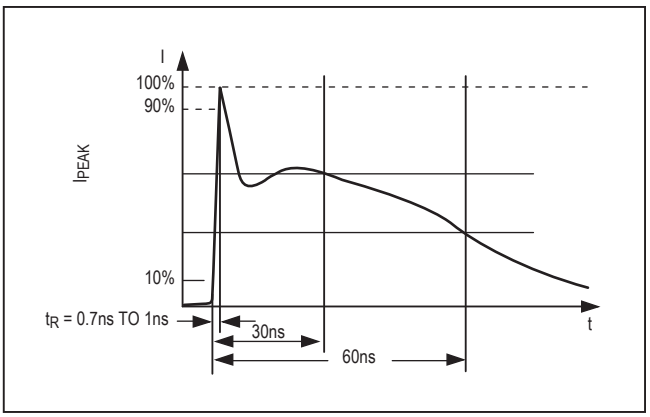
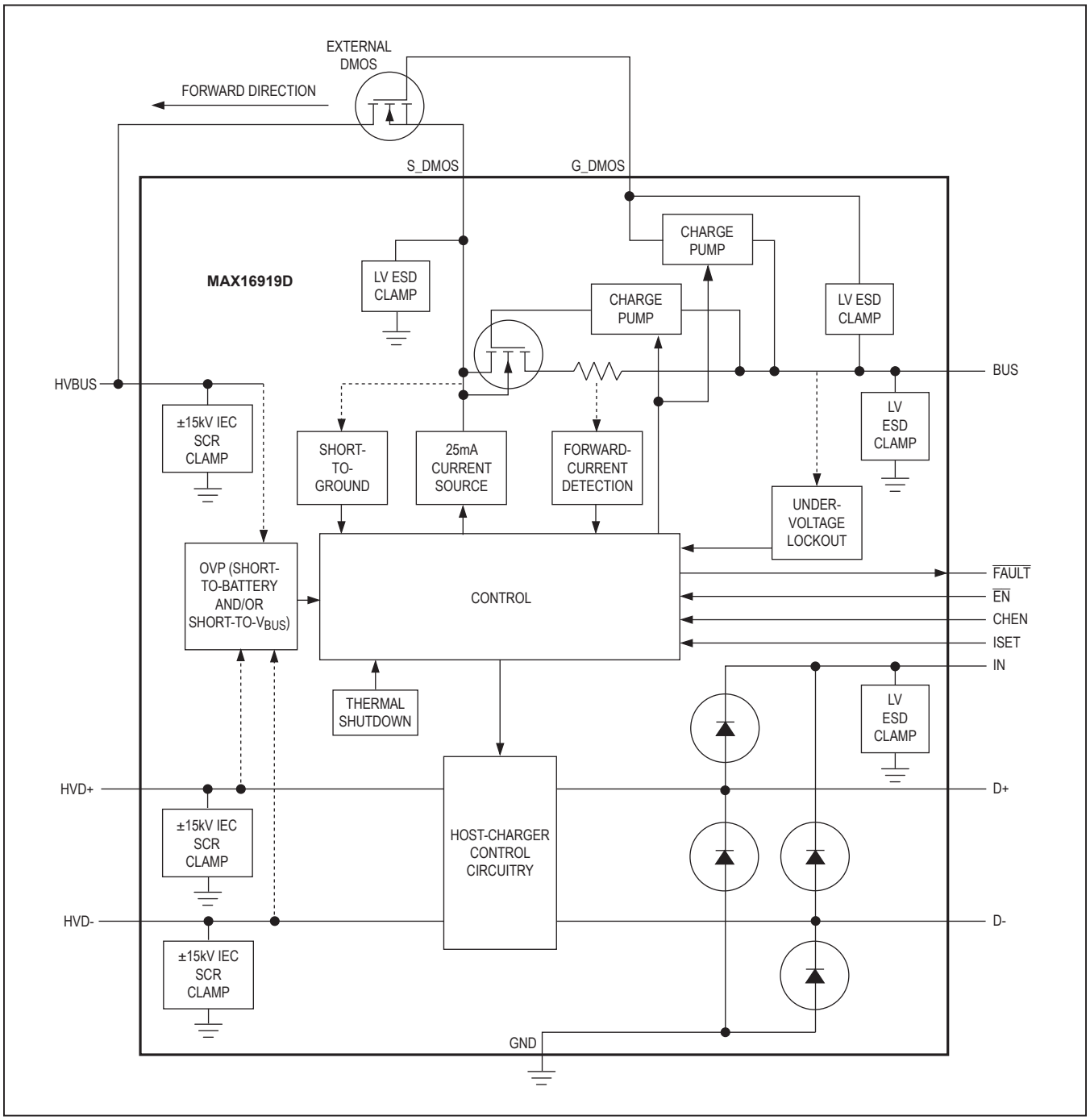


Figure 12. IEC 61000-4-2 ESD Generator Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The device helps users design equipment that meet Level 4 of IEC 61000-4-2. The Human Body Model testing is performed on unpowered devices, while IEC 61000-4-2 is performed while the device is powered. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 11), the ESD with-stand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 12 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Functional Diagram



Ordering Information

PART	PIN-PACKAGE	ENABLE INPUT LOGIC	FAULT OUTPUT LOGIC
MAX16919BGEE/V+	16 QSOP	High	Low
MAX16919DGEE/V+	16 QSOP	Low	Low

Note: *All devices operate over the -40°C to +105°C temperature range.*
/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+5	**21-0055**	**90-0167**