19-4443; Rev 0; 2/09

EVALUATION KIT AVAILABLE

AMD 2-/3-Output Mobile Serial VID Controller

General Description

The MAX17480 is a triple-output, step-down, fixed-frequency controller for AMD's serial VID interface (SVI) CPU and northbridge (NB) core supplies. The MAX17480 consists of two high-current SMPSs for the CPU cores and one 4A internal switch SMPS for the NB core. The two CPU core SMPSs run 180° out-of-phase for true interleaved operation, minimizing input capacitance. The 4A internal switch SMPS runs at twice the switching frequency of the core SMPS, reducing the size of the external components.

The MAX17480 is fully AMD SVI compliant. Output voltages are dynamically changed through a 2-wire SVI, allowing the SMPSs to be individually programmed to different voltages. A slew-rate controller allows controlled transitions between VID codes and controlled soft-start. SVI also allows each SMPS to be individually set into a low-power pulse-skipping state.

Transient phase repeat improves the response of the fixed-frequency architecture, reducing the total output capacitance for the CPU core. A thermistor-based temperature sensor provides a programmable thermal-fault output ($\overline{\text{VRHOT}}$).

The MAX17480 includes output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection. When any of these protection features detect a fault, the controller shuts down. True differential current sensing improves current limit and load-line accuracy. The MAX17480 has an adjustable switching frequency, allowing 100kHz to 600kHz operation per core SMPS, and twice that for the NB SMPS.

Applications

Mobile AMD SVI Core Supplies

Multiphase CPU Core Supplies

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Pin Configuration appears at end of data sheet.

Features

- Dual-Output Fixed-Frequency Core Supply Controller
    - Split or Combinable Outputs Detected at Power-Up
    - Dynamic Phase Selection Optimizes Active/Sleep Efficiency
    - Transient Phase Repeat Reduces Output Capacitance
    - True Out-of-Phase Operation Reduces Input Capacitance
    - Programmable AC and DC Droop
    - Accurate Current Balance and Current Limit
    - Integrated Drivers for Large Synchronous-Rectifier MOSFETs
    - Programmable 100kHz to 600kHz Switching Frequency
    - 4V to 26V Battery Input Voltage Range
- 4A Internal Switch Northbridge SMPS
    - 2.7V to 5.5V Input Voltage Range
    - 2x Programmable Switching Frequency
    - 75mΩ/40mΩ Power Switches
- ±0.5% V_{OUT} Accuracy over Line, Load, and Temperature
- AMD SVI-Compliant Serial Interface with Switchable Address
- 7-Bit On-Board DAC: 0 to +1.550V Output Adjust Range
- Integrated Boost Switches
- Adjustable Slew-Rate Control
- Power-Good (PWRGD) and Thermal-Fault ($\overline{\text{VRHOT}}$) Outputs
- System Power-OK (PGD_IN) Input
- Overvoltage, Undervoltage, and Thermal-Fault Protection
- Voltage Soft-Startup and Passive Shutdown
- < 1µA Typical Shutdown Current

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17480GTL+	-40°C to +105°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{DD}, V_{IN3}, V_{CC}, V_{DDIO} to AGND	-0.3V to +6V
$\overline{\text{PWRGD}}$ to AGND	-0.3V to +6V
$\overline{\text{SHDN}}$ to AGND	-0.3V to +6V
GNDS1, GNDS2, THRM, $\overline{\text{VRHOT}}$ to AGND	-0.3V to +6V
CSP_, CSN_, ILIM12 to AGND	-0.3V to +6V
SVC, SVD, PGD_IN to AGND	-0.3V to +6V
FBDC_, FBAC_, OUT3 to AGND	-0.3V to +6V
OSC, TIME, OPTION, ILIM3 to AGND	-0.3V to (V_{CC} + 0.3V)
BST1, BST2 to AGND	-0.3V to +36V
BST1, BST2 to V_{DD}	-0.3V to +30V
BST3 to AGND	(V_{DD} - 0.3V) to (V_{LX3} + 6V)
LX1 to BST1	-6V to +0.3V
LX3 RMS Current (Note 2)	±4A
LX2 to BST2	-6V to +0.3V
LX3 to PGND (Note 2)	-0.6V to +6V
DH1 to LX1	-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2	-0.3V to (V_{BST2} + 0.3V)
DL1 to PGND	-0.3V to (V_{DD} + 0.3V)
DL2 to PGND	-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)	
40-Pin TQFN (derate 22.2mW/°C above +70°C)	1778mW
Operating Temperature Range	-40°C to +105°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Absolute Maximum Ratings measured with 20MHz scope bandwidth.

Note 2: LX3 has clamp diodes to PGND and IN3. If continuous current is applied through these diodes, thermal limits must be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{\text{SHDN}}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET	4		26	V
	V_{BIAS}	V_{CC}, V_{DD}	4.5		5.5	
	V_{IN3}		2.7		5.5	
	V_{DDIO}		1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising, 50mV typical hysteresis, latched, UV fault	4.10	4.25	4.45	V
V_{CC} Power-On Reset Threshold		Falling edge, typical hysteresis = 1.1V, faults cleared and DL_ forced high when V_{CC} falls below this level		1.8		V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising, 100mV typical hysteresis, latched, UV fault	0.7	0.8	0.9	V
V_{IN3} Undervoltage-Lockout Threshold		V_{IN3} rising, 100mV typical hysteresis	2.5	2.6	2.7	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ and OUT3 forced above their regulation points		5	10	mA
Quiescent Supply Currents (V_{DD})	I_{DD}	Skip mode, FBDC_ and OUT3 forced above their regulation points, T_A = +25°C		0.01	1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}			10	25	µA
Quiescent Supply Current (IN3)	I_{IN3}	Skip mode, OUT3 forced above its regulation point		50	200	µA
Shutdown Supply Current (V_{CC})		$\overline{\text{SHDN}}$ = GND, T_A = +25°C		0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Currents (V_{DD})		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DDIO})		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (IN3)		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
INTERNAL DACs, SLEW RATE, PHASE SHIFT							
DC Output Voltage Accuracy (Note 1)	V_{OUT}	Measured at FBDC_ for the core SMPSs; measured at OUT3 for the NB SMPS; 30% duty cycle, no load, ILIM3 = V_{CC}, V_{OUT3} = V_{DAC3} + 12.5mV (Note 3)	DAC codes from 0.8375V to 1.5500V	-0.5		+0.5	%
			DAC codes from 0.5000V to 0.8250V	-5		+5	mV
			DAC codes from 12.5mV to 0.4875V	-10		+10	
OUT3 Offset					12.5		mV
SMPS1 to SMPS2 Phase Shift		SMPS2 starts after SMPS1			50		%
					180		Degrees
SMPS3 to SMPS1 and SMPS2 Phase Shift		SMPS3 starts after SMPS1 or SMPS2			25		%
Slew-Rate Accuracy		During transition	R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
		Startup			1		mV/µs
FBAC_ Input Bias Current	$I_{FBAC\_}$	CSP_ = CSN_, T_A = +25°C		-3		+3	µA
FBDC_ Input Bias Current	$I_{FBDC\_}$	T_A = +25°C		-250		+250	nA
Switching Frequency Accuracy	f_{OSC1}, f_{OSC2}, f_{OSC3}	R_{OSC} = 143kΩ (f_{OSC1} = f_{OSC2} = 300kHz nominal, f_{OSC3} = 600kHz nominal)		-7		+7	%
		R_{OSC} = 71.4kΩ (f_{OSC1} = f_{OSC2} = 600kHz nominal, f_{OSC3} = 1.2MHz nominal) to 432kΩ (f_{OSC1} = f_{OSC2} = 99kHz nominal, f_{OSC3} = 199kHz nominal)		-9		+9	
SMPS1 AND SMPS2 CONTROLLERS							
DC Load Regulation		Either SMPS, PWM mode, droop disabled; zero to full load			-0.1		%
Line Regulation Error		Either SMPS, 4V < V_{IN} < 26V			0.03		%/V
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode		-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined: $\Delta V_{OUT}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV		0.95	1.00	1.05	V/V
GNDS_ Input Bias Current	$I_{GNDS\_}$	T_A = +25°C		-2		+2	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined-Mode Detection Threshold		GNDS1, GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7	0.8	0.9	V
Maximum Duty Factor	D_{MAX}		90	92		%
Minimum On-Time	t_{ONMIN}				150	ns
SMPS1 AND SMPS2 CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.052 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Zero-Crossing Threshold	V_{ZX}	$V_{GND\_}$ - $V_{LX\_}$, skip mode		1		mV
Idle Mode™ Threshold	V_{IMIN}	$V_{CSP\_}$ - $V_{CSN\_}$, skip mode, 0.15 x V_{LIMIT}	-2		+2	mV
CS_ Input Leakage Current		CSP_ and CSN_, T_A = +25°C	-0.2		+0.2	µA
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
SMPS1 AND SMPS2 DROOP, CURRENT BALANCE, AND TRANSIENT RESPONSE						
AC Droop and Current Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +40mV	1.94	2.00	2.06	mS
AC Droop and Current Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$	-1.5		+1.5	mV
No-Load Positive Offset		OPTION = 2V or GND		+12.5		mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 10mV hysteresis (typ)	-47	-41	-33	mV
SMPS3 INTERNAL 4A STEP-DOWN CONVERTER						
OUT3 Load Regulation	R_{DROOP3}		4	5.5	7	mV/A
OUT3 Line Regulation		0 to 100% duty cycle		5		mV
OUT3 Input Current	I_{OUT3}	T_A = +25°C	-100	-5	+100	nA
LX3 Leakage Current	I_{LX3}	$\overline{SHDN}$ = GND, V_{LX3} = GND or 5.5V, V_{IN3} = 5.5V, T_A = +25°C	-20		+20	µA
Internal MOSFET On-Resistance	$R_{ON(NH3)}$	High-side n-channel		75	150	mΩ
	$R_{ON(NL3)}$	Low-side n-channel		40	75	
LX3 Peak Current Limit	I_{LX3PK}	ILIM3 = V_{CC}	4.75	5.25	6	A
		ILIM3 = GND	3.75	4.25	5	
LX3 Idle-Mode Trip Level	I_{LX3MIN}	Percentage of I_{LX3PK}		25		%
LX3 Zero-Crossing Trip Level	I_{ZX3}	Skip mode		20		mA
Maximum Duty Factor	D_{MAX}		84	87		%
Minimum On-Time	t_{ONMIN}				150	ns

Idle Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{\text{SHDN}}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
Output Overvoltage Trip Threshold (SMPS1 and SMPS2 Only)	$V_{OVP\_}$	Measured at FBDC_, rising edge	PWM mode	250	300	350	mV
			Skip mode and output has not reached the regulation voltage	1.80	1.85	1.90	V
			Minimum OVP threshold		0.8		
Output Overvoltage Fault Propagation Delay (SMPS1 and SMPS2 Only)	t_{OVP}	FBDC_ forced 25mV above trip threshold			10		µs
Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FBDC_ or OUT3 with respect to unloaded output voltage		-450	-400	-350	mV
Output Undervoltage Fault Propagation Delay	t_{UVP}	FBDC_ forced 25mV below trip threshold			10		µs
PWRGD Threshold		Measured at FBDC_ or OUT3 with respect to unloaded output voltage,15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD Propagation Delay	t_{PWRGD}	FBDC_ or OUT3 forced 25mV outside the PWRGD trip thresholds			10		µs
PWRGD, Output Low Voltage		I_{SINK} = 4mA				0.4	V
PWRGD Leakage Current	I_{PWRGD}	High state, PWRGD forced to 5.5V, T_A = +25°C				1	µA
PWRGD Startup Delay and Transition Blanking Time	t_{BLANK}	Measured from the time when FBDC_ and OUT3 reach the target voltage			20		µs
$\overline{\text{VRHOT}}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30	30.5	%
$\overline{\text{VRHOT}}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{\text{VRHOT}}$ trip threshold, falling edge			10		µs
$\overline{\text{VRHOT}}$, Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{\text{VRHOT}}$ Leakage Current		High state, $\overline{\text{VRHOT}}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage		T_A = +25°C		-100		+100	nA
Thermal-Shutdown Threshold	$T_{\overline{SHDN}}$	Hysteresis = 15°C			+160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V (Note 4)	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.5	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			0.7	2.0	Ω
		DL_, low state			0.25	0.6	

AMD 2-/3-Output Mobile Serial VID Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH_ Gate-Driver Source/Sink Current	$I_{DH\_}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		2.2		A
DL_ Gate-Driver Source Current	$I_{DL\_}$	DL_ forced to 2.5V		2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_ (SINK)}$	DL_ forced to 2.5V		8		A
Dead Time	t_{DH_DL}	DH_ low to DL_ high	9	20	35	ns
	t_{DL_DH}	DL_ low to DH_ high	9	20	35	
Internal BST1, BST2 Switch R_{ON}		BST1, BST2 to V_{DD}, I_{BST1} = I_{BST2} = 10mA		10	20	Ω
Internal BST3 Switch R_{ON}		BST3 to V_{DD}, I_{BST3} = 10mA		10	20	Ω
2-WIRE I^2C BUS LOGIC INTERFACE						
SVI Logic-Input Current		SVC, SVD, T_A = +25°C	-1		+1	µA
SVI Logic-Input Threshold		SVC, SVD, rising edge, hysteresis 0.14 x V_{DDIO} (V)	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}				3.4	MHz
START Condition Hold Time	$t_{HD;STA}$		160			ns
Repeated START Condition Setup Time	$t_{SU;STA}$		160			ns
STOP Condition Setup Time	$t_{SU;STO}$		160			ns
Data Hold	$t_{HD;DAT}$	A master device must internally provide a hold time of at least 300ns for the SVD signal (referred to the V_{IHMIN} of SVC signal) to bridge the undefined region of SVC's falling edge			70	ns
Data Setup Time	$t_{SU;DAT}$		10			ns
SVC Low Period	t_{LOW}		160			ns
SVC High Period	t_{HIGH}	Measured from 10% to 90% of V_{DDIO}	60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Input filters on SVD and SVC suppress noise spike less than 50ns			40	ns
Pulse Width of Spike Suppression				20		ns
INPUTS AND OUTPUTS						
Logic-Input Current		$\overline{SHDN}$, PGD_IN, T_A = +25°C	-1		+1	µA
		ILIM3, OPTION, T_A = +25°C	-200		+200	nA
Logic-Input Levels		$\overline{SHDN}$, rising edge, hysteresis = 225mV	0.8		2.0	V
Input Logic Levels		High, OPTION, ILIM3	V_{CC} - 0.4			V
		3.3V, OPTION	2.75		3.85	
		2V, OPTION	1.65		2.35	
		Low, OPTION, ILIM3			0.4	
PGD_IN Logic-Input Threshold		PGD_IN, rising edge, hysteresis = 65mV	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET		4		26	V
	V_{BIAS}	V_{CC}, V_{DD}		4.5		5.5	
	V_{IN3}			2.7		5.5	
	V_{DDIO}			1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising, 50mV typical hysteresis, latched, UV fault		4.10		4.45	V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising, 100mV typical hysteresis, latched, UV fault		0.7		0.9	V
V_{IN3} Undervoltage-Lockout Threshold		V_{IN3} rising, 100mV typical hysteresis		2.5		2.7	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ and OUT3 forced above their regulation points				10	mA
Quiescent Supply Current	I_{DDIO}					25	µA
Quiescent Supply Current (IN3)	I_{IN3}	Skip mode, OUT3 forced above its regulation point				200	µA
INTERNAL DACs, SLEW RATE, PHASE SHIFT							
DC Output Voltage Accuracy	V_{OUT}	Measured at FBDC_ for the core SMPSs; measured at OUT3 for the NB SMPS; 30% duty cycle, no load, ILIM3 = V_{CC}, V_{OUT3} = V_{DAC3} + 12.5mV (Note 3)	DAC codes from 0.8375V to 1.5500V	-0.7		+0.7	%
			DAC codes from 0.5000V to 0.8250V	-7.5		+7.5	mV
			DAC codes from 12.5mV to 0.4875V	-15		+15	
Slew-Rate Accuracy		During transition	R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
Switching Frequency Accuracy	f_{OSC1}, f_{OSC2}, f_{OSC3}	R_{OSC} = 143kΩ (f_{OSC1} = f_{OSC2} = 300kHz nominal, f_{OSC3} = 600kHz nominal)		-9		+9	%
		R_{OSC} = 71.4kΩ (f_{OSC1} = f_{OSC2} = 600kHz nominal, f_{OSC3} = 1.2MHz nominal) to 432kΩ (f_{OSC1} = f_{OSC2} = 99kHz nominal, f_{OSC3} = 199kHz nominal)		-12		+12	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS1 AND SMPS2 CONTROLLERS						
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode	-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined; $\Delta V_{OUT}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV	0.95		1.05	V/V
Combined-Mode Detection Threshold		GNDS1, GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7		0.9	V
Maximum Duty Factor	D_{MAX}		90			%
Minimum On-Time	t_{ONMIN}				150	ns
SMPS1 AND SMPS2 CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.052 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Idle-Mode Threshold Tolerance	V_{IMIN}	$V_{CSP\_}$ - $V_{CSN\_}$, skip mode, 0.15 x V_{LIMIT}	-2		+2	mV
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
SMPS1 AND SMPS2 DROOP, CURRENT BALANCE, AND TRANSIENT RESPONSE						
AC Droop and Current Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +40mV	1.94		2.06	mS
AC Droop and Current Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$	-1.5		+2.0	mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 10mV hysteresis (typ)	-47		-33	mV
SMPS3 INTERNAL 4A STEP-DOWN CONVERTER						
OUT3 Load Regulation	R_{DROOP3}		4		7	mV/A
Internal MOSFET On-Resistance	$R_{ON(NH3)}$	High-side n-channel			150	mΩ
	$R_{ON(NL3)}$	Low-side n-channel			75	
LX3 Peak Current Limit	I_{LX3PK}	ILIM3 = V_{CC}, skip mode	4.75		6	A
Maximum Duty Factor	D_{MAX}		84			%
Minimum On-Time	t_{ONMIN}				150	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{\text{SHDN}}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
Output Overvoltage Trip Threshold (SMPS1 and SMPS2 Only)	$V_{OVP\_}$	Measured at FBDC_, rising edge	PWM mode	250		350	mV
			Skip mode and output have not reached the regulation voltage	1.80		1.90	V
Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FBDC_ or OUT3 with respect to unloaded output voltage		-450		-350	mV
PWRGD Threshold		Measured at FBDC_ or OUT3 with respect to unloaded output voltage, 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
PWRGD, Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{\text{VRHOT}}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5		30.5	%
$\overline{\text{VRHOT}}$, Output Low Voltage		I_{SINK} = 4mA				0.4	V
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V (Note 4)	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.5	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state				2.0	Ω
		DL_, low state				0.6	
Dead Time	t_{DH_DL}	DH_ low to DL_ high		9		35	ns
	t_{DL_DH}	DL_ low to DH_ high		9		35	
Internal BST1, BST2 Switch R_{ON}		BST1, BST2 to V_{DD}, I_{BST1} = I_{BST2} = 10mA				20	Ω
Internal BST3 Switch R_{ON}		BST3 to V_{DD}, I_{BST3} = 10mA				20	Ω
2-WIRE I²C BUS LOGIC INTERFACE							
SVI Logic-Input Threshold		SVC, SVD, rising edge, hysteresis = 0.14 x V_{DDIO}(V)		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}					3.4	MHz
START Condition Hold Time	$t_{SU;STA}$			160			ns
Repeated START Condition Setup Time	$t_{SU;STA}$			160			ns
STOP Condition Setup Time	$t_{SU;STO}$			160			ns
Data Hold	$t_{HD;DAT}$	A master device must internally provide a hold time of at least 300ns for the SVD signal (referred to the V_{IHMIN} of SVC signal) to bridge the undefined region of SVC's falling edge				70	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{\text{SHDN}}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU;DAT}$		10			ns
SVC Low Period	t_{LOW}		160			ns
SVC High Period	t_{HIGH}	Measured from 10% to 90% of V_{DDIO}	60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Input filters on SVD and SVC suppress noise spike less than 50ns			40	ns
INPUTS AND OUTPUTS						
Logic-Input Levels		$\overline{\text{SHDN}}$, rising edge, hysteresis = 225mV	0.8		2.0	V
Input Logic Levels		High, OPTION, ILIM3	V_{CC} - 0.4			V
		3.3V, OPTION	2.75		3.85	
		2V, OPTION	1.65		2.35	
		Low, OPTION, ILIM3			0.4	
PGD_IN Logic-Input Threshold		PGD_IN, rising edge, hysteresis = 65mV	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V

Note 3: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage has a DC regulation level higher than the error-comparator threshold by 50% of the ripple. The core SMPSs have an integrator that corrects for this error. The NB SMPS has an offset determined by the ILIM3 pin, and a -6.5mV/A load line.

Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the TQFN package.

Note 5: Specifications to T_A = -40°C to +105°C are guaranteed by design, not production tested.

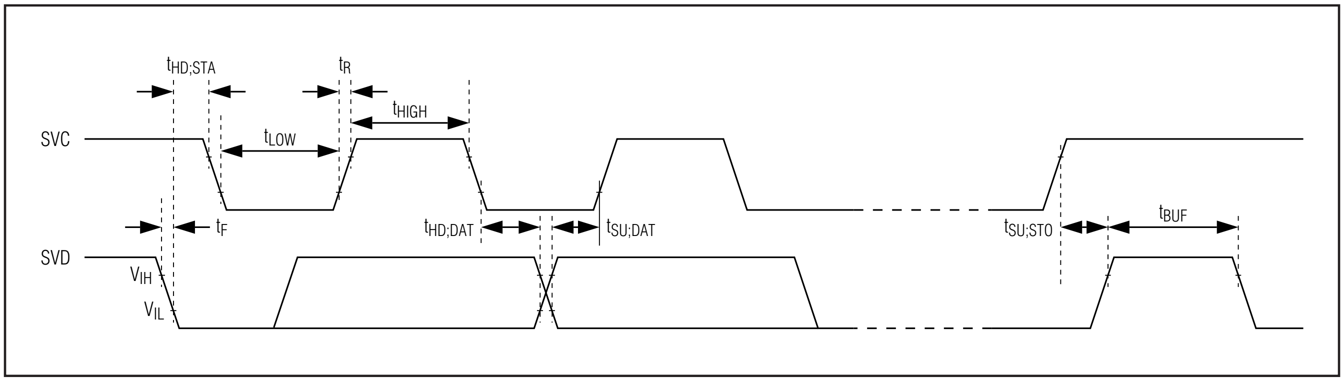
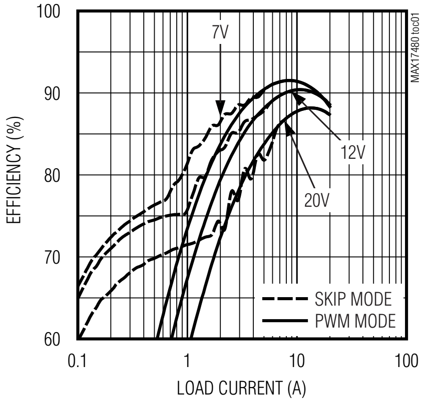


Figure 1. Timing Definitions Used in the Electrical Characteristics

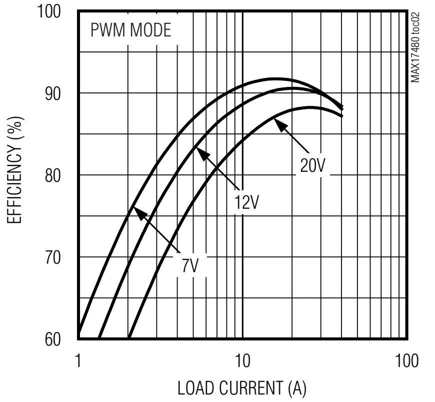
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

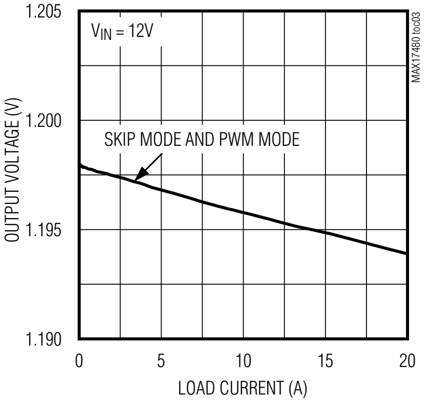
CORE SMPS 1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



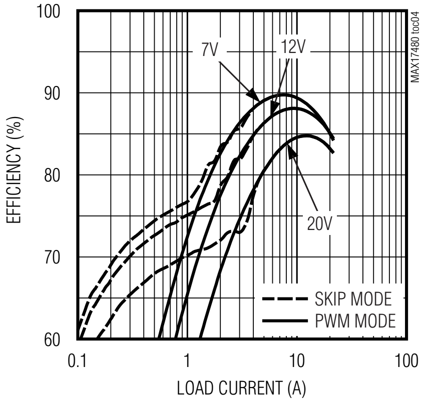
CORE SMPS 2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



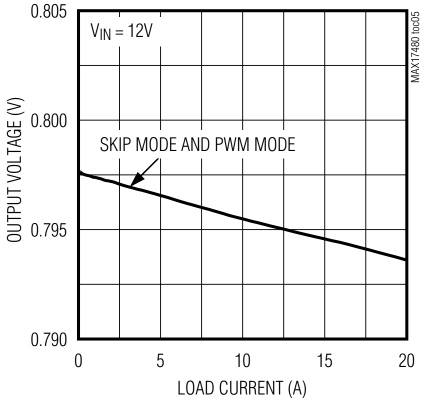
CORE SMPS OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2V)



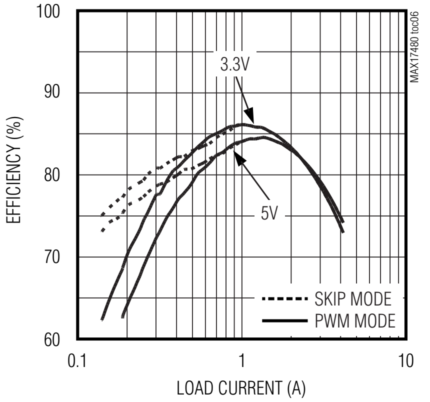
CORE SMPS 1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8V)



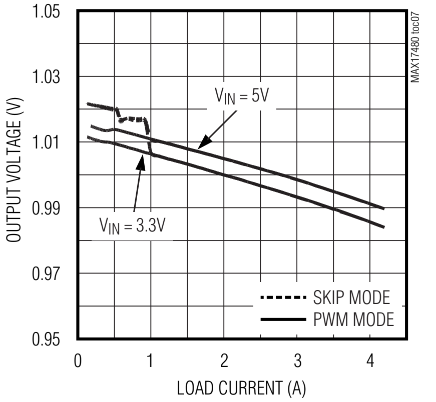
CORE SMPS OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.8V)



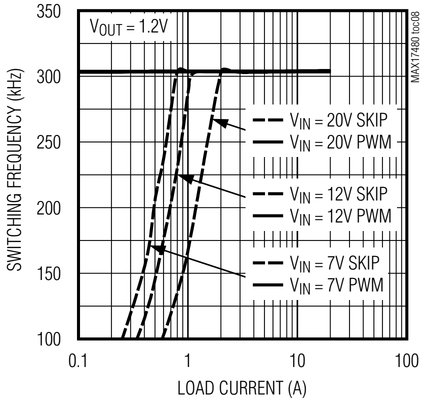
NB SMPS EFFICIENCY vs. LOAD CURRENT (1V)



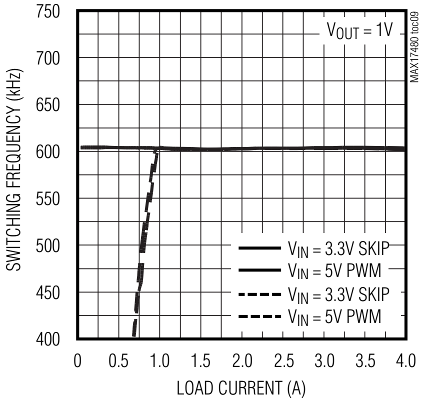
NB SMPS 1V OUTPUT VOLTAGE vs. LOAD CURRENT



CORE SMPS 1-PHASE SWITCHING FREQUENCY vs. LOAD CURRENT



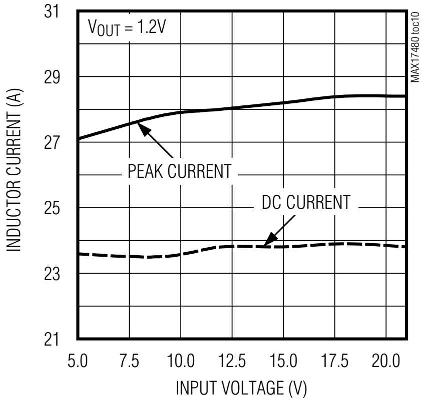
NB SMPS SWITCHING FREQUENCY vs. LOAD CURRENT



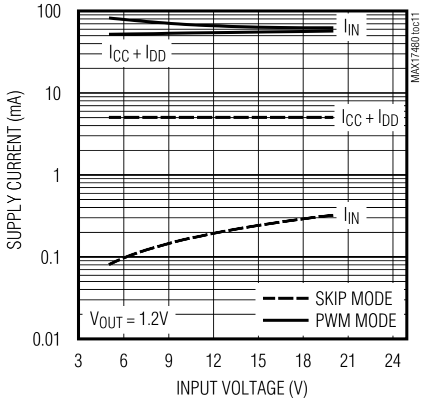
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

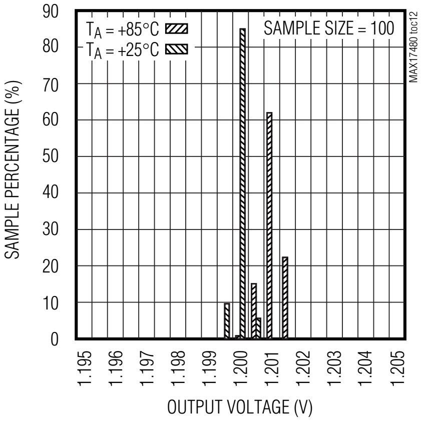
MAXIMUM INDUCTOR CURRENT vs. INPUT VOLTAGE



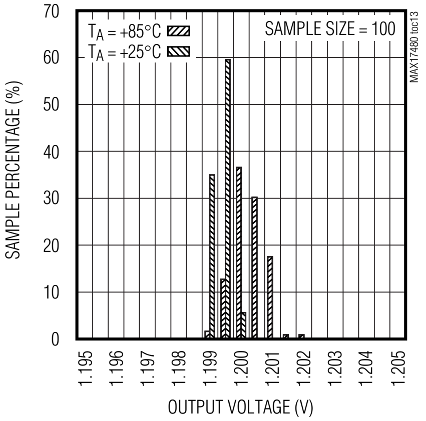
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



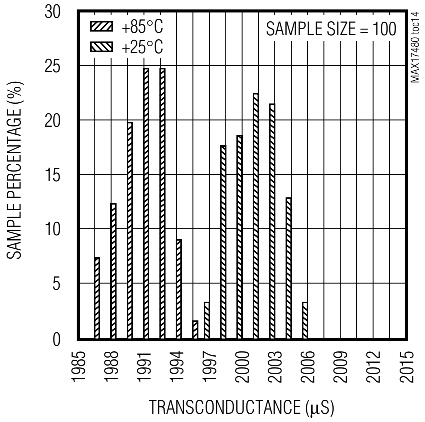
CORE SMPS VID = 1.2V OUTPUT VOLTAGE DISTRIBUTION



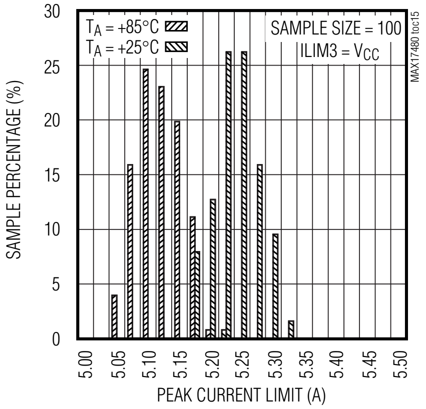
NB SMPS VID = 1.2V OUTPUT VOLTAGE DISTRIBUTION



$G_{m(FBAC)}$ TRANSCONDUCTANCE DISTRIBUTION



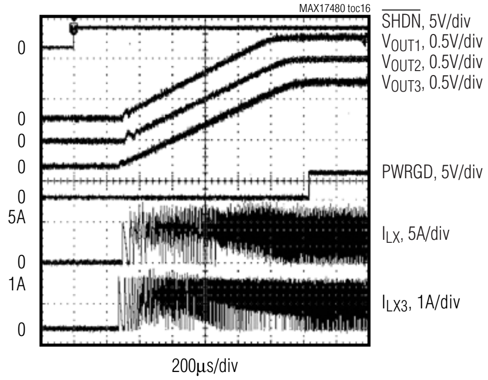
NB SMPS PEAK CURRENT-LIMIT DISTRIBUTION



Typical Operating Characteristics (continued)

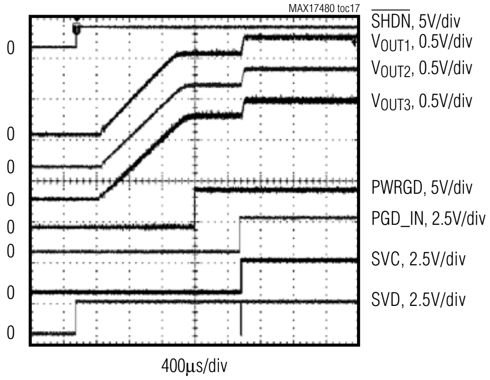
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

STARTUP WAVEFORMS



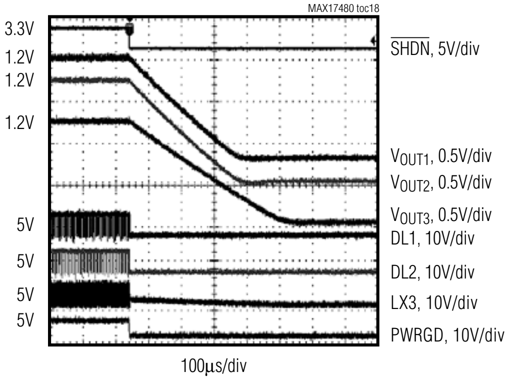
V_{IN} = 12V I_{LOAD1} = 3A
V_{BOOT} = 1V I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

STARTUP SEQUENCE



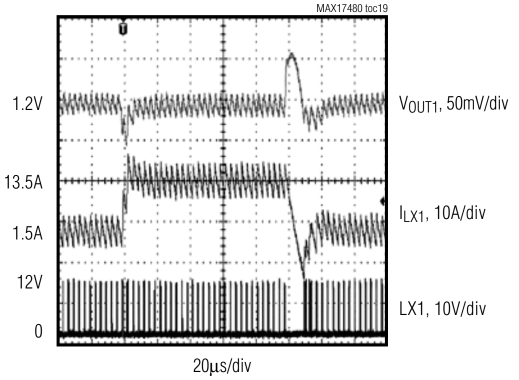
V_{IN} = 12V
V_{BOOT} = 1V
V_{SVID} = 1.2V

SHUTDOWN WAVEFORMS



V_{IN} = 12V I_{LOAD1} = 3A
V_{SVID} = 1.2V I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

CORE SMPS 1-PHASE LOAD-TRANSIENT RESPONSE



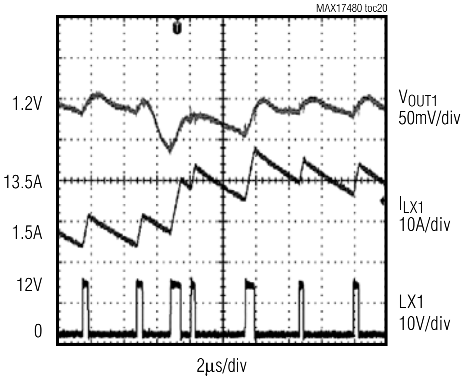
V_{IN} = 12V I_{LOAD1} = 1.5A TO 13.5A TO 1.5A
V_{OUT1} = 1.2V PWM MODE

AMD 2-/3-Output Mobile Serial VID Controller

Typical Operating Characteristics (continued)

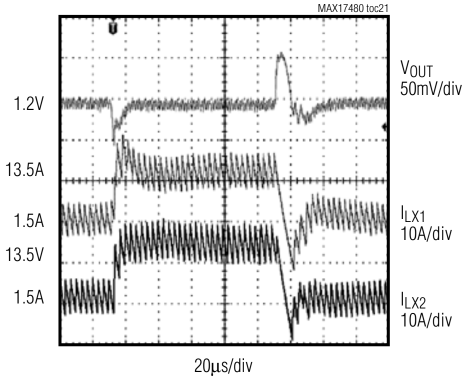
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

CORE SMPS 1-PHASE TRANSIENT PHASE REPEAT



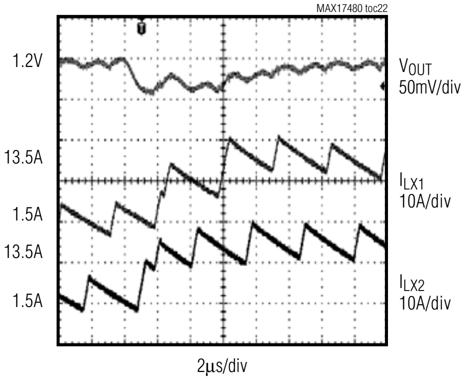
V_{IN} = 12V I_{LOAD1} = 1.5A TO 13.5A TO 1.5A
V_{OUT1} = 1.2V PWM MODE

CORE SMPS 2-PHASE LOAD-TRANSIENT RESPONSE



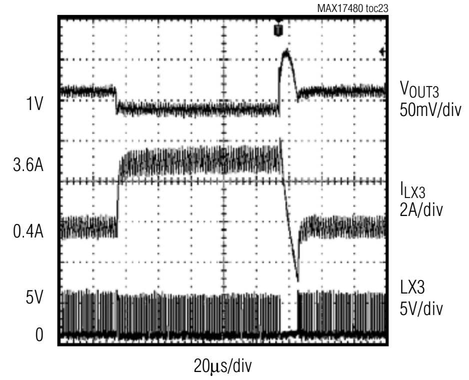
V_{IN} = 12V I_{LOAD} = 3A TO 27A TO 3A
V_{OUT1} = 1.2V PWM MODE

CORE SMPS 2-PHASE TRANSIENT PHASE REPEAT



V_{IN} = 12V I_{LOAD} = 3A TO 27A TO 3A
V_{OUT1} = 1.2V PWM MODE

NB SMPS LOAD-TRANSIENT RESPONSE

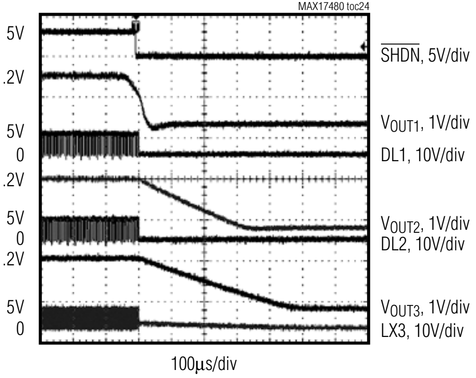


V_{IN3} = 5V I_{LOAD3} = 0.4A TO 3.6A TO 0.4A
V_{OUT3} = 1V PWM MODE

Typical Operating Characteristics (continued)

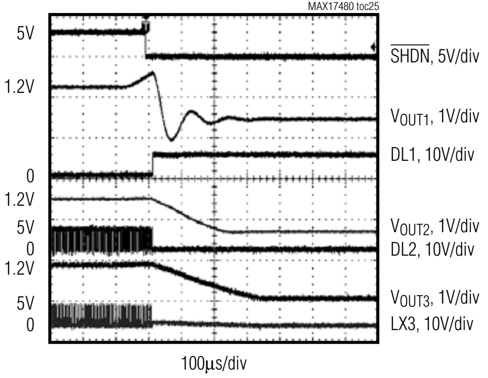
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

CORE SMPS OUTPUT OVERLOAD WAVEFORM (SEPARATE MODE)



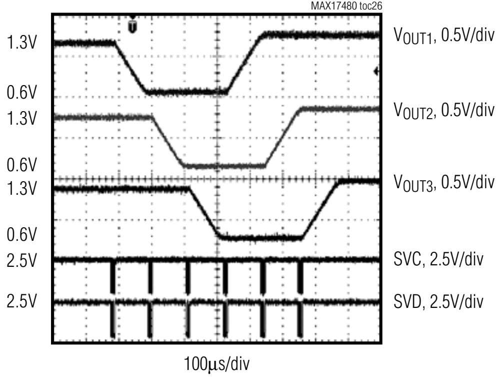
V_{IN} = 12V
V_{SVID} = 1.2V
I_{LOAD1} = 3A TO 40A
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

CORE SMPS OUTPUT OVERVOLTAGE WAVEFORM (SEPARATE MODE)



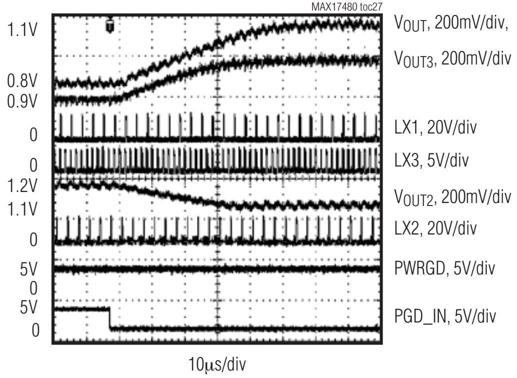
V_{IN} = 12V
V_{SVID} = 1.2V
I_{LOAD1} = NO LOAD
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (LIGHT LOAD)



V_{IN} = 12V
V_{SVID} = 1.3V TO 0.6V TO 1.3V

PGD_IN TRANSITION (LIGHT LOAD)



V_{IN} = 12V
V_{BOOT} = 1.1V
V_{OUT1} = 0.8V
V_{OUT2} = 1.2V
V_{OUT3} = 0.9V

Pin Description

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>ILIM12</td><td>SMPS1 and SMPS2 Current-Limit Adjust Input. The positive current-limit threshold voltage is 0.052 times the voltage between TIME and ILIM over a 0.2V to 1.0V range of V(TIME, ILIM). The I_{MIN12} minimum current-limit threshold voltage in skip mode is precisely 15% of the corresponding positive current-limit threshold voltage.</td></tr>
<tr><td>2</td><td>ILIM3</td><td>SMPS3 Current-Limit Adjust Input. Two-level current-limit setting for SMPS3. The I_{LX3MIN} minimum current-limit threshold in skip mode is precisely 25% of the corresponding positive current-limit threshold.
<table>
<tr><th>ILIM3</th><th>I_{LX3PK} (A)</th></tr>
<tr><td>V_{CC}</td><td>5.25</td></tr>
<tr><td>GND</td><td>4.25</td></tr>
</table></td></tr>
<tr><td>3, 4</td><td>IN3</td><td>Internal High-Side MOSFET Drain Connection for SMPS3. Bypass to PGND with a 10µF or greater ceramic capacitor close to the IC.</td></tr>
<tr><td>5, 6</td><td>LX3</td><td>Inductor Connection for SMPS3. Connect LX3 to the switched side of the inductor.</td></tr>
<tr><td>7</td><td>BST3</td><td>Boost Flying Capacitor Connection for SMPS3. An internal switch between V_{DD} and BST3 charges the flying capacitor during the time the low-side FET is on.</td></tr>
<tr><td>8</td><td>$\overline{\text{SHDN}}$</td><td>Active-Low Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA max shutdown state. During startup, the output voltage is ramped up to the voltage set by the SVC and SVD inputs at a slew rate of 1mV/µs. In shutdown, the outputs are discharged using a 20Ω switch through the CSN_ pins for the core SMPSs and through the OUT3 pin for the northbridge SMPS.
The MAX17480 powers up to the voltage set by the two SVI bits.
<table>
<tr><th>SVC</th><th>SVD</th><th>BOOT VOLTAGE V_{OUT} (V)</th></tr>
<tr><td>0</td><td>0</td><td>1.1</td></tr>
<tr><td>0</td><td>1</td><td>1.0</td></tr>
<tr><td>1</td><td>0</td><td>0.9</td></tr>
<tr><td>1</td><td>1</td><td>0.8</td></tr>
</table>
The MAX17480 **stores** the boot VID when PWRGD first goes high. The stored boot VID is cleared by a rising $\overline{\text{SHDN}}$ signal.</td></tr>
<tr><td>9</td><td>OUT3</td><td>Feedback Input for SMPS3. A 20Ω discharge FET is enabled from OUT3 to PGND when SMPS3 is shut down.</td></tr>
<tr><td>10</td><td>AGND</td><td>Analog Ground</td></tr>
<tr><td>11</td><td>SVD</td><td>Serial VID Data</td></tr>
<tr><td>12</td><td>SVC</td><td>Serial VID Clock</td></tr>
<tr><td>13</td><td>V_{DDIO}</td><td>CPU I/O Voltage (1.8V or 1.5V). Logic thresholds for SVD and SVC are relative to the voltage at V_{DDIO}.</td></tr>
<tr><td>14</td><td>GNDS2</td><td>SMPS2 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS2 internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the SMPS ground to the load ground.
Connect GNDS1 or GNDS2 above 0.9V combined-mode operation (unified core). When GNDS2 is pulled above 0.9V, GNDS1 is used as the remote ground-sense input.</td></tr>
</table>

Pin Description (continued)

PIN	NAME	FUNCTION
15	FBAC2	Output of the Voltage-Positioning Transconductance Amplifier for SMPS2. The RC network between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $R_{DROOP\_AC2} = \frac{R_{FBAC2} \times R_{FBDC2}}{R_{FBAC2} + R_{FBDC2} + R_{FB2} \parallel Z_{CFB2}} \times R_{SENSE2} \times G_{m(FBAC2)}$ where R_{DROOP_AC2} is the transient (AC) voltage-positioning slope that provides an acceptable trade-off between stability and load-transient response, $G_{m(FBAC2)}$ = 2mS (typ), and R_{SENSE2} is the value of the current-sense element that is used to provide the (CSP2, CSN2) current-sense voltage, Z_{CFB2} is the impedance of C_{FB2}, and FBAC2 is high impedance in shutdown.
16	FBDC2	Feedback-Sense Input for SMPS2. Connect a resistor R_{FBDC2} between FBDC2 and the positive side of the feedback remote sense, and a capacitor from FBAC2 to couple the AC ripple from FBAC2 to FBDC2. An integrator on FBDC2 corrects for output ripple and ground-sense offset. To enable a DC load-line less than the AC load-line, add a resistor from FBAC2 to FBDC2. To enable a DC load-line equal to the AC load-line, short FBAC2 to FBDC2. See the *Core Steady-State Voltage Positioning (DC Droop)* section. FBDC2 is high impedance in shutdown.
17	CSN2	Negative Current-Sense Input for SMPS2. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 20Ω discharge FET is enabled from CSN2 to PGND when the SMPS2 is shut down.
18	CSP2	Positive Current-Sense Input for SMPS2. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
19	PGD_IN	System Power-Good Input PGD_IN is low when $\overline{SHDN}$ first goes high. The MAX17480 decodes the two SVI bits to determine the boot voltage. The SVI bits can be changed dynamically during this time while PGD_IN remains low and PWRGD is still low. PGD_IN goes high after the MAX17480 reaches the boot voltage. This indicates that the SVI block is active, and the MAX17480 starts to respond to the SVI commands. The MAX17480 **stores** the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$. After PGD_IN has gone high, if at any time PGD_IN goes low, the MAX17480 regulates to the previously stored boot VID. The slew rate during this transition is set by the resistor between the TIME and GND pins. PWRGD follows the blanking for normal VID transition. The subsequent rising edge of PGD_IN does not change the stored VID.

Pin Description (continued)

PIN	NAME	FUNCTION
20	PWRGD	Open-Drain Power-Good Output. PWRGD is the wired-OR open-drain output of all three SMPS outputs. PWRGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions). During startup, PWRGD is held low for an additional 20µs after the MAX17480 reaches the startup boot voltage set by the SVC and SVD pins. The MAX17480 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{\text{SHDN}}$. PWRGD is forced low in shutdown. When SMPS is in pulse-skipping mode, the upper PWRGD threshold comparator for the respective SMPS is blanked during a downward VID transition. The upper PWRGD threshold comparator is re-enabled once the output is in regulation (Figure 6).
21	DH2	SMPS2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
22	LX2	SMPS2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to SMPS2's zero-crossing comparator.
23	BST2	Boost Flying Capacitor Connection for the DH2 High-Side Gate Driver. An internal switch between V_{DD} and BST2 charges the flying capacitor during the time the low-side FET is on.
24	DL2	SMPS2 Low-Side Gate-Driver Output. DL2 swings from GND2 to V_{DD}. DL2 is forced low in shutdown. DL2 is also forced high when an output overvoltage fault is detected. DL2 is forced low in skip mode after an inductor current zero crossing (GND2 - LX2) is detected.
25	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_ flying capacitors during the off-time. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 2.2µF or greater ceramic capacitor.
26	DL1	SMPS1 Low-Side Gate-Driver Output. DL1 swings from GND1 to V_{DD}. DL1 is forced low in shutdown. DL1 is also forced high when an output overvoltage fault is detected. DL1 is forced low in skip mode after an inductor current zero crossing (GND1 - LX1) is detected.
27	BST1	Boost Flying Capacitor Connection for the DH1 High-Side Gate Driver. An internal switch between V_{DD} and BST1 charges the flying capacitor during the time the low-side FET is on.
28	LX1	SMPS1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to SMPS1's zero-crossing comparator.
29	DH1	SMPS1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
30	$\overline{\text{VRHOT}}$	Active-Low Open-Drain Output of Internal Comparator. $\overline{\text{VRHOT}}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{\text{VRHOT}}$ is high impedance in shutdown.
31	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components so the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
32	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with a 1µF minimum capacitor. A V_{CC} UVLO event that occurs while the IC is functioning is latched, and can only be cleared by cycling V_{CC} power or by toggling $\overline{\text{SHDN}}$.

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>33</td><td>CSP1</td><td>Positive Current-Sense Input for SMPS1. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.</td></tr>
<tr><td>34</td><td>CSN1</td><td>Negative Current-Sense Input for SMPS1. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
A 20Ω discharge FET is enabled from CSN1 to PGND when the SMPS1 is shut down.</td></tr>
<tr><td>35</td><td>FBDC1</td><td>Feedback Sense Input for SMPS1. Connect a resistor R_{FBDC1} between FBDC1 and the positive side of the feedback remote sense, and a capacitor from FBAC1 to couple the AC ripple from FBAC1 to FBDC1. An integrator on FBDC1 corrects for output ripple and ground-sense offset.
To enable a DC load-line less than the AC load-line, add a resistor from FBAC1 to FBDC1.
To enable a DC load-line equal to the AC load-line, short FBAC1 to FBDC1. See the *Core Steady-State Voltage Positioning (DC Droop)* section.
FBDC1 is high impedance in shutdown.</td></tr>
<tr><td>36</td><td>FBAC1</td><td>Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS1. The RC network between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop:
$$R_{DROOP\_AC1} = \frac{R_{FBAC1} \times R_{FBDC1}}{R_{FBAC1} + R_{FBDC1} + R_{FB1} \parallel Z_{CFB1}} \times R_{SENSE1} \times G_{m(FBAC1)}$$
where R_{DROOP_AC1} is the transient (AC) voltage-positioning slope that provides an acceptable trade-off between stability and load-transient response, $G_{m(FBAC1)}$ = 2mS (typ), R_{SENSE1} is the value of the current-sense element that is used to provide the (CSP1, CSN1) current-sense voltage, Z_{CFB1} is the impedance of C_{FB1}, and FBAC1 is high impedance in shutdown.</td></tr>
<tr><td>37</td><td>GNDS1</td><td>SMPS1 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS1 internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the SMPS ground to the load ground.
Connect GNDS1 or GNDS2 above 0.9V combined-mode operation (unified core). When GNDS1 is pulled above 0.9V, GNDS2 is used as the remote ground-sense input.</td></tr>
<tr><td>38</td><td>OPTION</td><td>Four-Level Input to Enable Offset and Change Core SMPS Address
<table>
<tr><th>OPTION</th><th>OFFSET ENABLED</th><th>SMPS1 ADDRESS</th><th>SMPS2 ADDRESS</th></tr>
<tr><td>V_{CC}</td><td>0</td><td>BIT 1 (VDD0)</td><td>BIT 2 (VDD1)</td></tr>
<tr><td>3.3V</td><td>0</td><td>BIT 2 (VDD1)</td><td>BIT 1 (VDD0)</td></tr>
<tr><td>2V</td><td>1</td><td>BIT 1 (VDD0)</td><td>BIT 2 (VDD1)</td></tr>
<tr><td>GND</td><td>1</td><td>BIT 2 (VDD1)</td><td>BIT 1 (VDD0)</td></tr>
</table>
When OFFSET is enabled, the MAX17480 enables a fixed +12.5mV offset on SMPS1 and SMPS2 VID codes after PGD_IN goes high. This configuration is intended for applications that implement a load line. An external resistor at FBDC_ sets the load-line. The offset can be disabled by setting the PSI_L bit to 0 through the serial interface.
Additionally, the OPTION level also allows core SMPS1 and SMPS2 to take on either the VDD0 or VDD1 addresses. VDD0 refers to CORE0, and VDD1 refers to CORE1 for the AMD CPU.
The NB SMPS is not affected by the OPTION setting.</td></tr>
</table>

Pin Description (continued)

PIN	NAME	FUNCTION
39	OSC	Oscillator Adjustment Input. Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase): $f_{OSC} = 300kHz \times 143k\Omega/R_{OSC}$ A 71.4kΩ to 432kΩ resistor corresponds to switching frequencies of 600kHz to 100kHz, respectively, for SMPS1 and SMPS2. SMPS3 runs at twice the programmed switching frequency. Switching frequency selection is limited by the minimum on-time. See the Core Switching Frequency description in the *SMPS Design Procedure* section.
40	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate: $\text{PWM slew rate} = (6.25mV/\mu s) \times (143k\Omega/R_{TIME})$ where R_{TIME} is between 35.7kΩ and 357kΩ. This slew rate applies to both upward and downward VID transitions, and to the transition from boot mode to VID mode. Downward VID transition slew rate in skip mode can appear slower because the output transition is not forced by the SMPS. The slew rate for startup is fixed at 1mV/µs.
EP	PGND	Exposed Pad. Power ground connection and source connection of the internal low-side MOSFET.

Table 1. Component Selection for Standard Applications

COMPONENT	V_{IN} = 7V TO 24V, V_{OUT1} = V_{OUT2} = 1.0V TO 1.3V, 18A PER PHASE	V_{IN3} = 5V, V_{OUT3} = 1.0V TO 1.3V, 4A	V_{IN} = 4.5V TO 14V, V_{OUT1} = V_{OUT2} = 1.0V TO 1.3V, 18A PER PHASE	V_{IN3} = 3.3V, V_{OUT3} = 1.0V TO 1.3V, 4A
Mode	Separate, 2-phase mobile (GNDS1 = GNDS2 = low)	—	Separate, 2-phase mobile (GNDS1 = GNDS2 = low)	—
Switching Frequency	300kHz	600kHz	500kHz	1MHz
C_{IN}_ Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(1) 10µF, 6.3V TDK C2012X5R0J106M Taiyo Yuden JMK212BJ106M	(2) 10µF, 16V Taiyo Yuden TMK432BJ106KM	(1) 10µF, 6.3V TDK C2012X5R0J106M Taiyo Yuden JMK212BJ106M
C_{OUT}_ Output Capacitor	(2) 330µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSX0D331XE SANYO 2TPE330M6	(1) 220µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D221R SANYO 2TPE220M6	(2) 220µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D221R SANYO 2TPE220M6	(1) 47µF, ceramic capacitor
N_H_ High-Side MOSFET	(1) Vishay/Siliconix SI7634DP	None	(1) International Rectifier IRF7811W	None
N_L_ Low-Side MOSFET	(2) Vishay/Siliconix SI7336ADP	None	(2) Vishay/Siliconix SI7336ADP	None
D_L_ Schottky Rectifier (if needed)	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None
L_ Inductor	0.45µH, 21A, 1.1mΩ power inductor Panasonic ETQP4LR45WFC	1.5µH, 5A, 21mΩ power inductor NEC/Tokin MPLCH0525LIR5 Toko FDV0530-1R5M	0.36µH, 21A, 1.1mΩ power inductor Panasonic ETQP4LR36WFC	0.6µH, 4.95A, 16mΩ power inductor Sumida CDR6D23MN

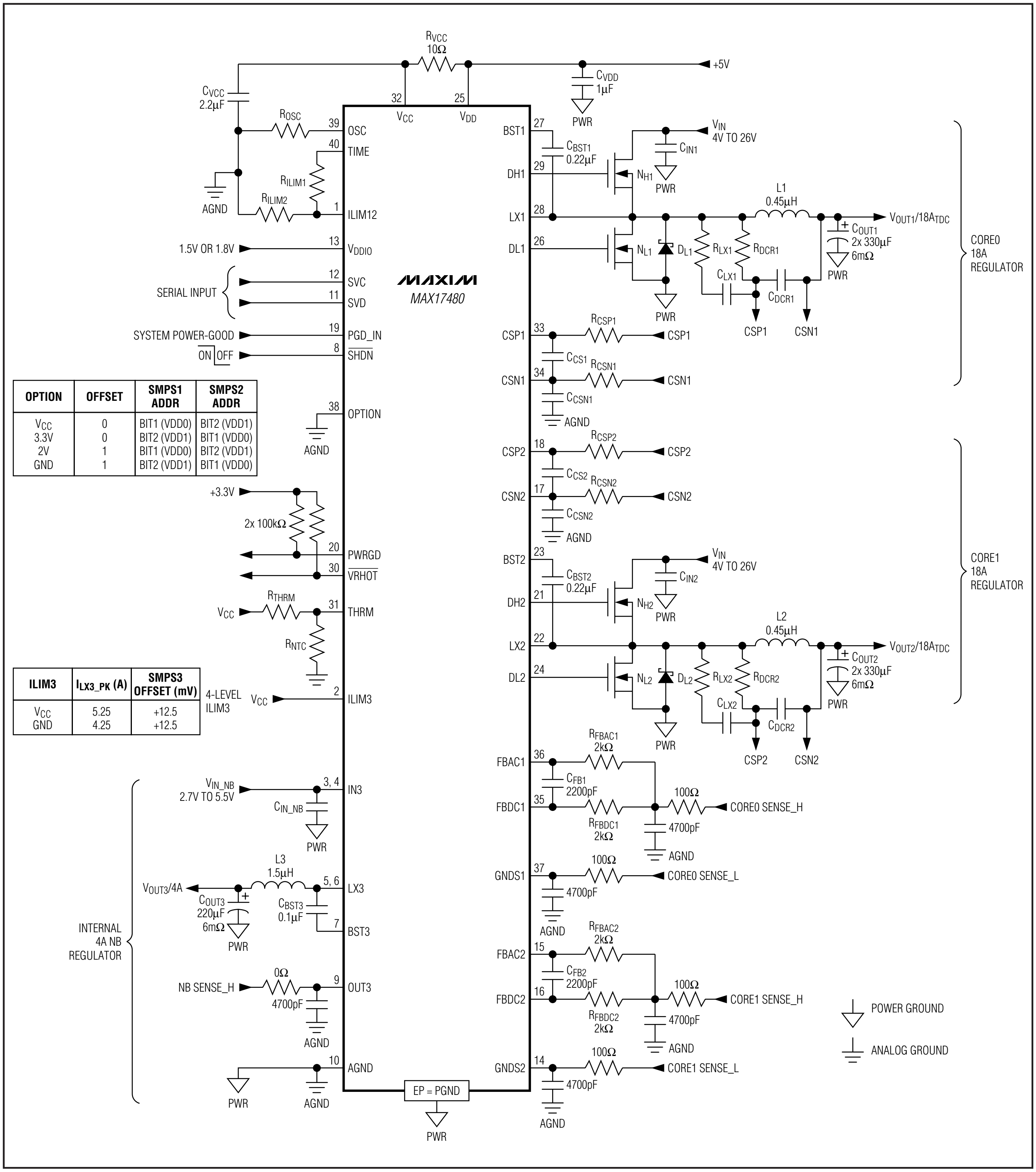
Note: *Mobile applications should be designed for separate mode operation. Component selection is dependent on AMD CPU AC and DC specifications.*

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corporation	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Siliconix (Vishay)	www.vishay.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

Standard Application Circuit

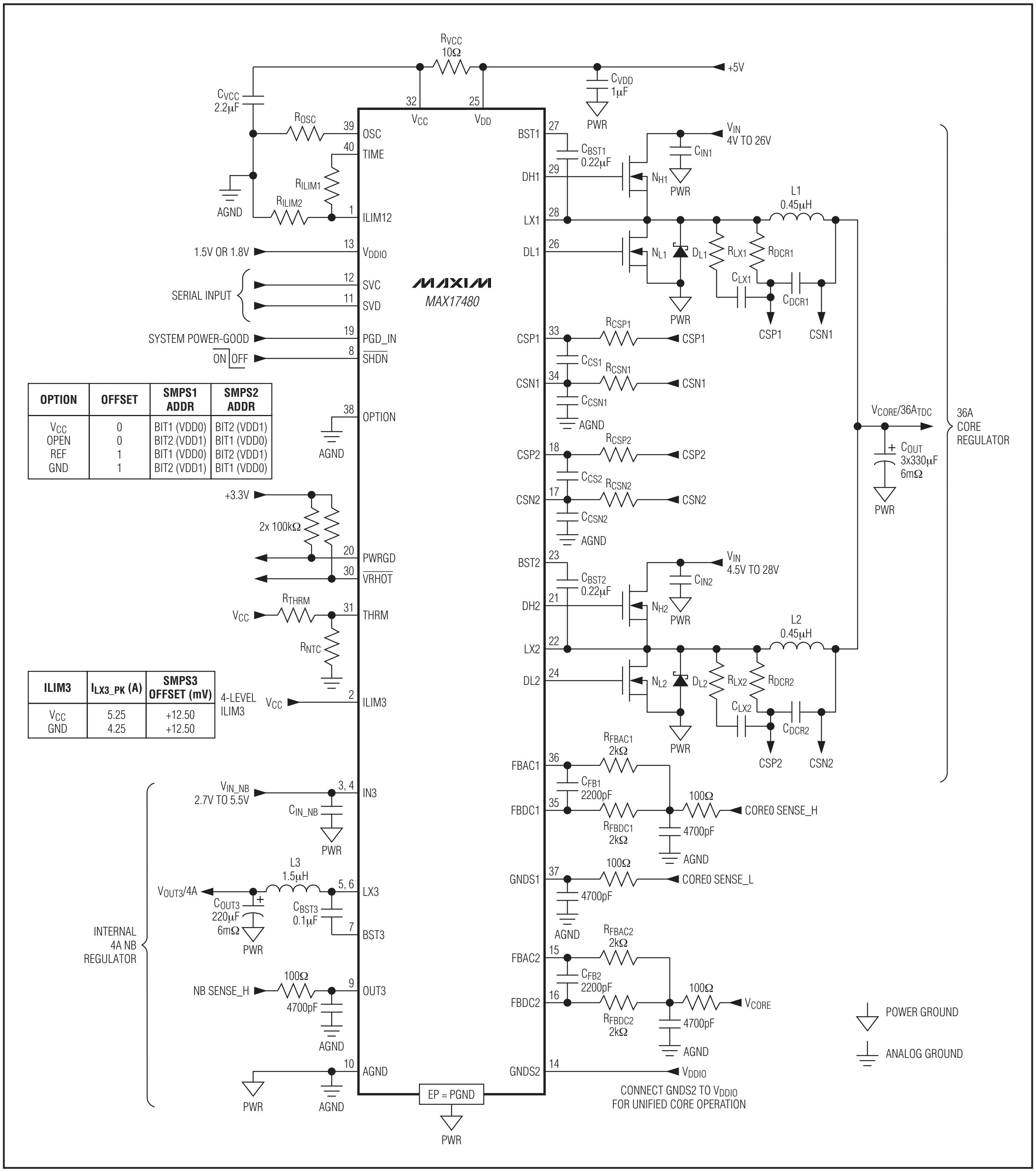
The MAX17480 standard application circuit (Figure 2) generates two independent 18A outputs and one 4A output for AMD mobile CPU applications. See Table 1 for component selections. Table 2 lists the component manufacturers.



OPTION	OFFSET	SMPS1 ADDR	SMPS2 ADDR
V_{CC}	0	BIT1 (VDD0)	BIT2 (VDD1)
3.3V	0	BIT2 (VDD1)	BIT1 (VDD0)
2V	1	BIT1 (VDD0)	BIT2 (VDD1)
GND	1	BIT2 (VDD1)	BIT1 (VDD0)

ILIM3	I_{LX3_PK} (A)	SMPS3 OFFSET (mV)
V_{CC}	5.25	+12.5
GND	4.25	+12.5

Figure 2. Griffin/Puma Standard Application Circuit



OPTION	OFFSET	SMPS1 ADDR	SMPS2 ADDR
V_{CC}	0	BIT1 (VDD0)	BIT2 (VDD1)
OPEN	0	BIT2 (VDD1)	BIT1 (VDD0)
REF	1	BIT1 (VDD0)	BIT2 (VDD1)
GND	1	BIT2 (VDD1)	BIT1 (VDD0)

ILIM3	I_{LX3_PK} (A)	SMPS3 OFFSET (mV)
V_{CC}	5.25	+12.50
GND	4.25	+12.50

Figure 3. Caspian/Tigris Standard Application Circuit

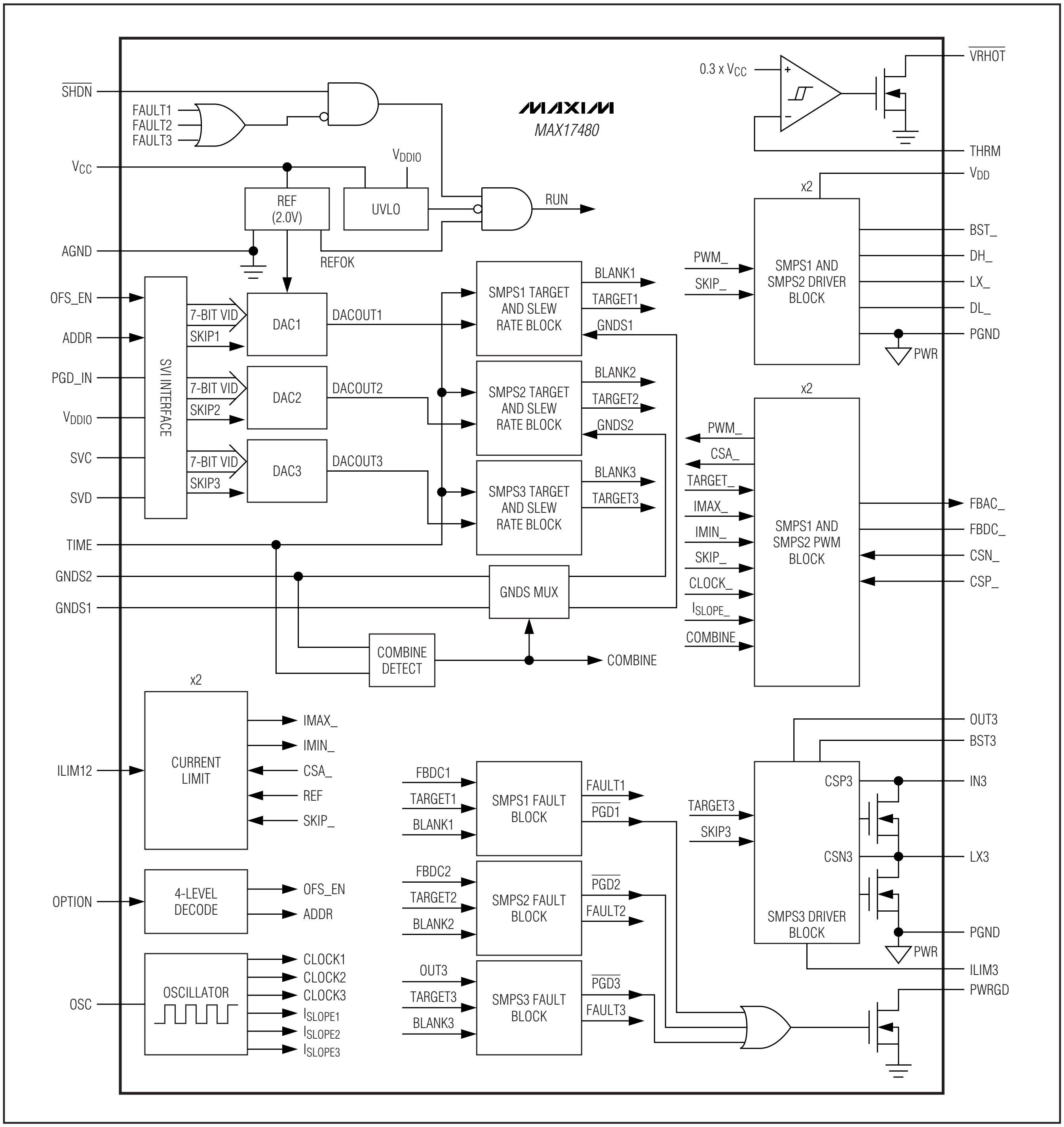


Figure 4. Functional Diagram

Detailed Description

The MAX17480 consists of a dual fixed-frequency PWM controller with external switches that generate the supply voltage for two independent CPU cores and one low-input-voltage internal switch SMPS for the separate NB SMPS. The CPU core SMPSs can be configured as independent outputs, or as a combined output by connecting the GNDS1 or GNDS2 pin-strap high (GNDS1 or GNDS2 pulled to 1.5V to 1.8V, which are the respective voltages for DDR3 and DDR2).

All three SMPSs can be programmed independently to any voltage in the VID table (see Table 4) using the serial VID interface (SVI). The CPU is the SVI bus master, while the MAX17480 is the SVI slave. Voltage transitions are commanded by the CPU as a single step command from one VID code to another. The MAX17480 slews the SMPS outputs at the slew rate programmed by the external R_{TIME} resistor during VID transitions and the transition from boot mode to VID mode.

During startup, the MAX17480 SMPSs are always in pulse-skipping mode. After exiting the boot mode, the individual PSI_L bit sets the respective SMPS into pulse-skipping mode or forced-PWM mode, depending on the system power state, and adds the +12.5mV offset for core supplies if enabled by the OPTION pin. In combined mode, the PSI_L bit adds the +12.5mV offset if enabled by the OPTION pin, and switches from 1-phase pulse-skipping mode to 2-phase PWM mode. Figure 4 is the MAX17480 functional diagram.

+5V Bias Supply (V_{CC}, V_{DD})

The MAX17480 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's main 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear SMPS that would otherwise be needed to supply the PWM circuit and gate drivers.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW\_CORE}Q_{G\_CORE} + f_{SW\_NB}Q_{G\_NB} = 50mA \text{ to } 70mA \text{ (typ)}$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW_CORE} and f_{SW_NB} are the respective core and NB SMPS switching frequencies, Q_{G_CORE} is the gate charge of the external MOSFETs as defined in the MOSFET data sheets, and Q_{G_NB} is approximately 2nC. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (OSC)

Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase):

$$f_{SW} = 300kHz \times 143k\Omega / R_{OSC}$$

A 71.4kΩ to 432kΩ resistor corresponds to switching frequencies of 600kHz to 100kHz, respectively, for the core SMPSs, and 1.2MHz to 200kHz for the NB SMPS. High-frequency (600kHz) operation for the core SMPS optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space.

The NB SMPS runs at twice the switching frequency of the core SMPSs. The low power of the NB rail allows for higher switching frequencies with little impact on the overall efficiency.

Minimum on-time ($t_{ON(MIN)}$) must be taken into consideration when selecting a switching frequency. See the Core Switching Frequency description in the *SMPS Design Procedure* section.

Interleaved Multiphase Operation

The MAX17480 interleaves both core SMPSs' phases—resulting in 180° out-of-phase operation that minimizes the input and output filtering requirements, reduces electromagnetic interference (EMI), and improves efficiency. The high-side MOSFETs do not turn on simultaneously during normal operation. The instantaneous input current is effectively reduced by the number of active phases, resulting in reduced input-voltage ripple, effective series resistance (ESR) power loss, and RMS ripple current (see the *Core Input Capacitor Selection* section). Therefore, the controller achieves high performance while minimizing the component count—which reduces cost, saves board space, and lowers component power requirements—making the MAX17480 ideal for high-power, cost-sensitive applications.

Transient Phase Repeat

When a transient occurs, the output voltage deviation depends on the controller's ability to quickly detect the transient and slew the inductor current. A fixed-frequency controller typically responds only when a clock edge occurs, resulting in a delayed transient response. To minimize this delay time, the MAX17480 includes enhanced transient detection and transient phase repeat capabilities. If the controller detects that the output voltage has dropped by 41mV, the transient detection comparator immediately retriggers the phase that completed its on-time last. The controller triggers the subsequent phases as normal, on the appropriate oscillator edges. This effectively triggers a phase a full cycle early, increasing the total inductor-current slew rate and providing an immediate transient response.

Core SMPS Feedback Adjustment Amplifiers

The MAX17480 provides an FBAC and FBDC pin for each SMPS to allow for flexible AC and DC droop settings. FBAC is the output of an internal transconductance amplifier that outputs a current proportional to the current-sense signal. FBDC is the feedback input that is compared against the internal target. Place resistors and capacitors at the FBAC and FBDC pins as shown in Figure 5. With this configuration, the DC droop is always less than or equal to the AC droop.

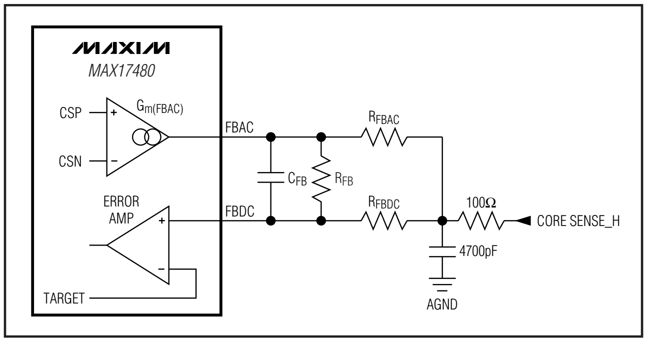


Figure 5. Core SMPS Feedback Connection

Core Steady-State Voltage Positioning (DC Droop)

FBDC is the feedback input to the error amplifier. Based on the configuration in Figure 5, the core SMPS output voltage is given by:

$$V_{OUT} = V_{TARGET} - \frac{R_{FBDC} \times R_{FBAC}}{R_{FBAC} + R_{FBDC} + R_{FB}} \times I_{FBAC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FBAC amplifier's output current (I_{FBAC}) is determined by each phase's current-sense voltage:

$$I_{FBAC} = G_{m(FBAC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FBAC)}$ is typically 2mS as defined in the *Electrical Characteristics* table. DC droop is typically used together with the +12.5mV offset feature to keep within the DC tolerance window of the application. See the *Offset and Address Change for Core SMPSs (OPTION)* section. The ripple voltage on FBDC must be less than the -33mV (max) transient phase repeat threshold:

$$\frac{\frac{R_{FBAC}}{R_{FBAC} + R_{FBDC} + R_{FB}} \Delta I_L R_{SENSE} G_{m(FBAC)} R_{FBDC} + \Delta I_L R_{ESR}}{2} \le 33\text{mV}$$

$$R_{FBDC} \le \frac{\left(66\text{mV} - \Delta I_L R_{ESR}\right)\left(R_{FBAC} + R_{FB}\right)}{R_{FBAC} \Delta I_L R_{SENSE} G_{m(FBAC)} - 66\text{mV}}$$

where ΔI_L is the inductor ripple current, R_{ESR} is the effective output ESR at the remote sense point, R_{SENSE} is the current-sense element, and $G_{m(FBAC)}$ is 2.06mS (max) as defined in the *Electrical Characteristics* table. The worst-case inductor ripple occurs at the maximum input-voltage and maximum output-voltage conditions:

$$\Delta I_{L(MAX)} = \frac{V_{OUT(MAX)}\left(V_{IN(MAX)} - V_{OUT(MAX)}\right)}{V_{IN(MAX)} f_{SW} L}$$

To make the DC and AC load-lines the same, directly short FBAC to FBDC.

To disable DC voltage positioning, remove R_{FB}, which connects FBAC to FBDC.

Core Transient Voltage-Positioning Amplifier (AC Droop)

Each of the MAX17480 core supply SMPSs includes one transconductance amplifier for voltage positioning. The amplifiers' inputs are generated by summing their respective current-sense inputs, which differentially sense the voltage across either current-sense resistor or the inductor's DCR.

The voltage-positioning droop amplifier's output (FBAC) connects to the remote-sense point of the output through an RC network that sets each phase's AC voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - \frac{R_{FBAC} \times R_{FBDC}}{R_{FBAC} + R_{FBDC} + R_{FB} \parallel Z_{CFB}} I_{FBDC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, Z_{CFB} is the effective impedance of C_{FB}, and the FBAC amplifier's output current (I_{FBAC}) is determined by each phase's current-sense voltage:

$$I_{FBAC} = G_{m(FBAC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FBAC)}$ is 2.06mS (max) as defined in the *Electrical Characteristics* table.

AC droop is required for stable operation of the MAX17480. A minimum of 1.5mV/A is recommended. AC droop must not be disabled.

Core Differential Remote Sense

The MAX17480 controller includes independent differential, remote-sense inputs for each CPU core to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense (FBDC_) input connects to the remote-sensed output through the resistance at FBDC_ ($R_{FBDC\_}$). The ground-sense (GNDS_) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the feedback-sense (FBDC_) $R_{FBDC\_}$ resistor and ground-sense (GNDS_) input directly to the respective CPU core's remote-sense outputs as shown in Figure 2.

GNDS1 and GNDS2 are dual-function pins. At power-on, the voltage levels on GNDS1 and GNDS2 configure the MAX17480 as two independent switching SMPSs, or one higher current 2-phase SMPS. Keep both GNDS1 and GNDS2 low during power-up to configure the MAX17480 in separate mode. Connect GNDS1 or GNDS2 to a voltage above 0.8V (typ) for combined-mode operation. In the AMD mobile system, this is automatically done by the CPU that is plugged into the socket that pulls GNDS1 or GNDS2 the V_{DDIO} voltage level.

When GNDS1 is pulled high to indicate combined-mode operation, the remote ground sense is automatically switched to GNDS2. When GNDS2 is pulled high to indicate combined-mode operation, the remote ground sense is automatically switched to GNDS1. GNDS1 and GNDS2 do not dynamically switch in the real application. It is only switched when one CPU is removed (e.g., split-core CPU), and another is plugged in (e.g., combined-core CPU). This should not be done when the socket is "hot" (i.e., powered).

The MAX17480 checks the GNDS1 and GNDS2 levels at the time when the internal REFOK signal goes high, and latches the operating mode information (separate or combined mode). This latch is cleared by cycling the $\overline{\text{SHDN}}$ pin.

Core Integrator Amplifier

An internal integrator amplifier forces the DC average of the FBDC_ voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 4), allowing accurate DC output-voltage regulation regardless of the output ripple voltage.

The MAX17480 disables the integrator during downward VID transitions done in pulse-skipping mode. The integrator remains disabled until the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

The integrator amplifier can shift the output voltage by ±80mV (min). The maximum difference between transient AC droop and DC droop should not exceed ±80mV at the maximum allowed load current to guarantee proper DC output-voltage accuracy over the full load conditions.

NB SMPS Feedback Adjustment Amplifiers

NB Steady-State Voltage Positioning (DC Droop)

The NB SMPS has a built-in load-line that is -5.5mV/A. The output peak voltage (V_{OUT3_PK+}) is set to:

$$V_{OUT3\_PK} = V_{TARGET3} - 5.5mV/A \times (I_{LOAD3} + \frac{\Delta I_{L3}}{2})$$

$$\Delta I_{L3} = \frac{(V_{IN3} - V_{OUT3}) \times V_{OUT3}}{L_3 \times V_{IN3} \times f_{SW3}}$$

where the target voltage ($V_{TARGET3}$) is defined in the *Nominal Output-Voltage Selection* section, f_{SW3} is the NB switching frequency, and I_{LOAD3} is the output load current of the NB SMPS.

2-Wire Serial Interface (SVC, SVD)

The MAX17480 supports the 2-wire, write-only, serial-interface bus as defined by the AMD serial VID interface specification. The serial interface is similar to the high-speed 3.4MHz I^2C bus, but without the master mode sequence. The bus consists of a clock line (SVC) and a data line (SVD). The CPU is the bus master, and the MAX17480 is the slave. The MAX17480 serial interface works from 100kHz to 3.4MHz. In the AMD mobile application, the bus runs at 3.4MHz.

The serial interface is active only after PGD_IN goes high in the startup sequence. The CPU sets the VID voltage of the three internal DACs and the PSI_L bit through the serial interface.

During the startup sequence, the SVC and SVD inputs serve an alternate function to set the 2-bit boot VID for all three DACs while PWRGD is low.

Nominal Output-Voltage Selection

Core SMPS Output Voltage

The nominal no-load output voltage (V_{TARGET}) for each SMPS is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) and the offset voltage (V_{OFFSET}) as defined in the following equation:

$$V_{TARGET} = V_{FBDC} = V_{DAC} + V_{GNDS} + V_{OFFSET}$$

where V_{DAC} is the selected VID voltage of the core SMPS DAC, V_{GNDS} is the ground-sense correction voltage for core supplies, and V_{OFFSET} is the +12.5mV offset enabled by the OPTION pin when the PSI_L is set high for core supplies.

NB SMPS Output Voltage

The nominal output voltage (V_{TARGET}) for the NB is defined by the selected voltage reference (VID DAC) plus the offset voltage (V_{OFFSET_NB}) as defined in the following equation:

$$V_{TARGET3} = V_{OUT3} = V_{DAC} + V_{OFFSET\_NB}$$

where V_{DAC} is the selected VID voltage of the NB DAC, and V_{OFFSET_NB} is +12.5mV.

7-Bit DAC

Inside the MAX17480 are three 7-bit digital-to-analog converters (DACs). Each DAC can be individually programmed to different voltage levels by the serial-interface bus. The DAC sets the target for the output voltage for the core and NB SMPSs. The available DAC codes and resulting output voltages are compatible with the AMD SVI (Table 4) specifications.

Boot Voltage

On startup, the MAX17480 slews the target for all three DACs from ground to the boot voltage set by the SVC and SVD pin-voltage levels. While the output is still below regulation, the SVC and SVD levels can be changed, and the MAX17480 sets the DACs to the new boot voltage. Once the programmed boot voltage is reached and PWRGD goes high, the MAX17480 stores the boot VID. Changes in the SVC and SVD settings do not change the output voltage once the boot VID is stored. When PGD_IN goes high, the MAX17480 exits boot mode, and the three DACs can be independently set to any voltage in the VID table by the serial interface.

If PGD_IN goes from high to low any time after the boot VID is stored, the MAX17480 sets all three DACs back to the voltage of the stored boot VID.

Table 3 is the boot voltage code table.

Table 3. Boot Voltage Code Table

SVC	SVD	BOOT VOLTAGE V_{OUT} (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Core SMPS Offset

A +12.5mV offset can be added to both core SMPS DAC voltages for applications that include DC droop. The offset is applied only after the MAX17480 exits boot mode (PGD_IN going from low to high), and the MAX17480 enters the serial-interface mode. The offset is disabled when the PSI_L bit is set, saving more power when the load is light.

The OPTION pin setting enables or disables the +12.5mV offset. Connect OPTION to OSC (2V) or GND to enable the offset. Keep OPTION connected to 3.3V or V_{CC} to disable the offset. See the *Offset and Address Change for Core SMPSs (OPTION)* section.

NB SMPS Offset

The NB SMPS output has a -5.5mV/A load line. A +12.5mV offset is added to keep the output within regulation over the full load. See the *Offset and Current-Limit Setting for NB SMPS (ILIM3)* section.

Output-Voltage Transition Timing

SMPS Output-Voltage Transition

The MAX17480 performs positive voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output-voltage level with the lowest possible peak currents for a given output capacitance. The slew rate (set by resistor R_{TIME}) must be set fast enough to ensure that the transition is completed within the maximum allotted time for proper CPU operation. R_{TIME} is between 35.7kΩ and 357kΩ for corresponding slew rates between 25mV/µs to 2.5mV/µs, respectively, for the SMPSs.

At the beginning of an output-voltage transition, the MAX17480 blanks both PWRGD comparator thresholds, preventing the PWRGD open-drain output from changing states during the transition. At the end of an upward VID transition, the controller enables both PWRGD thresholds approximately 20µs after the slew-rate controller reaches the target output voltage. At the end

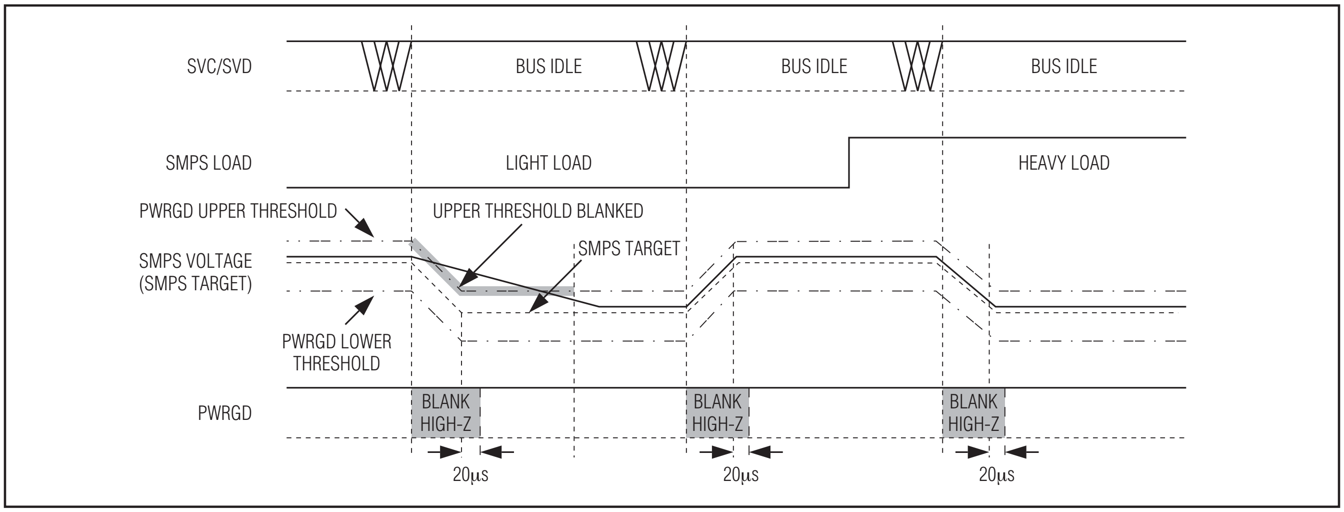


Figure 6. VID Transition Timing

of a downward VID transition, the upper PWRGD threshold is enabled only after the output reaches the lower VID code setting. Figure 6 shows VID transition timing.

The MAX17480 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current source programmed by R_{TIME} to transition the output voltage. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit set by ILIM12 for the core SMPSs and ILIM3 for the NB SMPS. For all dynamic positive VID transitions or negative VID transitions in forced-PWM mode (PSI_L set to 1), the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{\left[V_{NEW} - V_{OLD}\right]}{\left(dV_{TARGET}/dt\right)}$$

where $dV_{TARGET}/dt = 6.25mV/\mu s \times 143k\Omega/R_{TIME}$ is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See the Slew-Rate Accuracy in the *Electrical Characteristics* table for slew-rate limits.

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. The average inductor current per phase required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times \left(dV_{TARGET}/dt\right)$$

where dV_{TARGET}/dt is the required slew rate and C_{OUT} is the total output capacitance of each phase.

If the SMPS is in a pulse-skipping mode (PSI_L set to 0), the discharge rate of the output voltage during downward transitions is then dependent on the load current and total output capacitance for loads less than a minimum current, and dependent on the R_{TIME} programmed slew rate for heavier loads. The critical load current ($I_{LOAD(CRIT)}$) where the transition time is dependent on the load is:

$$I_{LOAD(CRIT)} \cong C_{OUT} \times \left(dV_{TARGET}/dt\right)$$

For load currents less than $I_{LOAD(CRIT)}$, the transition time is:

$$t_{TRAN} \cong \frac{C_{OUT} \times dV_{TARGET}}{I_{LOAD}}$$

For soft-start, the controller uses a fixed slew rate of 1mV/µs. In shutdown, the outputs are discharged using a 20Ω switch through the CSN_ pins for the core SMPSs and through the OUT3 pin for the NB SMPS.

Forced-PWM Operation

After exiting the boot mode and if the PSI_L bit is set to 1, the MAX17480 operates with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output-voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 50mA to 70mA, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light load conditions, the processor could switch the controller to a low-power pulse-skipping control scheme.

Pulse-Skipping Operation

During soft-start and in power-saving mode—when the PSI_L bit is set to 0—the MAX17480 operates in pulse-skipping mode. Pulse-skipping mode enables the driver's zero-crossing comparator, so the driver pulls its DL low when "zero" inductor current is detected (V_{GND} - V_{LX} = 0). This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light load conditions to avoid overcharging the output.

In pulse-skipping operation, the controller terminates the on-time when the output voltage exceeds the feedback threshold **and** when the current-sense voltage exceeds the idle-mode current-sense threshold (V_{IDLE} = 0.15 x V_{LIMIT} for the core SMPS and I_{LX3MIN} = 0.25 x I_{LX3PK} setting for the NB SMPS). Under heavy load conditions, the continuous inductor current remains above the idle-mode current-sense threshold, so the on-time depends only on the feedback voltage threshold. Under light load conditions, the controller remains above the feedback voltage threshold, so the on-time duration depends solely on the idle-mode current-sense threshold, which is approximately 15% of the full-load peak current-limit threshold set by ILIM12 for the core SMPSs and 25% of the full-load peak current-limit threshold set by ILIM3 for the NB SMPS.

During downward VID transitions, the controller temporarily sets the OVP threshold of the SMPSs to 1.85V (typ), preventing false OVP faults. Once the error amplifier detects that the output voltage is in regulation, the OVP threshold tracks the selected VID DAC code.

Each SMPS can be individually set to operate in pulse-skipping mode when its PSI_L bit is set to 0, or set to operate in forced-PWM mode when its PSI_L bit is set to 1.

When the core SMPSs are configured for combined-mode operation, core supplies operate in 1-phase pulse-skipping mode when PSI_L = 0, and core supplies are in 2-phase forced-PWM mode when PSI_L = 1.

Idle-Mode Current-Sense Threshold

The idle-mode current-sense threshold forces a lightly loaded SMPS to source a minimum amount of power with each on-time since the controller cannot terminate the on-time until the current-sense voltage exceeds the idle-mode current-sense threshold (V_{IDLE} = 0.15 x V_{LIMIT} for the core SMPS and I_{LX3MIN} = 0.25 x I_{LX3PK} setting for the NB SMPS). Since the zero-crossing comparator prevents the switching SMPS from sinking current, the controller must skip pulses to avoid overcharging the output. When the clock edge occurs, if the output voltage still exceeds the feedback threshold, the controller does not initiate another on-time. This forces the controller to actually regulate the valley of the output voltage ripple under light load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, the MAX17480 zero-crossing comparators are active. Therefore, an inherent automatic switchover to PFM takes place at light loads, resulting in a highly efficient operating mode. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The driver's zero-crossing comparator senses the inductor current across the low-side MOSFET. Once V_{GND} - V_{LX} drops below the zero-crossing threshold, the driver forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which the PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2V_{IN}f_{SW}L}$$

The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-off in PFM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Current Sense

Core SMPS Current Sense

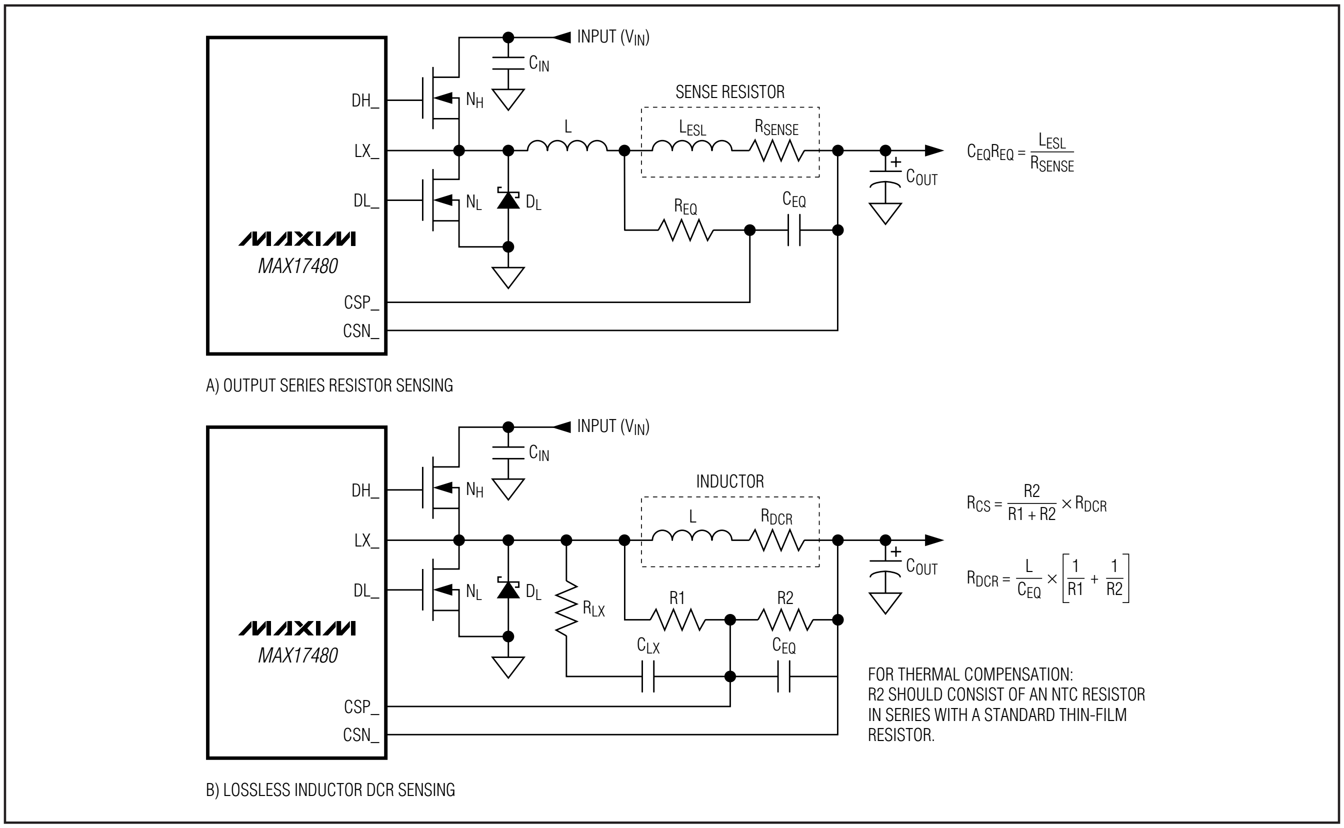
The output current of each phase is sensed differentially. A low offset voltage and high-gain differential current amplifier at each phase allows low-resistance current-sense resistors to be used to minimize power dissipation. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Table 4. Output-Voltage VID DAC Codes

SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500	110_0000	0.3500
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375	110_0001	0.3375
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250	110_0010	0.3250
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125	110_0011	0.3125
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000	110_0100	0.3000
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875	110_0101	0.2875
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750	110_0110	0.2750
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625	110_0111	0.2625
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500	110_1000	0.2500
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375	110_1001	0.2375
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250	110_1010	0.2250
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125	110_1011	0.2125
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000	110_1100	0.2000
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875	110_1101	0.1875
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750	110_1110	0.1750
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625	110_1111	0.1625
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500	111_0000	0.1500
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375	111_0001	0.1375
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250	111_0010	0.1250
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125	111_0011	0.1125
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000	111_0100	0.1000
001_0101	1.2875	011_0101	0.8875	101_0101	0.4875	111_0101	0.0875
001_0110	1.2750	011_0110	0.8750	101_0110	0.4750	111_0110	0.0750
001_0111	1.2625	011_0111	0.8625	101_0111	0.4625	111_0111	0.0625
001_1000	1.2500	011_1000	0.8500	101_1000	0.4500	111_1000	0.0500
001_1001	1.2375	011_1001	0.8375	101_1001	0.4375	111_1001	0.0375
001_1010	1.2250	011_1010	0.8250	101_1010	0.4250	111_1010	0.0250
001_1011	1.2125	011_1011	0.8125	101_1011	0.4125	111_1011	0.0125
001_1100	1.2000	011_1100	0.8000	101_1100	0.4000	111_1100	OFF
001_1101	1.1875	011_1101	0.7875	101_1101	0.3875	111_1101	OFF
001_1110	1.1750	011_1110	0.7750	101_1110	0.3750	111_1110	OFF
001_1111	1.1625	011_1111	0.7625	101_1111	0.3625	111_1111	OFF

Note: *The NB SMPS output voltage has an offset of +12.5mV.*

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 7). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and early current-limit detection. Similar to the inductor DCR sensing method above, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:



FOR THERMAL COMPENSATION:
R2 SHOULD CONSIST OF AN NTC RESISTOR IN SERIES WITH A STANDARD THIN-FILM RESISTOR.

Figure 7. Current-Sense Configurations

$$\frac{L_{ESL}}{R_{SENSE}} = R_{EQ}C_{SENSE}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{SENSE} and R_{EQ} are the time-constant matching components.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 7). The time constant of the RC network should match the inductor's time constant (L/R_{DCR}):

$$\frac{L}{R_{DCR}} = R_{EQ}C_{SENSE}$$

where C_{SENSE} and R_{EQ} are the time-constant matching components. To minimize the current-sense error due to the current-sense inputs' bias current (I_{CSP} and I_{CSN}), choose R_{EQ} less than 2kΩ and use the above equation to determine the sense capacitance (C_{SENSE}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Core Voltage Positioning and Loop Compensation* section for detailed information.

Additional R_{LX} and C_{LX} are always added between the LX_ and CSP_ pins if DCR sensing is used, and they provide additional overdrive to the current-sense signal to improve the noise immunity; otherwise, there might be too much jitter or the system could be unstable.

NB SMPS Current Sense

The NB current sense is achieved by sensing the voltage across the high-side internal MOSFET during the on-time. The current information is computed by dividing the sensed voltage by the MOSFET's on-resistance, $R_{ON(NH3)}$.

Combined-Mode Current Balance

When the core SMPSs are configured in combined mode (GNDS1 or GNDS2 pulled to V_{DDIO}), the MAX17480 current-mode architecture automatically forces the individual phases to remain current balanced. SMPS1 is the main voltage-control loop, and SMPS2 maintains the current balance between the phases. This control scheme regulates the peak inductor current of each phase, forcing them to remain properly balanced. Therefore, the average inductor current variation depends mainly on the variation in the current-sense element and inductance value.

Peak Current Limit

The MAX17480 current-limit circuit employs a fast peak inductor current-sensing algorithm. Once the current-sense signal of the SMPS exceeds the peak current-limit threshold, the PWM controller terminates the on-time. See the *Core Peak Inductor Current Limit (ILIM12)* section in the *Core SMPS Design Procedure* section.

Power-Up Sequence (POR, UVLO, PGD_IN)

Power-on reset (POR) occurs when V_{CC} rises above approximately 3V, resetting the fault latch and preparing the controller for operation. The V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching until V_{CC} rises above 4.25V (typ). The controller powers up the reference once the system enables the controller V_{CC} above 4.25V and $\overline{\text{SHDN}}$ is driven high. With the reference in regulation, the controller ramps the SMPS and NB voltages to the boot voltage set by the SVC and SVD inputs:

$$t_{START} = \frac{V_{BOOT}}{(1mV/\mu s)}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PWRGD becomes high impedance approximately 20µs after the SMPS outputs reach regulation. The boot VID is stored the first time PWRGD goes high. The MAX17480 is in pulse-skipping mode during soft-start. Figure 8 shows the MAX17480 startup sequence.

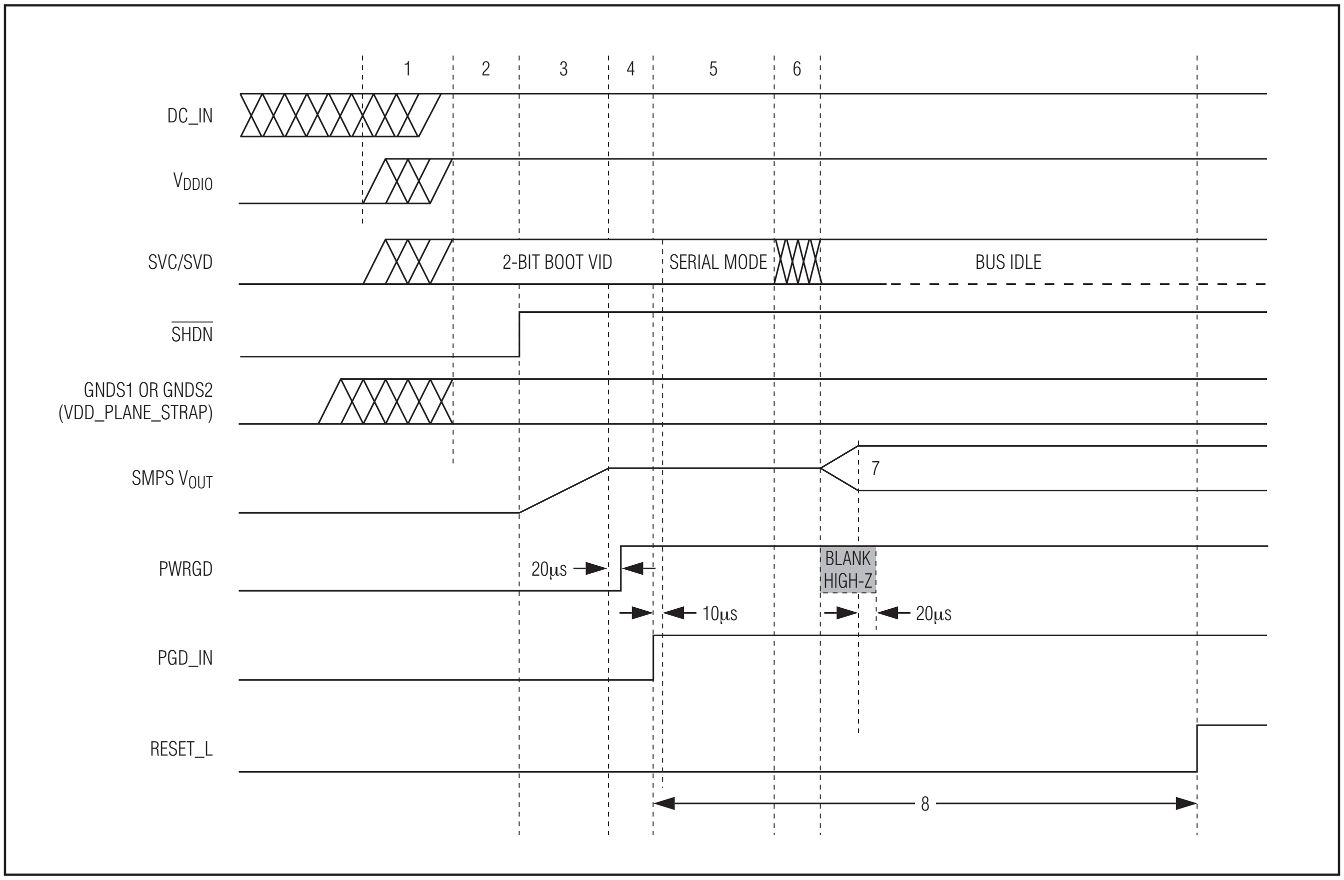


Figure 8. Startup Sequence

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling $\overline{\text{SHDN}}$ or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions and could also result in the stored boot VIDs being corrupted. As such, the MAX17480 immediately stops switching (DH_ and DL_ pulled low), latches off, and discharges the outputs using the internal 20Ω switches from CSN_ to GND.

Notes for Figure 8:

1) The relationship between DC_IN and V_{DDIO} is not guaranteed. It is possible to have V_{DDIO} powered when DC_IN is not powered, and it is possible to have DC_IN power up before V_{DDIO} powers up.
2) As the V_{DDIO} power rail comes within specification, VDD_Plane_Strap becomes valid and SVC and SVD are driven to the boot VID value by the processor. The system guarantees that V_{DDIO} is in specification and SVC and SVD are driven to the boot VID value for at least 10µs prior to $\overline{\text{SHDN}}$ being asserted to the MAX17480.
3) After $\overline{\text{SHDN}}$ is asserted, the MAX17480 samples and latches the VDD_Plane_Strap level at its GNDS1 and GNDS2 pins when REF reaches the REFOK threshold, and ramps up the voltage plane outputs to the level indicated by the 2-bit boot VID. The boot VID is stored in the MAX17480 for use when PGD_IN deasserts. The MAX17480 soft-starts the output rails to limit inrush current from the DC_IN rail. The MAX17480 operates in pulse-skipping mode in the boot mode regardless of PSI_L settings.
4) The MAX17480 asserts PWRGD. After PWRGD is asserted and all system-wide voltage planes and free-running clocks are within specification, then the system asserts PGD_IN.
5) The processor holds the 2-bit boot VID for at least 10µs after PGD_IN is asserted.
6) The processor issues the set VID command through SVI.
7) The MAX17480 transitions the voltage planes to the set VID. The set VID can be greater than or less than the boot VID voltage. The MAX17480 operates in pulse-skipping mode or forced-PWM mode according to the PSI_L setting.
8) The chipset enforces a 1ms delay between PGD_IN assertion and RESET_L deassertion.

PWRGD

The MAX17480 features internal power-good fault comparators for each SMPS. The outputs of these individual power-good fault comparators are logically ORed to drive the gate of the open-drain PWRGD output transistor. Each SMPS's power-good fault comparator has an upper threshold of +200mV (typ) and a lower threshold of -300mV (typ). PWRGD goes low if the output of either SMPS exceeds its respective threshold.

PWRGD is forced low during the startup sequence up to 20µs after the output is in regulation. The 2-bit boot VID is stored when PWRGD goes high during the startup sequence. PWRGD is immediately forced low when $\overline{\text{SHDN}}$ goes low.

PWRGD is blanked high impedance while any of the internal SMPS DACs are slewing during a VID transition, plus an additional 20µs after the DAC transition is completed. For downward VID transitions, the upper threshold of the particular power-good fault comparators remains blanked until the output reaches regulation again.

PWRGD is blanked high impedance for each SMPS whose internal DAC is in off mode, and is pulled low if all three SMPS DACs are in off mode.

PGD_IN

After the SMPS outputs reach the boot voltage, the MAX17480 switches to the serial-interface mode when PGD_IN goes high. Anytime during normal operation, a high-to-low transition on PGD_IN causes the MAX17480 to slew all three internal DACs back to the stored boot VIDs. The SVC and SVD inputs are disabled during the time that PGD_IN is low. The serial interface is reenabled when PGD_IN goes high again. Figure 9 shows PGD_IN timing.

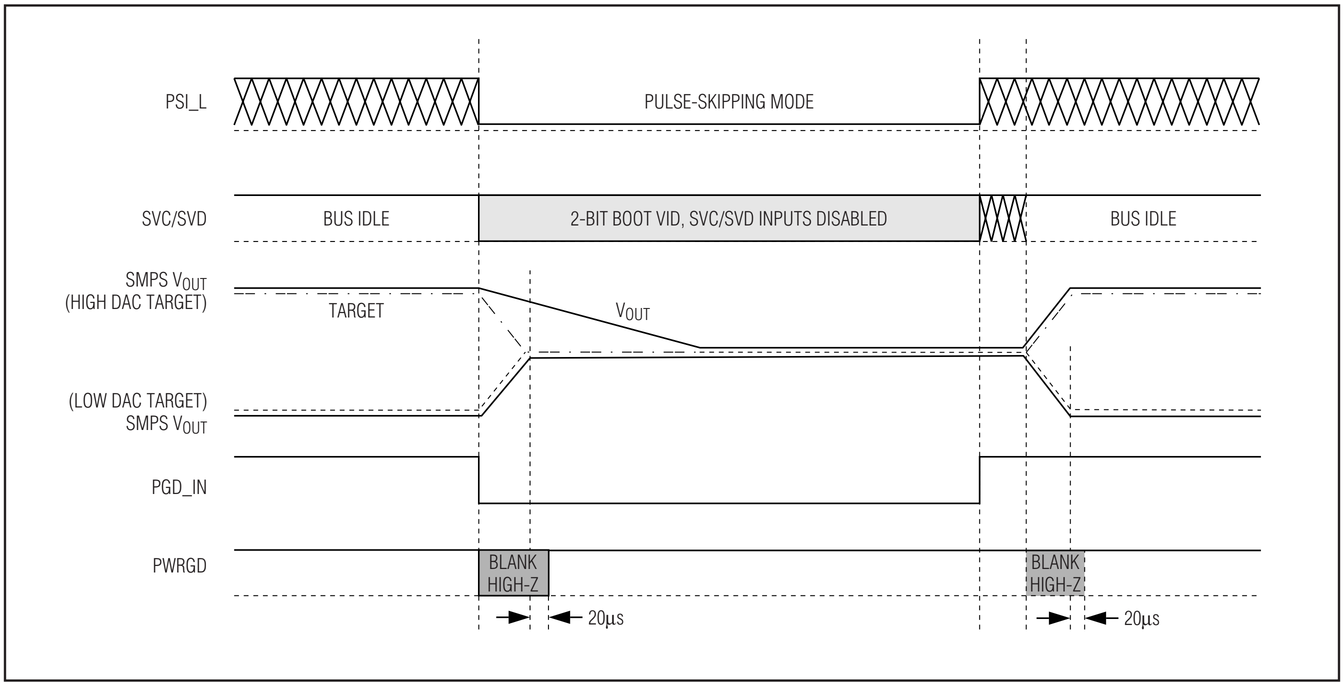


Figure 9. PGD_IN Timing

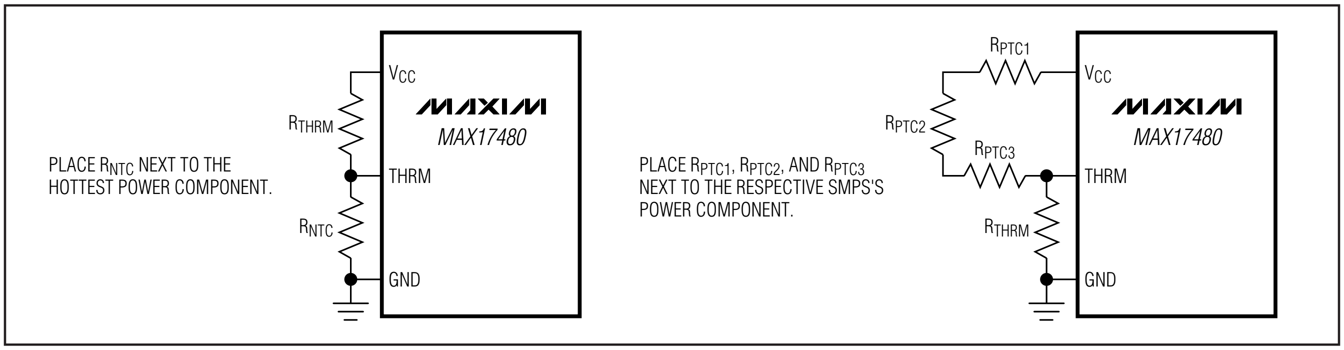


Figure 10. THRM Configuration

Shutdown

When $\overline{\text{SHDN}}$ goes low, the MAX17480 enters shutdown mode. PWRGD is pulled low immediately and forces all DH and DL low, and all three outputs are discharged through the 20Ω internal discharge FETs through the CSN pin for core SMPSs and through the OUT3 pin for NB SMPSs.

$\overline{\text{VRHOT}}$ Temperature Comparator

The MAX17480 features an independent comparator with an accurate threshold (V_{HOT}) that tracks the analog supply voltage ($V_{HOT} = 0.3V_{CC}$). Use a resistor- and thermistor-divider between V_{CC} and GND to generate a voltage-SMPS overtemperature monitor. Place the thermistor as close as possible to the MOSFETs and inductors.

Place three individual thermistors near to each SMPS to monitor the temperature of the respective SMPS. When core SMPSs are in combined-mode operation, the current-balance circuit balances the currents between core SMPS phases. As such, the power loss and heat in each phase should be identical, apart from the effects of placement and airflow over each phase. Single thermistors can be placed near either of the phases and still be effective for core SMPS temperature monitoring, and one thermistor can be saved. See Figure 10.

Fault Protection (Latched)

Output Overvoltage Protection (OVP)

The overvoltage protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17480 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set VID DAC voltage by more than 300mV. The OVP threshold tracks the VID DAC voltage except during a downward VID transition. During a downward VID transition, the OVP threshold is set at 1.85V (typ) until the output reaches regulation, when the OVP threshold is reset back to 300mV above the VID setting.

When the OVP circuit detects an overvoltage fault in core SMPSs, it immediately sets the fault latch and forces the external low-side driver high on the faulted SMPS. The nonfaulted SMPSs are also shut down by turning on the internal passive discharge MOSFET. The synchronous-rectifier MOSFETs of the faulted side are turned on with 100% duty, which rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. Toggle $\overline{\text{SHDN}}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

When the core SMPSs are configured in combined mode, the synchronous-rectifier MOSFETs of both phases are turned on with 100% duty in response to an overvoltage fault. Passive shutdown is initiated for the NB SMPS.

The NB SMPS has no OVP.

Output Undervoltage Protection (UVP)

If any of the MAX17480 output voltages are 400mV below the target voltage, the controller sets the fault latch, shuts down all the SMPSs, and activates the internal passive discharge MOSFET. Toggle $\overline{\text{SHDN}}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

V_{CC} Undervoltage-Lockout (UVLO) Protection

If the V_{CC} voltage drops below 4.2V (typ), the controller assumes that there is not enough supply voltage to make valid decisions and sets a fault latch. During a UVLO fault, the controller shuts down all the SMPSs immediately, forces DL and DH low, and pulls CSN1, CSN2, and OUT3 low through internal 20Ω discharge FETs. If the V_{CC} falls below the POR threshold (1.8V, typ), DL is forced low even if it was previously high due to a latched overvoltage fault.

Toggle $\overline{\text{SHDN}}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

V_{DDIO} Undervoltage-Lockout (UVLO) Protection

If the V_{DDIO} voltage drops below 0.7V (typ), the controller assumes that there is not enough supply voltage to make valid decisions and sets a UV fault latch. During V_{DDIO} UVLO, as with UVP, the controller shuts down all the SMPSs immediately, forces DL and DH low, and pulls CSN1, CSN2, and OUT3 low through internal 20Ω discharge FETs. If the V_{CC} falls below the POR threshold (1.8V, typ), DL is forced low even if it was previously high due to a latched overvoltage fault.

Toggle $\overline{\text{SHDN}}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

Thermal Fault Protection

The MAX17480 features a thermal fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and shuts down immediately, forcing DH and DL low and turning on the 20Ω discharge FETs for all SMPSs. Toggle $\overline{\text{SHDN}}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Other Fault Protection (Nonlatched)

V_{IN3} Undervoltage-Lockout (UVLO) Protection

If the V_{IN3} voltage drops below 2.5V (typ), the controller assumes that there is not enough input voltage for NB SMPSs. If V_{IN3} UVLO happens before or just after soft-start, the NB SMPS is disabled and the internal target voltage stays off. When the V_{IN3} subsequently rises past its UVLO rising threshold 2.6V (typ), NB goes through the soft-start sequence with a 1mV/µs slew rate.

If V_{IN3} UVLO happens while the MAX17480 is running, the NB SMPS is stopped, the NB target is reset to 0 immediately, and PWRGD is forced low. When V_{IN3} subsequently rises above the UVLO rising threshold 2.6V (typ), the NB SMPS restarts with 1mV/µs slew rate to the previous DAC target.

Core SMPS MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH) source and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17480 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.25Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces could require rising LX edges that do not pull up the low-side MOSFET’s gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET’s gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

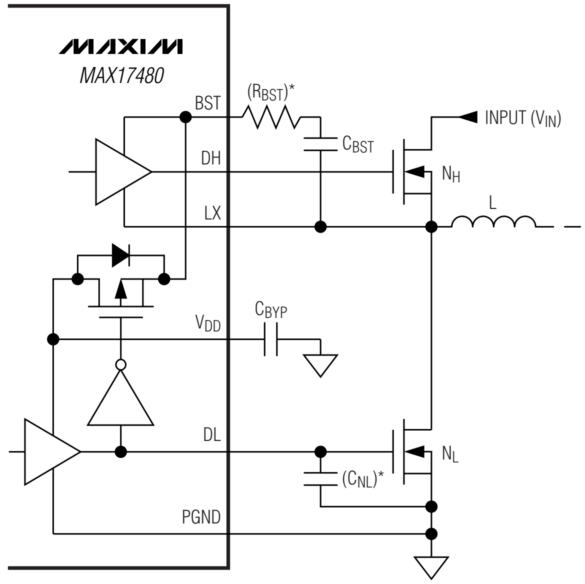
Typically, adding a 4700pF capacitor between DL and power ground (C_{NL} in Figure 11), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 11). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Offset and Address Change for Core SMPSs (OPTION)

The +12.5mV offset and the address change features of the MAX17480 can be selectively enabled and disabled by the OPTION pin setting. When the offset is enabled, setting the PSI_L bit to 0 disables the offset, reducing power consumption in the low-power state. See the *Core SMPS Offset* section for a detailed description of this feature.

In addition, the address of the core SMPSs can be exchanged, allowing for flexible layout of the MAX17480 with respect to the CPU placement on the same or opposite sides of the PCB. Table 5 shows the OPTION pin voltage levels and the features that are enabled.



(R_{BST})* OPTIONAL—THE RESISTOR LOWERS EMI BY DECREASING THE SWITCHING NODE RISE TIME.

(C_{NL})* OPTIONAL—THE CAPACITOR REDUCES LX-TO-DL CAPACITIVE COUPLING THAT CAN CAUSE SHOOT-THROUGH CURRENTS.

Figure 11. Gate-Drive Circuit

Table 5. OPTION Pin Settings

OPTION	OFFSET ENABLES	SMPS1 ADDRESS	SMPS2 ADDRESS
V_{CC}	0	BIT 1 (VDD0)	BIT 2 (VDD1)
3.3V	0	BIT 2 (VDD1)	BIT 1 (VDD0)
2V	1	BIT 1 (VDD0)	BIT 2 (VDD1)
GND	1	BIT 2 (VDD1)	BIT 1 (VDD0)

Note: *VDD0 refers to CORE0 and VDD1 refers to CORE1 for the AMD CPU.*

Table 6. ILIM3 Setting

ILIM3	PEAK CURRENT LIMIT (A)	SKIP CURRENT LIMIT (A)	MAX DC CURRENT (A)	FULL-LOAD DROOP (mV)	OFFSET (mV)
V_{CC}	5.25	1.3	4.75	-26.13	12.5
GND	4.25	1.05	3.75	-20.63	12.5

Offset and Current-Limit Setting for NB SMPS (ILIM3)

The offset and current-limit settings of the NB SMPS can be set by the ILIM3 pin setting. Table 6 shows the ILIM3 pin voltage levels and the corresponding settings for the offset and current limit of the NB SMPS. The NB offset is always present regardless of PSI_L setting.

The I_{LX3MIN} minimum current-limit threshold in skip mode is precisely 25% of the corresponding positive current-limit threshold.

SMPS Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

  For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

  $$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{PH}}$$

  where η_{PH} is the total number of active phases.
- **Core Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

  When selecting a switching frequency, the minimum on-time at the highest input voltage and lowest output voltage must be greater than the 150ns (max) minimum on-time specification in the *Electrical Characteristics* table:

  $$V_{OUT(MIN)}/V_{IN(MAX)} \times t_{SW} > t_{ON(MIN)}$$

  A good rule is to choose a minimum on-time of at least 200ns.

  When in pulse-skipping operation (PSI_L = 0), the minimum on-time must take into consideration the time needed for proper skip-mode operation. The on-time for a skip pulse must be greater than the 170ns (max) minimum on-time specification in the *Electrical Characteristics* table:

  $$t_{ON(MIN)} \leq \frac{LV_{IDLE}}{R_{SENSE}\left(V_{IN(MAX)} - V_{OUT(MIN)}\right)}$$
- **Inductor Operating Point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Core SMPS Design Procedure

Core Inductor Selection

By design, the AMD mobile serial VID application should regard each of the MAX17480 SMPSs as independent, single-phase SMPSs. The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where $I_{LOAD(MAX)}$ is the maximum current per phase, and f_{SW} is the switching frequency per phase.

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. If using a swinging inductor (where the inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} f_{SW} L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{PH}}\right) + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

Core Peak Inductor Current Limit (ILIM12)

The MAX17480 overcurrent protection employs a peak current-sensing algorithm that uses either current-sense resistors or the inductor's DCR as the current-sense element (see the *Current Sense* section). Since the controller limits the peak inductor current, the maximum average load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and input-to-output voltage difference. When combined with the output undervoltage-protection circuit, the system is effectively protected against excessive overload conditions.

The peak current-limit threshold is set by the voltage difference between ILIM and REF using an external resistor-divider:

$$V_{CS(PK)} = V_{CSP\_} - V_{CSN\_} = 0.052 \text{ x } (V_{REF} - V_{ILIM12})$$

$$I_{LIMIT(PK)} = V_{CS(PK)}/R_{SENSE}$$

where R_{SENSE} is the resistance value of the current-sense element (inductors' DCR or current-sense resistor), and $I_{LIMIT(PK)}$ is the desired peak current limit (per phase). The peak current-limit threshold voltage adjustment range is from 10mV to 50mV.

Core Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements. In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$\left(R_{ESR} + R_{PCB}\right) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage (V_{RIPPLE}) by reducing the total inductor ripple current. For nonoverlapping, multiphase operation ($V_{IN} \ge V_{OUT}$), the maximum ESR to meet the output-ripple-voltage requirement is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{\left(V_{IN} - V_{OUT}\right) V_{OUT}}\right] V_{RIPPLE}$$

where f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

The capacitance value required is determined primarily by the output transient-response requirements. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step. Therefore, the amount of output soar when the load is removed is a function of the output voltage and inductor value. The minimum output capacitance required to prevent overshoot (V_{SOAR}) due to stored inductor energy can be calculated as:

$$C_{OUT} \ge \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2 V_{OUT} V_{SOAR}}$$

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

Core Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. For a dual 180° interleaved controller, the out-of-phase operation reduces the RMS input ripple current, effectively lowering the input capacitance requirements. When both outputs operate with a duty cycle less than 50% ($V_{IN} > 2V_{OUT}$), the RMS input ripple current is defined by the following equation:

$$I_{RMS} = \sqrt{\left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1}\left(I_{OUT1} - I_{IN}\right) + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}\left(I_{OUT2} - I_{IN}\right)}$$

where I_{IN} is the average input current:

$$I_{IN} = \left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1} + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}$$

In combined mode (GNDS1 = V_{DDIO} or GNDS2 = V_{DDIO}) with both phases active, the input RMS current simplifies to:

$$I_{RMS} = I_{OUT}\sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{2} - \frac{V_{OUT}}{V_{IN}}\right)}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX17480 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Core Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The controller uses a transconductance amplifier to set the transient AC and DC output-voltage droop (Figure 5). The FBAC and FBDC configuration adjusts the steady-state regulation voltage as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Core Transient Droop and Stability

The inductor current ripple sensed across the current-sense inputs (CSP_ - CSN_) generates a proportionate current out of the FBAC pin. This AC current flowing across the effective impedance at FBAC generates an AC ripple voltage. Actual stability, however, depends on the AC voltage at the FBDC pin, and not on the FBAC pin. Based on the configuration shown in Figure 5, the ripple voltage at the FBDC pin can only be less than, or equal to, the ripple at the FBAC pin.

With the requirement that $R_{FBDC} = R_{FBAC}$, and ($Z_{CFB}//R_{FB}$) < 10% of R_{FBAC}, then:

$$R_{FBAC} = R_{FBDC} \geq \frac{1}{C_{OUT} f_{SW} R_{SENSE\_} G_{m(FBAC)}}$$

where $G_{m(FBAC\_)}$ is typically 2mS as defined in the *Electrical Characteristics* table, $R_{SENSE\_}$ is the effective value of the current-sense element that is used to provide the (CSP_, CSN_) current-sense voltage, and f_{SW} is the selected switching frequency.

Based on the above requirement for R_{FBAC} and R_{FBDC}, and with the other requirement for R_{FBDC} defined in the *Core Steady-State Voltage Positioning (DC Droop)* section, R_{FBAC} and R_{FBDC} can be chosen. The resultant AC droop is:

$$R_{DROOP\_AC} \approx \frac{R_{FBDC} R_{FBAC} R_{SENSE}}{R_{FBAC} + R_{FBDC}} G_{m(FBAC)}$$

Capacitor C_{FB} is required when the R_{DROOP_DC} is less than R_{DROOP_AC}. Choose C_{FB} according to the following equation:

$$C_{FB} \times \left[R_{FB} / (R_{FBAC} + R_{FBDC})\right] = 3 \times t_{SW}$$

Core Steady-State Voltage Positioning

With R_{DROOP_AC} defined, the steady-state voltage-positioning slope, R_{DROOP_DC}, can only be less than, or at most equal to, R_{DROOP_AC}:

$$R_{DROOP\_DC} = \frac{R_{FBDC} R_{FBAC} R_{SENSE}}{R_{FBAC} + R_{FBDC} + R_{FB}} G_{m(FBAC)}$$

Choose the R_{FBDC} and R_{FBAC} already previously chosen, then select R_{FB} to give the desired droop.

DC droop is typically used together with the +12.5mV offset feature to keep within the DC tolerance window of the application. See the *Offset and Address Change for Core SMPSs (OPTION)* section.

Core Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high-load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur (see the *Core SMPS MOSFET Gate Drivers* section).

Core MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (N_H\ \text{Resistive}) = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{LOAD}{}^2 R_{DS(ON)}$$

where I_{LOAD} is the per-phase current.

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ \text{Switching}) = \left(V_{IN(MAX)}\right)^2 \left(\frac{C_{RSS} f_{SW}}{I_{GATE}}\right) I_{LOAD}$$

where C_{RSS} is the reverse transfer capacitance of N_H, I_{GATE} is the peak gate-drive source/sink current (1A, typ), and I_{LOAD} is the per-phase current.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the C x $V_{IN}{}^2$ x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_L\ \text{Resistive}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit can be "overdesigned" to tolerate:

$$I_{LOAD(MAX)} = I_{PEAK(MAX)} - \frac{\Delta I_{INDUCTOR}}{2} = I_{PEAK(MAX)} - \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{PEAK(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current per phase. This diode is optional and can be removed if efficiency is not critical.

Core Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one SMPS, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume two IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

NB SMPS Design Procedure

NB Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L_3 = \left(\frac{V_{IN3} - V_{OUT3}}{f_{SW3} I_{LOAD3(MAX)} LIR}\right)\left(\frac{V_{OUT3}}{V_{IN3}}\right)$$

where $I_{LOAD3(MAX)}$ is the maximum current and f_{SW3} is the switching frequency of the NB regulator.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. If using a swinging inductor (where the inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT3}(V_{IN3} - V_{OUT3})}{V_{IN3} f_{SW3} L_3}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK3}):

$$I_{PEAK3} = I_{LOAD3(MAX)} + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

NB Peak Inductor Current Limit (ILIM3)

The MAX17480 NB regulator overcurrent protection employs a peak current-sensing algorithm that uses the high-side MOSFET $R_{ON(NH3)}$ as the current-sense element. Since the controller limits the peak inductor current, the maximum average load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-limit setting, inductor value, switching frequency, and input-to-output voltage difference. When combined with the output undervoltage-protection circuit, the system is effectively protected against excessive overload conditions.

The peak current-limit threshold is set by the ILIM3 pin setting (see the *Offset and Current-Limit Setting for NB SMPS (ILIM3)* section).

NB Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements. In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

The output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. For single-phase operation, the maximum ESR to meet the output-ripple-voltage requirement is:

$$R_{ESR} \le \left[\frac{V_{IN3} f_{SW3} L_3}{(V_{IN3} - V_{OUT3}) V_{OUT3}}\right] V_{RIPPLE3}$$

where f_{SW3} is the switching frequency. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

The capacitance value required is determined primarily by the stability requirements. However, the soar and sag calculations are still provided here for reference. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step. Therefore, the amount of output soar and sag when the load is applied or removed is a function of the output voltage and inductor value. The soar and sag voltages are calculated as:

$$V_{SOAR3} = \frac{\left(\Delta I_{LOAD3(MAX)}\right)^2 L_3}{2V_{OUT3}C_{OUT3}}$$

$$V_{SAG3} = \frac{\left(\Delta I_{LOAD3(MAX)}\right)^2 L_3}{2C_{OUT3}\left(V_{IN3} \times D_{MAX} - V_{OUT3}\right)} + \frac{\Delta I_{LOAD3(MAX)}\left(t_{SW3} - \Delta t\right)}{C_{OUT3}}$$

where D_{MAX} is the maximum duty cycle of the NB SMPS as listed in the *Electrical Characteristics* table, t_{SW3} is the NB switching period programmed by the OSC pin, and Δt equals $V_{OUT}/V_{IN} \times t_{SW}$ when in forced-PWM mode, or $L \times I_{LX3MIN}/(V_{IN} - V_{OUT})$ when in pulse-skipping mode.

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

NB Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD3}}{V_{IN3}}\right)\sqrt{V_{OUT3}\left(V_{IN3} - V_{OUT3}\right)}$$

The worst-case RMS current requirement occurs when operating with $V_{IN3} = 2V_{OUT3}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD3}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. The MAX17480 NB regulator is operated as the second stage of a two-stage power-conversion system. Tantalum input capacitors are acceptable. Choose an input capacitor that exhibits less than 10°C temperature rise at the RMS input current for optimal circuit longevity.

NB Steady-State Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. For NB, the load line is generated by sensing the inductor current through the high-side MOSFET on-resistance ($R_{ON(NH3)}$), and is internally preset to -5.5mV/A (typ). This guarantees the output voltage to stay in the static regulation window over the maximum load conditions per AMD specifications. See Table 6 for full-load voltage droop according to different ILIM3 settings.

NB Transient Droop and Stability

The voltage-positioned load-line of the NB SMPS also provides the AC ripple voltage required for stability. To maintain stability, the output capacitive ripple must be kept smaller than the internal AC ripple voltage. Hence, a minimum NB output capacitance is required as calculated below:

$$C_{OUT3} > \frac{1}{2 \times f_{SW3} \times R_{DROOP3(MIN)}}\left(1 + \frac{V_{OUT3}}{V_{IN3}}\right)$$

where $R_{DROOP3(MIN)}$ is 4mV/A as defined in the *Electrical Characteristics* table, and f_{SW3} is the NB switching frequency programmed by the OSC pin.

SVI Applications Information

I²C Bus-Compatible Interface

The MAX17480 is a receive-only device. The 2-wire serial bus (pins SVC and SVD) is designed to attach on a low-voltage I²C-like bus. In the AMD mobile application, the CPU directly drives the bus at a speed of 3.4MHz. The CPU has a push-pull output driving to the V_{DDIO} voltage level. External pullup resistors are not required.

When not used in the specific AMD application, the serial interface can be driven to as high as 2.5V, and can operate at the lower speeds (100kHz, 400kHz, or 1.7MHz). At lower clock speeds, external pullup resistors can be used for open-drain outputs. Connect both SVC and SVD lines to V_{DDIO} through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time, and should be less than 10% of the clock period. C_{BUS} is the total capacitance on the bus.

The MAX17480 is compatible with the standard SVI interface protocol as defined in the following subsections. Figure 12 shows the SVI bus START, STOP, and data change conditions.

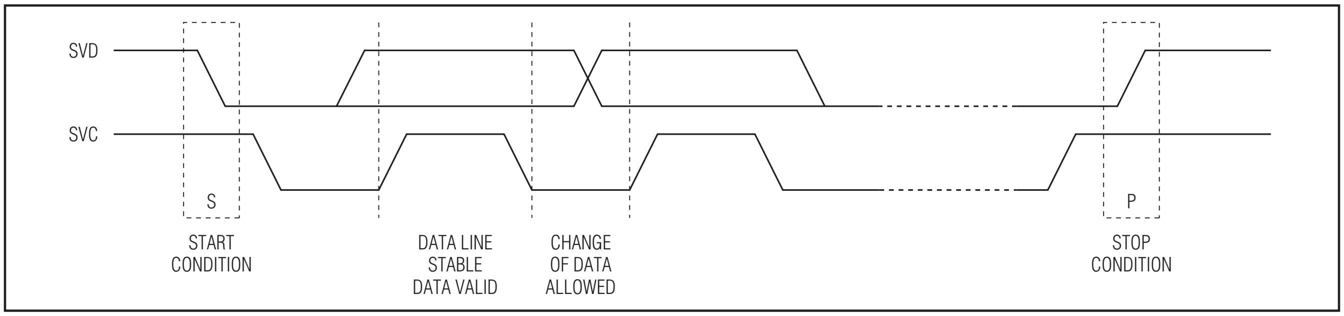


Figure 12. SVI Bus START, STOP, and Data Change Conditions

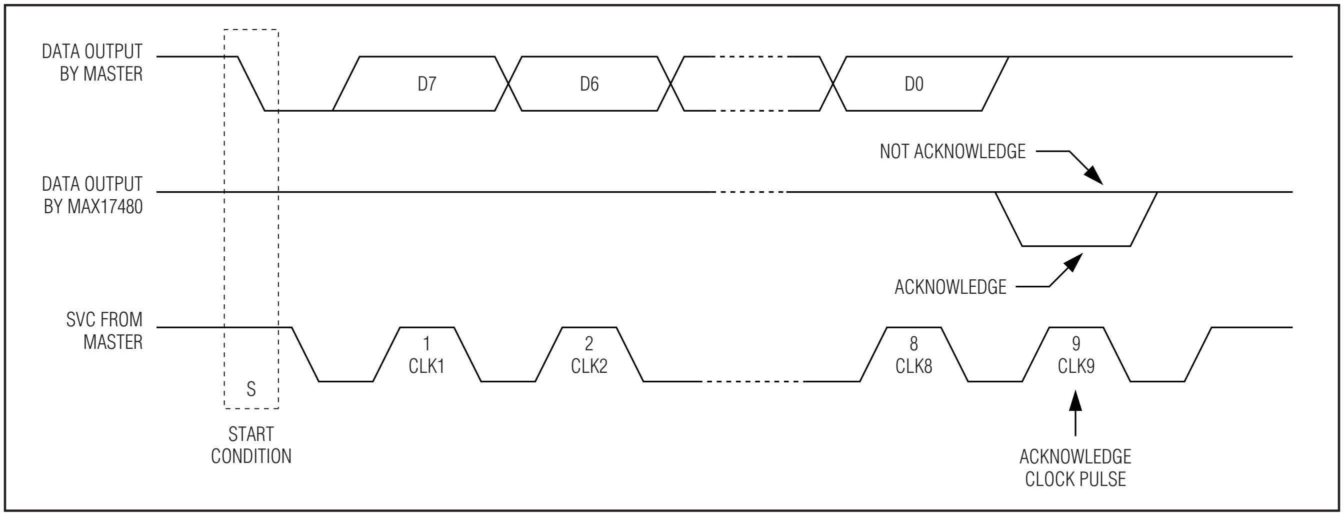


Figure 13. SVI Bus Acknowledge

Bus Not Busy

The SVI bus is not busy when both data and clock lines remain high. Data transfers can be initiated only when the bus is not busy. Figure 13 shows the SVI bus acknowledge.

Start Data Transfer (S)

Starting from an idle bus state (both SVC and SVD are high), a high-to-low transition of the data (SVD) line while the clock (SVC) is high determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (P)

A low-to-high transition of the SDA line while the clock (SVC) is high determines a STOP condition. All operations must be ended with a STOP condition.

Slave Address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (110xxxx) for the MAX17480. Since the MAX17480 is a write-only device, the eighth bit of the slave address is 0. The MAX17480 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

SVD Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. The device that acknowledges has to pull down the SVD line during the acknowledge clock pulse so that the SVD line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. See Figure 13.

Command Byte

A complete command consists of a START condition (S) followed by the MAX17480's slave address and a data phase, followed by a STOP condition (P). For the slave address, bits 6:4 are always 110 and bit 3 is X (don't care). The WR bit should always be 1 since read functions are not supported. Figure 14 is the SVI bus data-transfer summary. Table 7 is a description of the SVI send byte address and Table 8 describes serial VID 8-bit field encoding.

SMPS Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by stability requirements, not the minimum off-time ($t_{OFF(MIN)}$). The MAX17480 does not include slope compensation, so the controller becomes unstable with duty cycles greater than 50% per phase:

$$V_{IN(MIN)} \geq 2V_{OUT(MAX)}$$

However, the controller can briefly operate with duty cycles over 50% during heavy load transients.

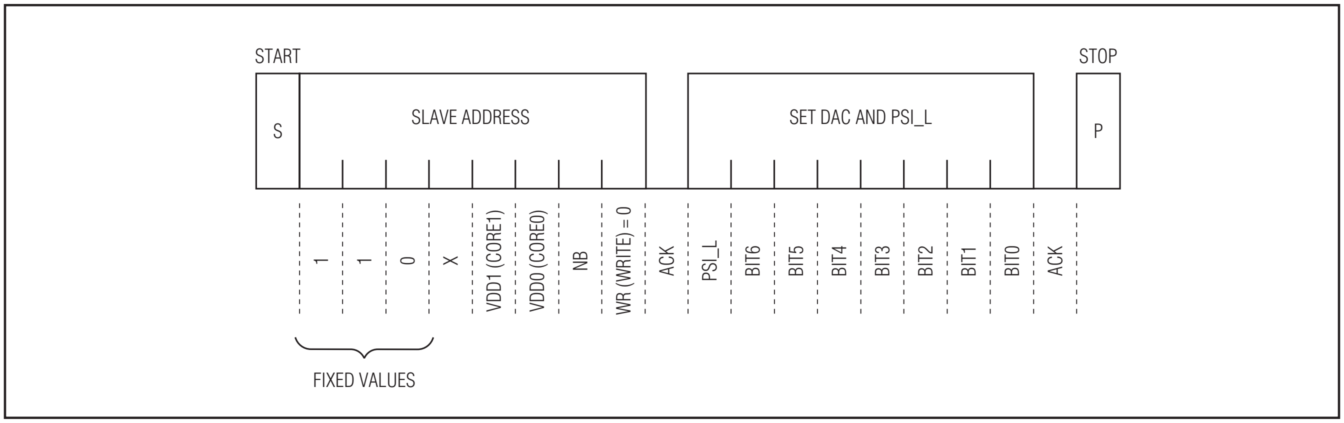


Figure 14. SVI Bus Data Transfer Summary

Table 7. SVI Send Byte Address Description

BIT	DESCRIPTION
6:4	Always 110b.
3	X—don't care.
2	VDD1, if set then the following data byte contains the VID for VDD1. Bit 2 is ignored in combined mode (GNDS1 or GNDS2 = V_{DDIO}). VDD1 refers to CORE1 of the AMD CPU.
1	VDD0, if set then the following data byte contains the VID for VDD0 in separate mode, and the unified VDD in combined mode. VDD0 refers to CORE0 of the AMD CPU.
0	VDDNB, if set then the following data byte contains the VID for VDDNB.

Table 8. Serial VID 8-Bit Field Encoding

BIT	DESCRIPTION
7	PSI_L: Power-Save Indicator 0 means the processor is at an optimal load and the SMPS(s) can enter power-saving mode. The SMPS operates in pulse-skipping mode after exiting the boot mode. Offset is disabled if previously enabled by the OPTION pin. The MAX17480 enters 1-phase operation if in combined mode (GNDS1 or GNDS2 = H). 1 means the processor is in a high current-consumption state. The SMPS operates in forced-PWM mode after exiting the boot mode. Offset is enabled if previously enabled by the OPTION pin. The MAX17480 returns to 2-phase operation if in combined mode (GNDS1 or GNDS2 = H).
6:0	SVID[6:0] as defined in Table 7.

Maximum Input Voltage

The MAX17480 controller has a minimum on-time, which determines the maximum input operating voltage that maintains the selected switching frequency. With higher input voltages, each pulse delivers more energy than the output is sourcing to the load. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, resulting in pulse-skipping operation regardless of the operating mode selected by PSI_L. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{SW} t_{ON(MIN)}}\right)$$

where f_{SW} is the per-phase switching frequency set by the OSC resistor, and $t_{ON(MIN)}$ is 150ns (max) minus the driver's turn-on delay (DL low to DH high). For the best high-voltage performance, use the slowest switching frequency setting (100kHz per phase, R_{OSC} = 432kΩ).

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 15). If possible, mount all the power components on the top side of the board with their ground terminals flush against one another, and mount the controller and analog components on the bottom layer so the internal ground layers shield the analog components from any noise generated by the power components. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane; then connect the analog ground to the GND pins of the controller. The following sensitive components connect to analog ground: V_{CC} and V_{DDIO} bypass capacitors, remote sense and GNDS bypass capacitors, and the resistive connections (ILIM12, OSC, TIME).
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Connections for current limiting (CSP, CSN) and voltage positioning (FBS, GNDS) must be made using Kelvin-sense connections to guarantee the current-sense accuracy. Place current-sense filter capacitors and voltage-positioning filter capacitors as close as possible to the IC.
- Route high-speed switching nodes and driver traces away from sensitive analog areas (REF, V_{CC}, FBAC, FBDC, OUT3, etc.). Make all pin-strap control input connections ($\overline{SHDN}$, PGD_IN, OPTION) to analog ground or V_{CC} rather than power ground or V_{DD}.
- Route the high-speed serial-interface signals (SVC, SVD) in parallel, keeping the trace lengths identical. Keep the SVC and SVD away from the high-current switching paths.
- Keep the drivers close to the MOSFET, with the gate-drive traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET rather than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and DL anode). If possible, make all these connections on the top layer with wide, copper-filled areas. For the NB SMPS, place CIN3 and L3 as near as possible to the MAX17480, using multiple vias to reduce inductance when connecting the different layers.
2) Use multiple vias to connect the exposed backside to the power ground plane (PGND) to allow for a low-impedance path for the SMPS3 internal low-side MOSFET.
3) Mount the MAX17480 close to the low-side MOSFETs. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the driver IC).
4) Group the gate-drive components (BST capacitors, V_{DD} bypass capacitor) together near the MAX17480.

5) Make the DC-DC controller ground connections as shown in the standard application circuit (Figure 2). This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND, V_{DD} bypass capacitor, and driver IC ground connection go; and the controller's analog ground plane, where sensitive analog components, the MAX17480's AGND pin, and V_{CC} bypass capacitor go. The controller's analog ground plane (AGND) must meet the power ground plane (PGND) only at a single point directly beneath the IC. The power ground plane should connect to the high-power output ground with a short, thick metal trace from PGND to the source of the low-side MOSFETs (the middle of the star ground).

6) Connect the output power planes (V_{CORE}, V_{OUT3}, and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

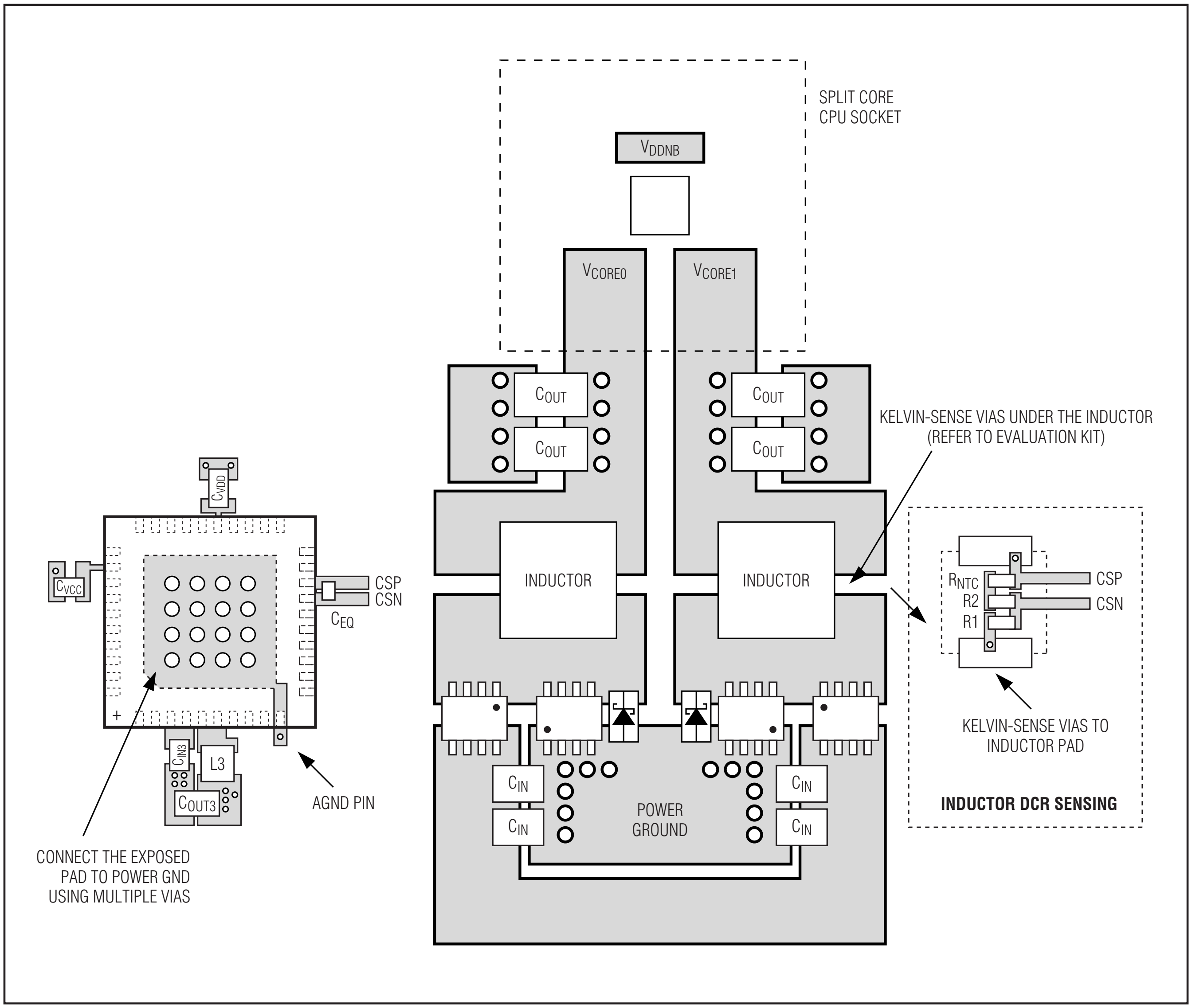


Figure 15. PCB Layout Example