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4.2V to 36V, 1A Current Limiter with OV, UV, Reverse Voltage Protection

MAX17523/MAX17523A

General Description

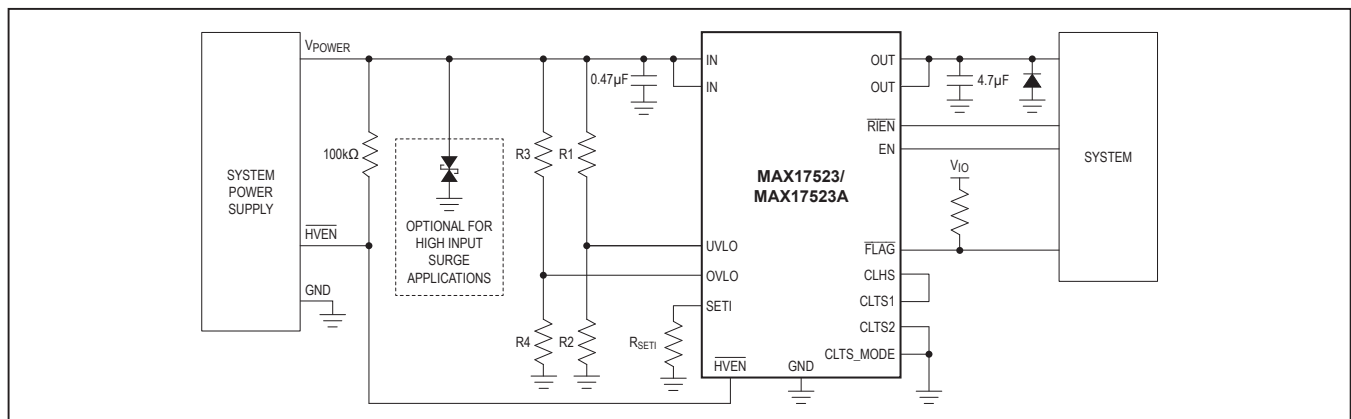
The Olympus series of ICs are the industry's smallest and robust integrated system protection solutions. The MAX17523/MAX17523A adjustable overvoltage and overcurrent protection devices are ideal for protecting systems against positive and negative input voltage faults up to $\pm 40\text{V}$, and feature low $190\text{m}\Omega$ (typ) R_{ON} integrated FETs.

The adjustable overvoltage range in MAX17523 is between 6V and 36V, while the adjustable undervoltage range is between 4.4V and 24V. The adjustable overvoltage range in MAX17523A is between 6V and 36V, while the adjustable undervoltage range is between 4.2V and 24V. The overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds are set using optional external resistors. The factory preset internal OVLO threshold is 33V (typ), and the preset internal UVLO threshold is 19V (typ).

The MAX17523/MAX17523A also feature programmable current-limit protection up to 1A. The devices can be set for autoretry, latch-off, or continuous fault response when an overcurrent event occurs. Once current reaches the threshold, the MAX17523/MAX17523A turn off after 21ms (typ) blanking time, and stay off during the retry period when set to autoretry mode. The devices latch off after the blanking time when set to latch-off mode. The devices limit the current continuously when set to continuous mode. The MAX17523/MAX17523A also feature reverse current and thermal shutdown protection.

The MAX17523 and MAX17523A are available in a small, 16-pin (3mm x 3mm) TQFN package. The MAX17523/MAX17523A operate over the -40°C to $+125^{\circ}\text{C}$ extended temperature range.

Typical Application Circuit



19-8450; Rev 5; 2/22

Benefits and Features

- Industrial Power Protection Increases Robustness
 - Wide Input Supply Range: +4.5V to +36V (MAX17523), +4.2V to +36V (MAX17523A)
 - Negative Input Tolerance to -36V
 - Low R_{ON} 190m Ω (typ)
 - Reverse Current Flow Control Input
 - Thermal Overload Protection
 - Extended -40°C to $+125^{\circ}\text{C}$ Temperature Range
- Flexible Design Options Eases Designs
 - Adjustable OVLO and UVLO Thresholds
 - Programmable Forward-Current Limit: 0.15A to 1A
 - Programmable Overcurrent Fault Response: Autoretry, Latch-Off, and Continuous
 - Dual Enable Inputs: EN and High Voltage $\overline{\text{HVEN}}$
- Saves Space
 - 16-Pin, 3mm x 3mm, TQFN Package

Applications

- Sensor Systems
- Condition Monitoring
- Factory Sensors
- Process Analytics
- Process Instrumentation
- Weighing and Batching Systems

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

(All voltages referenced to GND.)

IN to GND.....	-40V to +40V
IN to OUT.....	-40V to +40V
OUT.....	-0.3V to +40V
HVEN.....	-40V to +40V
OVLO, UVLO, FLAG, EN, RIEN, CLTS1, CLTS2, CLTS_MODE.....	-0.3V to +6V
SET1.....	-0.3V to min(V _{IN} , 1.22V)+0.3V
CLHS.....	-0.3V to min(V _{IN} , 5V)+0.3V

I _{IN} (DC Operating)(Note 1).....	1.1A
Continuous Power Dissipation (T _A = +70°C) TQFN (derate 20.8mW/°C above +70°C).....	1667mW
Operating Temperature Range.....	-40°C to +125°C
Maximum Junction Temperature (Note 2).....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (soldering, 10s).....	+300°C
Soldering Temperature (reflow).....	+260°C

- Note 1:** DC current is also limited by the thermal design of the system.
Note 2: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN

Package Code	T1633+5C
Outline Number	21-0136
Land Pattern Number	90-0032
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ _{JA})	48°C/W
Junction to Case (θ _{JC})	10°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN} = 4.2V$ to $36V$ (MAX17523A), $V_{IN} = 4.5V$ to $36V$ (MAX17523), $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{IN} = 24V$, $R_{SET1} = 12k\Omega$, $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage	V_{IN}	(MAX17523A)	4.2		36	V
		(MAX17523)	4.5		36	
Shutdown IN Current	I_{SHDN}	$V_{EN} = 0V, V_{HVEN} = 5V$		6.6	16	μA
Shutdown OUT Current	I_{OFF}	$V_{EN} = 0V, V_{HVEN} = 5V, V_{OUT} = 0V$		0.1	2	μA
Reverse IN Current	I_{IN_RVS}	$V_{IN} = -40V, V_{OUT} = V_{GND} = 0V$	-10			μA
Supply Current	I_{IN}	$V_{IN} = 15V, V_{HVEN} = 0V$		530	800	μA
Internal Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	32	33	34.3	V
		V_{IN} falling	30.3	32	33.7	
Internal Undervoltage Trip Level	V_{UVLO}	V_{IN} falling	17.5	18.5	19.5	V
		V_{IN} rising	18.2	19.2	20.2	
External OVLO Adjustment Range		(Note 4)	6		36	V
External OVLO Select Threshold Voltage	V_{SEL_OVLO}		0.3	0.4	0.5	V
External OVLO Leakage	I_{OVLO_LEAK}	$V_{OVLO} < 1.2V$	-100		+100	nA
External UVLO Adjustment Range		(Note 4) (MAX17523A only)	4.2		24	V
		(Note 4) (MAX17523 only)	4.4		24	
External UVLO Select Threshold Voltage	V_{SEL_UVLO}		0.3	0.4	0.5	V
External UVLO Leakage	I_{UVLO_LEAK}	$V_{UVLO} < 1.2V$	-100		+100	nA
External UVLO Threshold Levels	V_{UVLO_R}	V_{UVLO} rising	1.216	1.256	1.296	V
	V_{UVLO_F}	V_{UVLO} falling	1.197	1.222	1.247	
External OVLO Threshold Levels	V_{OVLO_R}	V_{OVLO} rising	1.197	1.222	1.247	V
	V_{OVLO_F}	V_{OVLO} falling	1.151	1.192	1.233	
CLHS Voltage	V_{CLHS}	Source $100\mu A$	2.0	3.5		V
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	$I_{LOAD} = 100mA, V_{IN} \geq 8V$		190	370	m Ω
Current-Limit Adjustment Range	I_{LIM}	(Note 5)	0.15		1.0	A
Current-Limit Accuracy		$0.15A \leq I_{LIM} < 0.3A$	-20		+20	%
		$0.3A \leq I_{LIM} < 1.0A$	-10		+10	
\overline{FLAG} Assertion Drop Voltage Threshold	V_{FA}	Increase ($V_{IN} - V_{OUT}$) drop until \overline{FLAG} asserts, $V_{IN} = 24V$	400	600	800	mV
\overline{FLAG} Output Logic-Low Voltage		$I_{SINK} = 1mA$			0.4	V
\overline{FLAG} Output Leakage Current		$V_{IN} = V_{\overline{FLAG}} = 5V, \overline{FLAG}$ deasserted			2	μA
Reverse Current-Blocking Threshold	V_{RIB}	$V_{OUT} - V_{IN}$		40	80	mV

Electrical Characteristics (continued)

(V_{IN} = 4.2V to 36V (MAX17523A), V_{IN} = 4.5V to 36V (MAX17523), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, R_{SETI} = 12kΩ, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse-Current-Blocking Response Time	t _{RIB}	(Note 6)		0.6	1.0	μs
Reverse-Blocking Supply Current into OUT pin	I _{RBL}	V _{OUT} - V _{IN} > 1V		1.3	3.0	mA
LOGIC INPUTS						
HVEN Threshold Voltage	V _{HVENTH}		1	2	3.5	V
HVEN Threshold Hysteresis				2		%
HVEN Input Current	I _{HVEN_}	V _{HVEN} = 36V		26	41	μA
HVEN Input Reverse Current	I _{HVEN_R}	V _{IN} = V _{HVEN} = -36V	-43	-28		μA
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Logic-High	V _{IH}		1.4			V
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Logic- Low	V _{IL}				0.4	V
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Leakage Current	I _{LEAK}	V _{LOGIC} = 5V	-1		+1	μA
TIMING CHARACTERISTICS						
Switch Turn-On Time	t _{ON}	From OFF to ON (see Table 2), R _{LOAD} = 240Ω, C _{OUT} = 470μF		500		μs
Switch Turn-Off Time	t _{OFF}	From ON to I _{OUT} falling below 10%, R _{LOAD} = 47Ω		35		μs
Overvoltage Switch Turn-Off Time	t _{OFF_OVP}	From (V _{IN} > V _{OVLO}) to (V _{OUT} = 80% of V _{IN_OVLO}), R _{LOAD} = 47Ω		3		μs
Overcurrent Switch Turn-Off Time	t _{OFF_OCP}	After t _{BLANK}		3		μs
IN Debounce Time	t _{DEB}	From (V _{IN_UVLO} < V _{IN} < V _{IN_OVLO}) and (EN = high or HVEN = low) to V _{OUT} = 10% of V _{IN}	14	16.5	19	ms
Blanking Time	t _{BLANK}		17.8	21	24.1	ms
Autoretry Time	t _{RETRY}	After blanking time from I _{OUT} > I _{LIM} to FLAG deasserted (Note 7)	527	620	713	ms
THERMAL PROTECTION						
Thermal Shutdown	T _J			150		°C
Thermal Shutdown Hysteresis	T _{J(HYS)}			30		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design; not production tested.

Note 4: User settable. See the [Overvoltage Lockout \(OVLO\)](#) and [Undervoltage Lockout \(UVLO\)](#) sections for instructions.

Note 5: The current limit can be set below 150mA with a decreased accuracy.

Note 6: Guaranteed by design; not production tested.

Note 7: The ratio between autoretry time and blanking time is fixed and equal to 29.5.

Timing Diagrams

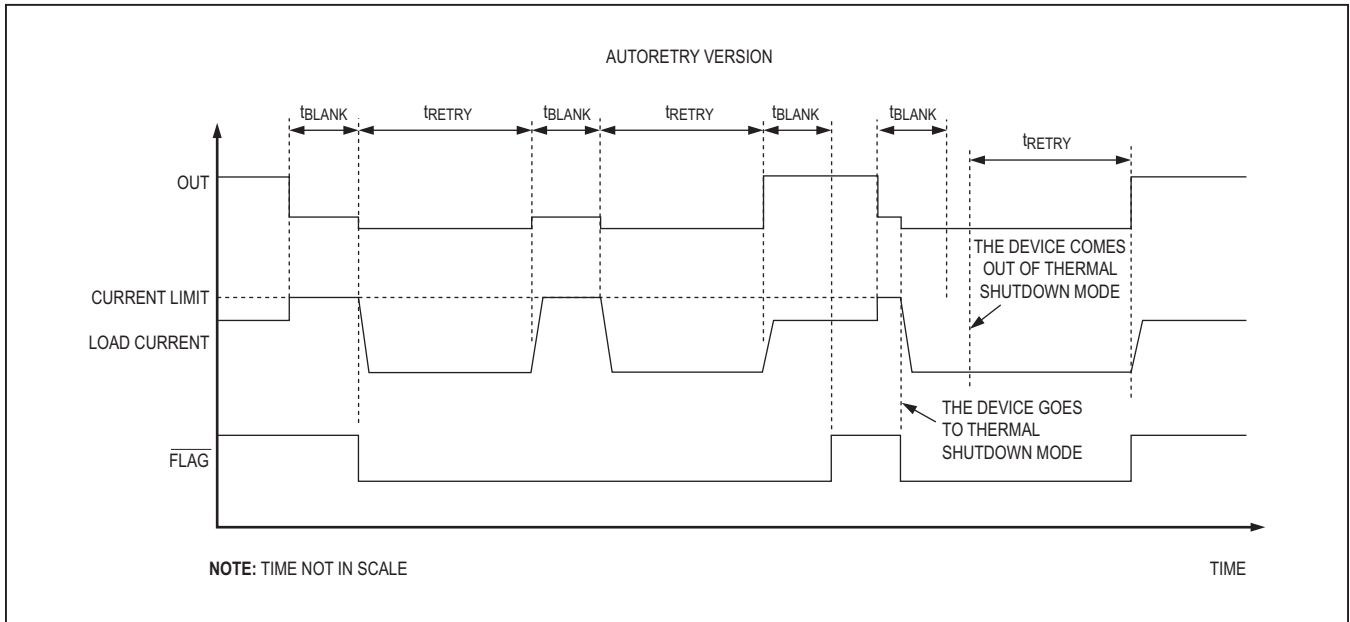


Figure 1. Autoretry Fault Diagram

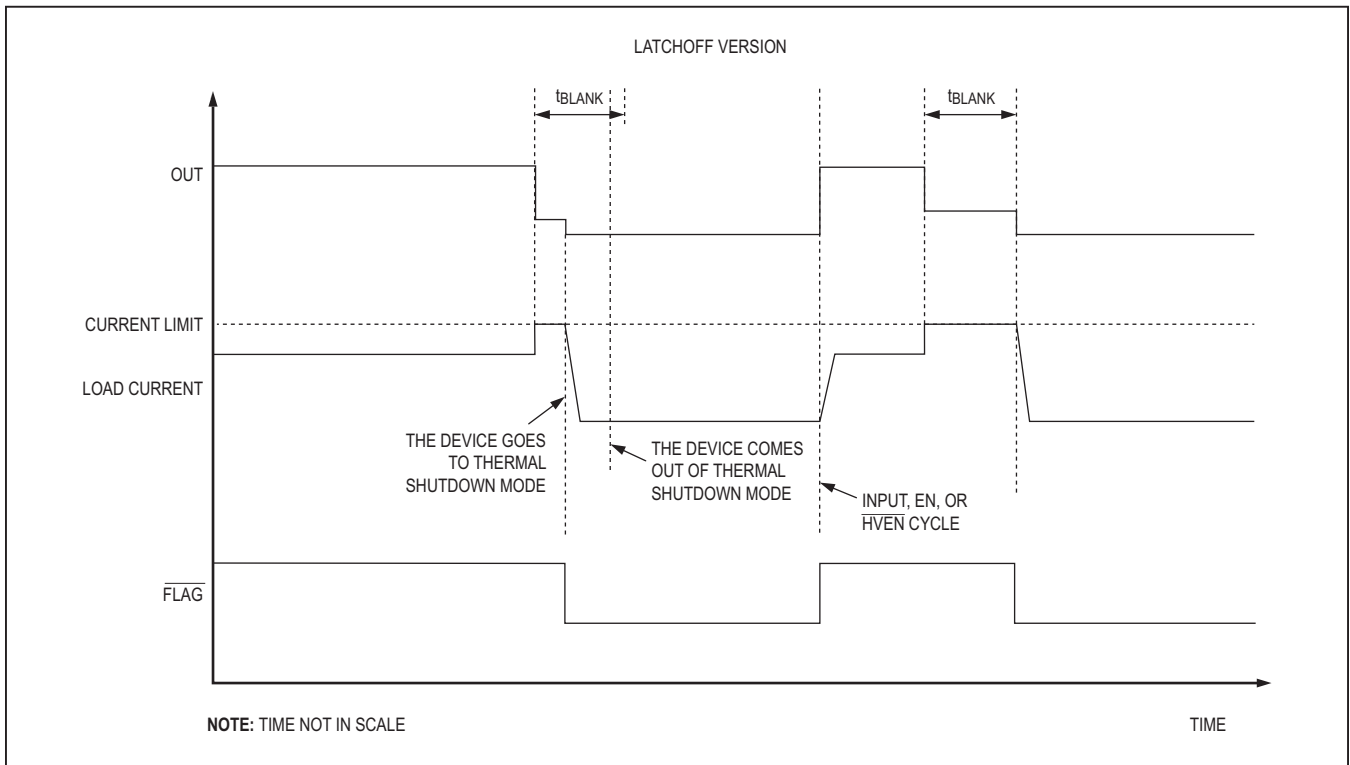


Figure 2. Latchoff Fault Diagram

Timing Diagrams (continued)

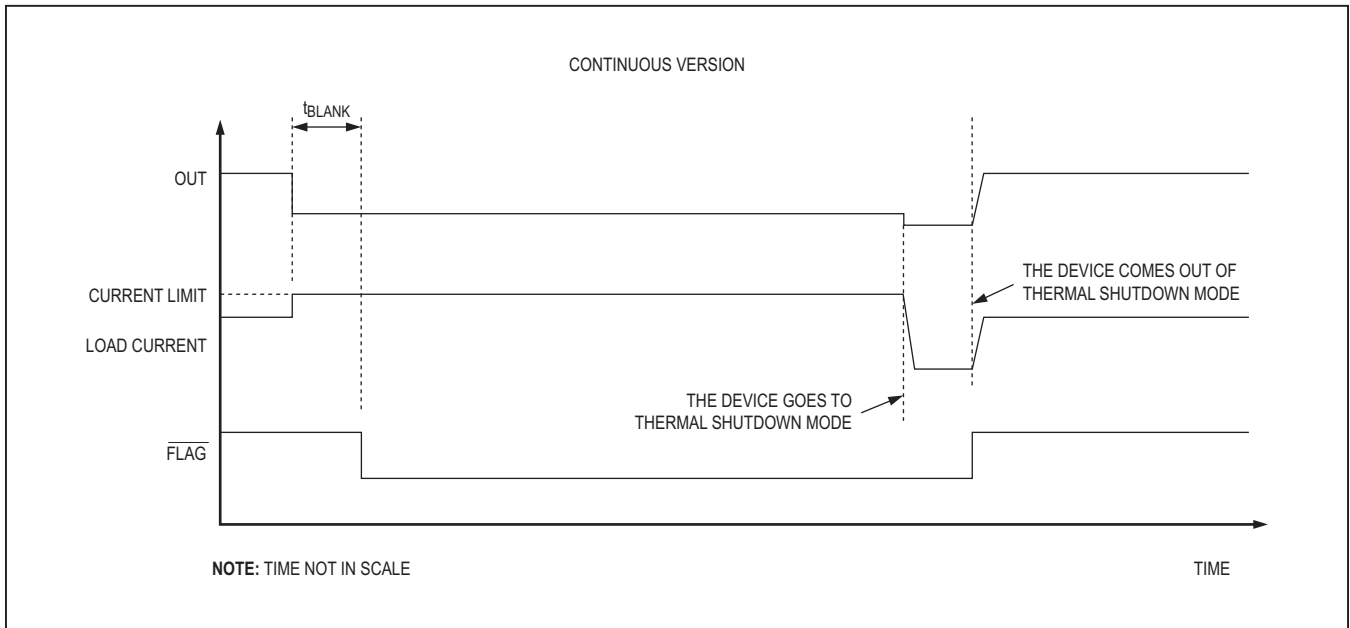


Figure 3. Continuous Fault Diagram

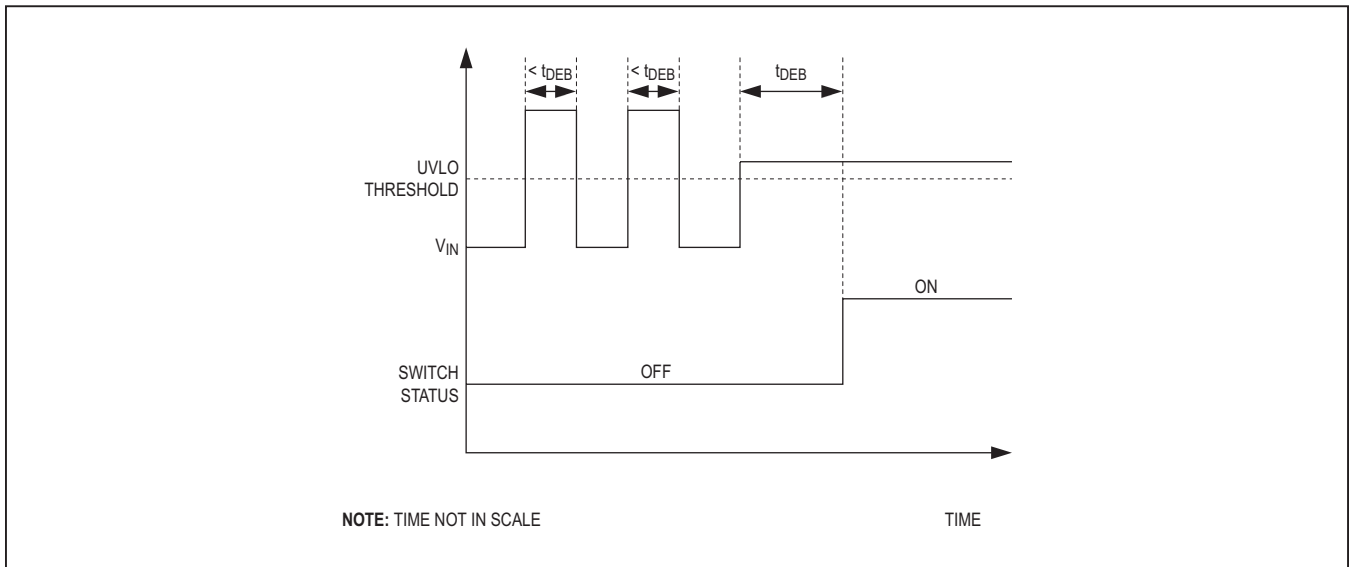
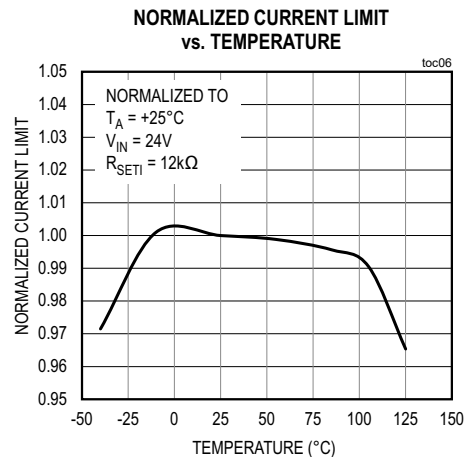
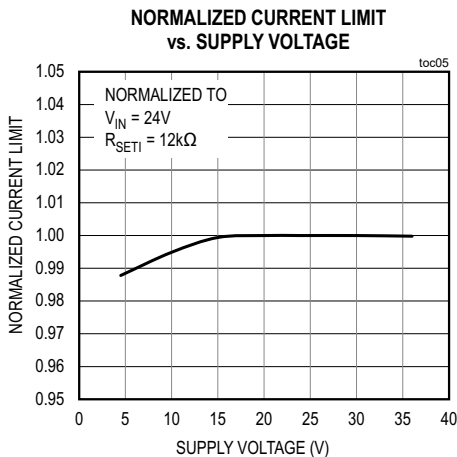
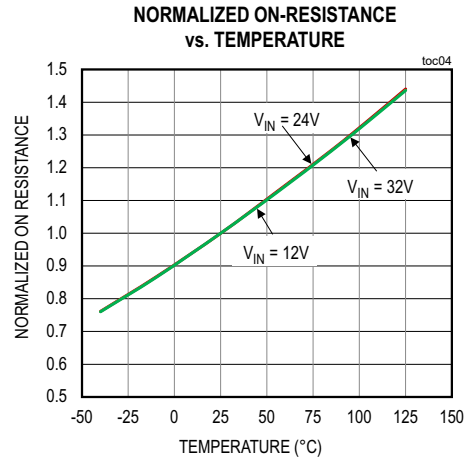
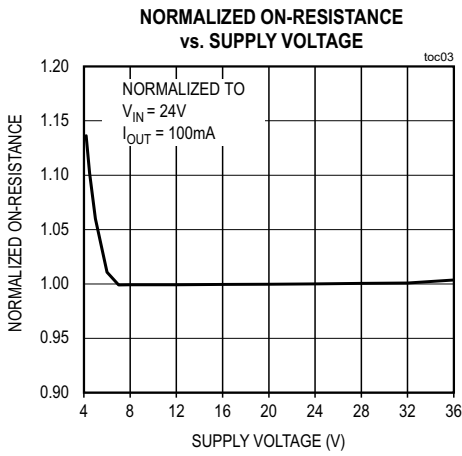
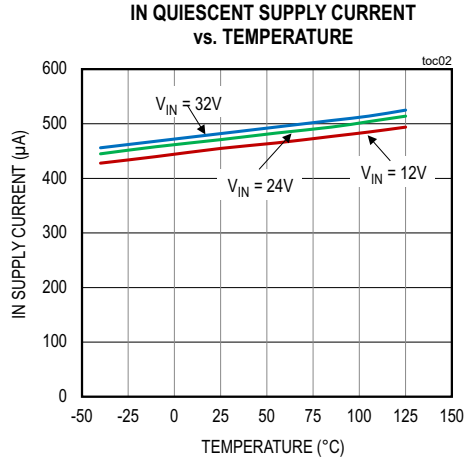
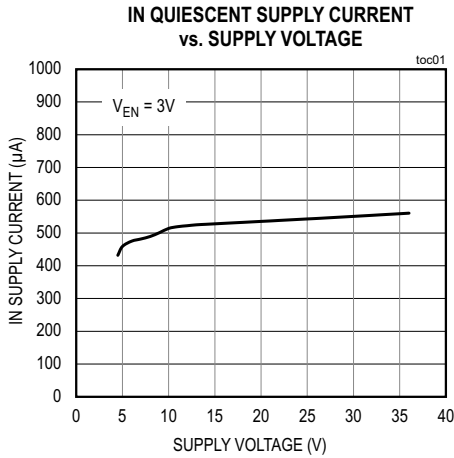


Figure 4. Debounce Timing

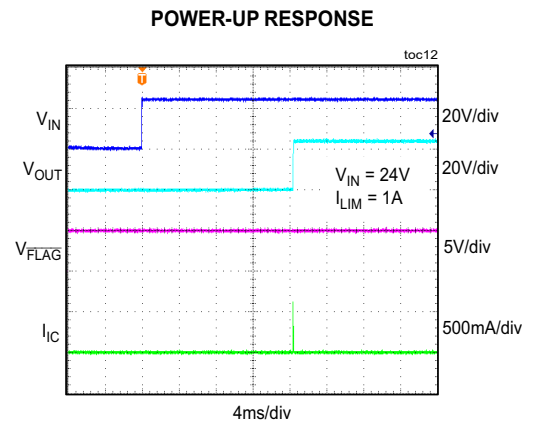
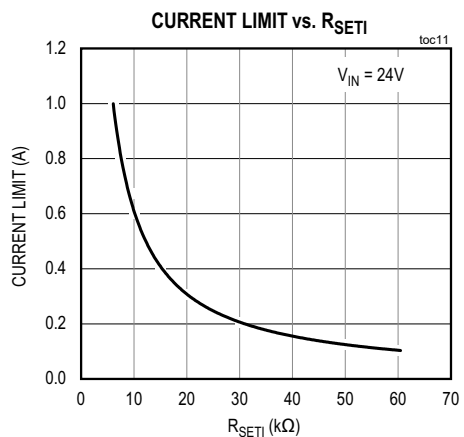
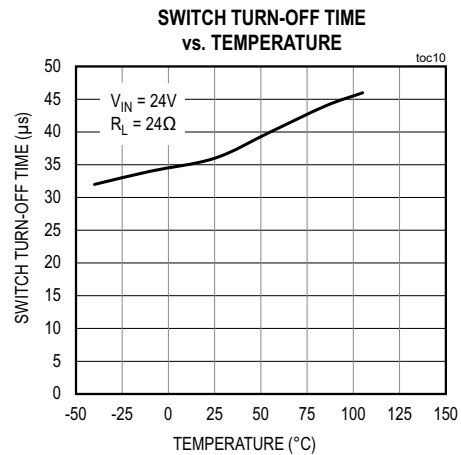
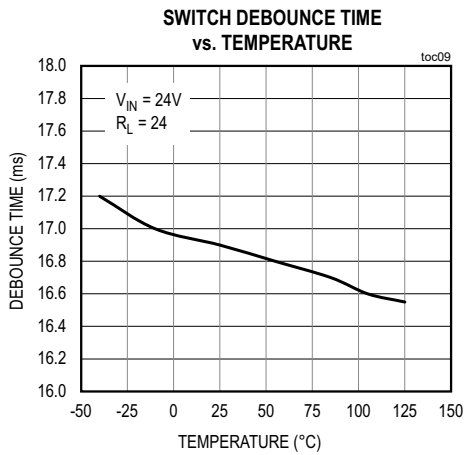
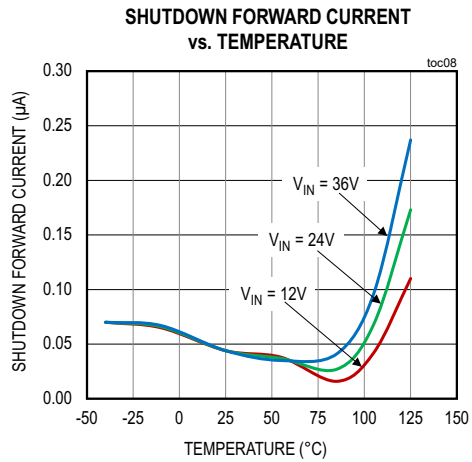
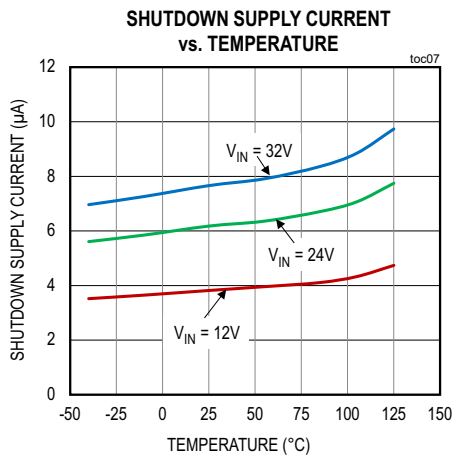
Typical Operating Characteristics

($C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



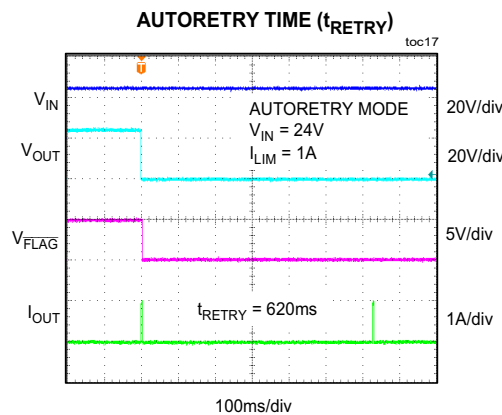
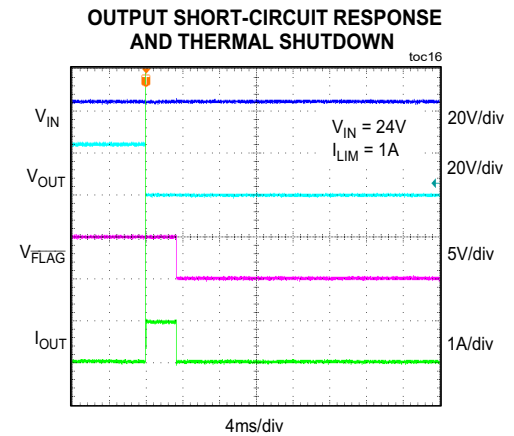
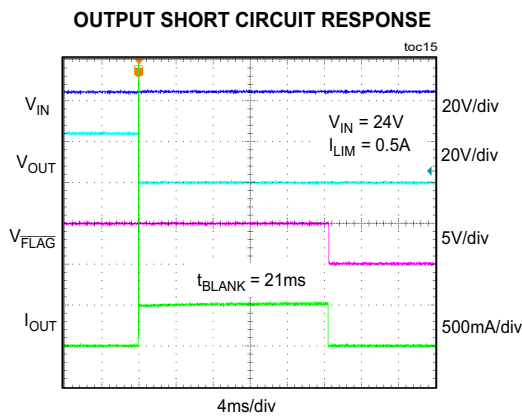
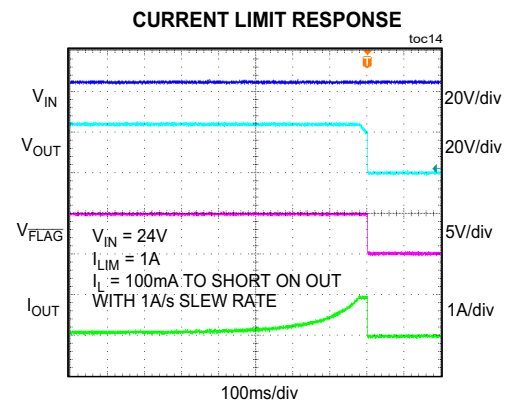
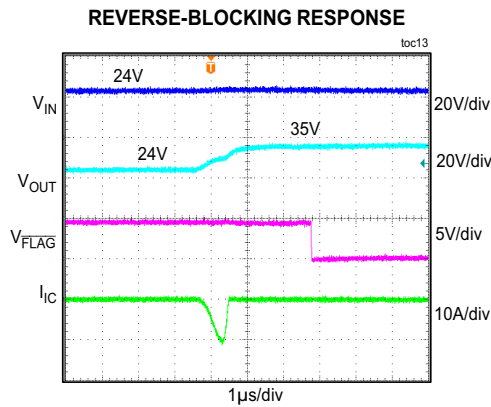
Typical Operating Characteristics (continued)

($C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

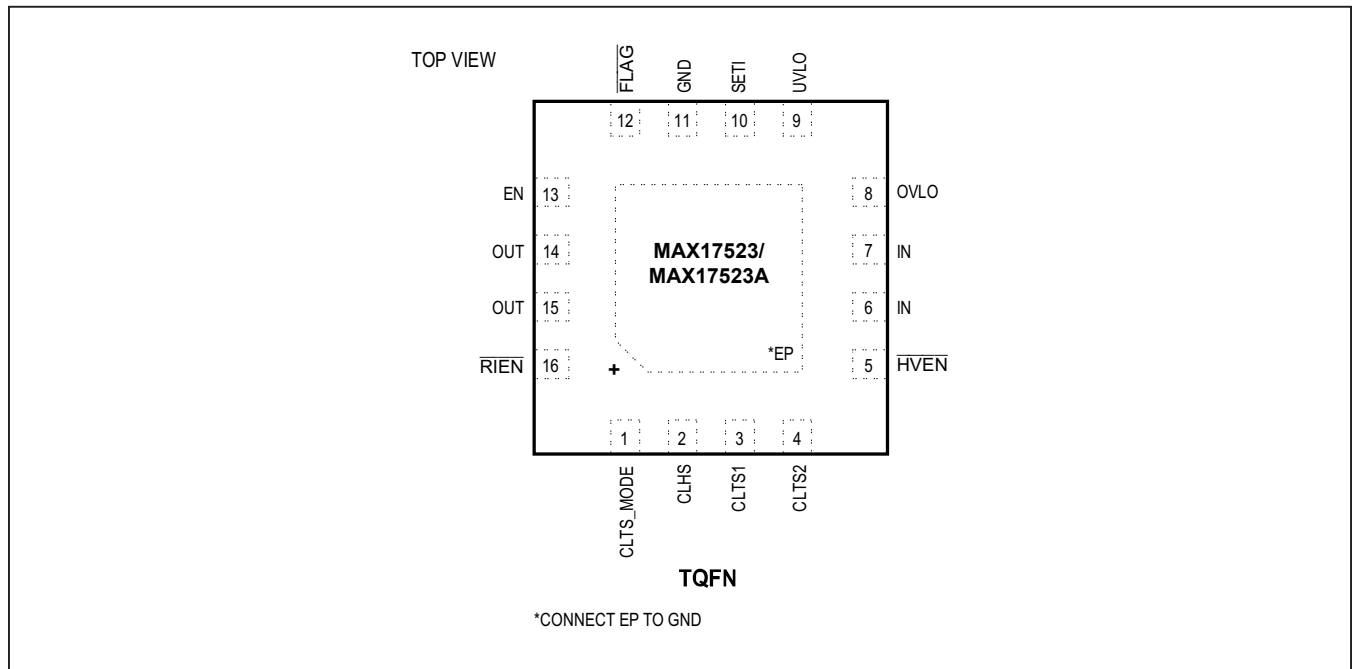


Typical Operating Characteristics (continued)

($C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configuration



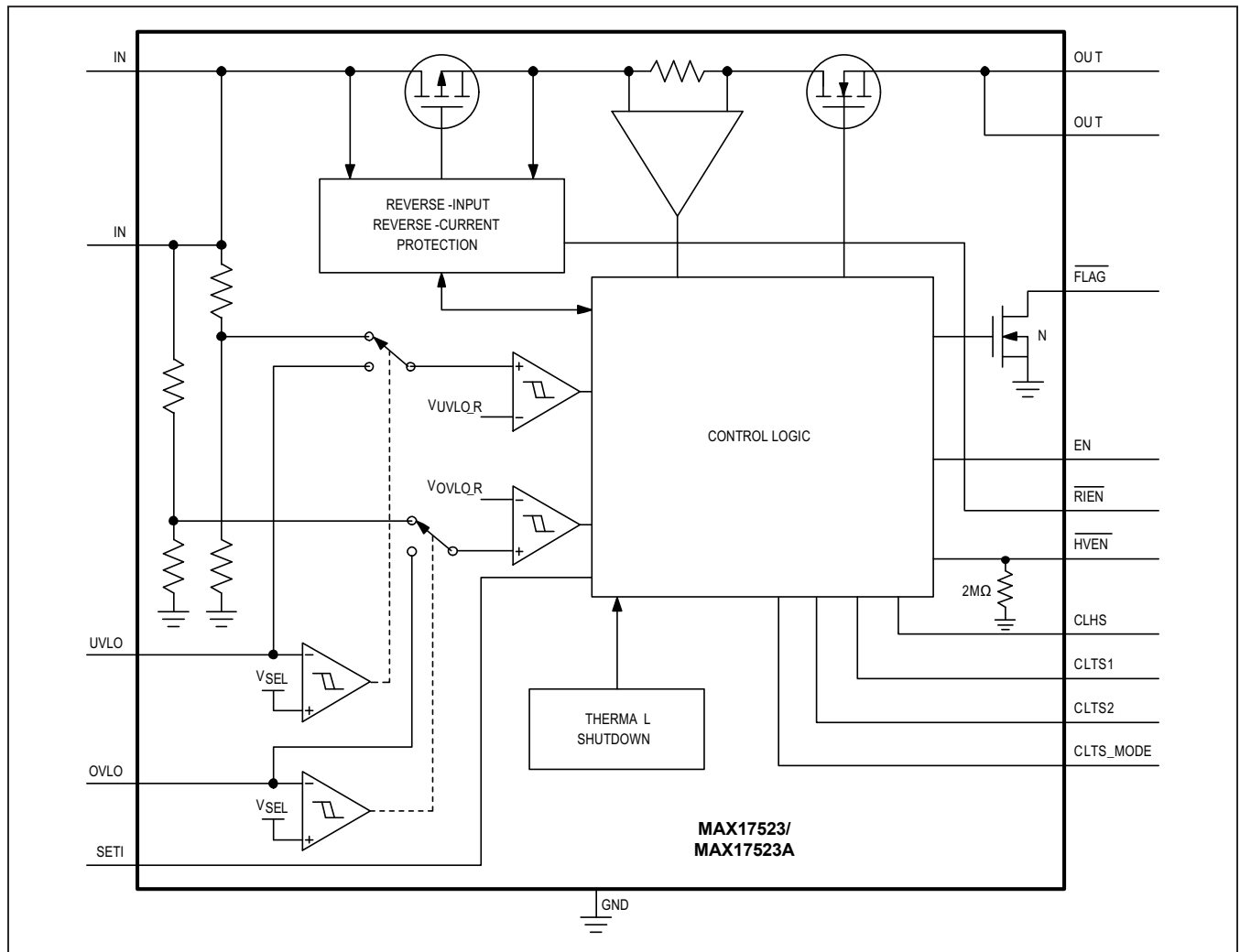
Pin Description

PIN	NAME	FUNCTION
1	CLTS_MODE	Current-Limit-Type Select Mode. CLTS_MODE = 0: CLTS1 and CLTS2 are sampled only when $(V_{IN} - V_{OUT}) < 0.6V$. CLTS_MODE = 1: CLTS1 and CLTS2 are continuously sampled.
2	CLHS	Current-Limit-Type-Select Logic-High Voltage. Connect CLTS_MODE/CLTS1/CLTS2 to CLHS for logic-high.
3	CLTS1	Current-Limit-Type Select 1. See Table 1.
4	CLTS2	Current-Limit-Type Select 2. See Table 1.
5	\overline{HVEN}	36V Capable Active-Low Enable Input. See Table 2.
6, 7	IN	Input Pins. Bypass IN to ground with a 0.47 μ F ceramic capacitor.
8	OVLO	Externally Programmable Overvoltage Lockout Threshold. Connect OVLO to GND to use the default internal OVLO threshold. Connect OVLO to an external resistor-divider to define a threshold externally and override the preset internal OVLO threshold.
9	UVLO	Externally Programmable Undervoltage Lockout Threshold. Connect UVLO to GND to use the default internal UVLO threshold. Connect UVLO to an external resistor-divider to define a threshold externally and override the preset internal UVLO threshold.
10	SETI	Overload-Current-Limit Adjust. Connect a resistor from SETI to GND to program the overcurrent limit. SETI must be connected to a resistor. If SETI is connected to GND, the FETs turn off and \overline{FLAG} is asserted. Do not connect more than 10pF to SETI.
11	GND	Ground

Pin Description (continued)

PIN	NAME	FUNCTION
12	FLAG	Open-Drain Fault Indicator Output. FLAG goes low when the fault duration exceeds the blanking time, reverse current is detected, thermal shutdown mode is active, OVLO threshold is reached, or SETI is connected to GND.
13	EN	Active-High Enable Input. See Table 2.
14, 15	OUT	Output Pins. Output of internal FETs. Bypass OUT to GND with a 1µF ceramic capacitor placed as close to the device as possible.
16	RIEN	Reverse-Current Enable Input. Connect RIEN to GND to enable the reverse-current flow protection. Connect RIEN to logic-high to disable the reverse-current flow protection.
—	EP	Exposed Pad. Connect EP to ground. Do not use EP as the only ground connection.

Functional Diagram



Detailed Description

The MAX17523/MAX17523A are adjustable overvoltage and overcurrent protection devices designed to protect systems against positive and negative input voltage faults up to $\pm 40V$, and feature a low $190m\Omega$ (typ) on-resistance FET. If the input voltage exceeds the OVLO threshold or falls below the UVLO, the internal FETs are turned off to prevent damage to the protected components. If the OVLO or the UVLO pin is set below the external OVLO or UVLO select threshold (V_{SEL_OVLO} , V_{SEL_UVLO}), the devices automatically select the internal $\pm 5\%$ accurate trip thresholds. The internal OVLO threshold is preset to 33V (typ), and the internal UVLO threshold is preset to 19V (typ).

Current-Limit Type Select

The MAX17523 power-up current-limit default is latch-off mode when CLTS_MODE is low. The MAX17523A power-up current-limit default is continuous mode when CLTS_MODE is low. After power up, the current-limit type can be programmed externally through CLTS1 and CLTS2 (Table 1). When CLTS_MODE is high, CLTS1 and CLTS2 are sampled continuously. When CLTS_MODE is low, CLTS1 and CLTS2 are sampled only when $V_{IN} - V_{OUT} < 0.6V$. Connect CLTS1, CLTS2, and CLTS_MODE to CLHS for logic-high or to GND for logic-low.

Autoretry

When the current threshold is reached, the t_{BLANK} timer begins counting. The \overline{FLAG} asserts if the overcurrent condition is present for t_{BLANK} . The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. A retry time delay (t_{RETRY}) is started immediately after t_{BLANK} has elapsed and during t_{RETRY} time, the FETs are off. At the end of t_{RETRY} , the FETs are turned on again. If the fault still exists, the cycle is repeated and the \overline{FLAG} stays low. When the fault is removed, the FETs stay on. (Figure 1)

The autoretry feature reduces the system power in case of overcurrent or short-circuit conditions. During t_{BLANK} time, when the switch is on, the supply current is held at the current limit. During t_{RETRY} time, when the switch is off, there is no current through the switch. Thus,

Table 1. Current-Limit Type Select

CLTS2	CLTS1	CURRENT-LIMIT TYPE
0	0	LATCHOFF
0	1	AUTORETRY
1	0	CONTINUOUS
1	1	CONTINUOUS

the output current is much less than the programmed current limit. Calculate the average output current using the following equation.

$$I_{LOAD} = I_{LIM} \left[\frac{t_{BLANK}}{t_{BLANK} + t_{RETRY}} \right]$$

With a 21ms (typ) t_{BLANK} and 620ms (typ) t_{RETRY} , the duty cycle is 3.3%, resulting in a 96.7% power saving.

Latch-Off

When the current threshold is reached, the t_{BLANK} timer begins counting. The \overline{FLAG} asserts if the overcurrent condition is present for t_{BLANK} . The timer resets when the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond the blanking time. To reset the switch, either toggle the control logic \overline{EN} or \overline{HVEN} (by changing the voltage level on the EN or \overline{HVEN} pins to a complementary status voltage level for at least 1.5 μs , and then back to the original status), or cycle the input voltage (Figure 2). The MAX17523/MAX17523A have a leakage current of up to 24 μA flowing from OUT pin when it is latched off.

Continuous

When the current threshold is reached, the MAX17523/MAX17523A limit the output current to the programmed current limit. The \overline{FLAG} asserts if the overcurrent condition is present for t_{BLANK} and deasserts when the overload condition is removed. (Figure 3)

Reverse-Current Block Enable (\overline{RIEN})

This feature disables the reverse-current protection and enables reverse-current flow from OUT to IN. The reverse-current block enable feature is useful in applications with inductive loads.

Fault Flag Output

\overline{FLAG} is an open-drain fault indicator output and requires an external pull-up resistor to a DC supply. \overline{FLAG} goes low when any of the following conditions occur:

- The blanking time has elapsed
- The reverse-current protection has tripped
- The die temperature exceeds $+150^{\circ}C$
- SET1 is connected to ground
- OVLO threshold is reached

Thermal Shutdown Protection

The devices have a thermal-shutdown feature to protect the devices from overheating. The devices turn off and the $\overline{\text{FLAG}}$ asserts when the junction temperature exceeds +150°C (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools by 30°C (typ), except when in latching mode, the devices remain latched off.

The thermal limit behaves similar to the current limit. For autoretry mode, the thermal limit works with auto retry timer. When the devices come out of the thermal limit, they start after the retry time. For latching mode, the devices latch off until power or EN cycle. For continuous mode, the devices only disable while the temperature is over the limit. There is no blanking time for thermal protection.

Overvoltage Lockout (OVLO)

The MAX17523/MAX17523A have a 33V (typ) preset OVLO threshold when the voltage at OVLO is set below the external OVLO select voltage (V_{SEL}). Connect OVLO to GND to activate the preset OVLO threshold. Connect the external resistors to OVLO pin as shown in the *Typical Application Circuit* to externally adjust the OVLO threshold. Use the following equation to adjust the OVLO rising threshold. The recommended value for R3 is 2.2MΩ.

$$V_{\text{OVLO}} = V_{\text{OVLO_R}} \times \left[1 + \frac{R3}{R4} \right]$$

where $V_{\text{OVLO_R}}$ is the OVLO rising threshold.

When the voltage on the OVLO pin exceeds $V_{\text{OVLO_R}}$, the MAX17523/MAX17523A enter an overvoltage lockout (OVLO) condition, turn OFF, and assert $\overline{\text{FLAG}}$. The devices exit OVLO condition and turn ON when the voltage on the OVLO pin falls below $V_{\text{OVLO_F}}$.

Undervoltage Lockout (UVLO)

The MAX17523/MAX17523A have a 19V (typ) preset UVLO threshold when the voltage at UVLO is set below the external UVLO select voltage (V_{SEL}). Connect UVLO to GND to activate the preset UVLO threshold. Connect the external resistors to UVLO pin as shown in the *Typical Application Circuit* to externally adjust the UVLO threshold. Use the following equation to adjust the UVLO threshold. The recommended value for R1 is 2.2MΩ.

$$V_{\text{UVLO}} = V_{\text{UVLO_R}} \times \left[1 + \frac{R1}{R2} \right]$$

where $V_{\text{UVLO_R}}$ is the UVLO rising threshold.

When the voltage on the UVLO pin rises above $V_{\text{UVLO_R}}$, the MAX17523/MAX17523A exit an undervoltage lockout (UVLO) condition and turn ON. The devices enter UVLO condition and turn OFF when the voltage on UVLO pin falls below $V_{\text{UVLO_F}}$.

Switch Control

There are two independent enable inputs ($\overline{\text{HVEN}}$ and EN) for the MAX17523/MAX17523A. $\overline{\text{HVEN}}$ is a high-voltage capable input. $\overline{\text{HVEN}}$ and EN can be used to turn ON/OFF the internal switches of the MAX17523/MAX17523A as shown in *Table 2*. Also, when latch-off protection mode is selected, toggle $\overline{\text{HVEN}}$ or EN to a complementary voltage level for at least 1.5μs, and then back to the original status to reset the fault condition once a short circuit is detected and the device shuts down.

Input Debounce Protection

The MAX17523/MAX17523A feature input debounce protection. When the input voltage is higher than the UVLO threshold voltage for a period greater than the debounce time (t_{DEB}), the internal FETs are turned on. This feature is intended for applications where the EN or $\overline{\text{HVEN}}$ signal is present when the power supply ramps up (Figure 4).

Applications Information

Setting the Current Limit/Threshold

A resistor from SET1 to ground programs the current-limit/threshold value for the device. Leaving SET1 unconnected selects a 0A current limit/threshold. Connecting SET1 to ground asserts $\overline{\text{FLAG}}$.

Use the following formula to calculate the current limit:

$$R_{\text{SET1}}(\text{k}\Omega) = \frac{6100}{I_{\text{LIM}}(\text{mA})}$$

IN Bypass Capacitor

Connect a minimum of 0.47μF capacitor from IN to GND to limit the input voltage drop during momentary output short-circuit conditions. Larger capacitor values further reduce the voltage undershoot at the input.

Table 2. Enable Inputs

$\overline{\text{HVEN}}$	EN	SWITCH STATUS
0	0	ON
0	1	ON
1	0	OFF
1	1	ON

Hot Plug-In at IN Terminal

In many system powering applications, an input filtering capacitor is required to lower the radiated emission, enhance the ESD capability, etc. In hot plug applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when the powered cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. An input voltage of 24V can easily exceed the absolute maximum rating of 40V, which may permanently damage the device. A transient voltage suppressor (TVS) is often used for industrial applications to protect the system from these conditions. We recommend using a TVS that is capable of limiting the input surge to 40V placed close to the input terminal.

OUT Capacitor

For stable operation over the full temperature range and over the entire programmable current-limit range, connect a 4.7μF ceramic capacitor from OUT to ground. Excessive output capacitance can cause a false overcurrent condition due to decreased dv/dt across the capacitor. Calculate the maximum capacitive load (C_{MAX}) value that can be connected to OUT by using the following formula:

$$C_{MAX}(\mu\text{F}) = \frac{I_{LIM}(\text{mA}) \times t_{BLANK(TYP)}(\text{ms})}{V_{IN}(\text{V})}$$

For example, for $V_{IN} = 24\text{V}$, $t_{BLANK(TYP)} = 20\text{ms}$, and $I_{LIM} = 1\text{A}$, C_{MAX} equals 833μF.

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal.

Power dissipation under steady-state normal operation is calculated as:

$$P_{(SS)} = I_{OUT}^2 \times R_{ON}$$

If the output is continuously shorted to ground at the maximum supply voltage, the switches with the autoretry option do not cause thermal shutdown detection to trip. Power dissipation in the devices operating in autoretry mode is calculated using the following equation:

$$P_{(MAX)} = \frac{V_{IN(MAX)} \times I_{OUT(MAX)} \times t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

Attention must be given to continuous current-limit mode when the power dissipation during a fault condition can cause the device to reach the thermal-shutdown threshold. Thermal vias from the exposed pad to ground plane are highly recommended to increase the system thermal capacitance while reducing the thermal resistance to the ambient.

MAX17523/MAX17523A

4.2V to 36V, 1A Current Limiter with
OV, UV, Reverse Voltage Protection

Ordering Information

PART	TEMP RANGE	TOP MARK	PIN-PACKAGE
MAX17523ATE+T	-40°C to +125°C	ALF	16 TQFN-EP*
MAX17523ATE+	-40°C to +125°C	ALF	16 TQFN-EP*
MAX17523AATE+	-40°C to +125°C	ARV	16 TQFN-EP*
MAX17523AATE+T	-40°C to +125°C	ARV	16 TQFN-EP*

+ Denotes a lead(Pb)-free package/RoHS-compliant package.

T = Tape and reel

*EP = Exposed pad

Chip Information

PROCESS: BiCMOS