*Click **here** for production status of specific part numbers.*

MAX17524

4.5V to 60V, Dual 3A, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The MAX17524 dual 3A, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFETs operates over an input-voltage range of 4.5V to 60V. The device can deliver up to 3A on each output and generates output voltages from 0.9V up to 90% of V_{IN}. This device features internal compensation.

The MAX17524 uses peak current-mode control, and can be operated in pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous-conduction mode (DCM) to enable high efficiency under light-load conditions.

The feedback-voltage regulation accuracy is accurate to within ±1.4% over -40°C to +125°C. The device is available in a 32-pin (5mm x 5mm) Thin QFN (TQFN) package. Simulation models are available.

Applications

- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage Single-Board Systems

***Ordering Information** appears at end of data sheet.*

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky - Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable Output Range from 0.9V up to 90% of V_{IN}
  - Delivers up to 3A on Each Output Over the Temperature Range
  - 100kHz to 1.1MHz Adjustable Frequency with External Clock Synchronization
  - Available in a 32-Pin, 5mm x 5mm TQFN Package
- Independent Input-Voltage Pins for Each Output
- Reduces Power Dissipation
  - Peak Efficiency of 94.4%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap Supply (EXTVCC) for Improved Efficiency
  - 5.2µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Independent Adjustable Soft-Start Pin and Programmable EN/UVLO Pin for Each Output
  - Monotonic Startup with Prebiased Output Voltage
  - Built-in Independent Output-Voltage Monitoring with $\overline{\text{RESET}}$ for Each Output
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range / -40°C to +150°C Junction Temperature Range

19-100201; Rev 1; 8/19

maxim integrated™

Absolute Maximum Ratings

IN_ to PGND_ .....-0.3V to +65V
PGND_ to SGND.....-0.3V to +0.3V
EXTVCC_ to SGND .....-0.3V to +26V
EN/UVLO_ to SGND .....-0.3V to +65V
FB_ , $V_{CC\_}$ to SGND .....-0.3V to +6V
RESET_, SS_, MODE/SYNC_, CF_, RT to SGND .....-0.3V to $V_{CC\_}$ +0.3V
BST_ to PGND_.....-0.3V to +70V
BST_ to LX_.....-0.3V to +6V
BST_ to $V_{CC\_}$.....-0.3V to +65V
LX_ to PGND_..... -0.3V to $V_{IN\_}$ + 0.3V
DL_ to PGND_ .....-0.3V to $V_{CC\_}$ +0.3V
LX_ Total RMS Current 4.8A
Continuous Power Dissipation
(Multilayer Board) (T_A = +70°C,
derate 34.5mW/°C above +70°C.).....2758.6mW
Output Short-Circuit Duration.....Continuous
Operating Temperature Range (Note 1).....-40°C to 125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 32 TQFN	
Package Code	T3255+4C
Outline Number	**21-0140**
Land Pattern Number	**90-0012**
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction to Ambient (θ_{JA})	23°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.
Note 2: Package thermal resistances were obtained using the MAX17524 Evaluation Kit (EV kit).

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = Open (f_{SW} = 450 kHz), C_{VCC} = 2.2µF, $V_{MODE/SYNC}$ = V_{SGND} = V_{PGND} = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND and the data is intended for both the converters, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input-Voltage Range	V_{IN}		4.5		60	V
Input-Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		5.2	9.5	µA
Input-Quiescent Current	I_{Q_PFM}	MODE/SYNC = Open		1400		µA
		MODE/SYNC = Open, R_{RT} = 22.1kΩ		1400		
	I_{Q_DCM}	DCM Mode, V_{LX} = 0.1V		1.36	2	mA
	I_{Q_PWM}	V_{FB} = 0.8V, EXTVCC = DL = Open		5		
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.216	1.245	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.065	1.089	1.116	
V_{CC} (LDO)						
V_{CC} Output-Voltage Range	V_{CC}	1mA ≤ I_{VCC} ≤ 20mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V, I_{VCC} = 1mA	4.75	5	5.25	
V_{CC} Current Limit	$I_{VCC(MAX)}$	V_{CC} = 4.3V, V_{IN} = 6V	50	90	140	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 25mA			0.4	V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.09	4.2	4.29	V
	V_{CC_UVF}	V_{CC} falling	3.69	3.8	3.89	
EXTVCC						
EXTVCC Switchover Threshold	$V_{EXTVCC-R}$	V_{EXTVCC} rising	4.56	4.7	4.84	V
EXTVCC Switchover Voltage Hysteresis			0.205	0.232	0.26	V
HIGH-SIDE MOSFET AND LOW-SIDE DRIVER						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		85	180	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = (V_{PGND} +1V) to (V_{IN} - 1V), T_A = +25°C	-4	1	+4	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	MODE/SYNC = SGND or MODE/SYNC = V_{CC}	0.888	0.9	0.912	V
		MODE/SYNC = Open	0.9	0.915	0.943	
FB Input-Bias Current	I_{FB}	0 ≤ V_{FB} ≤ 1V, T_A = 25°C	-100		+100	nA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = Open (f_{SW} = 450 kHz), C_{VCC} = 2.2µF, $V_{MODE/SYNC}$ = V_{SGND} = V_{PGND} = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND and the data is intended for both the converters, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE/SYNC = V_{CC} (DCM mode)	V_{CC} - 0.6			V
	V_{M-PFM}	MODE/SYNC = Open (PFM mode)		V_{CC}/2		
	V_{M-PWM}	MODE/SYNC = SGND (PWM mode)			0.6	
SYNC Frequency-Capture Range	f_{SYNC}	f_{SW} set by R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2			V
	V_{IL}				0.8	
Number of Pulses Required to Enter into SYNC Mode				8		
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		4.2	4.6	5.1	A
Runaway Peak Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		5.1	5.6	6.3	A
PFM Peak Current-Limit Threshold	I_{PFM}	MODE/SYNC = Open		1.15		A
Negative Current-Limit Threshold	$V_{NEG-LIM}$	MODE/SYNC = Open OR MODE/SYNC = V_{CC}	-8	0	+8	mV
		MODE/SYNC = SGND	42	50	60	
RT						
Switching Frequency	f_{SW}	R_{RT} = 100kΩ	97.5	105	112.5	kHz
		R_{RT} = 22.1kΩ	430	454	478	
		R_{RT} = 8.25kΩ	950	1100	1250	
		R_{RT} = Open	420	450	480	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$		0.56	0.58	0.61	V
HICCUP Timeout		(Note 4)		32768		Cycles
Minimum On-Time	t_{ON-MIN}			90	140	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		165	ns
LX Dead Time	LX_{DT}			22		ns

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = Open (f_{SW} = 450 kHz), C_{VCC} = 2.2µF, $V_{MODE/SYNC}$ = V_{SGND} = V_{PGND} = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND and the data is intended for both the converters, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$						
$\overline{RESET}$ Output-Level Low	V_{RESETL}	$I_{\overline{RESET}}$ = 10mA		110	200	mV
$\overline{RESET}$ Output-Leakage Current	$I_{RESETLKG}$	T_A = T_J = 25°C, $V_{\overline{RESET}}$ = 5.5V	-100		100	nA
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.4	92.5	94.6	%
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.4	95.5	97.7	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				1024		cycles
THERMAL SHUTDOWN (TEMP)						
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

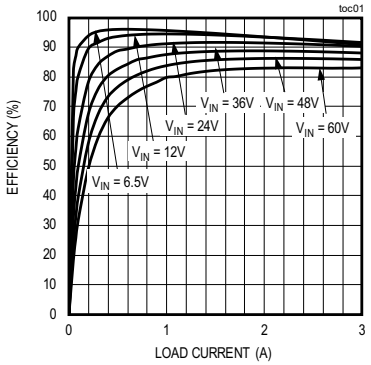
Note 3: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 4: See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details

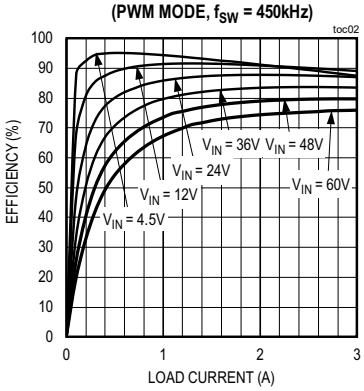
Typical Operating Characteristics

($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

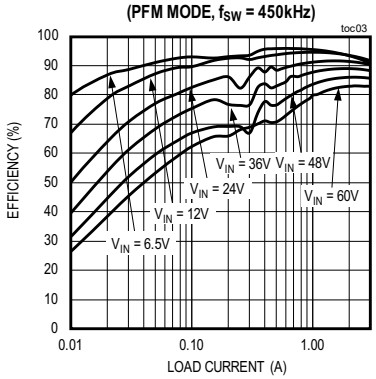
MAX17524, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, f_{SW} = 450kHz)



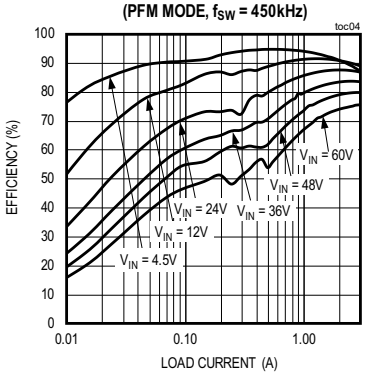
MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, f_{SW} = 450kHz)



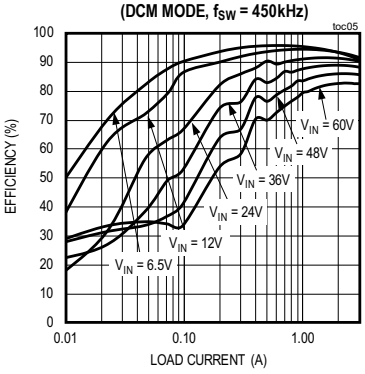
MAX17524, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, f_{SW} = 450kHz)



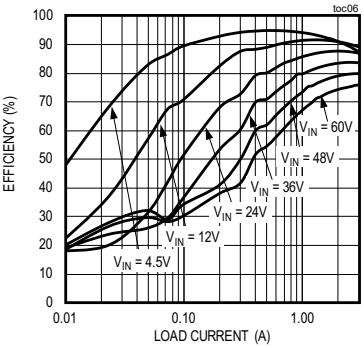
MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, f_{SW} = 450kHz)



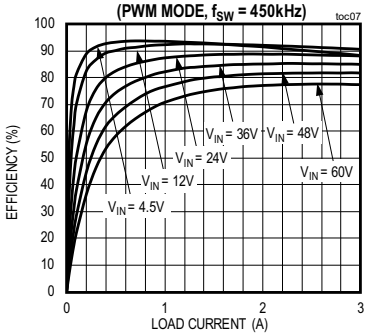
MAX17524, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, f_{SW} = 450kHz)



MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, f_{SW} = 450kHz)

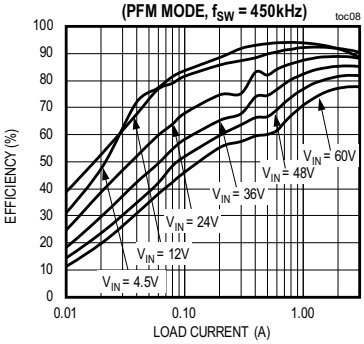


MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, f_{SW} = 450kHz)



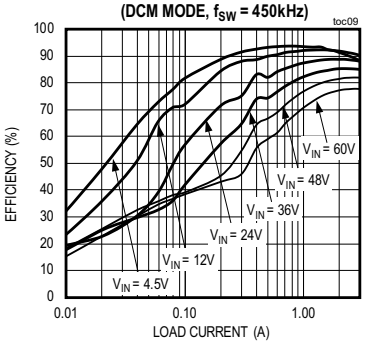
CONDITIONS: EXTVCC2 IS CONNECTED TO V_{OUT1} THROUGH AN RC FILTER OF 4.7Ω and 0.1µF

MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, f_{SW} = 450kHz)



CONDITIONS: EXTVCC2 IS CONNECTED TO V_{OUT1} THROUGH AN RC FILTER OF 4.7Ω and 0.1µF

MAX17524, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, f_{SW} = 450kHz)

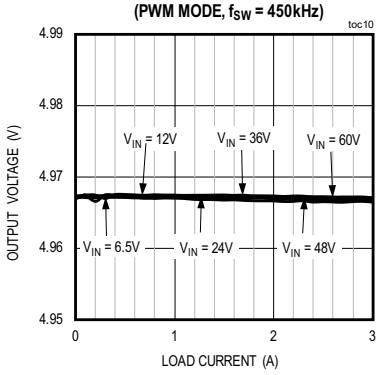


CONDITIONS: EXTVCC2 IS CONNECTED TO V_{OUT1} THROUGH AN RC FILTER OF 4.7Ω and 0.1µF

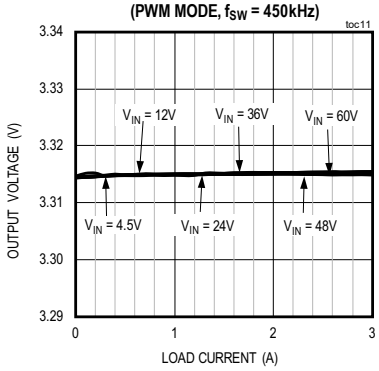
Typical Operating Characteristics (continued)

($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

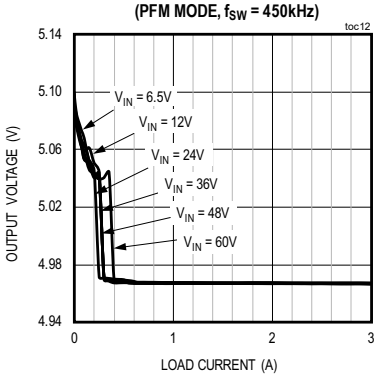
MAX17524, 5V OUTPUT LOAD AND LINE REGULATION (PWM MODE, f_{SW} = 450kHz)



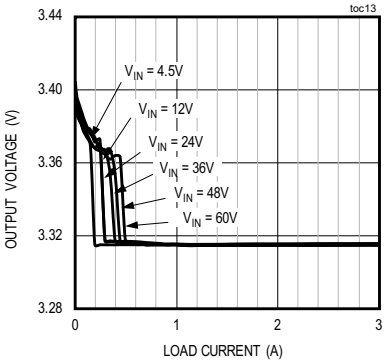
MAX17524, 3.3V OUTPUT LOAD AND LINE REGULATION (PWM MODE, f_{SW} = 450kHz)



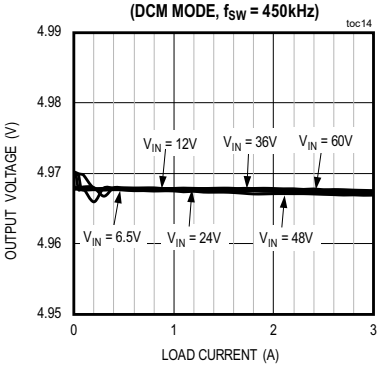
MAX17524, 5V OUTPUT LOAD AND LINE REGULATION (PFM MODE, f_{SW} = 450kHz)



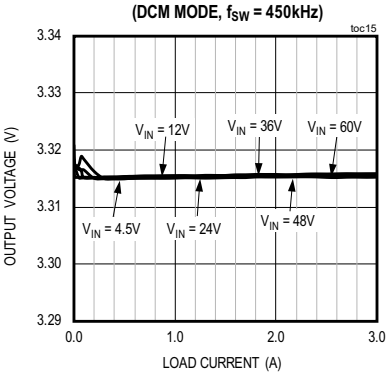
MAX17524, 3.3V OUTPUT LOAD AND LINE REGULATION (PFM MODE, f_{SW} = 450kHz)



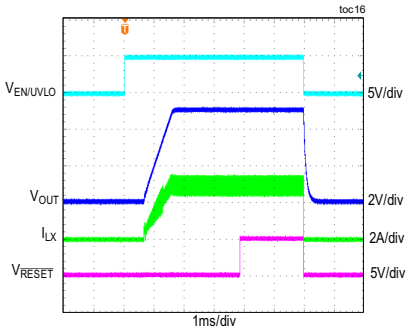
MAX17524, 5V OUTPUT LOAD AND LINE REGULATION (DCM MODE, f_{SW} = 450kHz)



MAX17524, 3.3V OUTPUT LOAD AND LINE REGULATION (DCM MODE, f_{SW} = 450kHz)

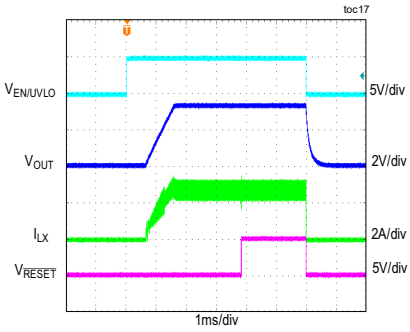


MAX17524, 5V OUTPUT SOFT-START/SHUTDOWN THROUGH EN/UVLO (f_{SW} = 450kHz, PWM MODE, 1.66Ω RESISTIVE LOAD)



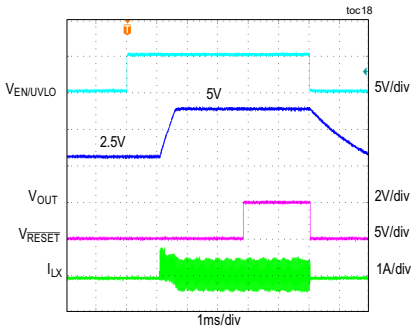
CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC}

MAX17524, 3.3V OUTPUT SOFT-START/SHUTDOWN THROUGH EN/UVLO (PWM MODE, 1.1Ω RESISTIVE LOAD, f_{SW} = 450kHz)



CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC}

MAX17524, 5V OUTPUT SOFT-START WITH PREBIAS VOLTAGE OF 2.5V (PWM MODE, 1kΩ RESISTIVE LOAD, f_{SW} = 450kHz)

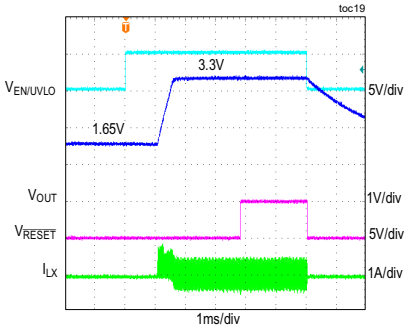


CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC}

Typical Operating Characteristics (continued)

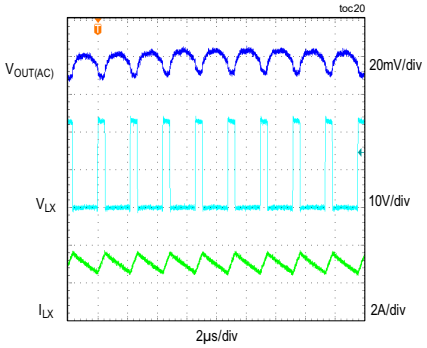
($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

MAX17524, 3.3V OUTPUT SOFT-START WITH PREBIAS VOLTAGE OF 1.65V (PWM MODE, 0.66kΩ RESISTIVE LOAD, f_{SW} = 450kHz)

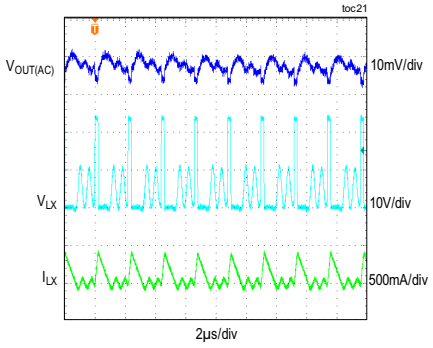


CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC}

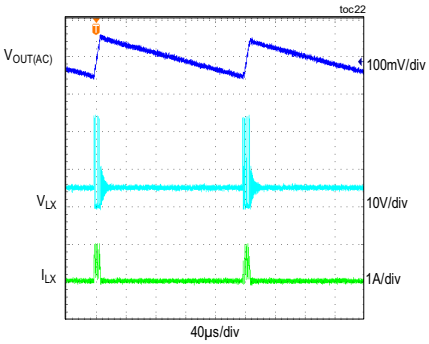
MAX17524, 5V OUTPUT STEADY STATE, (PWM MODE, 3A LOAD, f_{SW} = 450kHz)



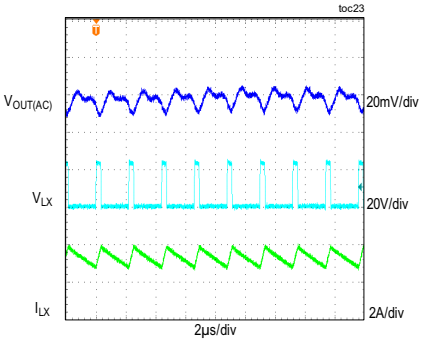
MAX17524, 5V OUTPUT STEADY STATE (f_{SW} = 450kHz, DCM MODE, 75mA LOAD)



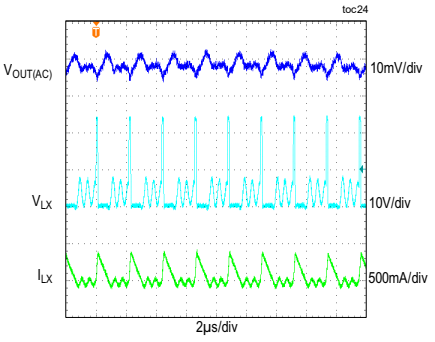
MAX17524, 5V OUTPUT STEADY STATE (f_{SW} = 450kHz, PFM MODE, 25mA LOAD)



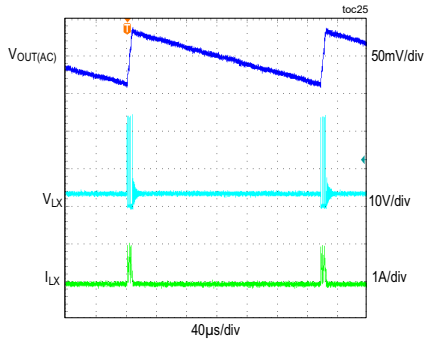
MAX17524, 3.3V OUTPUT STEADY STATE (f_{SW} = 450kHz, PWM MODE, 3A LOAD)



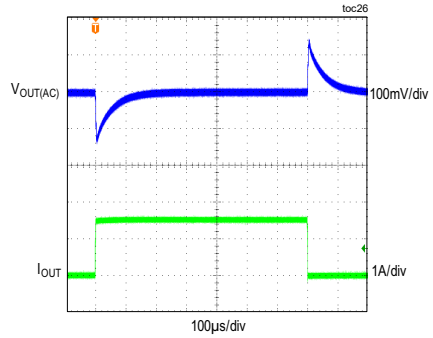
MAX17524, 3.3V OUTPUT STEADY STATE (f_{SW} = 450kHz, DCM MODE, 75mA LOAD)



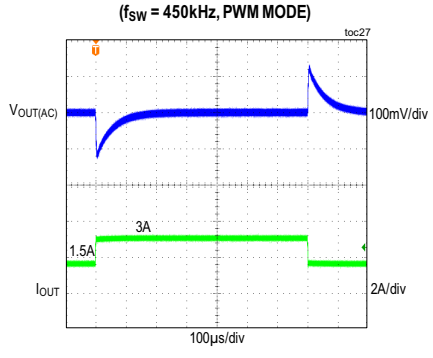
MAX17524, 3.3V OUTPUT STEADY STATE (f_{SW} = 450kHz, PFM MODE, 25mA LOAD)



MAX17524, 5V OUTPUT LOAD TRANSIENT BETWEEN 0A AND 1.5A (f_{SW} = 450kHz, PWM MODE)



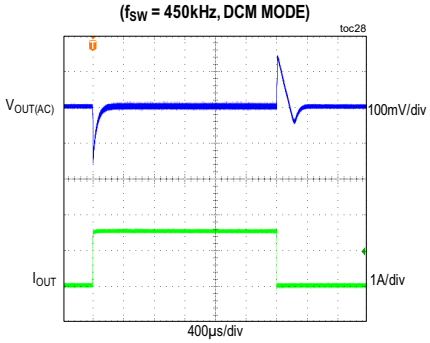
MAX17524, 5V OUTPUT LOAD TRANSIENT BETWEEN 1.5A AND 3A (f_{SW} = 450kHz, PWM MODE)



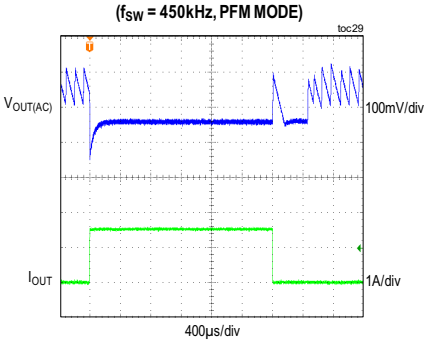
Typical Operating Characteristics (continued)

($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

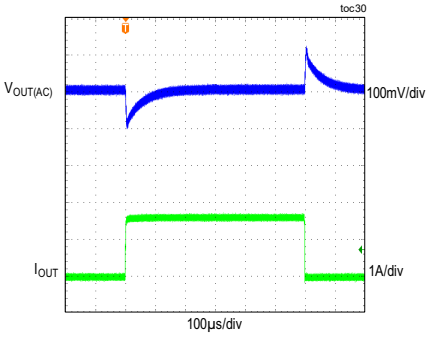
MAX17524, 5V OUTPUT LOAD TRANSIENT BETWEEN 50mA AND 1.5A (f_{SW} = 450kHz, DCM MODE)



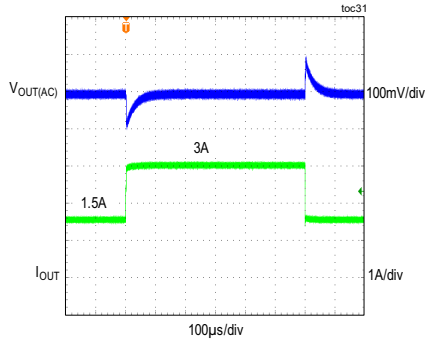
MAX17524, 5V OUTPUT LOAD TRANSIENT BETWEEN 50mA AND 1.5A (f_{SW} = 450kHz, PFM MODE)



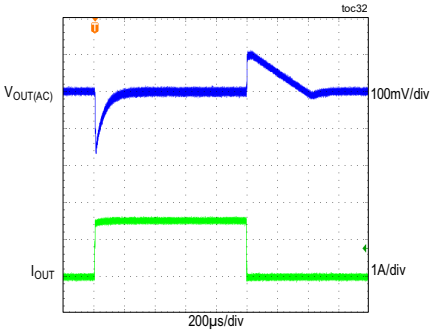
MAX17524, 3.3V OUTPUT LOAD TRANSIENT BETWEEN 0A AND 1.5A (f_{SW} = 450kHz, PWM MODE)



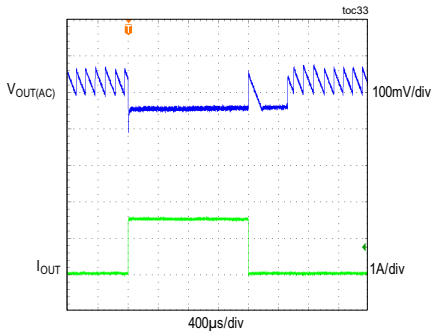
MAX17524, 3.3V OUTPUT LOAD TRANSIENT BETWEEN 1.5A AND 3A (f_{SW} = 450kHz, PWM MODE)



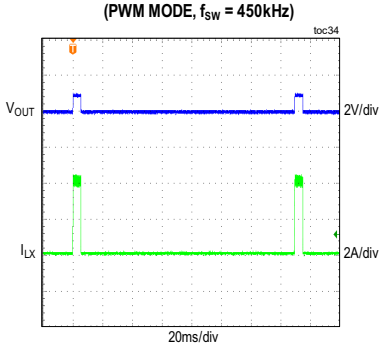
MAX17524, 3.3V OUTPUT LOAD TRANSIENT BETWEEN 50mA AND 1.5A (f_{SW} = 450kHz, DCM MODE)



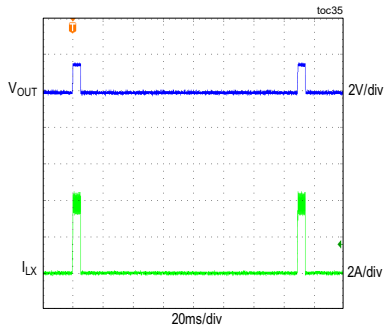
MAX17524, 3.3V OUTPUT LOAD TRANSIENT BETWEEN 50mA AND 1.5A (f_{SW} = 450kHz, PFM MODE)



MAX17524, 5V OUTPUT OVERLOAD PROTECTION (PWM MODE, f_{SW} = 450kHz)



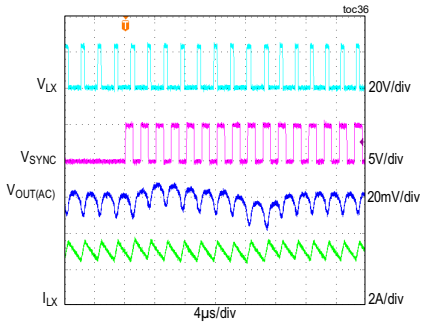
MAX17524, 3.3V OUTPUT OVERLOAD PROTECTION (PWM MODE, f_{SW} = 450kHz)



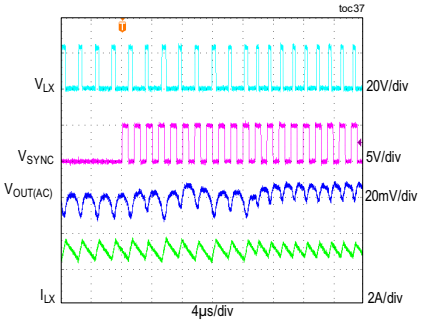
Typical Operating Characteristics (continued)

($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

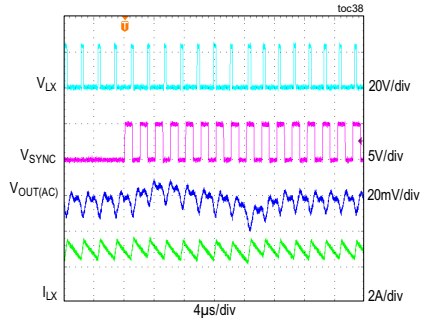
MAX17524, 5V OUTPUT EXTERNAL CLOCK SYNCHRONIZATION WITH 495kHz (PWM MODE, 3A LOAD)



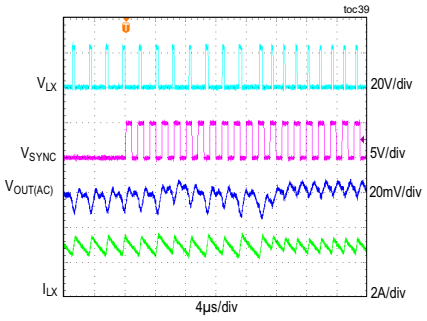
MAX17524, 5V OUTPUT EXTERNAL CLOCK SYNCHRONIZATION WITH 630kHz (PWM MODE, 3A LOAD)



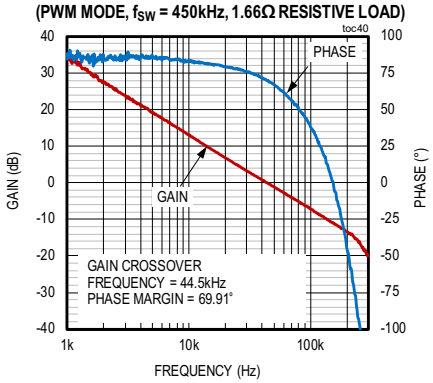
MAX17524, 3.3V OUTPUT EXTERNAL CLOCK SYNCHRONIZATION WITH 495kHz (PWM MODE, 3A LOAD)



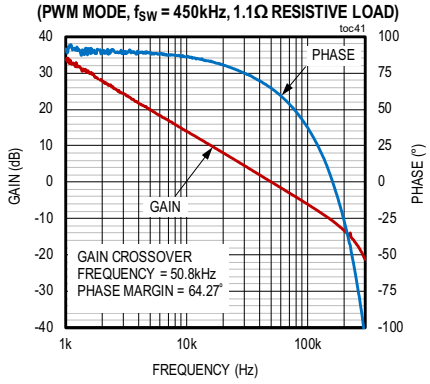
MAX17524, 3.3V OUTPUT EXTERNAL CLOCK SYNCHRONIZATION WITH 630kHz (PWM MODE, 3A LOAD)



MAX17524, 5V OUTPUT BODE PLOT (PWM MODE, f_{SW} = 450kHz, 1.66Ω RESISTIVE LOAD)



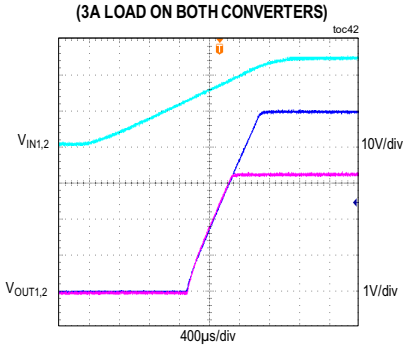
MAX17524, 3.3V OUTPUT BODE PLOT (PWM MODE, f_{SW} = 450kHz, 1.1Ω RESISTIVE LOAD)



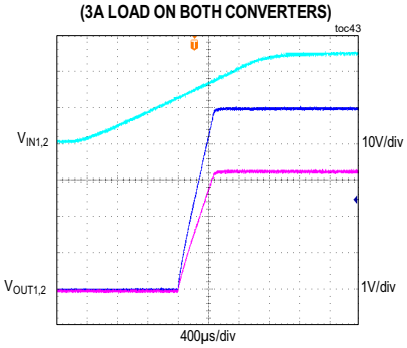
Typical Operating Characteristics (continued)

($V_{EN/UVLO1}$ = V_{IN1} = $V_{EN/UVLO2}$ = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2µF, C_{BST1} = C_{BST2} = 0.1µF, C_{SS1} = C_{SS2} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

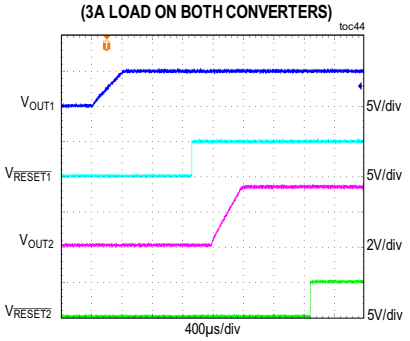
MAX17524, FIGURE 4
STARTUP IN COINCIDENT TRACKING MODE
(3A LOAD ON BOTH CONVERTERS)



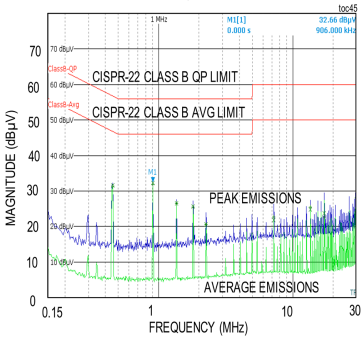
MAX17524, FIGURE 5
STARTUP IN RATIOMETRIC TRACKING MODE
(3A LOAD ON BOTH CONVERTERS)



MAX17524, FIGURE 6
STARTUP IN SEQUENTIAL TRACKING MODE
(3A LOAD ON BOTH CONVERTERS)

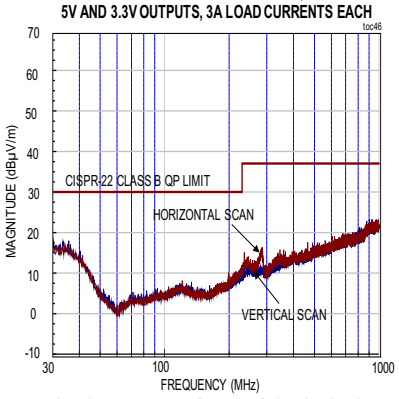


CONDUCTED EMISSIONS PLOT,
5V AND 3.3V OUTPUTS, 3A LOAD CURRENTS EACH



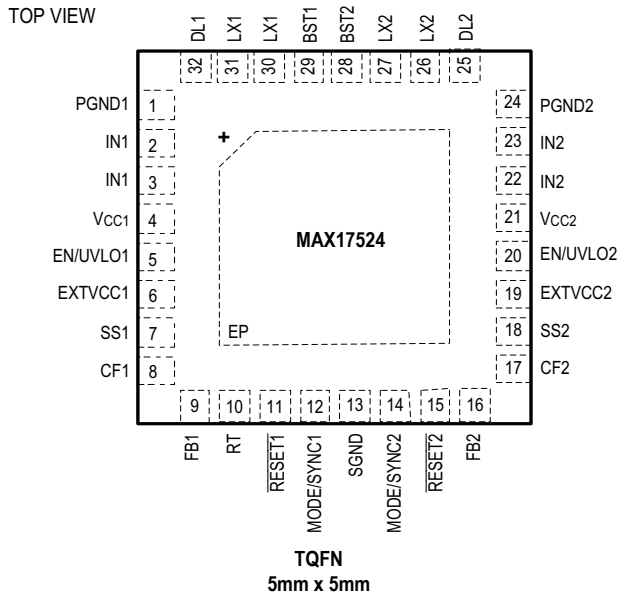
TESTED ON MAX17524EVKITE# WITH L3 = 15µH, C6 = C8 = 2.2µF/100V/X7R/1210

RADIATED EMISSIONS PLOT,
5V AND 3.3V OUTPUTS, 3A LOAD CURRENTS EACH



TESTED ON MAX17524EVKITE# WITH L3 = SHORT, C6 = C8 = OPEN

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 24	PGND1, PGND2	Power Ground Pins of Converter 1 and 2. Connect the PGND1 and PGND2 pins externally to their respective power-ground planes. Connect the PGND1, PGND2 and SGND pins together. Refer to the MAX17524 EV kit data sheet for a layout example.
2, 3	IN1	Power-Supply Input for Converter 1. 4.5V to 60V Input-Supply Range. Connect the IN1 pins together. Decouple to PGND1 with a 4.7µF capacitor; place the capacitor close to the IN1 and PGND1 pins. Refer to the MAX17524 EV kit data sheet for a layout example.
4	V_{CC1}	5V LDO Output for Converter 1. Bypass V_{CC1} with a 2.2µF ceramic capacitance to SGND. LDO does not support the external loading on V_{CC1}.
5	EN/UVLO1	Enable/Undervoltage Lockout Pin for Converter 1. Drive EN/UVLO1 high to enable the output of converter 1. Connect to the center of the resistor-divider between IN1 and SGND to set the input voltage at which converter 1 turns on. Connect to the IN1 pins for always-on operation. Pull lower than V_{ENF} for disabling the converter.
6	EXTVCC1	External Power-Supply Input for the Internal LDO of Converter 1. Applying a voltage between V_{EXTVCC} (4.7V typ) and 24V at the EXTVCC1 pin bypasses the internal LDO and improves the overall efficiency. Add a local bypassing cap (0.1µF) on EXTVCC1 pin to SGND and also, add a 4.7Ω resistor from buck converter output node to EXTVCC1 pin to limit V_{CC1} bypass-cap discharge current during an output short-circuit condition. When EXTVCC1 is not used, connect it to SGND.

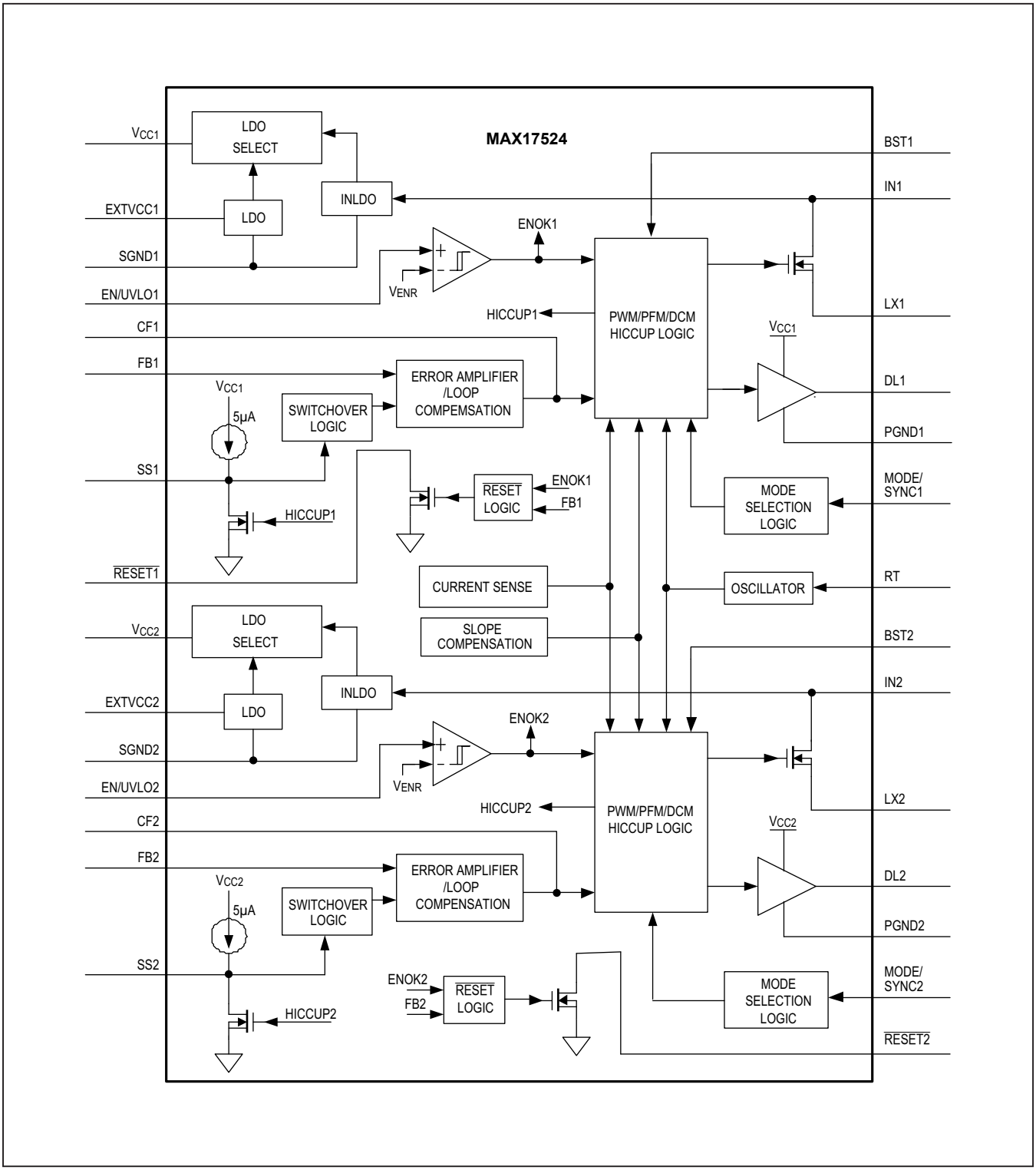
Pin Description (continued)

PIN	NAME	FUNCTION
7	SS1	Soft-Start Input for Converter 1. Connect a capacitor from SS1 to SGND to set the soft-start time.
8	CF1	Compensator Output for Converter 1. At switching frequencies, lower than 450kHz, connect a capacitor from CF1 to FB1. Leave CF1 open if the switching frequency is equal to, or more than 450kHz. See the *Loop Compensation* section for more details.
9	FB1	Feedback Input for Converter 1. Connect FB1 to the center tap of an external resistor-divider from the output node of converter 1 to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
10	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the switching frequency of both the converters. Leave RT open for the default 450kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
11	$\overline{\text{RESET1}}$	Open-Drain $\overline{\text{RESET1}}$ Output. The $\overline{\text{RESET1}}$ output is driven low if FB1 drops below 92.5% of its set value. $\overline{\text{RESET1}}$ goes high 1024 cycles after FB1 rises above 95.5% of its set value.
12	MODE/ SYNC1	Mode Selection and External Clock Synchronization Input for Converter 1. The MODE/SYNC1 Pin configures the converter 1 to operate either in PWM, PFM or DCM modes of operation. Leave MODE/ SYNC1 unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC1 to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC1 to V_{CC1} for DCM operation at light loads. MODE/SYNC1 can also be used to synchronize the converter 1 to an external clock irrespective of the operating condition of converter 2. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
13	SGND	Analog Ground
14	MODE/ SYNC2	Mode Selection and External Clock Synchronization Input for Converter 2. The MODE/SYNC2 Pin configures the converter 2 to operate either in PWM, PFM or DCM modes of operation. Leave MODE/ SYNC2 unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC2 to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC2 to V_{CC2} for DCM operation at light loads. MODE/SYNC2 can also be used to synchronize the converter 2 to an external clock irrespective of the operating condition of converter 1. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
15	$\overline{\text{RESET2}}$	Open-Drain $\overline{\text{RESET2}}$ Output. The $\overline{\text{RESET2}}$ output is driven low if FB2 drops below 92.5% of its set value. $\overline{\text{RESET2}}$ goes high 1024 cycles after FB2 rises above 95.5% of its set value.
16	FB2	Feedback Input for Converter 2. Connect FB2 to the center tap of an external resistor-divider from the output node of converter 2 to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
17	CF2	Compensator Output for Converter 2. At switching frequencies, lower than 450kHz, connect a capacitor from CF2 to FB2. Leave CF2 open if the switching frequency is equal to, or more than 450kHz. See the *Loop Compensation* section for more details.
18	SS2	Soft-Start Input for Converter 2. Connect a capacitor from SS2 to SGND to set the soft-start time.
19	EXTVCC2	External Power-Supply Input for the Internal LDO of Converter 2. Applying a voltage between V_{EXTVCC} (4.7V typ) and 24V at the EXTVCC2 pin bypasses the internal LDO and improves efficiency. Add a local bypassing cap (0.1µF) on EXTVCC2 pin to SGND and also add a 4.7Ω resistor from the buck converter output node to the EXTVCC2 pin to limit V_{CC2} bypass-cap discharge current during an output short-circuit condition. When EXTVCC2 is not used, connect it to SGND.

Pin Description (continued)

PIN	NAME	FUNCTION
20	EN/UVLO2	Enable/Undervoltage Lockout Pin for Converter 2. Drive EN/UVLO2 high to enable the output of converter 2. Connect to the center of the resistor-divider between IN2 and SGND to set the input voltage at which converter 2 turns on. Connect to the IN2 pins for always-on operation. Pull lower than V_{ENF} for disabling the converter.
21	V_{CC2}	5V LDO Output for Converter 2. Bypass V_{CC2} with a 2.2µF ceramic capacitance to SGND. LDO does not support the external loading on V_{CC2}.
22, 23	IN2	Power-Supply Input for Converter 2. 4.5V to 60V Input-Supply Range. Connect the IN2 pins together. Decouple to PGND2 with a 4.7µF capacitor; place the capacitor close to the IN2 and PGND2 pins. Refer to the MAX17524 EV kit data sheet for a layout example.
25	DL2	Low-Side Gate Driver Output for Converter 2. Use DL2 pin to drive the gate of the low-side external nMOSFET.
26, 27	LX2	Switching Node of Converter 2. Connect LX2 pins to the switching side of the inductor.
28	BST2	Boost Flying Capacitor of Converter 2. Connect a 0.1µF ceramic capacitor between BST2 and LX2.
29	BST1	Boost Flying Capacitor of Converter 1. Connect a 0.1µF ceramic capacitor between BST1 and LX1.
30, 31	LX1	Switching Node of Converter 1. Connect LX1 pins to the switching side of the inductor.
32	DL1	Low-Side Gate Driver Output for Converter 1. Use DL1 pin to drive the gate of the low-side external nMOSFET.
–	EP	Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large SGND plane with several thermal vias for best thermal performance. Refer to the MAX17524 EV kit data sheet for an example of EP connection and thermal vias.

Functional Diagram



Detailed Description

The MAX17524 dual 3A, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFETs operate over an input-voltage range of 4.5V to 60V. Output voltages from 0.9V up to 90% of V_{IN} can be generated, and 3A load on each output can be delivered by the device. Each converter features internal compensation. The feedback-voltage regulation accuracy is accurate to within ±1.4% over -40°C to +125°C.

The MAX17524 features a peak-current-mode control architecture. Internal transconductance error amplifiers produce integrated-error voltages at two internal nodes, which set the duty cycles using PWM comparators, high-side current-sense amplifiers, and slope-compensation generators. At each rising edge of the clock, the high-side MOSFETs turn on and remain on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFETs' on-time, the inductor currents ramp up. During the second half of the switching cycle, high-side MOSFETs turn off and the low-side MOSFETs turn on. The inductors release the stored energy as their currents ramp down and provide current to the outputs.

The MAX17524 features a RT pin to program the switching frequency and two MODE/SYNC pins to program the modes of operation and to synchronize the internal clocks to external clocks. The device also features independent adjustable-input undervoltage lockout, adjustable soft-start, open-drain $\overline{RESET}$, and auxiliary bootstrap LDO for improved efficiency.

Mode Selection and External Clock Synchronization (MODE/SYNC)

The MAX17524 features two independent mode selection pins for the two converters. The logic state of the MODE/SYNC pin is latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the state of the MODE/SYNC pin is open at power-up, the converter operates in PFM mode at light loads. If the voltage at the MODE/SYNC pin is lower than V_{M-PWM} at power-up, the converter operates in constant-frequency PWM mode at all loads. If the voltage at the MODE/SYNC pin is higher than V_{M-DCM} at power-up, the converter operates in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

The internal clocks of the MAX17524 can be synchronized to external clock signals on the MODE/SYNC pins. The external clock synchronization frequency must be between 1.1 × f_{SW} and 1.4 × f_{SW}, where f_{SW} is the switching frequency programmed by the resistor connected at the RT pin. The external clock signals on the MODE/SYNC pins can have different frequency, but with in 1.1 × f_{SW} and 1.4 × f_{SW}. When an external clock is applied to MODE/SYNC pins, the internal oscillator frequency changes to external clock frequency (from the original frequency based on the RT pin setting) after detecting 8 external clock edges. When the external clock is applied on-fly then the converter operates in PWM mode during synchronization operation irrespective of the initial mode. After the exit from external clock synchronization, the converter enters into its original mode, which was set before synchronization. Only if the initial mode is PFM, after the exit from external clock synchronization, the part enters into DCM mode initially and after 32 internal clock cycles, the part enters PFM mode. MODE/SYNC pin of one converter can be synchronized to the external clock irrespective of the MODE/SYNC state of the other converter. The minimum external clock pulse-width high should be greater than 50ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of I_{PFM} (1.15A (typ)) every clock cycle until the output rises to 103.5% of the set nominal output voltage. Once the output reaches 103.5% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the converter enters hibernate operation until the load discharges the output to 101% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the set nominal output voltage, the converters come out of hibernate operation, turn on all internal blocks, and again commence the process of delivering pulses of energy to the output until it reaches 103.5% of the set nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, not by skipping pulses, but by disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The output-voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode.

Linear Regulator (V_{CC} and EXTVCC)

The MAX17524 has two internal LDO (Low-dropout) regulators for each converter that power V_{CC}. One LDO is powered from the IN pin V_{IN} and the other LDO is powered from EXTVCC. Only one of the two LDOs is in operation at a time depending on the voltage levels present at the EXTVCC pin. When V_{CC} is above its UVLO and if EXTVCC is greater than V_{EXTVCC} (4.7V typ), internal V_{CC} is powered by EXTVCC and LDO from the IN pin is disabled. If EXTVCC is less than V_{EXTVCC}, V_{CC} is powered up from the IN pin. For output voltages greater than V_{EXTVCC}, EXTVCC pins can be tied to their respective output nodes. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. The voltage at the EXTVCC pin should not exceed 24V.

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor. Both LDOs can source up to $I_{VCC(MAX)}$ (90mA typ). The MAX17524 employs an undervoltage-lockout circuit that forces both the converters off when V_{CC} falls below V_{CC_UVF}. The buck converter gets re-enabled when $V_{CC} > V_{CC\_UVR}$. The 400mV insert (typ) UVLO hysteresis prevents chattering on power-up and power-down.

Add a local bypassing cap of 0.1µF on the EXTVCC pin to SGND. Also, add a 4.7Ω resistor from buck converter output node to the EXTVCC pin to limit V_{CC} bypass cap discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit condition. In applications where the buck-converter output is connected to the EXTVCC pin, if the output is shorted to ground, then the transfer from EXTVCC to internal LDO happens seamlessly without any impact to the normal functionality. Connect EXTVCC pin to SGND when the pin is not being used.

Setting the Switching Frequency (RT)

The switching frequency of both the converters can be programmed from 100kHz to 1.1MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{10500}{f_{SW}} - 1.23$$

Where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open makes the converters operate at the default switching frequency of 450kHz. See Table 1 for RT resistor values for a few common switching frequencies.

Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output-voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF\text{-}MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{OFF\text{-}MIN(MAX)}$ = Worst-case minimum switch off-time (165 ns)

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (140 ns)

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances of the external low-side and internal high-side MOSFETs, respectively.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
100	105
200	51.1
450	Open or 22.1
1100	8.25

Overcurrent Protection (OCP)/Hiccup Mode

MAX17524 has a robust overcurrent-protection (OCP) scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ (4.6A (typ)). A runaway peak current limit on the high-side switch current at $I_{RUNAWAY-LIMIT}$ (5.6A (typ)) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, feedback voltage drops to $V_{FB-HICF}$ any time after soft-start is complete and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload conditions, if feedback voltage does not exceed $V_{FB-HICF}$, the device continues to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The MAX17524 includes two independent $\overline{\text{RESET}}$ comparators to monitor the status of the output voltages of the two converters. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above V_{FB-OKR} of the designed set nominal output voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below V_{FB-OKF} of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the converter starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Shutdown Protection

The MAX17524 features independent thermal-shutdown protection for both the converters to limit the junction temperature. When the junction temperature of the converter exceeds +165°C, an on-chip thermal sensor shuts down the converter, allowing the converter to cool. The device turns on with soft-start after the junction temperature reduces by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown during normal operation.

Applications Information

Input-Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}.$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

D = V_{OUT}/V_{IN} is the duty ratio of the converter

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Low-Side MOSFET Selection

The MAX17524 requires an external nMOSFET for each converter to operate and the low-side gate drive output DL pin drives the nMOSFET. The key selection parameters to select the nMOSFET include:

- Maximum Drain-Source Voltage (V_{DS-MAX})
- Miller Plateau Voltage during all operating conditions < 3.5V
- Low Drain-Source On-State Resistance ($R_{DS(ON)}$)
- Total Gate Charge (Q_g)
- Output Capacitance (C_{oss})
- Power-Dissipation Rating and Package Thermal Resistance

The nMOSFET must be of logic-level type with guaranteed on-state resistance specification at $V_{GS} \approx 4.5V$. It is also important that the chosen nMOSFET has suitable dynamic parameters so that the MAX17524 is able to turn it on and off within the specified dead time (LX_{DT}). Ensure that the losses in the selected MOSFET do not exceed its power rating. Using a low body diode reverse recovery charge (Q_{rr}) MOSFET reduces the converter loss.

The negative current capability of the low-side MOSFET is limited by $V_{NEG-LIM}$. $V_{NEG-LIM}$ translates to negative current limit ($I_{NEG-LIM}$) by the following relation:

$$V_{NEG-LIM} = I_{NEG-LIM} \times R_{DS(ON)LS}$$

where $R_{DS(ON)LS}$ is the on-state resistance of the low-side MOSFET.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value (L) in Henry as follows:

$$L = \frac{0.9 \times V_{OUT}}{f_{SW}}$$

where V_{OUT} is the output voltage in V and f_{SW} is the switching frequency in Hz.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit ($I_{PEAK-LIMIT}$).

Output-Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where:

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output-voltage deviation

f_C = Target closed-loop crossover frequency

Select f_C to be 1/10th of f_{SW} if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 50kHz. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Adjusting Output Voltage

Set the output voltage of each converter with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see Figure 1). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{TOP} from the output to the FB pin as follows:

$$R_{TOP} = \frac{301 \times 10^3}{\left(f_C \times C_{OUT\_SEL}\right)}$$

where:

R_{TOP} is in kΩ

f_C = Crossover frequency is in kHz

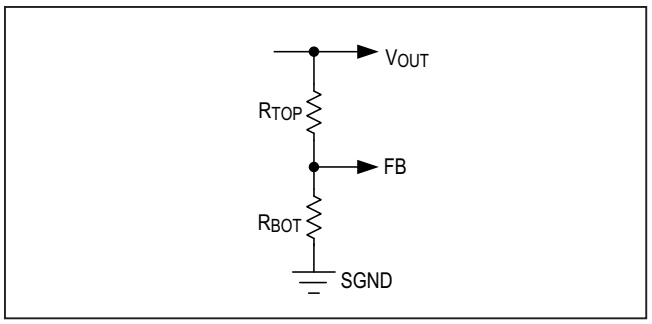


Figure 1. Setting the Output Voltage

C_{OUT_SEL} = Actual capacitance of the selected output capacitor at DC-bias voltage in µF.

Calculate resistor R_{BOT} from the FB pin to SGND as follows:

$$R_{BOT} = \frac{R_{TOP} \times 0.9}{(V_{OUT} - 0.9)}$$

R_{BOT} is in kΩ.

Loop Compensation

The MAX17524 is internally loop compensated. However, if the switching frequency is less than 450kHz, connect a 0402 capacitor (C_F) between the CF pin and the FB pin. Use Table 2 to select the value of C_F.

Soft-Start Capacitor Selection

The MAX17524 implements independent adjustable soft-start operation to reduce inrush currents for both the converters. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{OUT\_SEL} \times V_{OUT}$$

Table 2. Selection of Capacitor C_F

SWITCHING FREQUENCY RANGE (kHz)	C_F (pF)
200 to 300	2.2
300 to 450	1.2

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that during start-up, the device operates at half the programmed switching frequency until the output voltage reaches 67% of set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

The MAX17524 features two independent EN/UVLO pins for the two converters. Each EN/UVLO pin has an adjustable input undervoltage-lockout level. Set the voltage at which the converter turns on with a resistive voltage-divider connected from V_{IN} to SGND as shown in Figure 2. Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.216}{(V_{INU} - 1.216)}$$

where V_{INU} is the input-voltage level at which the converter is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power up (slower than soft-start)/power down. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin, to reduce voltage ringing on the line.

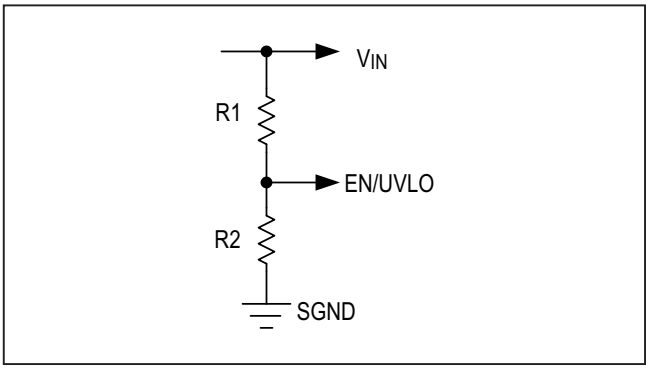


Figure 2. Setting the Input Undervoltage Lockout

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{IC\_LOSS} = P_{IC\_LOSS1} + P_{IC\_LOSS2}$$

$$P_{IC\_LOSS1} = \left(P_{OUT1} \times \left(\frac{1}{\eta 1} - 1\right)\right) - \left(I_{OUT1}{}^2 \times R_{DCR1}\right) - P_{ACLOSS\_L1} - \left(I_{OUT1}{}^2 \times R_{DS\_ON1(LS)} \times (1 - D_1)\right) - \left(V_{IN1} \times \left(\frac{1}{2} Q_{oss1} + Q_{rr1}\right) \times f_{SW}\right)$$

$$P_{OUT1} = V_{OUT1} \times I_{OUT1}$$

The expressions for P_{IC_LOSS2} and P_{OUT2} are same as of P_{IC_LOSS1} and P_{OUT1}, where:

$P_{OUT\_}$ = Output power of the converter.

$\eta\_$ = Efficiency of the converter.

$R_{DCR\_}$ = DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

$P_{ACLOSS\_L\_}$ = AC loss of the inductor.

$R_{DS\_ON\_(LS)}$ = On-state resistance of the low side MOSFET.

$Q_{rr\_}$ = Body-diode reverse-recovery charge of the low-side MOSFET.

$D\_$ = Duty cycle of the converter.

$Q_{oss\_}$ = Output charge of the low side MOSFET.

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 23°C/W$$
$$\theta_{JC} = 1.7°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{IC\_LOSS}\right)$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + \left(\theta_{JC} \times P_{IC\_LOSS}\right)$$

Note: Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor at the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous (unbroken) as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17524 EV kit layout available at **www.maximintegrated.com**.

Coincident/ Ratiometric Tracking and Output Voltage Sequencing

The soft-start pins (SS1 and SS2) can be used to track the output voltages to that of another power supply at startup. Figure 3 shows the independent soft-start of each converter output. Figure 4 shows the coincident tracking of the converter outputs. Figure 5 shows the ratiometric tracking of the converter outputs. Figure 6 shows the output voltage sequencing where converter 1 is the master.

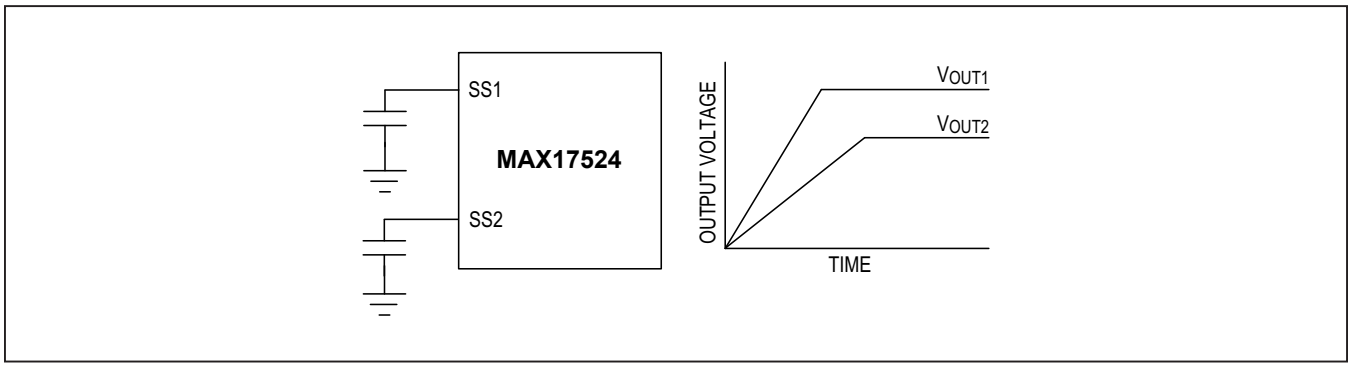


Figure 3. Independent Soft-Start of Each Converter Output

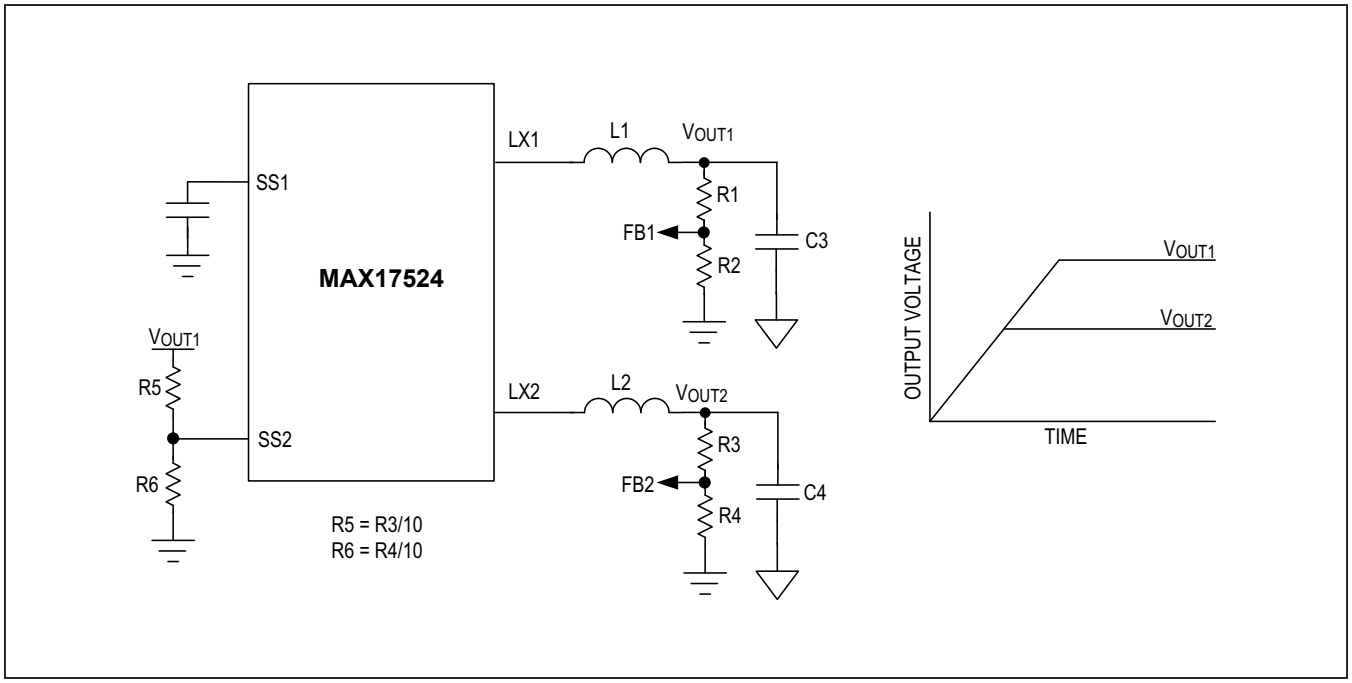


Figure 4. Coincident Tracking of the Converter Outputs

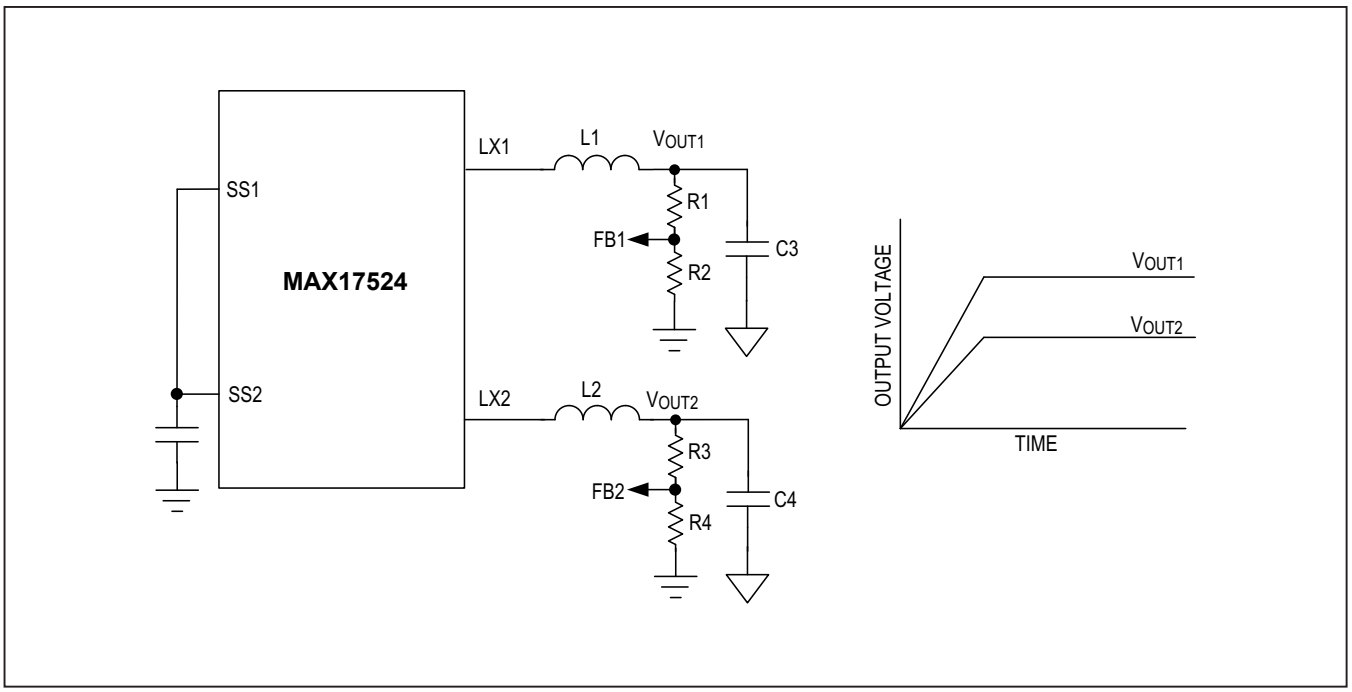


Figure 5. Ratiometric Tracking of the Converter Outputs

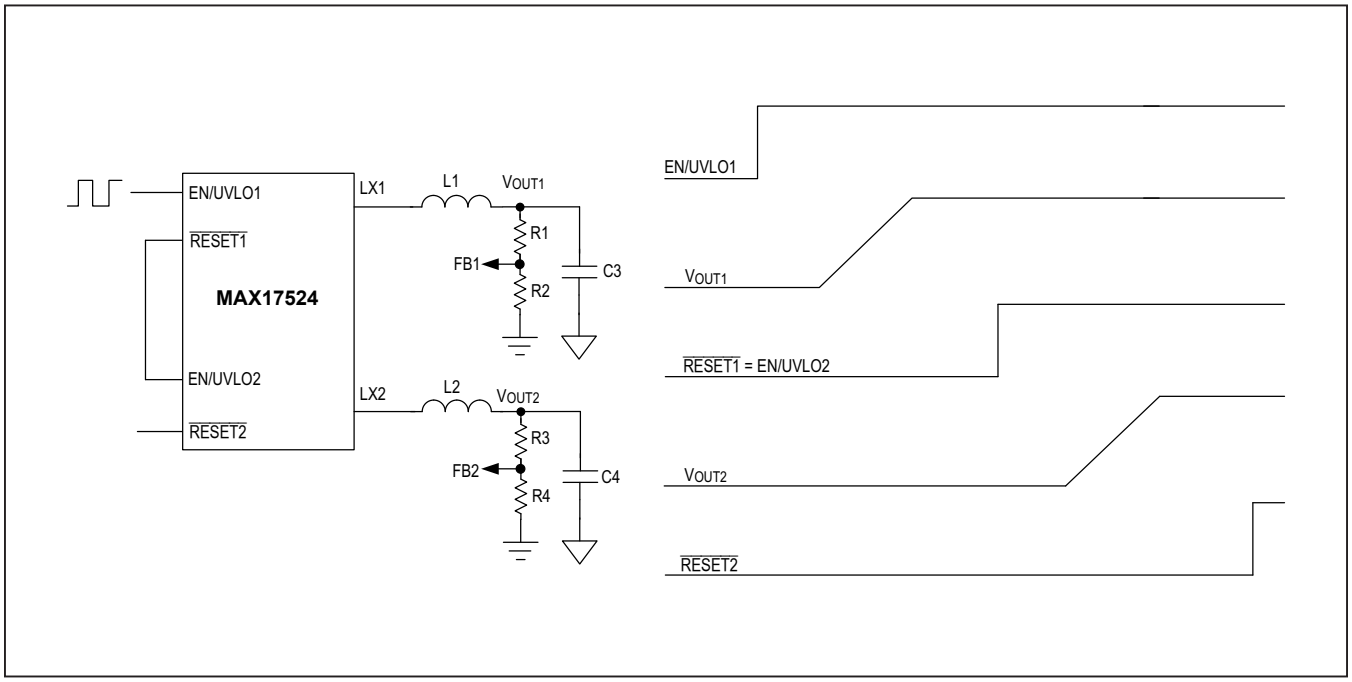
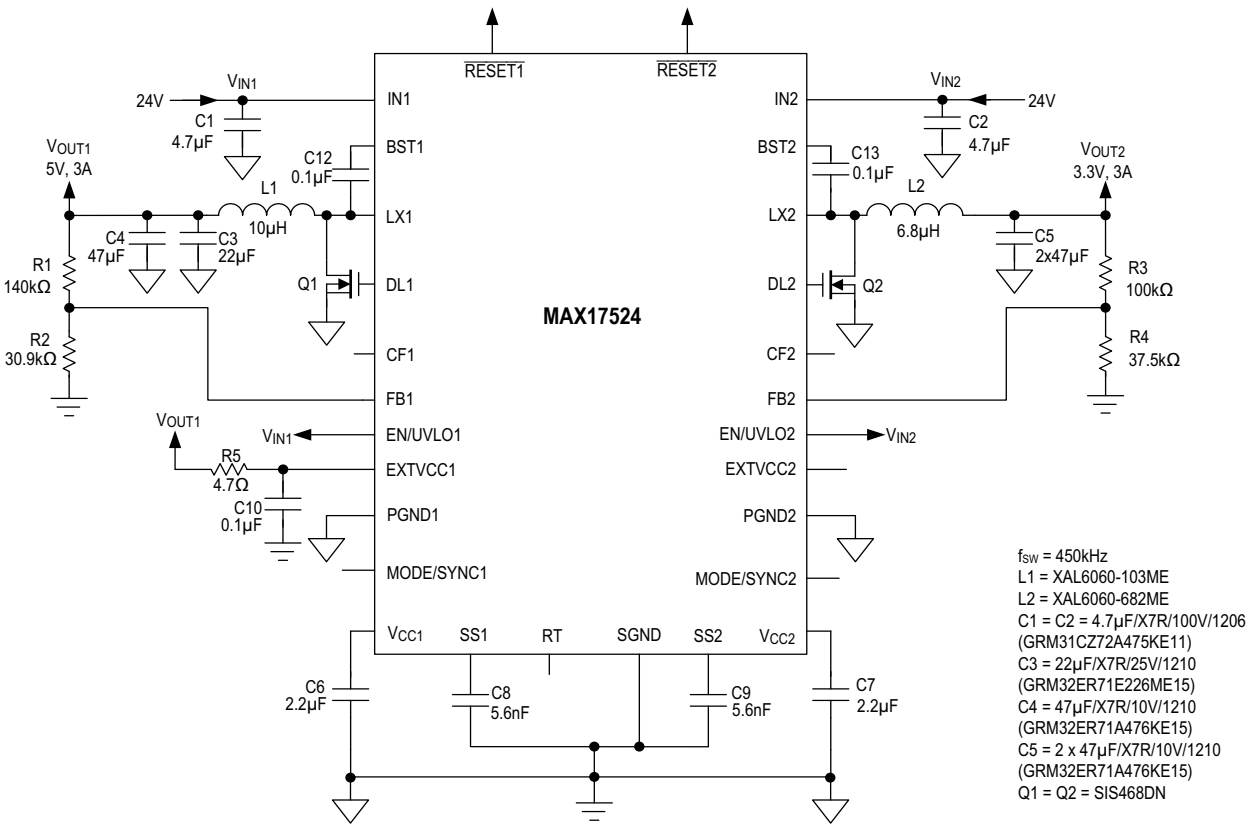


Figure 6. Output-Voltage Sequencing

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX17524ATJ+	-40°C to +125°C	32 TQFN (5mm x 5mm)

+Denotes a lead(Pb)-free/RoHS compliant package.