5.5V to 60V, 6A Current-Limiter with OV, UV, Reverse Protection, and Power Limit

MAX17526A/MAX17526B/ MAX17526C

General Description

The Olympus series of ICs are the industry's smallest and robust integrated system protection solutions. The MAX17526A adjustable power limiter offers a unique feature to limit power drawn from supplies or delivered to loads, amongst a host of protection features. These protection features include adjustable input overvoltage and undervoltage protection, positive and negative input voltage protection, overcurrent protection, reverse-current protection and overtemperature protection. The device features a built-in low R_{ON} (30mΩ typ) NFET, and an integrated gate drive for an optional external NFET.

The device highlights a power limit feature that allows programmed reduction in current limit, as an inverse function of an external voltage. Input or output power limit is achieved by limiting the current through the device as a function of input or output voltages.

Input undervoltage protection level is adjustable between 5.5V and 24V, and input overvoltage protection level is adjustable between 6V and 40V. The input undervoltage lockout (UVLO) threshold and overvoltage lockout (OVLO) threshold are adjusted using external resistors. The device offers a factory preset internal UVLO and OVLO thresholds at 12.4V (typ) and 36.2V (typ) respectively. The factory preset levels can be invoked by connecting the UVLO and/or the OVLO pins to GND.

The device features programmable current limit protection up to 6A. Current limit threshold is programmed by connecting a resistor from the SETI pin to GND. When the device current reaches the programmed threshold, the controller inside the device prevents further increase in current by modulating the internal NFET resistance. The device offers three different behavioral modes under current limited operation: Continuous mode, Autoretry mode, and Latch-off mode. The continuous current limit feature offers control of inrush current at startup while charging high capacitances at the output side. Two additional part options that feature a dual-stage current-limit mode, in which the current is continuously limited to 1.5x (MAX17526B) and 2.0x (MAX17526C), the programmed limits, are available upon request. The power limit feature is disabled in the MAX17526B/C part options. The voltage appearing on the SETI pin is proportional to the instantaneous current flowing through the device, and can be read by the supervisory system.

MAX17526A also offers reverse-current protection and input reverse voltage polarity protection when deployed with an external NFET, and built-in overtemperature protection. It is available in a 20-pin 5mm x 5mm TQFN-EP package. The device operates over -40°C to +125°C extended temperature range.

Benefits and Features

- Robust Protection Reduces System Downtime
  - Wide Input-Supply Range: +5.5V to +60V
  - Active Power Limit to Protect Supply or Load (MAX17526A)
  - Programmable Input Overvoltage Setting up to 40V
  - Negative Input Fault Tolerant (with External NFET)
  - Reverse Current Protection (with External NFET)
  - Low R_{ON} Internal NFET (30mΩ typ)
- Dual-Stage Current Limiting
  - 1.0x Startup Current (MAX17526A)
  - 1.5x Startup Current (MAX17526B)
  - 2.0x Startup Current (MAX17526C)
- Fast Startup and Brownout Recovery
  - Continuous Current-Limit During Startup
  - Thermal Foldback Current-Limit
- Flexible Design to Maximize Reuse and Minimize Requalification
  - Adjustable UVLO and OVLO Thresholds
  - Programmable Forward-Current Limit: 0.2A to 0.6A with ±10% Accuracy and 0.6A to 6.0A with ±8.5% Accuracy Over Full Temperature Range
  - Programmable Overcurrent Response: Continuous, Autoretry, and Latch-Off Modes
  - Logic Level and High-Voltage Enable Inputs (EN and $\overline{HVEN}$)
  - Protected External NFET Gate Drive
- Reduced Solution Footprint
  - 20-Pin 5mm x 5mm TQFN-EP Package
  - Integrated NFET for Common-Use Protection Requirements

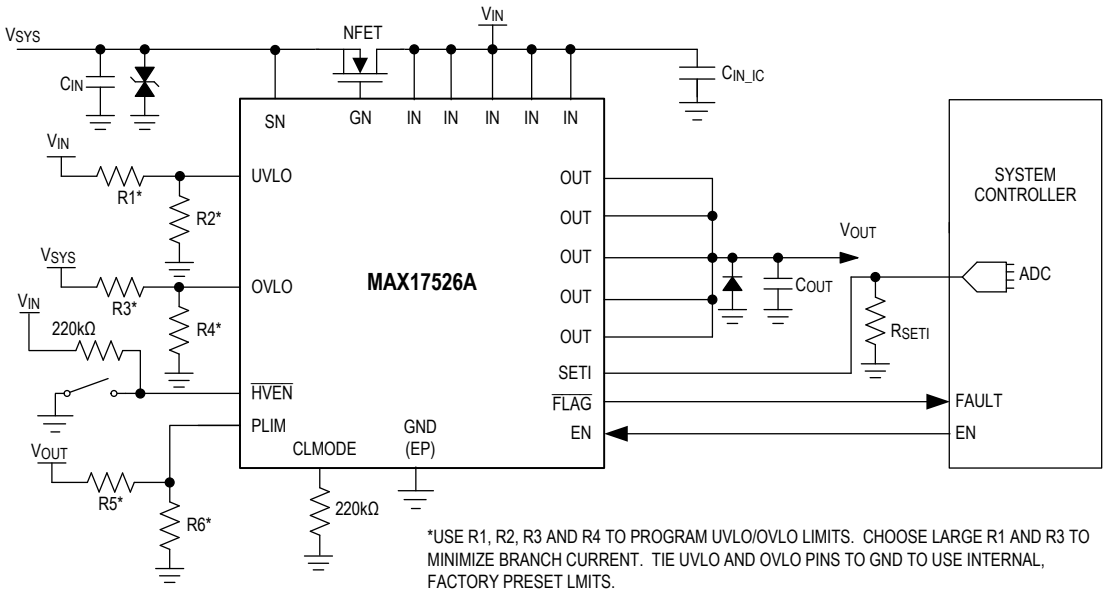
Applications

- Industrial Power Distribution Systems
- Control and Automation
- Motion Control Drives
- Human Machine Interfaces

Ordering Information appears at end of data sheet.

19-100358; Rev 4; 9/22

Typical Operating Circuit



*USE R1, R2, R3 AND R4 TO PROGRAM UVLO/OVLO LIMITS. CHOOSE LARGE R1 AND R3 TO MINIMIZE BRANCH CURRENT. TIE UVLO AND OVLO PINS TO GND TO USE INTERNAL, FACTORY PRESET LMITS.

*USE R5 AND R6 TO PROGRAM POWER LIMIT. TIE PLIM TO GND TO DISABLE POWER LIMIT FUNCTION.

Absolute Maximum Ratings

IN to GND (Note 1).....-0.3V to +64V
OUT to GND.....-0.3V to V_{IN} + 0.3V
$\overline{HVEN}$ to GND (Note 1).....-0.3V to V_{IN} + 0.3V
SN to GND .....-62V to +64V
GN to GND.....(SN - 0.3V) to (SN + 6V)
UVLO, OVLO, PLIM, $\overline{FLAG}$ to GND .....-0.3V to (V_{IN} + 0.3V)
EN, CLMODE to GND.....-0.3V to 6V
SETI to GND .....-0.3V to min (V_{IN} + 0.3V, 6V)
IN Current (DC).....6.51A
Continuous Power Dissipation (T_A = +70°C, TQFN derate 34.5mW/°C above +70°C.)..... 2758mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature..... -40°C to +150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: An external NFET or diode is required to achieve negative input protection.

Package Information

PACKAGE TYPE: 20-PIN TQFN	
Package Code	T2055+6C
Outline Number	**21-0140**
Land Pattern Number	**90-0010**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
IN Voltage Range	V_{IN}		5.5		60.0	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{IN} = V_{SN} = 24V		9.9	17.0	µA
		V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{IN} = V_{SN} = 40V		16	28	
Shutdown Output Current	I_{OFF}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{SN} = V_{IN} = V_{OUT} = 40V		80	170	µA
Supply Current	I_{IN}	V_{SN} = V_{IN} = V_{OUT} = 24V, $V_{\overline{HVEN}}$ = 0V		1.26	1.90	mA
UVLO, OVLO						
Internal Undervoltage-Trip Level	V_{UVLO}	V_{IN} rising, UVLO connected to GND	11.9	12.4	13.0	V
		V_{IN} falling, UVLO connected to GND	11.5	12.0	12.5	
UVLO Threshold Hysteresis				3		%
Internal Overvoltage-Trip Level	V_{OVLO}	V_{SN} rising, OVLO connected to GND	34.7	36.2	37.6	V
		V_{SN} falling, OVLO connected to GND	32.2	34.1	35.8	
OVLO Threshold Hysteresis				6		%
Undervoltage-Trip Level on Output	V_{UVLO_OUT}	V_{OUT} rising	12.2	12.8	13.4	V
		V_{OUT} falling, UVLO trip point	11.9	12.4	12.9	
External UVLO Set Voltage	V_{SET_UVLO}	UVLO rising	1.20	1.26	1.33	V
		UVLO falling	1.18	1.22	1.27	
External UVLO Select Voltage	V_{UVLO_SEL}		0.15	0.38	0.50	V
External UVLO Leakage Current	I_{UVLO_LEAK}		-250		+250	nA
External OVLO Set Voltage	V_{SET_OVLO}	OVLO rising	1.18	1.22	1.27	V
		OVLO falling	1.09	1.15	1.20	
External OVLO Select Voltage	V_{OVLO_SEL}		0.15	0.38	0.50	V
External OVLO Leakage Current	I_{OVLO_LEAK}		-250		+250	nA
External UVLO Adjustment Range		(Note 3)	5.5		24.0	V
External OVLO Adjustment Range		(Note 3)	6		40	V
GN, SN						
External NFET Gate Drive Voltage	V_{GN-SN}	V_{IN} < 8V, V_{EN} = 5V, no reverse condition	3.9	4.2	5.5	V
		V_{EN} = 5V, no reverse condition	4.98	5.25	5.60	
Gate Active Pullup Current		V_{EN} = 5V, V_{GN} = V_{SN} , no reverse condition	9	18	28	µA
Gate Active Pulldown Resistance		V_{EN} = 5V, reverse condition		140		mΩ
Shutdown Gate Pulldown Resistance		V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{GN} - V_{SN} = 1.5V		2.7	6.1	kΩ
		V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{GN} - V_{SN} = 0.5V		3.9	8.0	MΩ

Electrical Characteristics (continued)

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} ≥ 10V, T_A = +25ºC		30	42	mΩ
Current-Limit Adjustment Range	I_{LIM}		0.2		6.0	A
Current-Limit Accuracy	I_{LIM_ACC}	0.6A ≤ I_{LIM} ≤ 6A (T_A = +25°C), V_{PLIM} < V_{PLIM_TH}	-6		+6	%
		0.2A ≤ I_{LIM} < 0.6A, V_{PLIM} < V_{PLIM_TH}	-10		+10	
		0.6A ≤ I_{LIM} ≤ 6A, V_{PLIM} < V_{PLIM_TH}	-8.5		+8.5	
Overcurrent Protection Threshold	I_{OCP}	(Note 8)	15.0	24.0	34.5	A
$\overline{FLAG}$ Assertion Drop-Voltage Threshold	V_{FA}	Increase in (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V		490		mV
Slow Reverse-Current-Blocking Threshold	V_{RIB_SLOW}	V_{IN} - V_{OUT}, falling	-0.5	-5.4	-10.5	mV
Slow Reverse-Current-Blocking Response Time	t_{RIB_SLOW}	(Note 4)		17	30	µs
Fast Reverse-Current-Blocking Threshold	V_{RIB_FAST}	V_{IN} - V_{OUT}, falling	-78	-98	-118	mV
Fast Reverse-Current-Blocking Response Time	t_{RIB_FAST}	(Note 5, Note 8), C_{GS} = 10nF		108	135	ns
Reverse-Current-Blocking Rising Threshold	V_{RIB_RISING}	V_{SN} - V_{OUT}, rising	65	100	135	mV
Reverse Output Current	I_{OUT_REV}	V_{SN} = 0V, V_{OUT} = 24V, IN floating		3.20	5.11	mA
PLIM						
PLIM Limit Threshold Voltage	V_{PLIM_TH}		0.867	1.009	1.151	V
PLIM Limit Operation Range			V_{PLIM_TH}		3 x V_{PLIM_TH}	
SETI						
R_{SETI} x I_{LIM}	V_{RI}	V_{PLIM} < V_{PLIM_TH}		1.5		V
Current-Mirror Output Ratio	C_{IRATIO}			25000		A/A
LOGIC INPUT ($\overline{HVEN}$, CLMODE, EN)						
$\overline{HVEN}$ Threshold Voltage	$V_{\overline{HVEN}\_TH}$	$\overline{HVEN}$ rising	1.05	2.00	3.30	V
		$\overline{HVEN}$ falling	1.0	1.9	2.8	
$\overline{HVEN}$ Threshold Hysteresis				5		%
$\overline{HVEN}$ Input Leakage Current	$I_{\overline{HVEN}\_LEAK}$	$V_{\overline{HVEN}}$ = 60V		51	72	µA
EN Input-Logic High	V_{IH}		1.4			V
EN Input-Logic Low	V_{IL}				0.4	V
EN Input Leakage Current	I_{EN_LEAK}	V_{EN} = 0V, 5V	-1		+1	µA

Electrical Characteristics (continued)

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLMODE Input-Logic High	V_{CLMODE_IH}		3.59	4.00	4.52	V
CLMODE Input-Logic Low	V_{CLMODE_IL}		0.49	0.78	1.01	V
CLMODE Pullup Current			5.3	10.0	14.6	µA
LOGIC OUTPUT ($\overline{FLAG}$)						
Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
Input Leakage Current		V_{IN} = 5.5V, $\overline{FLAG}$ open drain off			1	µA
$\overline{FLAG}$ Protection Current		$\overline{FLAG}$ open drain on	4			mA
TIMING CHARACTERISTICS (NOTE 6)						
Switch Turn-On Time	t_{ON}	V_{IN} = 24V, switch OFF to ON, R_{LOAD} = 240Ω, I_{LIM} = 1A, C_{OUT} = 4.7µF, V_{OUT} from 20% to 80% of V_{IN}		68		µs
Fault Recovery nFET Turn-On Time	t_{ON_NFET}	Turn-on delay after fault timers expired		200	500	µs
Fault Recovery External NFET Turn-On Time	t_{ON_EXNFET}	V_{OUT} > V_{UVLO_OUT}, turn-on delay of external NFET after fault timers expired	1.09	1.20	1.32	ms
OVP Switch Response Time	t_{OVP_RES}			3		µs
Overcurrent Protection Response time	t_{OCP_RES}	I_{LIM} = 5A, I_{OUT} step from 3A to 30A. Time to turn the switch off.		3		µs
Startup Timeout	t_{STO}	Initial start current-limit foldback timeout (Figure 5)	1090	1200	1320	ms
Startup Initial Time	t_{STI}	(Figure 5)	21.8	24.0	26.4	ms
IN Debounce Time	t_{DEB}	Additional turn-on delay if V_{OUT} < V_{UVLO_OUT}, see Figures 5–8	1.09	1.20	1.32	ms
Blanking Time	t_{BLANK}	Figures 7 and 8	21.8	24.0	26.4	ms
Autoretry Time	t_{RETRY}	Figure 7 (Note 7)	654	720	792	ms
THERMAL PROTECTION						
Thermal Foldback	$T_{J(FB)}$			150		°C
Thermal Shutdown	T_J			165		°C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			10		°C

Note 2: All devices are 100% production-tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design; not production tested.

Note 3: Not production-tested, user-adjustable. See the *Overvoltage Lockout (OVLO)* and *Undervoltage Lockout (UVLO)* sections.

Note 4: Time from V_{IN} - V_{OUT} voltage transition from 200mV to -50mV until GN pin voltage falls to V_{SN} + 1V (Figure 1).

Note 5: Time from V_{IN} - V_{OUT} voltage transition from 200mV to -250mV until GN pin voltage falls to V_{SN} + 1V (Figure 2).

Note 6: All timing is measured using 20% and 80% levels, unless otherwise specified.

Note 7: The autoretry time-to-blanking time ratio is fixed and is equal to 30.

Note 8: Guaranteed by design, not production tested.

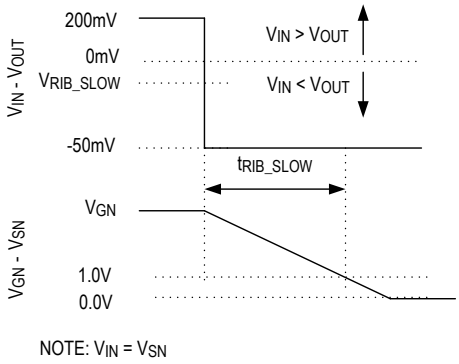


Figure 1. Slow Reverse-Current-Blocking Response Time

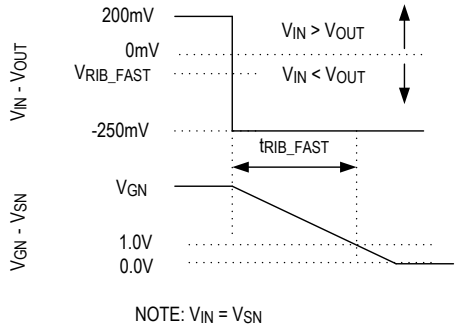
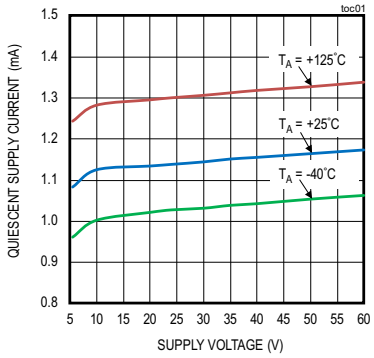


Figure 2. Fast Reverse-Current-Blocking Response Time

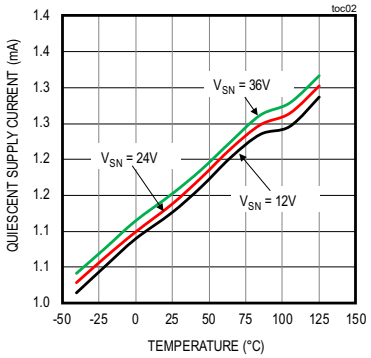
Typical Operating Characteristics

(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

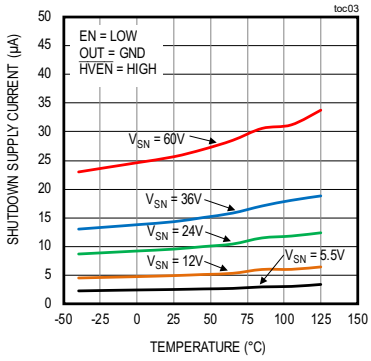
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



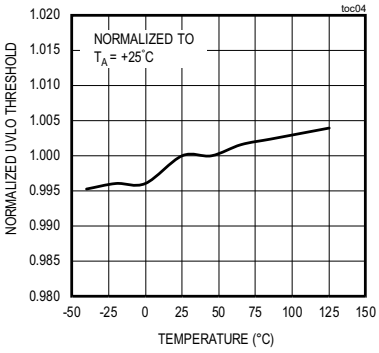
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



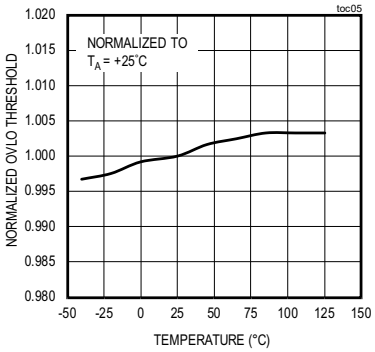
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



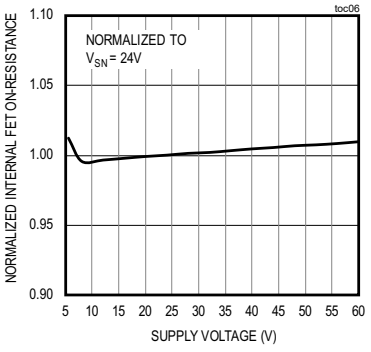
NORMALIZED UVLO THRESHOLD vs. TEMPERATURE



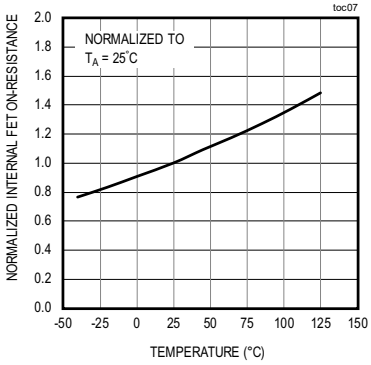
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



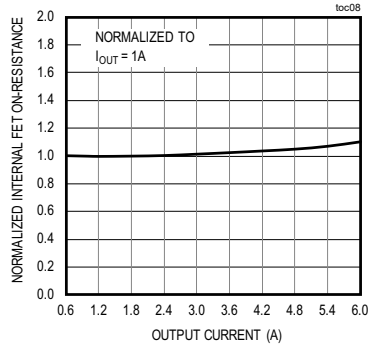
NORMALIZED INTERNAL FET ON-RESISTANCE vs. SUPPLY VOLTAGE



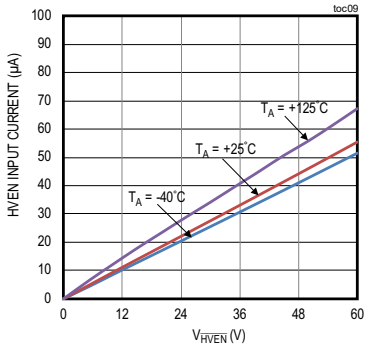
NORMALIZED INTERNAL FET ON-RESISTANCE vs. TEMPERATURE



NORMALIZED INTERNAL FET ON-RESISTANCE vs. OUTPUT CURRENT



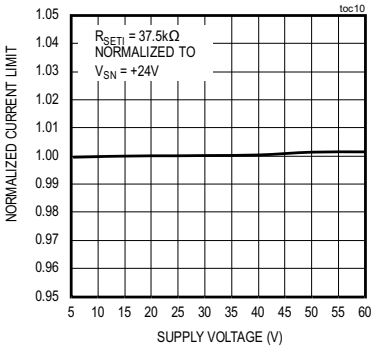
$\overline{HVEN}$ INPUT CURRENT vs. $V_{\overline{HVEN}}$



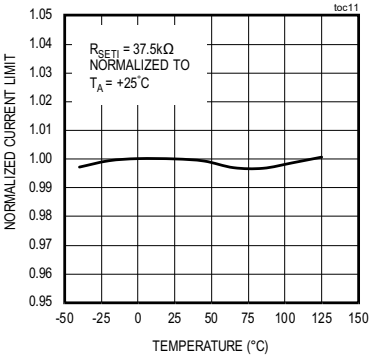
Typical Operating Characteristics (continued)

(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

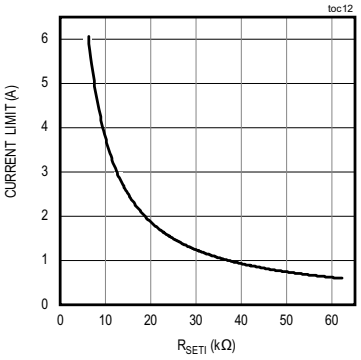
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



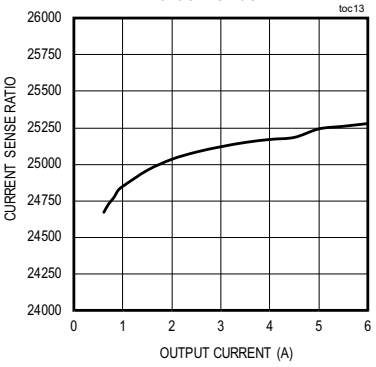
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



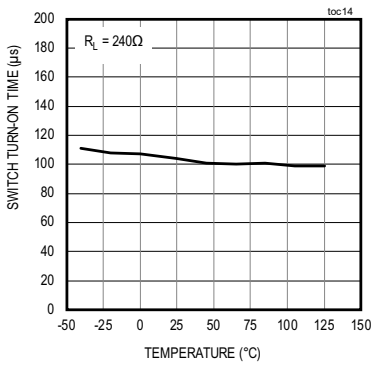
CURRENT LIMIT vs. R_{SETI}



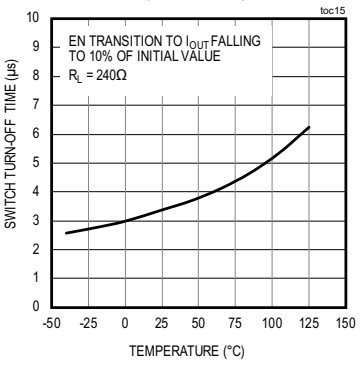
CURRENT SENSE RATIO vs. OUTPUT CURRENT



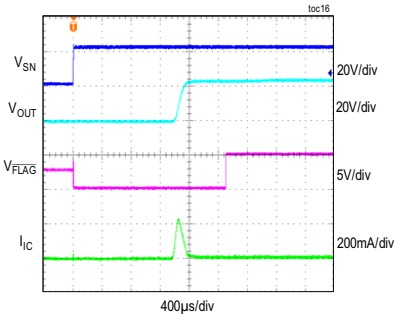
SWITCH TURN-ON TIME vs. TEMPERATURE



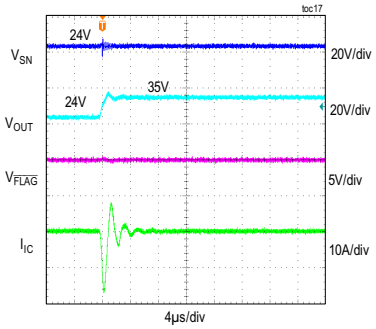
SWITCH TURN-OFF TIME vs. TEMPERATURE



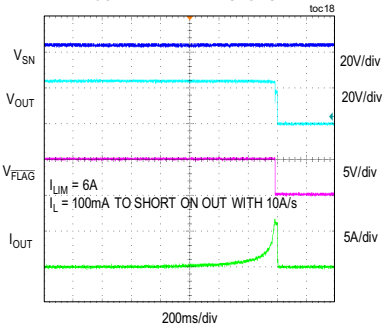
POWER-UP RESPONSE



REVERSE-BLOCKING RESPONSE



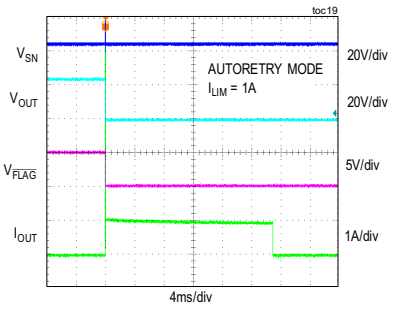
CURRENT-LIMIT RESPONSE



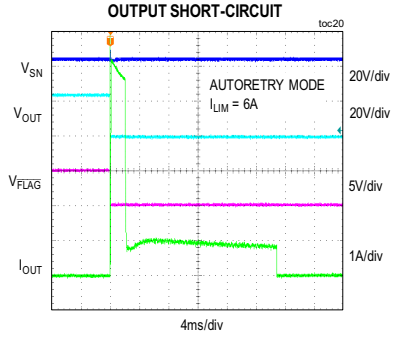
Typical Operating Characteristics (continued)

(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

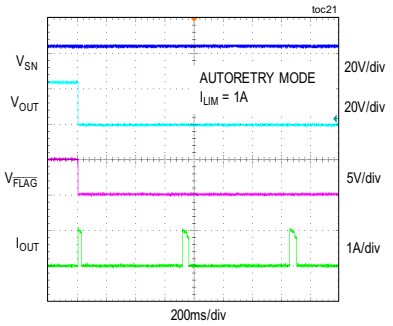
OUTPUT SHORT-CIRCUIT RESPONSE



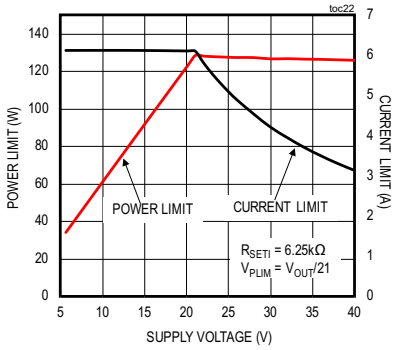
THERMAL FOLDBACK DUE TO OUTPUT SHORT-CIRCUIT



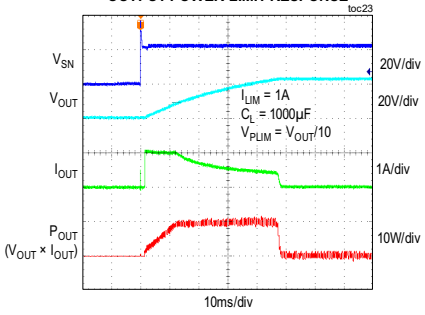
AUTORETRY TIME (t_{RETRY})



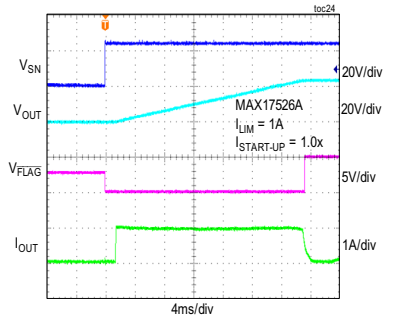
CURRENT LIMIT, POWER LIMIT vs. SUPPLY VOLTAGE



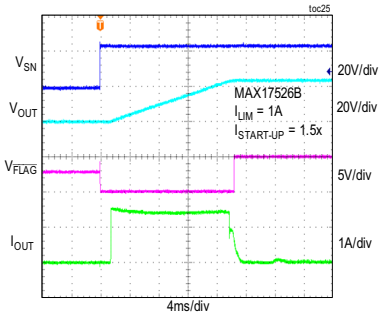
OUTPUT POWER-LIMIT RESPONSE



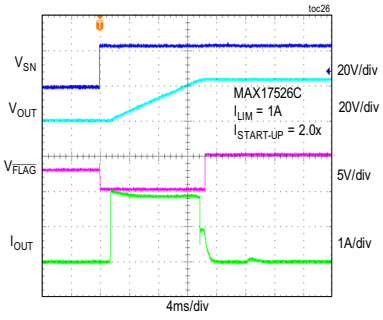
POWER-UP RESPONSE WITH 1000µF CAPACITOR AT NO LOAD



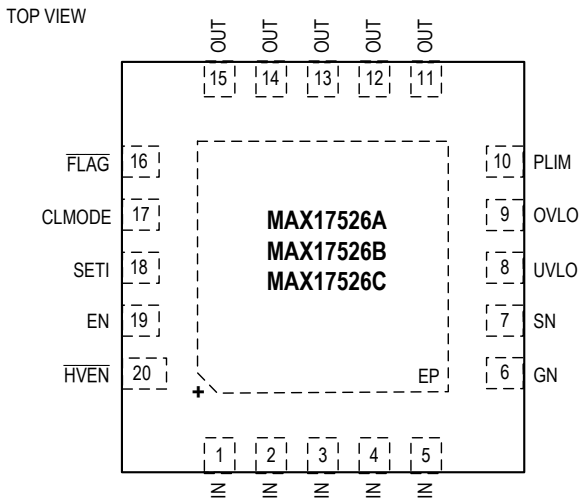
POWER-UP RESPONSE WITH 1000µF CAPACITOR AT NO LOAD



POWER-UP RESPONSE WITH 1000µF CAPACITOR AT NO LOAD



Pin Configuration

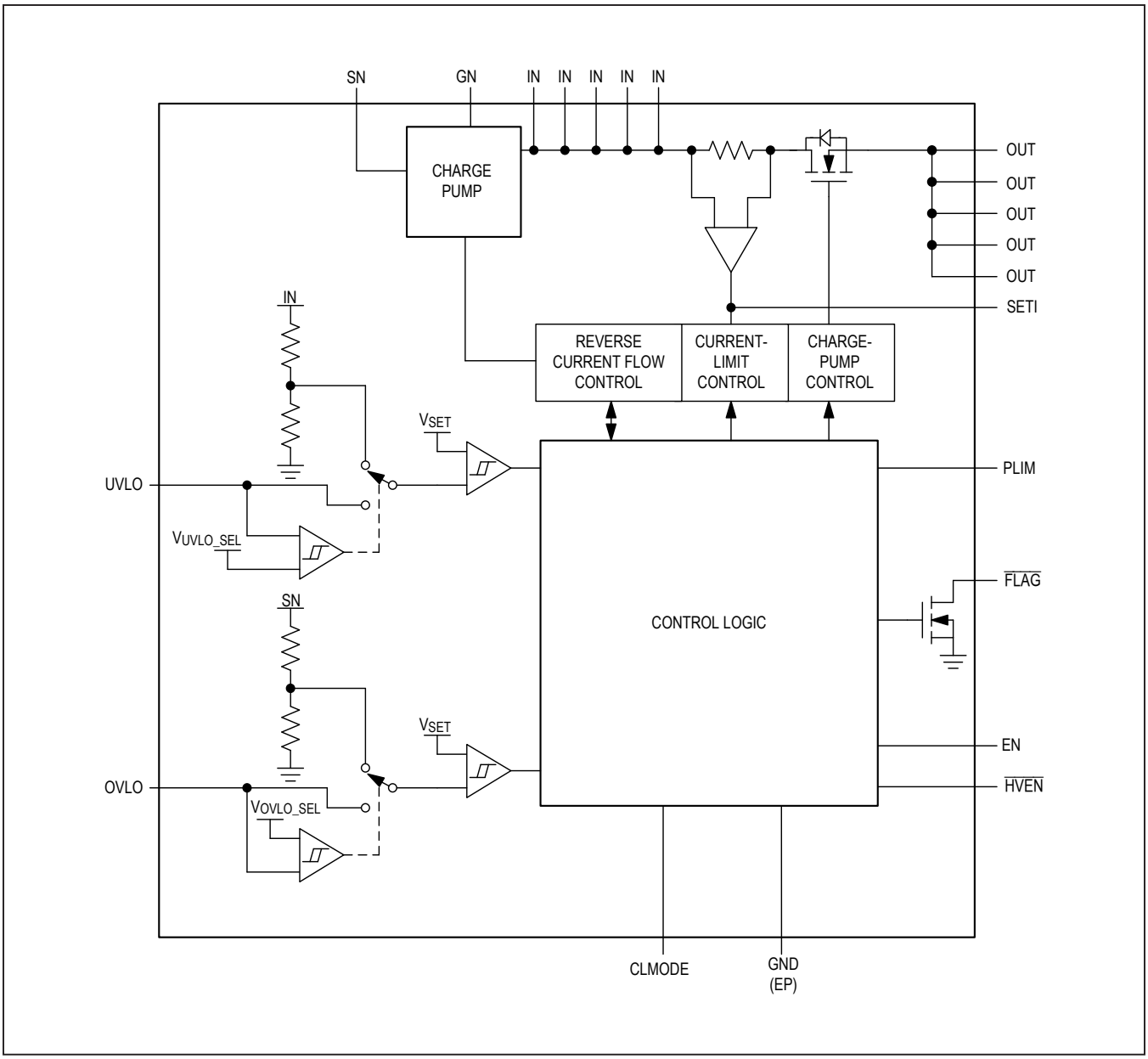


TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION
1–5	IN	Input Pins. Bypass IN to GND with a 1µF cermic capacitor. For Hot Plug-In applications, see the *Applications Information* section.
6	GN	Gate Driver Output for External NFET.
7	SN	Return for External NFET Gate Drive and Input Voltage Sense Pin. Connect to source of external NFET as shown in the *Typical Operating Circuit*. Bypass SN to GND with a 4.7µF capacitor. SN serves as the undervoltage/overvoltage sensed input when preprogrammed UVLO/OVLO is used. Connect SN to IN if external NFET is not used.
8	UVLO	UVLO Adjustment Pin. Connect UVLO to GND to use the default internal UVLO threshold. Connect resistive potential divider from SN/IN to GND to set the UVLO threshold externally and override the preset internal UVLO threshold.
9	OVLO	OVLO Adjustment Pin. Connect OVLO to GND to use the default internal OVLO threshold. Connect resistive potential divider from SN/IN to GND to set the OVLO threshold externally and override the preset internal OVLO threshold.
10	PLIM	Power Limit Adjustment Pin. Connect PLIM to an external resistive potential divider to define a threshold at which the power limit feature starts reducing the current-limit threshold. Connect PLIM to GND to disable this feature and have the current-limit set only by the resistor placed on SETI.
11-15	OUT	Output Pins. For a long output cable or inductive load, see the *Applications Information* section.
16	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when: • The (V_{IN} - V_{OUT}) voltage exceeds V_{FA}. • Thermal shutdown is active. • Input voltage falls below UVLO threshold or rises above OVLO threshold. • R_{SETI} is less than 3.2kΩ.
17	CLMODE	Current-Limit Mode Selector Pin. Leave CLMODE unconnected for Continuous mode. Connect CLMODE to GND for Autoretry mode. Connect a 220kΩ resistor between CLMODE and GND for Latch-off mode.
18	SETI	Overcurrent Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set overcurrent limit. See the *Setting the Current-Limit Threshold* section. Do not connect more than 30pF to SETI.
19	EN	Active-High Enable Input. See Table 1.
20	$\overline{HVEN}$	60V Capable Active-Low Enable Input. See Table 1.
-	GND/EP	Ground/Exposed Pad. Connect GND/EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17526A EV kit data sheet for a reference layout design.

Functional Diagrams



Detailed Description

The MAX17526A offers adjustable protection boundaries for systems against input voltage faults, and overcurrent fault, in addition to a programmable power limiting function. Input voltage faults (with positive polarity) are protected up to +60V, by an internal NFET featuring low ON-resistance (30mΩ typ). The device features fixed or programmable overvoltage lockout (OVLO) and undervoltage lockout (UVLO) thresholds by using internal or external voltage-dividers. Factory preset internal fixed thresholds may be invoked by connecting the OVLO and/or UVLO pin(s) to GND. Input undervoltage protection can be programmed between 5.5V and 24V, while the overvoltage protection can be independently programmed between 6V and 40V.

Input reverse polarity protection is realized using an external NFET that is controlled by MAX17526A. The magnitude of reverse polarity voltage protection is dependent on the operating load bus voltage (V_{OUT}) and the voltage blocking capability of the external NFET. Example: for protection down to -55V input range with V_{OUT} = 30V, an external NFET rated at 85V is needed. The external NFET is also needed for the optional reverse-current protection. If reverse polarity protection and reverse-current protection are not needed, SN must be connected to IN and GN must be left floating.

The current-limit of the device is programmed by connecting a resistor from the SETI pin to GND. The current limit can be programmed from 0.2A to 6.0A. When the current through the device reaches or exceeds the set current limit, the resistance of the internal NFET is modulated to limit the current. The device offers three current limit behavioral modes: Continuous, Auto-retry, and Latch-off modes.

The SETI pin presents a current proportional to the device current, under normal operation. Together with the current limit program resistor (between SETI and GND), the SETI pin presents a voltage that is proportional to the device current. This voltage may be read by a monitoring system for recording instantaneous current of the device.

Power limit function is realized either at the input supply side or output load side, by sampling the input or output voltage, through a potential divider connecting to the PLIM pin. The power limit feature reduces the programmed current limit when the external voltage increases above the programmed threshold.

The device can be turned On or Off through two independent enable inputs, EN and $\overline{HVEN}$, by a master supervisory system. This allows the master supervisory system to Turn On or Off power delivery to connected loads.

The device offers a status announcement signal ($\overline{FLAG}$) to indicate operational and fault signals. $\overline{FLAG}$ is an open drain pin, and requires an external pullup resistor to the appropriate system interface voltage. The device also offers internal thermal shutdown protection against excessive power dissipation.

Undervoltage Lockout (UVLO)

The device has a 12.4V (typ) preset UVLO threshold on the IN pin when the voltage at the UVLO pin is less than the external UVLO select threshold (V_{UVLO_SEL}). Connect the UVLO pin to GND to select the preset UVLO threshold. If the voltage at the UVLO pin rises above V_{UVLO_SEL}, the device enters adjustable UVLO mode. The device has a UVLO adjustment range from 5.5V to 24V. Connect an external resistive potential divider to the UVLO pin as shown in the *Typical Operating Circuit* to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. The recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{SET} \times \left[1 + \frac{R1}{R2}\right]$$

where V_{SET} = 1.22V.

Alternatively, R2 can be calculated using the following equation:

$$R2 = \frac{R1}{\left(\frac{V_{UVLO}}{V_{SET}} - 1\right)}$$

When the voltage on the UVLO pin is below V_{SET}, the internal NFET remains turned Off and $\overline{FLAG}$ is asserted. When the UVLO condition is removed, the device takes input debounce time (t_{DEB}) to start the switch turn-on process if V_{OUT} is below the V_{UVLO_OUT} threshold. The internal NFET is turned on after fault recovery internal NFET turn-on time (t_{ON_NFET}), and the external NFET is turned on after fault recovery external NFET turn-on time ($t_{ON\_EXTNFET}$) and $\overline{FLAG}$ is deasserted.

Overvoltage Lockout (OVLO)

The device has a 36.2V (typ) preset OVLO threshold on the SN pin when the voltage at the OVLO pin is less than the external OVLO select threshold (V_{OVLO_SEL}). Connect the OVLO pin to GND to select the preset OVLO threshold. If the voltage at the OVLO pin rises above V_{OVLO_SEL}, the device enters adjustable OVLO mode. The device has an OVLO adjustment range from 6V to 40V. Connect an external resistive potential divider to the OVLO pin as shown in the *Typical Operating Circuit* to adjust the OVLO threshold voltage. Use the following equation to adjust the OVLO threshold. The recommended value of R3 is 2.2MΩ.

$$V_{OVLO} = V_{SET} \times \left[1 + \frac{R3}{R4}\right]$$

where V_{SET} = 1.22V.

Alternatively, R4 can be calculated using the following equation:

$$R4 = \frac{R3}{\left(\frac{V_{OVLO}}{V_{SET}} - 1\right)}$$

The OVLO reference voltage (V_{SET}) is set at 1.22V. If the voltage at the OVLO pin exceeds V_{SET}, the switch is turned off and $\overline{FLAG}$ is asserted. When the OVLO condition is removed, the device takes input debounce time (t_{DEB}) to start the switch turn-on process if V_{OUT} is below the V_{UVLO_OUT} threshold. The internal NFET is turned on after fault recovery internal NFET turn-on time (t_{ON_NFET}), and the external NFET is turned on after fault recovery external NFET turn-on time ($t_{ON\_EXTNFET}$) and the $\overline{FLAG}$ is deasserted. Figure 3 depicts typical behavior in overvoltage conditions.

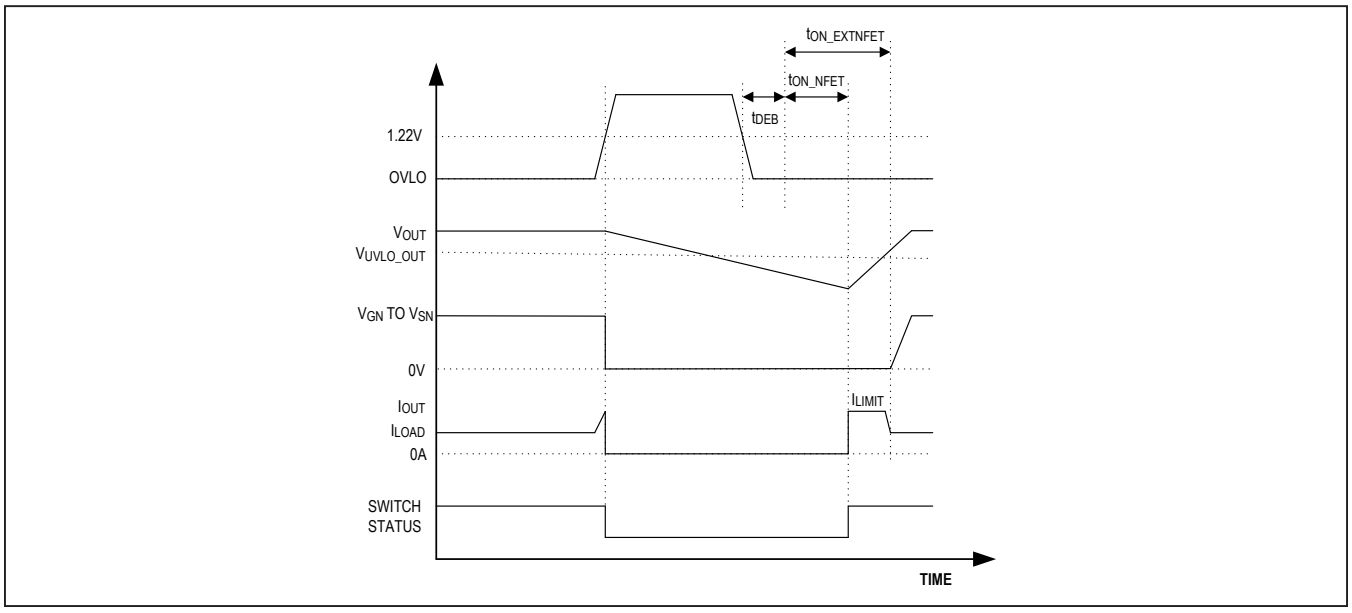


Figure 3. Overvoltage-Fault Timing Diagram

Input Debounce Protection

The device features input debounce protection. The device starts operation (turn on the internal NFET) only if the input voltage is higher than the UVLO threshold for a period greater than the debounce time (t_{DEB}). In case the voltage at IN falls below the UVLO threshold before t_{DEB} has passed, the switch remains off. If the voltage at OUT is already above the undervoltage trip level on output (V_{UVLO_OUT}) when the device is turned on through UVLO/OVLO conditions, there is no t_{DEB} time. This is due to the device already being out of the power-on reset POR condition with OUT above V_{UVLO_OUT}. When the device is turned on through EN or $\overline{HVEN}$, the t_{DEB} time is always present. Figure 4 depicts typical debounce timing diagram.

Switch Control

The device is enabled or disabled through two independent enable inputs, $\overline{HVEN}$ and EN. $\overline{HVEN}$ is a high-voltage-capable input, accepting signals up to 60V or V_{IN}, whichever is lower. EN is a low-voltage input, accepting a maximum voltage of 5.5V. The device can be used to turn on or off power delivery to connected loads using the EN or $\overline{HVEN}$ pins. Toggling $\overline{HVEN}$ or EN resets the fault condition once a short circuit is detected and the device shuts down. Table 1 shows the truth table of the enable inputs to control the switch turn on or off status.

Table 1. Enable Inputs

$\overline{HVEN}$	EN	SWITCH STATUS
0	0	ON
0	1	ON
1	0	OFF
1	1	ON

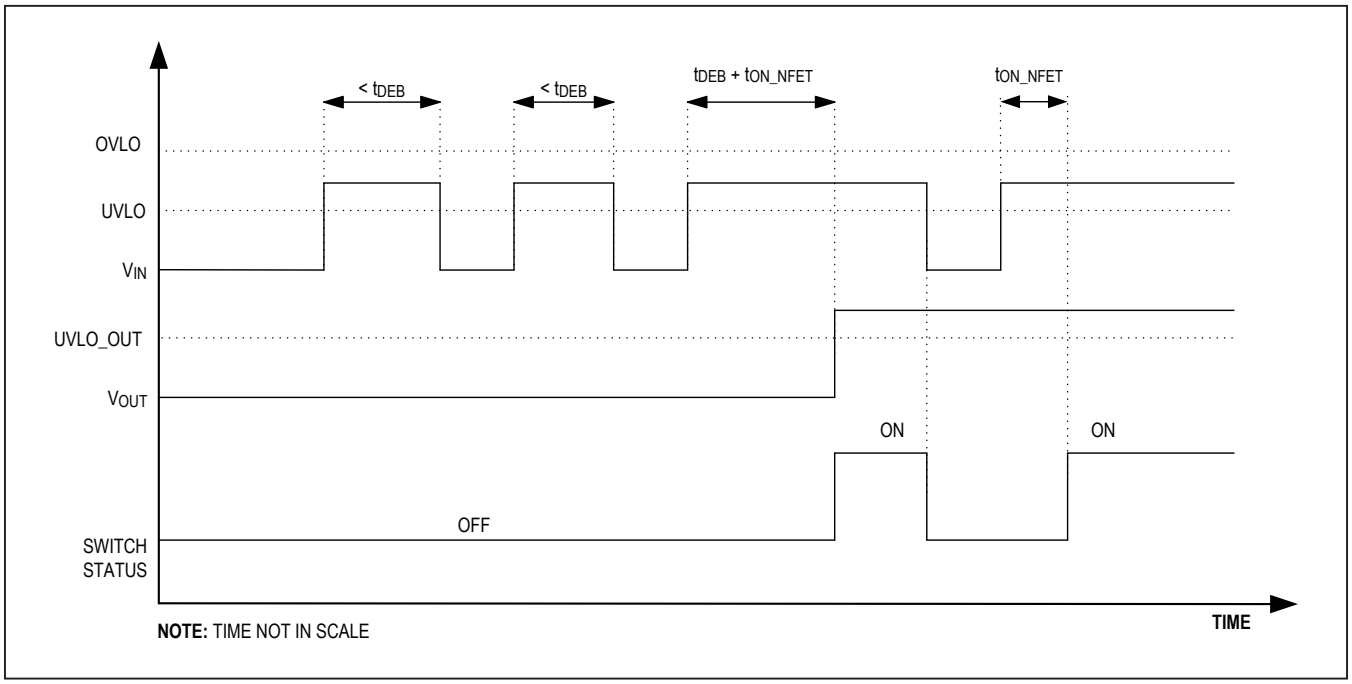


Figure 4. Debounce Timing Diagram

Startup Control

The device features a startup sequence that continuously limits the current to the set current limit during the startup initial time (t_{STI}), allowing large capacitors present on the output of the switch to be rapidly charged. If the temperature of device rises to the thermal foldback threshold ($T_{J(FB)}$), the device enters power-limiting mode. In this mode, the device thermally regulates the current through the switch to protect itself while still delivering as much current as possible to the output regardless of the current-limit type selected. If the output is not charged within the startup timeout period (t_{STO}), the switch turns off and IN, EN, or $\overline{HVEN}$ must be toggled to resume normal operation. The t_{STO} timeout period is also applied when there is a restart after a turn-off event caused by UVLO or OVLO. If the output is not charged to (V_{IN} - V_{FA}) level during this time, the device turns off and IN, EN, or $\overline{HVEN}$ must be toggled to resume normal operation.

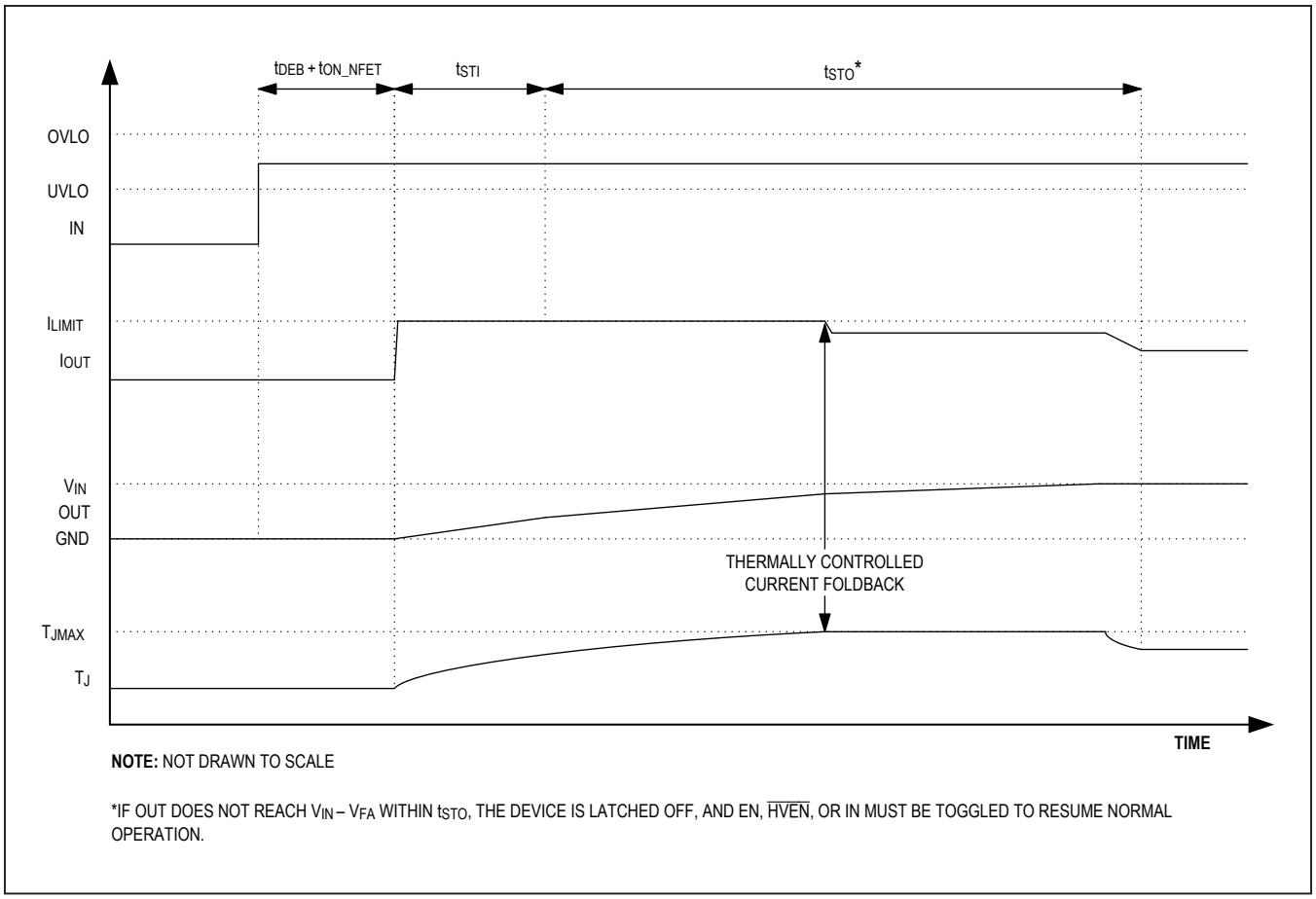


Figure 5. Startup Timing Diagram

Setting the Current-Limit Threshold

Connect a resistor between SETI and GND to program the current-limit threshold in the device. Use the following equation to calculate current-limit setting resistor:

$$R_{SETI}\ (k\Omega) = \frac{37500}{I_{LIM}\ (mA)}$$

where I_{LIM} is the desired current limit in mA.

Do not use a R_{SETI} smaller than 6kΩ. Table 2 shows current-limit thresholds for different resistor values.

The device read-out of the current flowing into the IN pin. A current mirror, with a ratio of C_{IRATIO}, is implemented, using a current-sense auto-zero operational amplifier. The mirrored current flows out through the SETI pin, into the external current-limit resistor. The voltage on the SETI pin provides information about the IN current with the following relationship:

$$I_{IN-OUT}\ (mA) = \frac{V_{SETI}\ (V)}{R_{SETI}\ (k\Omega)} \times C_{IRATIO}$$

If SETI is left unconnected, $V_{SETI} \geq 1.5V$. The current regulator does not allow any current to flow. The device performs a check on the SETI pin for the first time it exits a shutdown condition. If the resistor placed on SETI is below 3.2kΩ, the switch remains off and the $\overline{FLAG}$ pin asserts. For best damped measurement, the capacitance on the SETI pin shall be limited to 30pF.

Table 2. Current-Limit Threshold vs. SETI-Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT (A)
187.50	0.2
62.50	0.6
37.50	1.0
25.00	1.5
18.75	2.0
15.00	2.5
12.50	3.0
10.71	3.5
9.37	4.0
8.33	4.5
7.50	5.0
6.82	5.5
6.25	6.0

Current-Limit Type Select

The MAX17526A features three selectable current-limiting modes. During power-up, the device defaults to continuous mode and follows the procedure defined in the *Startup Control* section. Once the part has been successfully powered on and t_{STO} has expired, the device senses the condition of CLMODE. The CLMODE pin is used to program the overcurrent response of the device in one of the following three modes:

- Autoretry mode: CLMODE is connected to GND
- Continuous mode: CLMODE pin is left unconnected
- Latch-off mode: a 220kΩ resistor is connected between CLMODE and GND

In addition to the selectable current-limit modes, the device has a protection feature against a severe overload condition. If the output current exceeds the overcurrent protection threshold (I_{OCP}) of 24A (typ), the device turns off the internal and external NFETs. The off duration depends on the fault condition that occurs after the FETs turn off, with the shortest one being < 500µs (t_{ON_NFET} max) that occurs if there is no fault and $V_{OUT} > V_{OUT\_UVLO}$. If the overload is still present when the device turns on in current-limit, it behaves according to the current-limit type selected.

Continuous Current Limit

In continuous current-limit mode, when current through the device reaches the current limit threshold, the device limits the current to the programmed current limit. The $\overline{FLAG}$ pin asserts when the voltage drop across the switch rises above V_{FA}, and deasserts when it falls below V_{FA}.. Figure 6 depicts typical behavior in continuous current-limit mode.

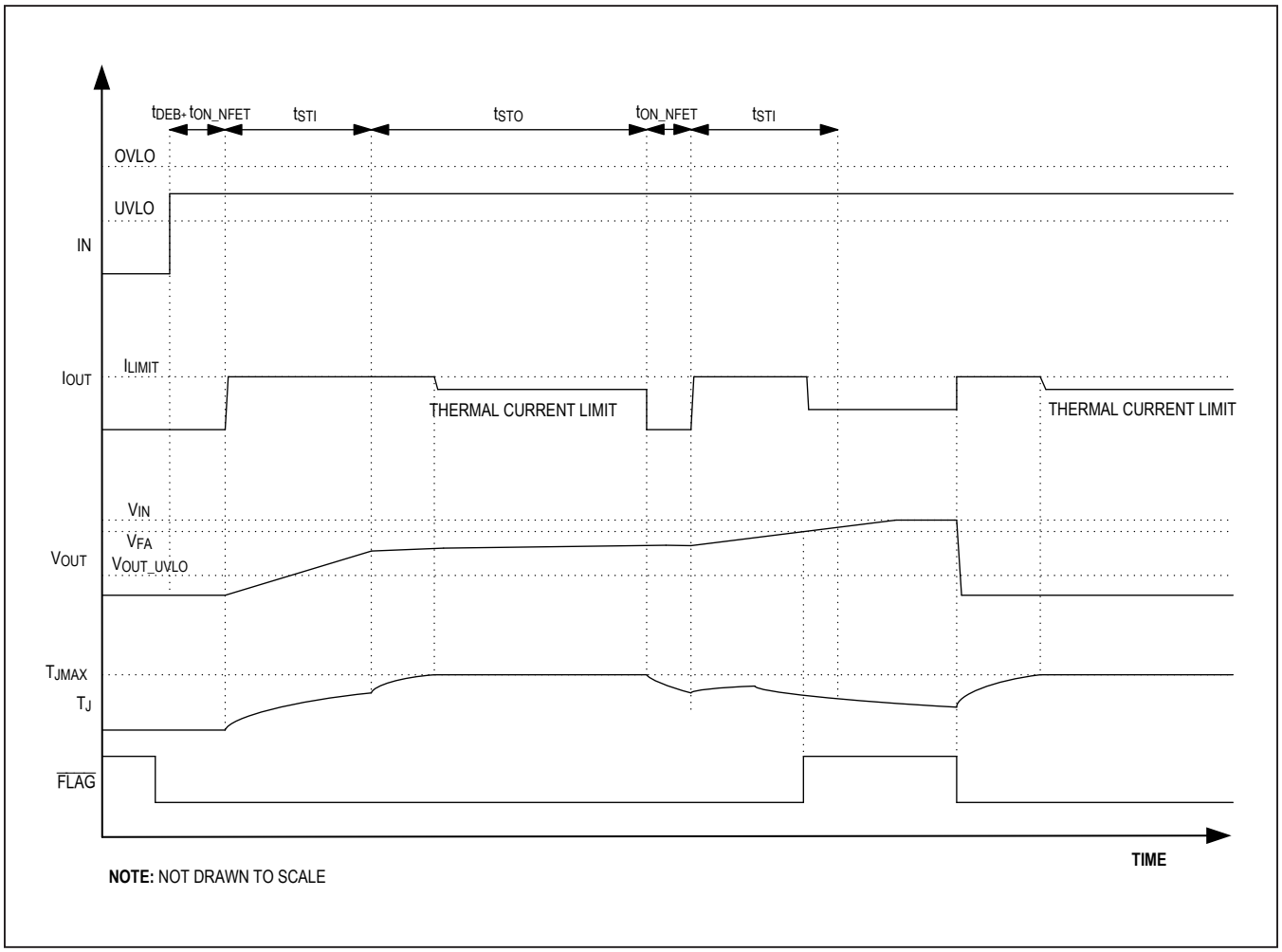


Figure 6. Continuous-Fault Timing Diagram

Autoretry Current Limit

In autoretry current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts when the voltage drop across the switch rises above V_{FA} and deasserts when it falls below V_{FA}. The timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed. A retry time delay (t_{RETRY}) starts immediately after t_{BLANK} has elapsed. During t_{RETRY} time, the switch remains off. Once t_{RETRY} has elapsed, the switch is turned back on again. If the fault still exists, the cycle is repeated and the $\overline{FLAG}$ pin remains asserted. If the overcurrent condition is resolved, the switch stays on.

The autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is on during t_{BLANK} time, the supply current is held at the current-limit. During t_{RETRY} time, there is no current through the switch. Thus, output current is much less than the programmed current-limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK} + t_{STI} \times K}{t_{BLANK} + t_{RETRY} + t_{STI}}\right]$$

where,

K = 1 for MAX17526A,

K = 1.5 for MAX17526B, and

K = 2 for MAX17526C

With a 24ms (typ) t_{BLANK}, 24ms (typ) t_{STI}, K = 1 and 720ms (typ) t_{RETRY}, the duty cycle is 6.25%, resulting in 93.75% power reduction when compared to the switch being on the entire time. Figure 7 depicts typical behavior in the autoretry current-limit mode.

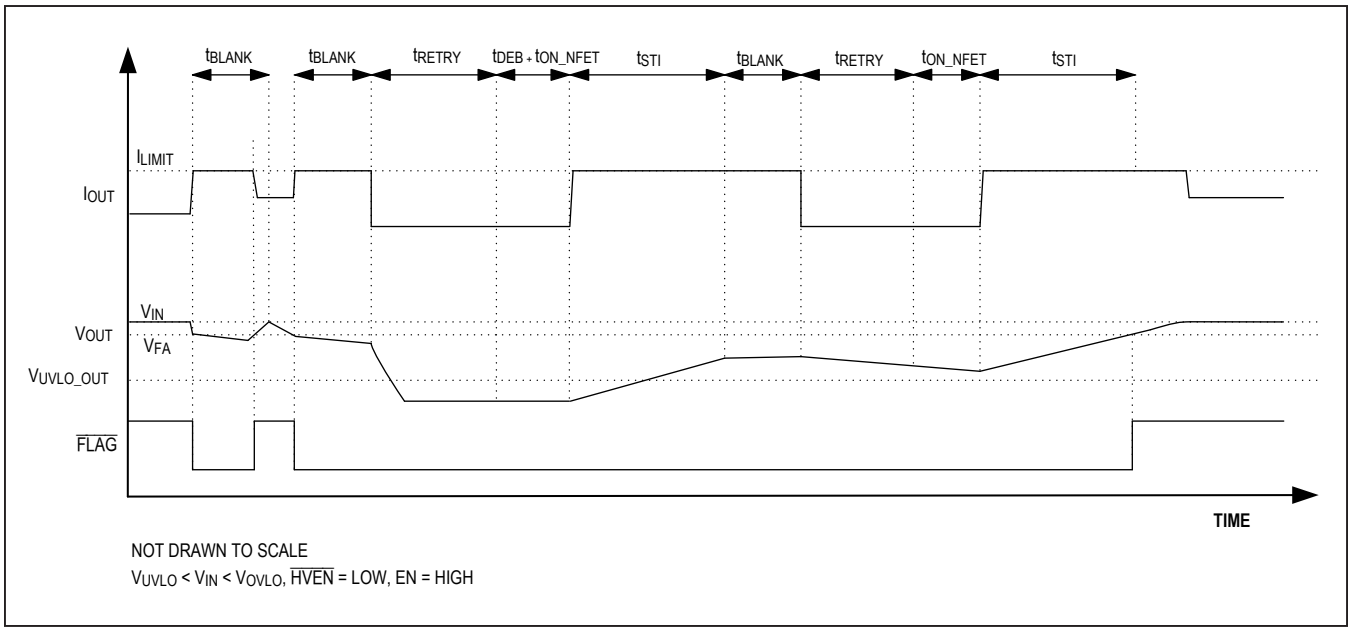


Figure 7. Autoretry-Fault Timing Diagram

Latch-Off Current Limit

In latch-off current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts when the voltage drop across the switch rises above V_{FA} and deasserts when it falls below V_{FA}. The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond t_{BLANK}. To reset the switch, either toggle the control logic (EN or $\overline{HVEN}$) or cycle the input voltage. Figure 8 depicts typical behavior in latch-off current-limit mode.

Reverse Current Protection

In the device, the reverse current-protection feature is enabled when used with external NFET and it prevents reverse current flow from OUT to IN pins.

If a reverse current condition is detected ((V_{IN} - V_{OUT}) < $V_{RIBRISING\_}$), the external NFET is turned off. When the reverse current condition no longer exists ((V_{SN} - V_{OUT}) > $V_{RIBRISING\_}$), the external NFET is turned back ON after $t_{ON\_EXTNFET}$. If the reverse current condition is the only fault (no UVLO, no thermal fault, no forward overcurrent fault), then the internal NFET is kept ON, otherwise the internal NFET is also turned OFF. Figure 9 depicts typical behavior in slow or fast reverse current condition.

The device contains two reverse-current thresholds with slow (< 17µs) and fast (< 108ns) response time for reverse current protection. The threshold values for slow reverse is 5.4mV (typ) whereas for fast reverse, it is 100mV (typ). This feature results in robust operation in a noisy environment, while still delivering fast protection for severe fault, such as input short-circuit or hot plug-in at the OUT pins.

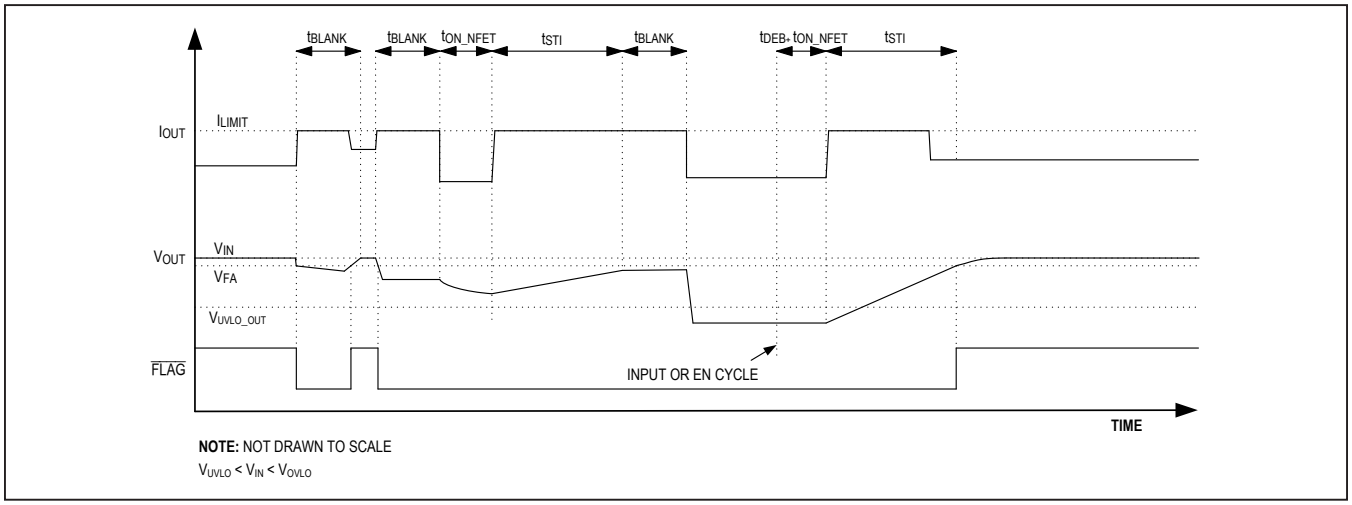


Figure 8. Latchoff-Fault Timing Diagram

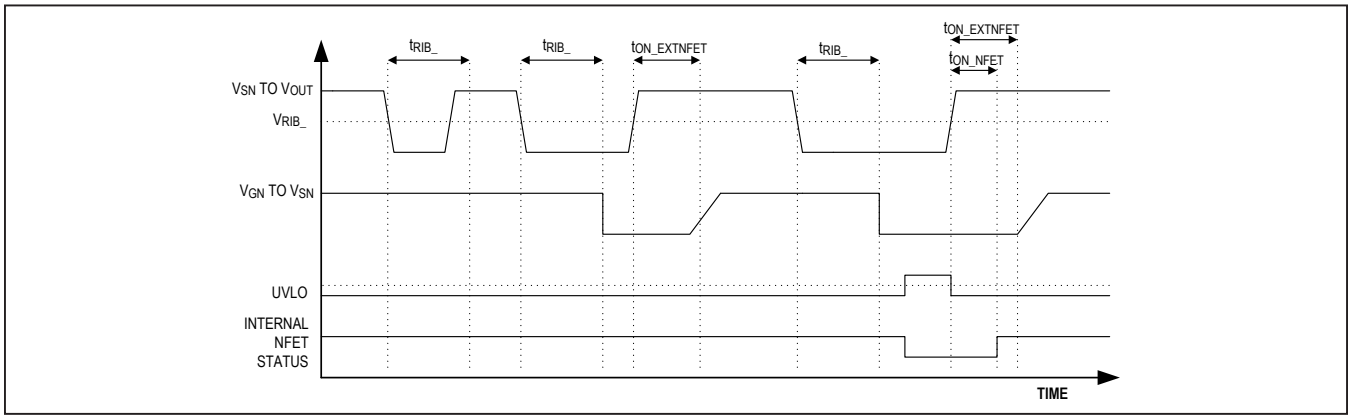


Figure 9. Reverse-Current-Fault Timing Diagram

Power Limit

The device features a unique Power Limit feature that allows the set current limit to be modified automatically based on an external voltage (V_{EXT}). The device monitors a fraction of this external voltage on the PLIM pin and dynamically adjusts the current limit set by the SETI pin resistor based on the below relationship:

when $V_{PLIM} \leq V_{PLIM\_TH}$,

Current is limited to I_{LIM} value set by R_{SETI}

when $V_{PLIM} > V_{PLIM\_TH}$,

Current is limited to $\frac{I_{LIM} \times V_{PLIM\_TH}}{V_{PLIM}}$

Assuming the resistor-divider ratio of K for the resistors R5, R6 configured as shown in the *Typical Operating Circuit*, the above algorithm limits the power (P) delivered by the external voltage source as shown below:

$$V_{PLIM} = V_{EXT} \times K$$

$$P = \frac{V_{EXT} \times I_{LIM} \times V_{PLIM\_TH}}{V_{PLIM}}$$

Hence, $P = \frac{I_{LIM} \times V_{PLIM\_TH}}{K}$, where I_{LIM}, K and V_{PLIM_TH} are essentially constants with tolerances dictated by the design. The device is designed for ±14% V_{PLIM_TH} accuracy for the range $V_{PLIM\_TH} < V_{PLIM} < 3 \times V_{PLIM\_TH}$, which covers a 3x variation of external voltage (V_{EXT}).

In an input Power Limit application V_{IN} is equal to V_{EXT}, and the PLIM resistor divider is set to determine the input voltage at which the current limit starts decreasing. By setting this voltage and setting the maximum current limit, the maximum "Input Power Limit" for the application is set. The current limit can also be dynamically modified based on the output voltage by using V_{OUT} equal to V_{EXT}. This feature implements an "Output Power Limit" function that potentially allows larger output currents to be delivered to charge the output reservoir capacitors at low output voltage conditions experienced after input power returns after an "Outage," provided there are no thermal limitations due to excessive power dissipation. The Power Limit feature is disabled by connecting the PLIM pin to GND. A simplified Block diagram of the PLIM feature is shown below in Figure 10.

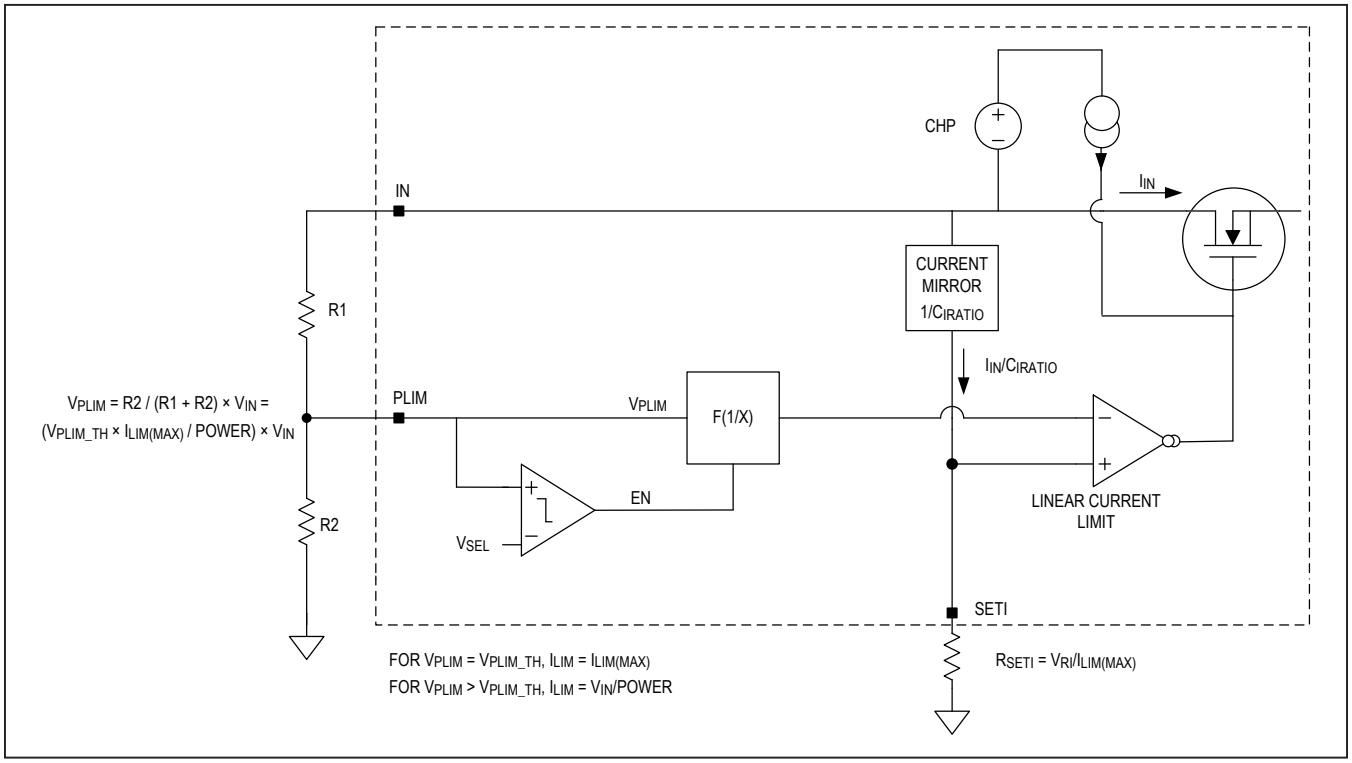


Figure 10. Power Limit Circuit

Fault Output

The device has an open-drain fault-indicator output, $\overline{FLAG}$. It requires an external pullup resistor to a DC supply. $\overline{FLAG}$ is held low when any of the following conditions occur:

- V_{IN} - V_{OUT} > V_{FA}.
- Die temperature exceeds +165°C.
- R_{SETI} is less than 3.2kΩ (max).
- Input voltage falls below the UVLO threshold.
- Input voltage rises above the OVLO threshold.

The below table describes the status of the FETs along with various fault condition. The $\overline{FLAG}$ pin is also 60V tolerant and when the open drain is on, it has a current protection that turns off the open drain if the current exceeds 4mA. The open drain is then turned back on if the fault condition is cycled.

Thermal Shutdown Protection

The device has a thermal shutdown feature to protect against overheating. The device turns off and the $\overline{FLAG}$ pin asserts when the junction temperature exceeds +165°C (typ). The device exits thermal shutdown and resumes normal operation after the junction temperature cools by 10°C (typ), except in latch-off mode when the device remains latched off.

The thermal limit behaves similarly to current limit. In autoretry mode, the thermal limit works with the autoretry timer. When the junction temperature falls below the falling thermal shutdown threshold, the device turns on after the t_{RETRY}. In latch-off mode, the device latches off until the power cycled or one of the enable pins is toggled. In continuous mode, the device is only disabled while the temperature is over the limit and turns back on after t_{DEB} when the temperature reaches the falling thermal shutdown threshold. There is no blanking time for thermal protection. Figure 6, Figure 7, and Figure 8 depict typical behavior under different current limit modes.

Table 3. FETs Status During Faults

CONDITION	INTERNAL NFET STATUS	EXTERNAL NFET STATUS	$\overline{FLAG}$ STATUS
No Fault	ON	ON	HIGH
UVLO	OFF	OFF	LOW
OVLO	OFF	OFF	LOW
Reverse with No Other Fault	ON	OFF	HIGH
Overcurrent Protection (I_{OCP}, 24A)	OFF	OFF	LOW
Thermal Shutdown	OFF	OFF	LOW
SETI Grounded*	OFF	OFF	LOW
V_{IN} - V_{OUT} > V_{FA}	X**	X**	LOW

*this condition is checked only at the first power on.

**the status of the FETs in this condition depends on the timing and the current limit mode selected.

Applications Information

IN Capacitor

A 1µF capacitor from the IN pin to EP/GND is recommended to hold input voltage during sudden load-current changes.

Hot Plug-In at IN Terminal

In many powering applications, an input-filtering capacitor is required to lower the radiated emission and enhance the ESD capability. In hot plug-in applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to 60V (max) should be placed close to the input terminal for enhanced protection.

Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The device detects reverse current entering at the OUT pin and flowing out of the IN pin and turns off the external NFET. The magnitude of the reverse current depends on the inductance of input circuitry and any capacitance installed near the IN pins.

OUT Capacitor

The maximum capacitive load (C_{MAX}) that can be connected is a function of current-limit setting (I_{LIM} in A), the startup initial time (t_{STI} in ms) and startup timeout (t_{STO} in ms) and the input voltage. The C_{MAX} is calculated using the following relationship:

$$C_{MAX}\ (mF) = I_{LIM}\ (A) \times \left[\frac{t_{STI}\ (ms) + t_{STO}\ (ms)}{V_{IN}\ (V)}\right]$$

For example, for V_{IN} = 24V, t_{STO} (typ) = 1200ms, t_{STI} (typ) = 24ms, and I_{LIM} = 3A, C_{MAX} is 153mF.

Output capacitor values in excess of C_{MAX} can trigger false overcurrent conditions. Note that above expression assumes no load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current resulting in a large charging period; hence, the possibility of a false overcurrent condition.

In practical applications, the C_{MAX} value is limited by the thermal performance of the PCB. Poor thermal design can cause the thermal foldback current-limiting function of the device to kick in too early, which can further limit the maximum capacitance that can be charged. Therefore, good thermal PCB design is imperative to charge large capacitor banks.

Hot Plug-In at OUT Terminal

In some applications, there might be a possibility of applying an external voltage at the OUT terminal of the devices with or without the presence of an input voltage. During these conditions, devices detect any reverse current entering at the OUT pin and flowing out of the IN pin and turn off the external NFET. Parasitic cable inductance along with input and output capacitors cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the absolute maximum ratings.

OUT Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response to output short-circuit conditions, it is important to reduce the effect of undesirable parasitic inductance by keeping all traces as short as possible. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During steady-state operation, the power dissipation is typically low and the package temperature change is usually minimal. PCB layout designs need to meet two challenges: high-current input and output paths and important heat dissipation.

Maxim recommends the use of 2oz copper on an FR4 isolator in a four-layer configuration. The layer stack needs to be Top (routing), GND (plane), Power (plane, connected to V_{OUT}), and Bottom (routing), in this order, from top to bottom. Install the IC on an exposed pad landing of minimum 100 mils x 100 mils, with at least five through vias to the GND plane. The vias should be 32mils in diameter, with a 16mils plated hole. The hole plating needs to be at least 0.5oz copper. Provide a minimum of 1in x 1in area of copper plane on all four layers. It is important to remember that the inner planes do not contribute much to heat dissipation due to FR4 isolation, but are important from an electrical point of view. If possible, keep the top and bottom copper areas clear of solder mask, as this greatly improves heat dissipation. Use a similarly large copper area connected directly to the OUT pins. A dimension of 1in x 1in is also recommended. This might look oversized for current path requirements, but is essential for heat dissipation. Keep in mind that heat is generated at the drain junction of the internal nMOS pass FET, which is then eliminated through the five OUT pins and needs to be dissipated on this same copper area.

Connect all five IN pins to a copper area that is at least 150mils wide. Using 2oz copper can reduce this requirement to 100mils. Remember to provide the same copper trace width on the source connection, when using the external NMOS pass FET (with the source connected to the IN pins). Use extreme caution when placing the decoupling capacitors to the IN and OUT pins. The tendency to go as close as possible to the IC pins might interfere with the minimum requirement of the tracewidth above. It is important to note that the return load current does not flow through the IC; therefore, it is important to provide an external ground trace of at least the same width as the input/output one. Maxim recommends the use of a GND plane. Connect the input and output grounds to this plane using at least four plated vias each. The vias should be 84mils in diameter (or 60mils x 60mils, if square) with a 35mils plated hole.

ESD Protection

No capacitor is required for ±2kV (HBM) (typ) ESD on IN. All pins have ±2kV (HBM) ESD protection. In applications in which an external NFET is used, see the *IN Capacitor* section.

Figure 11 shows the Human Body Model and Figure 12 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

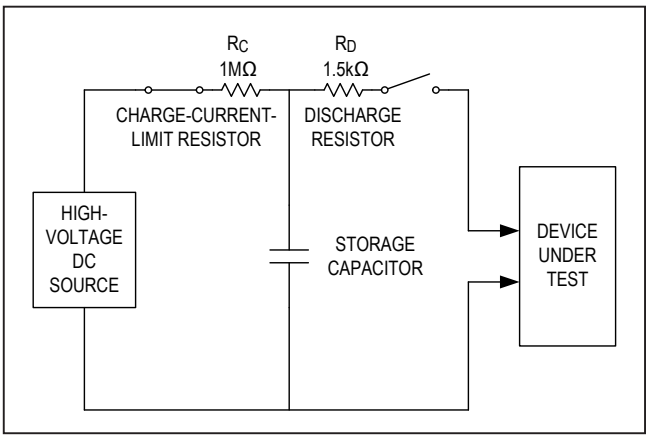


Figure 11. Human Body ESD Test Model

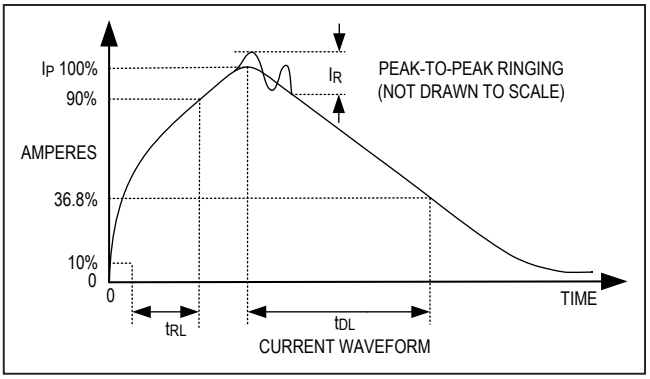


Figure 12. Human Body Current Waveform

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INITIAL CURRENT LIMIT	POWER LIMIT FEATURE
MAX17526AATP+	-40°C to +125°C	20 TQFN-EP*	1.0x	Enabled
MAX17526AATP+T	-40°C to +125°C	20 TQFN-EP*	1.0x	Enabled
MAX17526BATP+**	-40°C to +125°C	20 TQFN-EP*	1.5x	Disabled
MAX17526BATP+T**	-40°C to +125°C	20 TQFN-EP*	1.5x	Disabled
MAX17526CATP+**	-40°C to +125°C	20 TQFN-EP*	2.0x	Disabled
MAX17526CATP+T**	-40°C to +125°C	20 TQFN-EP*	2.0x	Disabled

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*
***Future product—contact factory for availability.*