Click here to ask an associate for production status of specific part numbers.

5.5V to 60V, 6A Power Limiter with OV, UV, Reverse Polarity, Loss of Ground Protection

MAX17527A

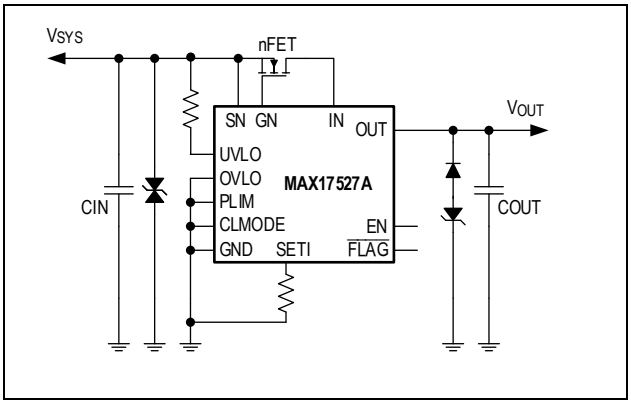
Product Highlights

- Robust Protection Reduces System Downtime
  - Wide Input-Supply Range: +5.5V to +60V
  - ±4% Accurate Programmable Current Limit between 3A to 6A Across Full Temperature Range
  - ±5% Accurate Programmable Current Limit between 0.6A to 6A Across Full Temperature Range
  - ±7% Accurate Power Limit at 100W, 24V for Class 2 Applications.
  - Input-Voltage Reverse-Polarity Protection (with External nFET)
  - Dual-Stage Reverse-Current Protection (with External nFET) with fast 108ns response time
  - Low R_{ON} Internal nFET (30mΩ)
  - Output-Voltage Reverse-Polarity Tolerant
  - Loss of Ground Protection
- Flexible Design to Maximize Reuse and Minimize Requalification
  - Adjustable UVLO and OVLO Thresholds
  - ±3% Accurate SETI Current Read-Out
  - Programmable Overcurrent Response: Continuous, Autoretry, and Latch-Off Modes
  - Logic Level Enable Input (EN)
  - Protected External nFET Gate Drive
  - Open-Drain Fault Indicator, $\overline{FLAG}$
  - Continuous Current-Limit During Startup
  - Thermal Foldback Current-Limit
- Reduced Solution Footprint
  - 20-Pin 5mm x 5mm TQFN-EP Package
  - Integrated nFET for Common-Use Protection Requirements

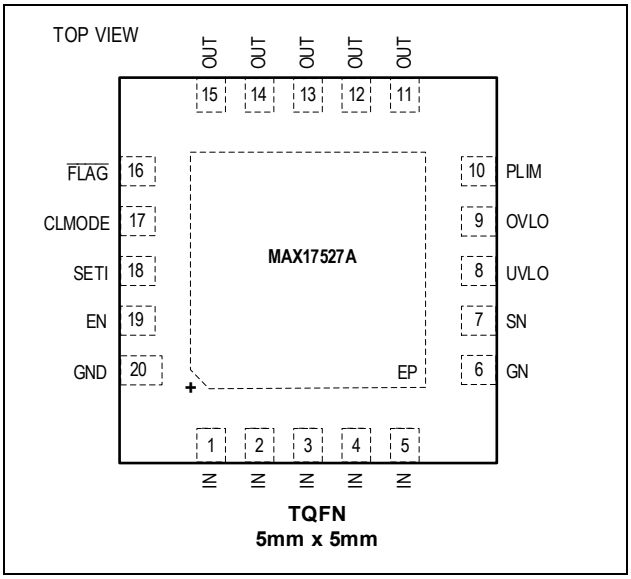
Key Applications

- Loss of Ground Protection:
  The MAX17527A interrupts load current and disconnects the output from the input in a loss of ground event, such as when the single-fault safety fuse on its ground path opens up.
- UL1310 Class 2 Power Limiter:
  The ±4% Accurate Current Limit between 3A and 6A and ±7% Accurate Power Limit of MAX17527A offers tight protection boundary in UL1310 Class 2 power supply applications and maximizes power delivery to the load.

Simplified Application Diagram



Pin Description



***Ordering Information* appears at end of data sheet**

19-101626; Rev 0; 11/22

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Absolute Maximum Ratings

IN to GND ..... -0.3V to +65V

OUT to GND ..... -65V to (V_{IN} + 0.3V)

IN to OUT ..... -0.3V to +65V

SN to GND (Note 1) ..... -62V to +65V

GN to SN ..... - 0.3V to + 6V

UVLO, OVLO, PLIM, $\overline{FLAG}$ to GND ..... -0.3V to (V_{IN} + 0.3V)

EN, CLMODE to GND ..... -0.3V to +6V

SETI to GND ..... -0.3V to +6V

IN Current (DC) 6.3A

Continuous Power Dissipation (T_A = +70°C, TQFN derate 34.5mW/°C above +70°C) 2758mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

Note 1: An external nFET or diode is required to achieve negative input protection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20 TQFN

Package Code	T2055+6C
Outline Number	21-0140
Land Pattern Number	90-0010
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
IN Voltage Range	V_{IN}		5.5		60.0	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = V_{SN} = 24V, V_{OUT} = 0V		21	48	µA
		V_{EN} = 0V, V_{IN} = V_{SN} = 40V, V_{OUT} = 0V		31	67	
Shutdown Output Current	I_{OFF}	V_{EN} = 0V, V_{SN} = V_{IN} = Unconnected, V_{OUT} = 40V		94	240	µA
Shutdown IN to OUT Current	I_{SHDN_IN-OUT}	V_{EN} = 0V, V_{IN} - V_{OUT} = 60V		13	27	µA
Supply Current	I_{IN}	V_{SN} = V_{IN} = V_{OUT} = 24V, V_{EN} = Open		1.46	2.20	mA
UVLO, OVLO						
Internal Undervoltage-Trip Level	V_{UVLO}	V_{IN} rising, UVLO connected to GND	11.9	12.4	13.0	V
		V_{IN} falling, UVLO connected to GND	11.5	12.0	12.5	
Internal Overvoltage-Trip Level	V_{OVLO}	V_{SN} rising, OVLO connected to GND	34.7	36.2	37.6	V
		V_{SN} falling, OVLO connected to GND	32.2	34.1	35.8	
Undervoltage-Trip Level on Output	V_{UVLO_OUT}	V_{OUT} rising	12.2	12.7	13.2	V
		V_{OUT} falling, UVLO trip point	11.9	12.4	12.9	
External UVLO Set Voltage	V_{SET_UVLO}	UVLO rising	1.20	1.26	1.33	V
		UVLO falling	1.18	1.22	1.27	
External UVLO Select Voltage	V_{UVLO_SEL}		0.15	0.38	0.50	V
External UVLO Leakage Current	I_{UVLO_LEAK}	V_{UVLO} = 0 to 2V	-250		+250	nA
External OVLO Set Voltage	V_{SET_OVLO}	OVLO rising	1.18	1.22	1.27	V
		OVLO falling	1.09	1.15	1.20	
External OVLO Select Voltage	V_{OVLO_SEL}		0.15	0.38	0.50	V
External OVLO Leakage Current	I_{OVLO_LEAK}	V_{OVLO} = 0 to 2V	-250		+250	nA
External UVLO Adjustment Range		(Note 3)	5.5		59.0	V
External OVLO Adjustment Range		(Note 3)	6.0		60.0	V
GN, SN						
External nFET Gate Drive Voltage	V_{GN-SN}	V_{EN} = 5V, no reverse condition	4.45	4.75	4.95	V
Gate Active Pullup Current		V_{EN} = 5V, V_{GN} = V_{SN}, no reverse condition	9	18	28	µA
Gate Active Pulldown Resistance		V_{EN} = 5V, reverse condition		140		mΩ
Shutdown Gate Pulldown Resistance		V_{EN} = 0V, V_{GN} - V_{SN} = 1.5V		2.7	6.1	kΩ
		V_{EN} = 0V, V_{GN} - V_{SN} = 0.5V		3.9	8.0	MΩ
INTERNAL nFETs						
Internal nFETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} ≥ 10V		30	57	mΩ

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Adjustment Range	I_{LIM}		0.6		6.0	A
Current-Limit Accuracy	I_{LIM_ACC}	3A ≤ I_{LIM} ≤ 6A, V_{PLIM} < V_{PLIM_TH}	-4.0		+4.0	%
		0.6A ≤ I_{LIM} ≤ 6A, V_{PLIM} < V_{PLIM_TH}	-5.0		+5.0	
$\overline{FLAG}$ Assertion Drop-Voltage Threshold	V_{FA}	Increase in (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V	390	470	550	mV
Overcurrent Protection Threshold	I_{OCP}	(Note 4)	20	26	32	A
Slow Reverse-Current-Blocking Threshold	V_{RIB_SLOW}	V_{IN} - V_{OUT}, falling	-0.5	-5.4	-10.5	mV
Slow Reverse-Current-Blocking Response Time	t_{RIB_SLOW}	(Note 5)		17	30	µs
Fast Reverse-Current-Blocking Threshold	V_{RIB_FAST}	V_{IN} - V_{OUT}, falling	-78	-98	-118	mV
Fast Reverse-Current-Blocking Response Time	t_{RIB_FAST}	(Note 6, Note 4), C_{GS} = 10nF		108	135	ns
Reverse-Current-Blocking Rising Threshold	V_{RIB_RISING}	V_{SN} - V_{OUT}, rising	65	100	135	mV
Reverse Output Current	I_{OUT_REV}	V_{SN} = 0V, V_{OUT} = 24V, IN unconnected		2	5	mA
PLIM						
PLIM Limit Threshold Voltage	V_{PLIM_TH}		0.744	0.800	0.856	V
PLIM Limit Operation Range			V_{PLIM_TH}		3 x V_{PLIM_TH}	V
Power-Limit Accuracy		P = 100W, V_{IN} = 24V	-7.0		+7.0	%
SETI						
R_{SETI} x I_{LIM}	V_{RI}	V_{PLIM} < V_{PLIM_TH}		1.5		V
Current-Mirror Output Ratio	C_{IRATIO}			25000		A/A
LOGIC INPUT (CLMODE, EN)						
EN Input-Logic High	V_{IH}		1.4			V
EN Input-Logic Low	V_{IL}				0.4	V
Internal EN Pullup Voltage		EN pin unconnected		1.45	1.80	V
EN Input Current		V_{EN} = 5.5V		33	48	µA
EN Pullup Current		V_{EN} = 0.4V	2.2	5.8	12.0	µA
CLMODE Input-Logic High	V_{CLMODE_IH}		3.6	4.3	4.7	V
CLMODE Input-Logic Low	V_{CLMODE_IL}		0.4	0.8	1.1	V
CLMODE Pullup Current			5.3	9.2	14.0	µA
LOGIC OUTPUT ($\overline{FLAG}$)						
Logic-Low Voltage		I_{SINK} = 1mA			0.4	V

(V_{IN} = 5.5V to 60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 24V, T_A = +25°C) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		V_{IN} = 5.5V, $\overline{FLAG}$ open drain off			1	µA
$\overline{FLAG}$ Protection Current		$\overline{FLAG}$ open drain on	4			mA
TIMING CHARACTERISTICS (NOTE 7)						
Switch Turn-On Time	t_{ON}	V_{IN} = 24V, switch OFF to ON, R_{LOAD} = 240Ω, I_{LIM} = 1A, C_{OUT} = 4.7µF, V_{OUT} from 20% to 80% of V_{IN}		110		µs
Fault Recovery nFET Turn-On Time	t_{ON_NFET}	Turn-on delay after fault timers expired		200	400	µs
Fault Recovery External nFET Turn-on Time	t_{ON_EXNFET}	V_{OUT} > V_{UVLO_OUT}, turn-on delay of external nFET after fault timers expired	1.09	1.20	1.32	ms
OVP Switch Response Time	t_{OVP_RES}			3		µs
Overcurrent Protection Response Time	t_{OCP_RES}	I_{LIM} = 5A, I_{OUT} step from 3A to 30A. Time to turn the switch off		3		µs
Startup Timeout	t_{STO}	Initial start current-limit foldback timeout (*Figure 12*)	1090	1200	1320	ms
Startup Initial Time	t_{STI}	(*Figure 12*)	21.8	24.0	26.4	ms
IN Debounce Time	t_{DEB}	Additional turn-on delay if V_{OUT} < V_{UVLO_OUT}, see *Figure 12* to *Figure 18*	1.09	1.20	1.32	ms
Blanking Time	t_{BLANK}	*Figure 17* and *Figure 18*	22.5	24.0	25.5	ms
Autoretry Time	t_{RETRY}	*Figure 17* (Note 8)	654	720	792	ms
Loss-of-Ground Switch Turn-Off Time	$t_{OFF\_GNDLOSS}$	C_{IN_IC} = 100nF			100	ms
THERMAL PROTECTION						
Thermal Foldback	$T_{J(FB)}$			150		°C
Thermal Shutdown	T_J			165		°C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			10		°C

Note 2: All devices are 100% production-tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design; not production tested.

Note 3: Not production-tested, user-adjustable. See the *Overvoltage Lockout (OVLO)* and *Undervoltage Lockout (UVLO)* sections.

Note 4: Guaranteed by design, not production tested.

Note 5: Time from V_{IN} - V_{OUT} voltage transition from 200mV to -50mV until GN pin voltage falls to V_{SN} + 1V (*Figure 1*).

Note 6: Time from V_{IN} - V_{OUT} voltage transition from 200mV to -250mV until the GN pin voltage falls to V_{SN} + 1V (*Figure 2*).

Note 7: All timing is measured using 20% and 80% levels, unless otherwise specified.

Note 8: The autoretry time-to-blanking-time ratio is fixed and is equal to 30.

Timing Diagrams

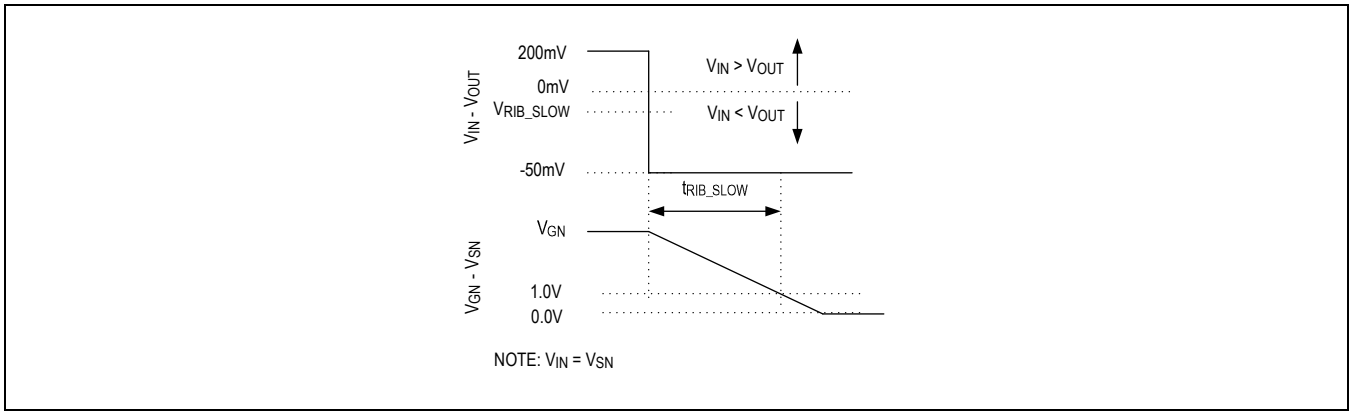


Figure 1. Slow Reverse-Current-Blocking Response Time

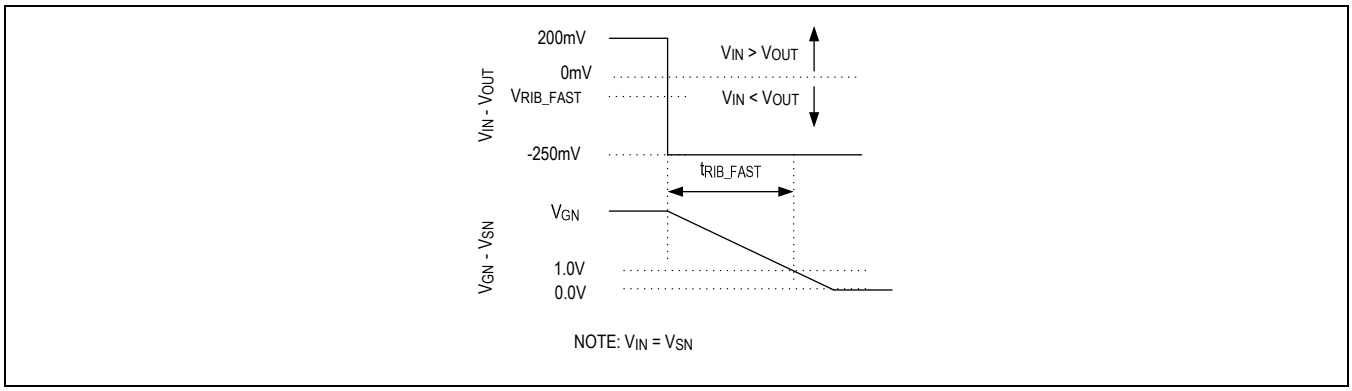
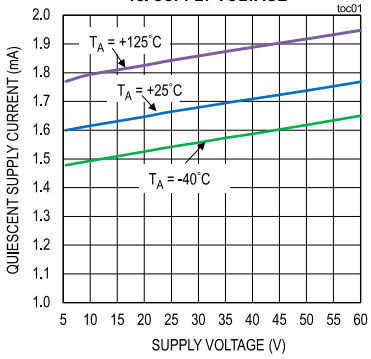


Figure 2. Fast Reverse-Current-Blocking Response Time

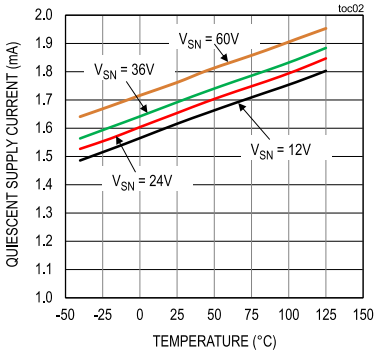
Typical Operating Characteristics

(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

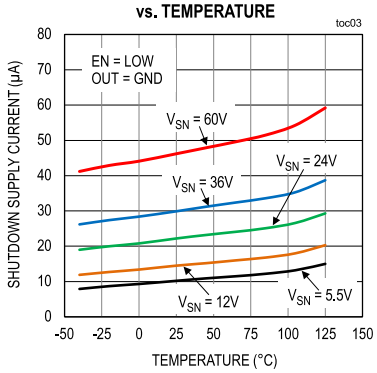
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



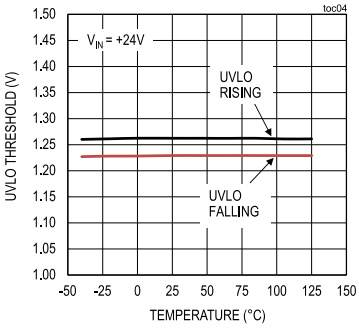
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



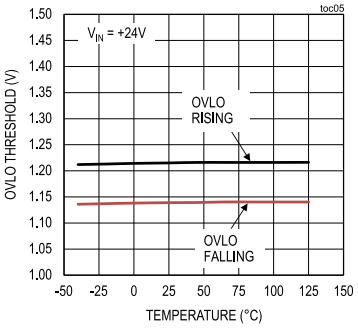
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



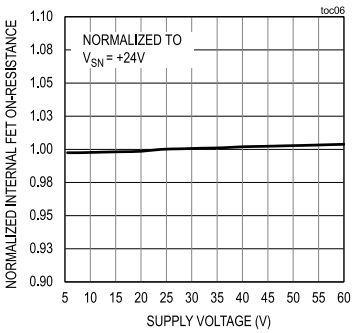
UVLO THRESHOLD vs. TEMPERATURE



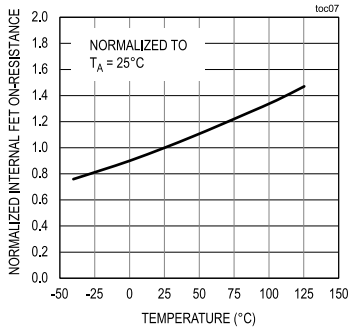
OVLO THRESHOLD vs. TEMPERATURE



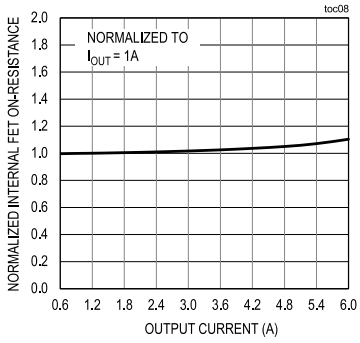
NORMALIZED INTERNAL FET ON-RESISTANCE vs. SUPPLY VOLTAGE



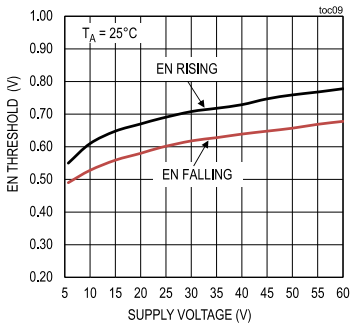
NORMALIZED INTERNAL FET ON-RESISTANCE vs. TEMPERATURE



NORMALIZED INTERNAL FET ON-RESISTANCE vs. OUTPUT CURRENT

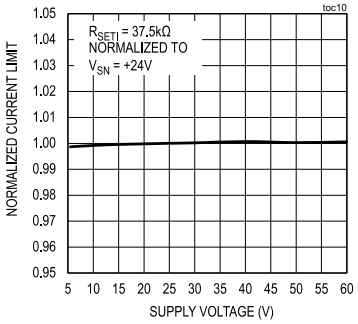


EN THRESHOLD vs. SUPPLY VOLTAGE

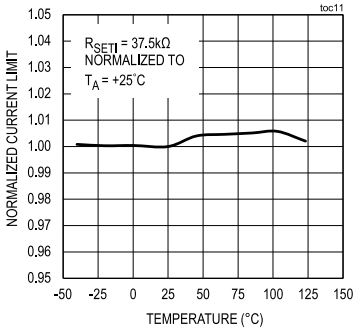


(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

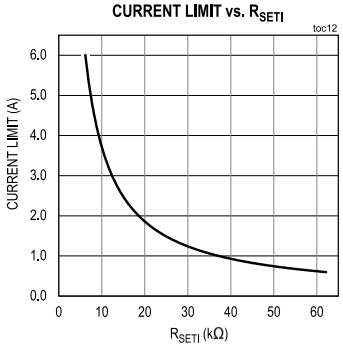
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



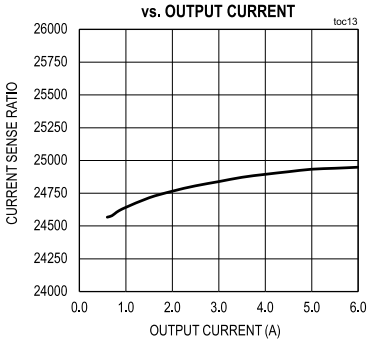
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



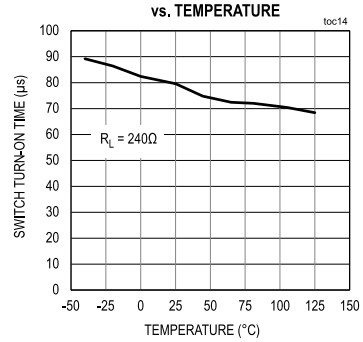
CURRENT LIMIT vs. R_{SETI}



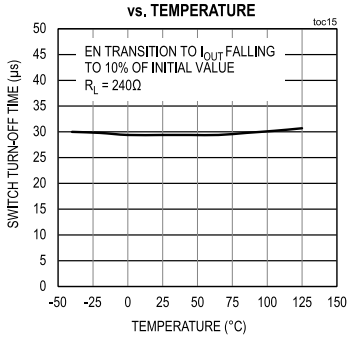
CURRENT SENSE RATIO vs. OUTPUT CURRENT



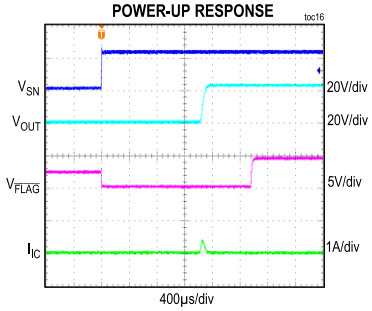
SWITCH TURN-ON TIME vs. TEMPERATURE



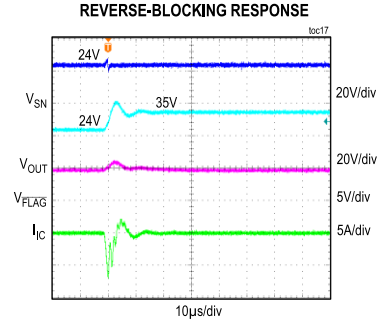
SWITCH TURN-OFF TIME vs. TEMPERATURE



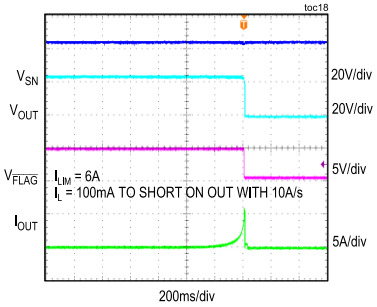
POWER-UP RESPONSE



REVERSE-BLOCKING RESPONSE

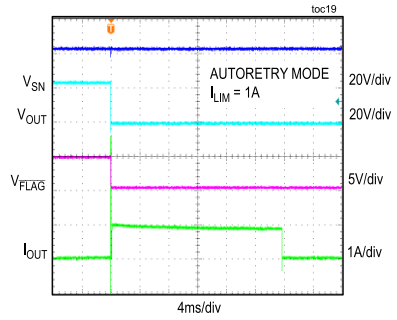


CURRENT-LIMIT RESPONSE

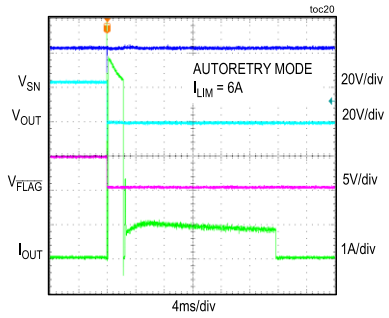


(V_{IN} = 24V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

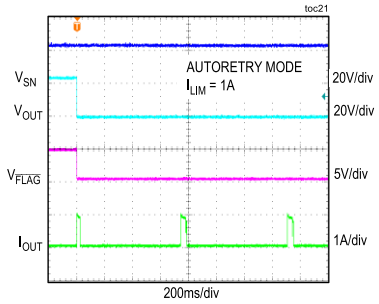
OUTPUT SHORT-CIRCUIT RESPONSE



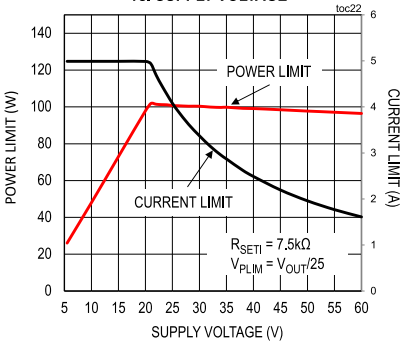
THERMAL FOLDBACK DUE TO OUTPUT SHORT-CIRCUIT



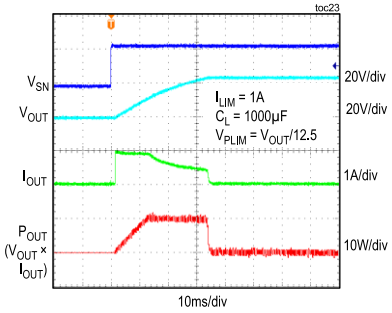
AUTORETRY TIME (t_{RETRY})



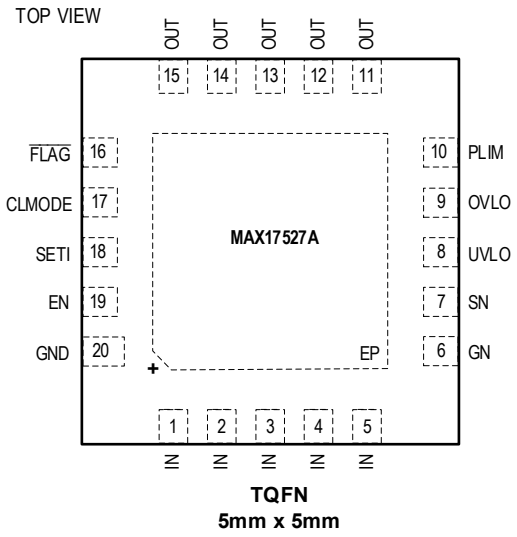
CURRENT LIMIT, POWER LIMIT vs. SUPPLY VOLTAGE



OUTPUT POWER-LIMIT RESPONSE



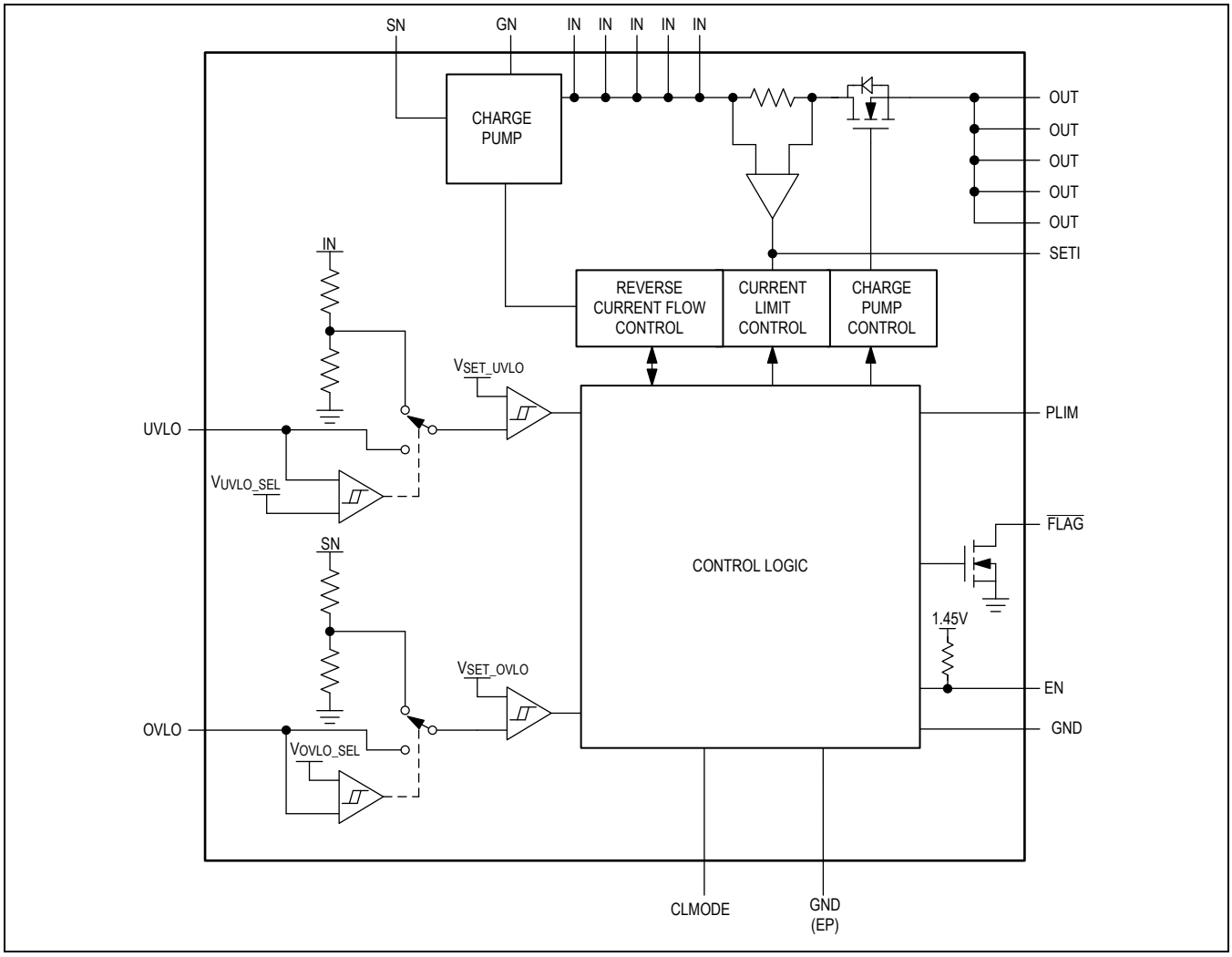
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1–5	IN	Input Pins. Bypass IN to GND with minimum 1µF ceramic capacitor. For Hot Plug-In applications, see the *Applications Information* section.
6	GN	Gate Driver Output for External nFET. If external nFET is not used, leave GN pin unconnected.
7	SN	Return for External nFET Gate Drive and Input Voltage Sense Pin. Connect to source of external nFET as shown in the *Typical Operating Circuit*. Bypass SN to GND with minimum 4.7µF capacitor. SN serves as the undervoltage/overvoltage sensed input when preprogrammed UVLO/OVLO is used. Connect SN to IN if external nFET is not used.
8	UVLO	UVLO Adjustment Pin. Connect UVLO to GND to use the default internal UVLO threshold. Connect resistive potential divider from SN/IN to GND to set the UVLO threshold externally and override the preset internal UVLO threshold.
9	OVLO	OVLO Adjustment Pin. Connect OVLO to GND to use the default internal OVLO threshold. Connect resistive potential divider from SN/IN to GND to set the OVLO threshold externally and override the preset internal OVLO threshold.
10	PLIM	Power Limit Adjustment Pin. Connect PLIM to an external resistive potential divider to define a threshold at which the power limit feature starts reducing the current-limit threshold. Connect PLIM to GND to disable this feature and have the current-limit set only by the resistor placed on SETI.
11–15	OUT	Output Pins. For a long output cable or inductive load, see the *Applications Information* section.
16	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when: • The (V_{IN} - V_{OUT}) voltage exceeds V_{FA}. • Thermal shutdown is active. • Input voltage falls below UVLO threshold or rises above OVLO threshold. • R_{SETI} is less than 3.2kΩ.
17	CLMODE	Current-Limit Mode Selector Pin. Leave CLMODE unconnected for continuous mode. Connect CLMODE to GND for Autoretry mode. Connect a 220kΩ resistor between CLMODE and GND for Latch-off mode.
18	SETI	Overcurrent Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set overcurrent limit. See the *Setting the Current Limit Threshold* section. Do not connect more than 30pF to SETI.
19	EN	Active-High Enable Input. Internally pulled up to 1.45V.
20	GND	Ground. Reference pin for all control signals.
—	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17527A EV kit data sheet for a reference layout design.

Simplified Block Diagram



Detailed Description

The MAX17527A offers adjustable protection boundaries for systems against input voltage faults and overcurrent faults. In addition, the MAX17527A offers a programmable power limiting function. Input-voltage faults (with positive polarity) are protected up to +60V by an internal nFET featuring low ON-resistance (30mΩ typ). The device features fixed or programmable overvoltage lockout (OVLO) and undervoltage lockout (UVLO) thresholds by using internal or external voltage-dividers. Factory preset internal fixed thresholds can be invoked by connecting the OVLO and/or UVLO pin(s) to GND. Input undervoltage protection can be programmed between 5.5V and 59V, while the overvoltage protection can be independently programmed between 6V and 60V.

Input reverse-polarity protection is realized using an external nFET that is controlled by the MAX17527A. The magnitude of reverse-polarity voltage protection is dependent on the operating load-bus voltage (V_{OUT}) and the voltage blocking capability of the external nFET. For example, for protection down to a -55V input range with V_{OUT} = 30V, an external nFET rated at 85V is needed. The external nFET is also needed for the optional reverse-current protection. If reverse polarity protection and reverse-current protection are not needed, SN must be connected to IN and GN must be left unconnected. The MAX17527A is tolerant against accidental output reverse-polarity application due to incorrect wiring across the output terminals.

The current limit of the device is programmed by connecting a resistor from the SETI pin to GND. The current limit can be programmed from 0.6A to 6.0A. When the current through the device reaches or exceedes the set current limit, the resistance of the internal nFET is modulated to limit the current. The device offers three current limit behavioral modes: Continuous, Auto-retry, and Latch-off modes.

The SETI pin presents a current proportional to the device current under normal operation. Together with the current limit program resistor (between SETI and GND), the SETI pin presents a voltage that is proportional to the device current. This voltage can be read by a monitoring system for recording instantaneous current of the device.

The power limit function is realized either at the input supply side or output load side by sampling the input or output voltage through a potential divider connecting to the PLIM pin. The power limit feature reduces the programmed current limit when the external voltage increases above the programmed threshold. The device can be turned On or Off through enable input EN by a master supervisory system. This allows the master supervisory system to Turn On or Off the power delivery to connected loads.

The device offers loss-of-ground protection where it safely turns Off the device operation during a loss-of-ground fault event, i.e., when the safety ground fuse opens up in a redundant-safety application.

The device offers a status announcement signal ($\overline{FLAG}$) to indicate operational and fault signals. $\overline{FLAG}$ is an open drain pin, and requires an external pullup resistor to the appropriate system interface voltage. The device also offers internal thermal shutdown protection against excessive power dissipation.

Undervoltage Lockout (UVLO)

The device has a 12.4V (typ) preset UVLO threshold on the IN pin when the voltage at the UVLO pin is less than the external UVLO select threshold (V_{UVLO_SEL}). Connect the UVLO pin to GND to select the preset UVLO threshold. If the voltage at the UVLO pin rises above V_{UVLO_SEL}, the device enters adjustable UVLO mode. The device has a UVLO adjustment range from 5.5V to 59V. Connect an external resistive potential divider to the UVLO pin as shown in the *Typical Operating Circuit* to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. The recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{SET\_UVLO} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{SET_UVLO} = 1.26V and V_{UVLO} is the input-supply voltage at which the device exits the UVLO condition. A 40mV (typ) hysteresis is provided on the UVLO pin; thus, causing the part to enter a UVLO condition when the UVLO pin falls to 1.22V (typ).

Alternatively, R2 can be calculated using the following equation:

$$R2 = \frac{R1}{\left(\frac{V_{UVLO}}{V_{SET\_UVLO}} - 1\right)}$$

When the voltage on the UVLO pin falls below V_{SET_UVLO}, the internal nFET quickly turns Off and $\overline{FLAG}$ is asserted. When the UVLO condition is removed, the device takes the input debounce time (t_{DEB}) to start the switch turn-on process if V_{OUT} is below the V_{UVLO_OUT} threshold. The internal nFET is turned on after fault recovery internal nFET turn-on time (t_{ON_NFET}) and the external nFET is turned on after fault recovery external nFET turn-on time ($t_{ON\_EXTNFET}$), and $\overline{FLAG}$ is deasserted. In the case where V_{OUT} is above the V_{UVLO_OUT} threshold, t_{DEB} is not present during the switch turn-on process. If the UVLO function is not used, the UVLO pin must be connected to IN. The UVLO pin must not be left unconnected.

Overvoltage Lockout (OVLO)

The device has a 36.2V (typ) preset OVLO threshold on the SN pin when the voltage at the OVLO pin is less than the external OVLO select threshold (V_{OVLO_SEL}). Connect the OVLO pin to GND to select the preset OVLO threshold. If the voltage at the OVLO pin rises above V_{OVLO_SEL}, the device enters adjustable OVLO mode. The device has an OVLO adjustment range from 6V to 60V. Connect an external resistive potential divider to the OVLO pin as shown in the *Typical Operating Circuit* to adjust the OVLO threshold voltage. Use the following equation to adjust the OVLO threshold. The recommended value of R3 is 2.2MΩ.

$$V_{OVLO} = V_{SET\_OVLO} \times \left(1 + \frac{R3}{R4}\right)$$

where V_{SET_OVLO} = 1.22V and V_{OVLO} is the input supply voltage at which the device enters the OVLO condition. A 70mV (typ) hysteresis is provided on the OVLO pin causing the part to exit the OVLO condition when the OVLO pin falls to 1.15V (typ).

Alternatively, R4 can be calculated using the following equation:

$$R4 = \frac{R3}{\left(\frac{V_{OVLO}}{V_{SET}} - 1\right)}$$

The OVLO reference voltage (V_{SET_OVLO}) is set at 1.22V. If the voltage at the OVLO pin exceeds V_{SET_OVLO}, the switch is turned off to protect the downstream circuits and $\overline{FLAG}$ is asserted. When the OVLO condition is removed, the device takes input debounce time (t_{DEB}) to start the switch turn-on process if V_{OUT} is below the V_{UVLO_OUT} threshold. The internal nFET is turned on after fault recovery internal nFET turn-on time (t_{ON_NFET}) and the external nFET is turned on after fault recovery external nFET turn-on time ($t_{ON\_EXTNFET}$), and the $\overline{FLAG}$ is deasserted. *Figure 3* depicts typical behavior in overvoltage conditions. In the case where V_{OUT} is above the V_{UVLO_OUT} threshold, t_{DEB} is not present during the switch turn-on process. If the OVLO function is not used, the OVLO pin must be connected to GND. The OVLO pin must not be left unconnected.

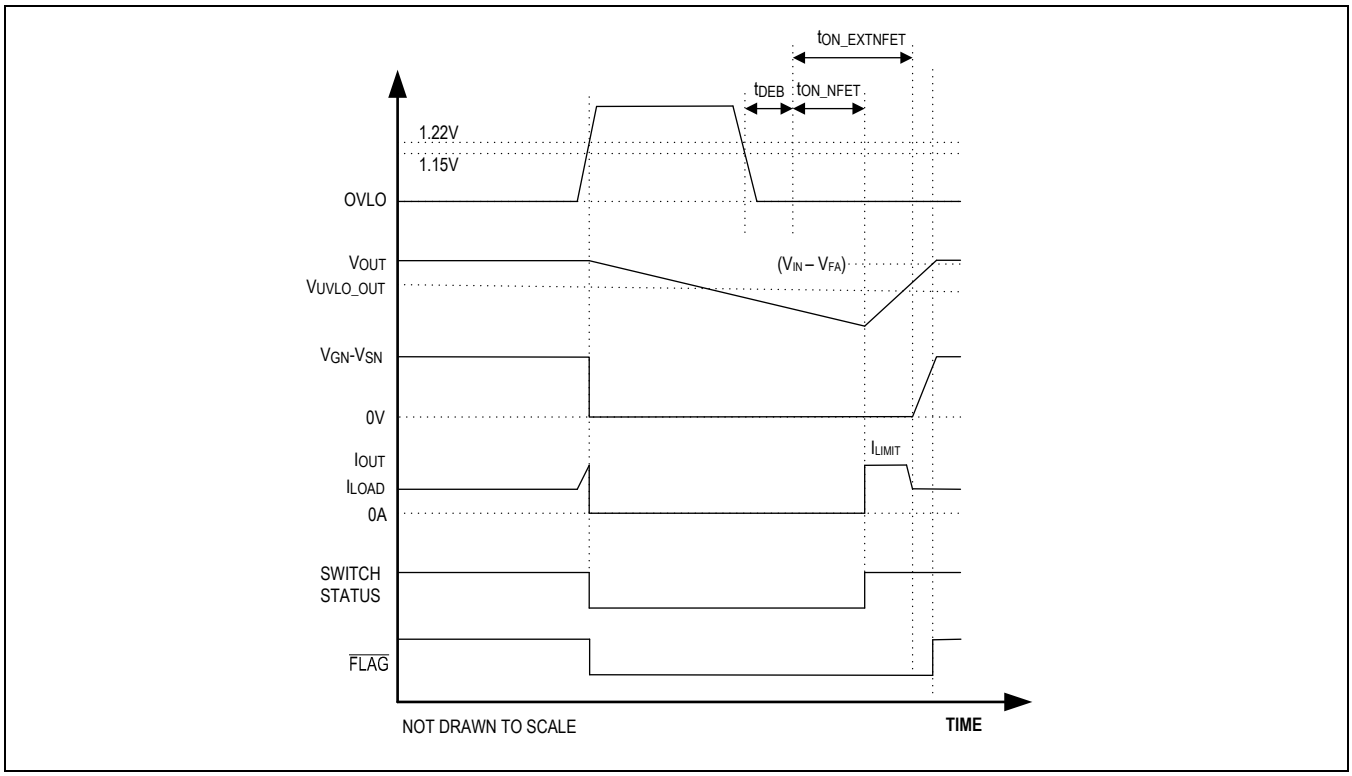


Figure 3. Overvoltage-Fault Timing Diagram

Input Reverse-Polarity Protection

Input reverse-polarity protection is realized using an external nFET that is controlled by the MAX17527A. Due to incorrect wiring on the input power supply terminals, negative supply may appear on the device's input pins. Connect an external N-channel MOSFET (Q1) with the source connected to the SN pin, drain to the IN pin, and gate to the GN pin as shown in the *Typical Operating Circuit*. During an input reverse polarity voltage fault, this external nFET turns off and protects the load. The external nFET is also needed for the optional reverse-current protection. If reverse-polarity protection and reverse-current protection are not needed, the SN pin must be connected to the IN pin, and the GN pin must be left unconnected.

The magnitude of reverse-polarity voltage protection is dependent on the operating load bus voltage (V_{OUT}) and the voltage blocking capability of the external nFET. For example, for protection down to a -55V input voltage with V_{OUT} = 30V, an external nFET rated for 85V is needed. The MAX17527A provides a gate drive (GN) of 4.75V (typ). *Figure 4* shows the reverse-polarity protection of MAX17527A with V_{OUT} = 0V and V_{SN} = -24V. *Figure 5* shows the reverse-polarity protection of MAX17527A with V_{OUT} = +24V and V_{SN} = -24V.

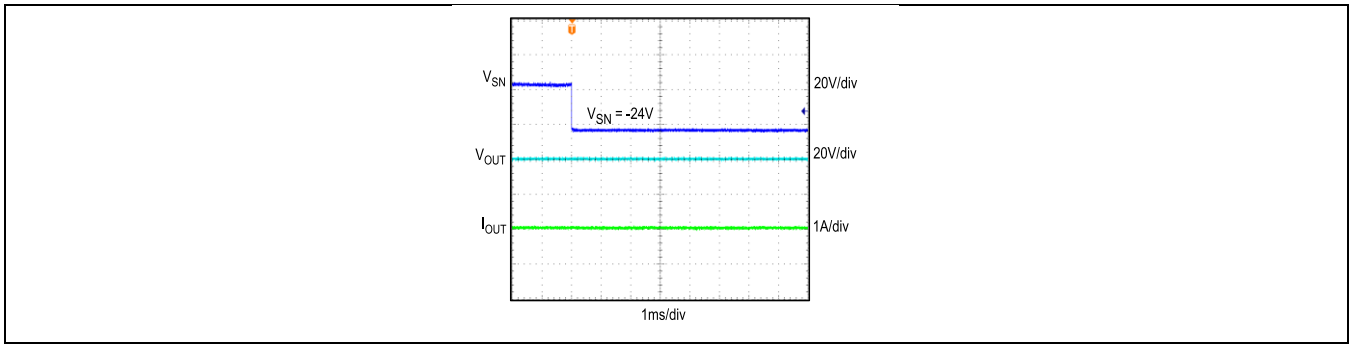


Figure 4. Input Reverse-Polarity Protection at V_{OUT} = 0V and V_{SN} = -24V

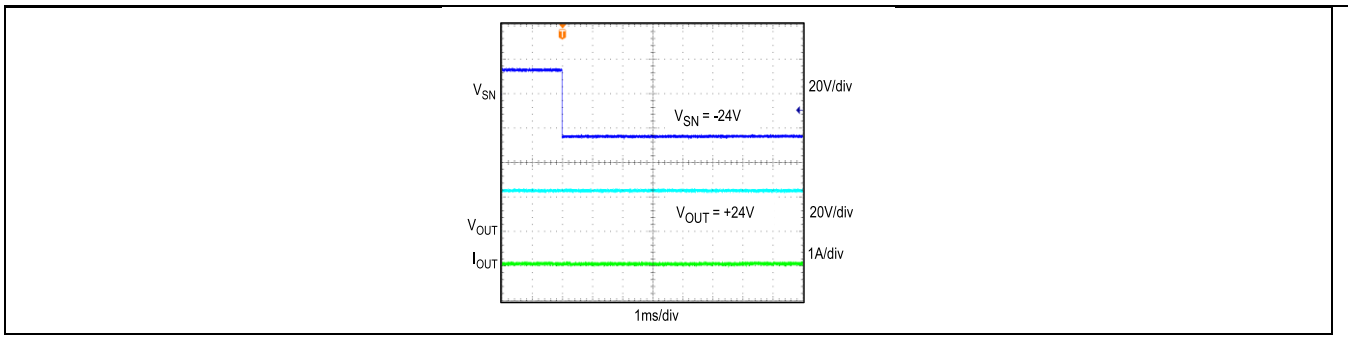


Figure 5. Input Reverse-Polarity Protection at V_{OUT} = +24V and V_{SN} = -24V

Output Reverse-Polarity Protection

The MAX17527A protects itself and input-power connections from accidental reverse output-voltage polarity connections. Reverse output voltage can appear across the OUT and GND pins due to inductive loads or incorrect wiring connections of live loads across the output terminals.

Figure 6 shows the output reverse-polarity protection of the MAX17527A with V_{OUT} = -24V and V_{SN} = 24V and Figure 7 shows the response with V_{OUT} = -24V and V_{SN} = 0V (typical case incorrect wiring). The device can protect the circuit negative output voltage up to –(65 - V_{IN})V. Figure 8 shows the recovery performance from an output reverse polarity fault condition.

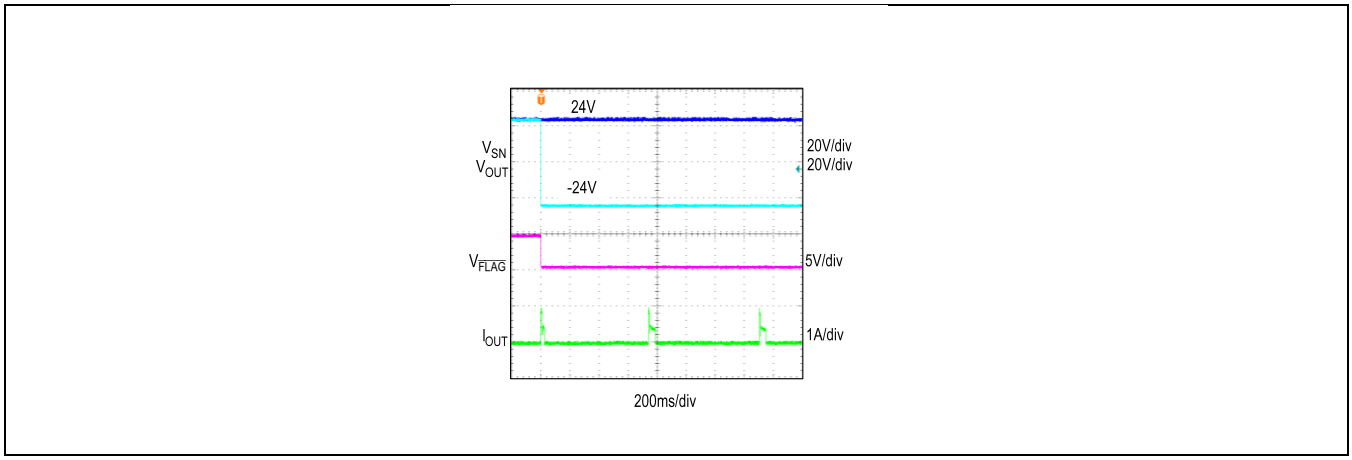


Figure 6. Output Reverse-Polarity Protection in Autotry Mode with V_{OUT} = -24V and V_{SN} = 24V

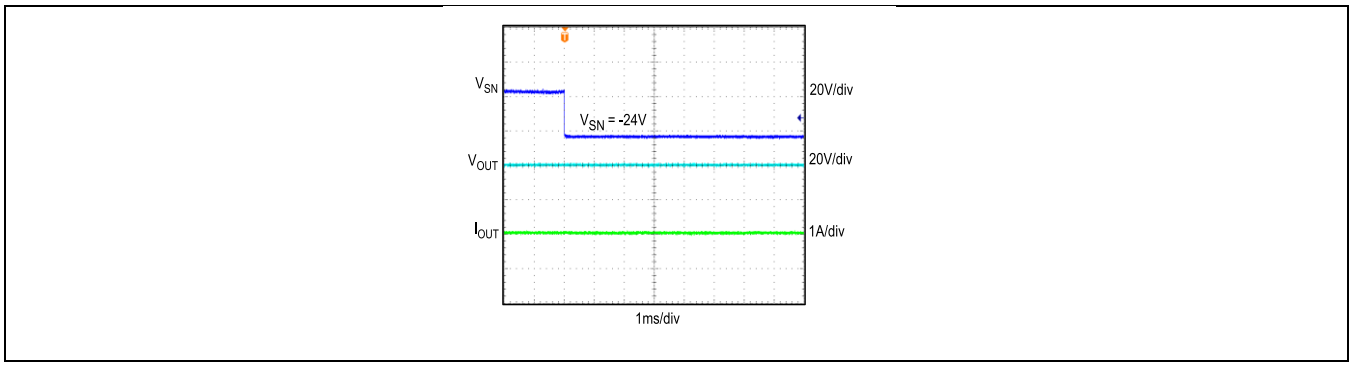


Figure 7. Output Reverse-Polarity Protection in Autotry Mode with V_{OUT} = -24V and V_{SN} = 0V

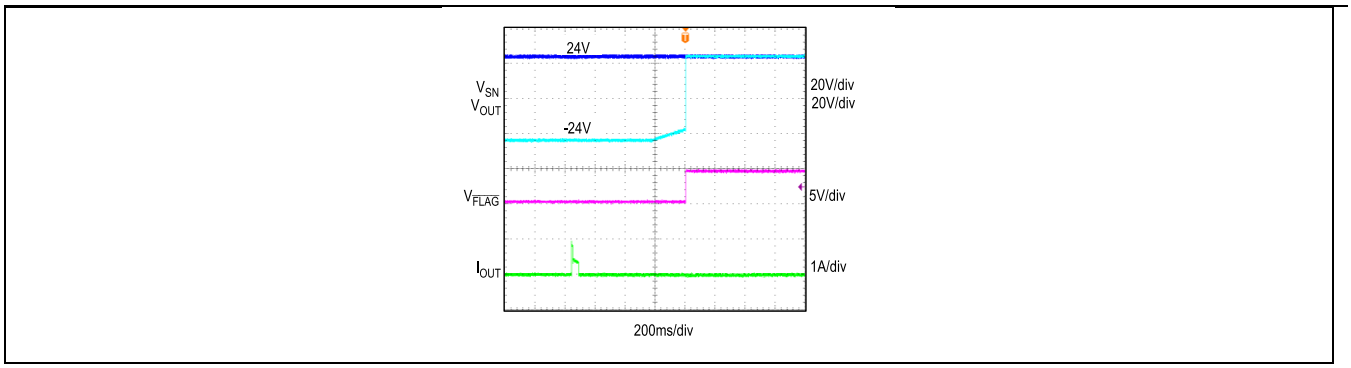


Figure 8. Recovery Performance from the Output Reverse-Polarity Fault with V_{OUT} = -24V Initial Condition and V_{SN} = 24V

Input Debounce Protection

The device features input debounce protection. The device starts operation (turn on the internal nFET) only if the input voltage is higher than the UVLO threshold for a period greater than the debounce time (t_{DEB}). In case the voltage at IN falls below the UVLO threshold before t_{DEB} has passed, the switch remains off. If the voltage at OUT is already above the undervoltage trip level on output (V_{UVLO_OUT}) when the device is turned on through a UVLO/OVLO condition, there is no t_{DEB} time. This is because the device is already out of the power-on reset POR condition with OUT voltage above V_{UVLO_OUT}. When the device is turned on through EN, the t_{DEB} time is always present. *Figure 9* depicts a typical debounce timing diagram.

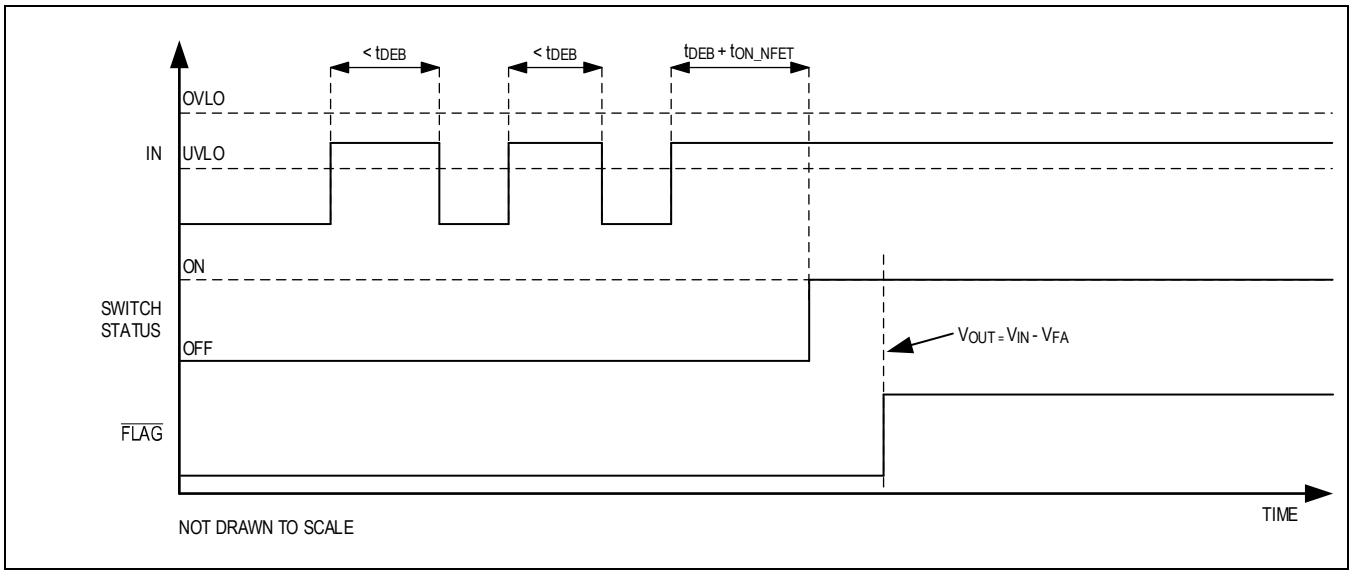


Figure 9. Debounce Timing Diagram

Enable

The MAX17527A can be turned on or off using the enable input pin (EN) to control the power delivery to connected loads. In Latch-Off Mode, the EN pin must be pulled low below 0.4V for at least 30µs (typ) to reset the fault condition, and the device resumes operation. The EN pin is internally pulled up to 1.45V to have an always ON operation when it is left open. *Figure 10* and *Figure 11* show turn-on and turn-off control with EN.

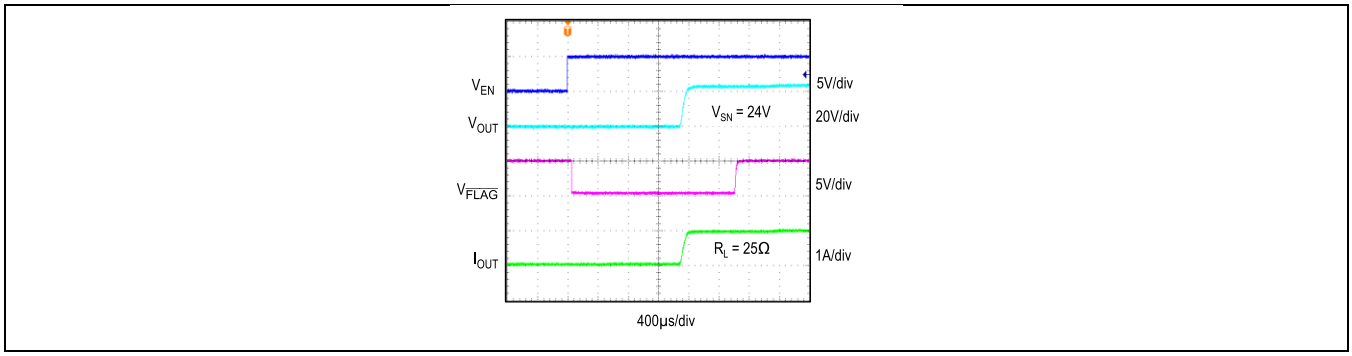


Figure 10. Turn-On Control Through EN Pin

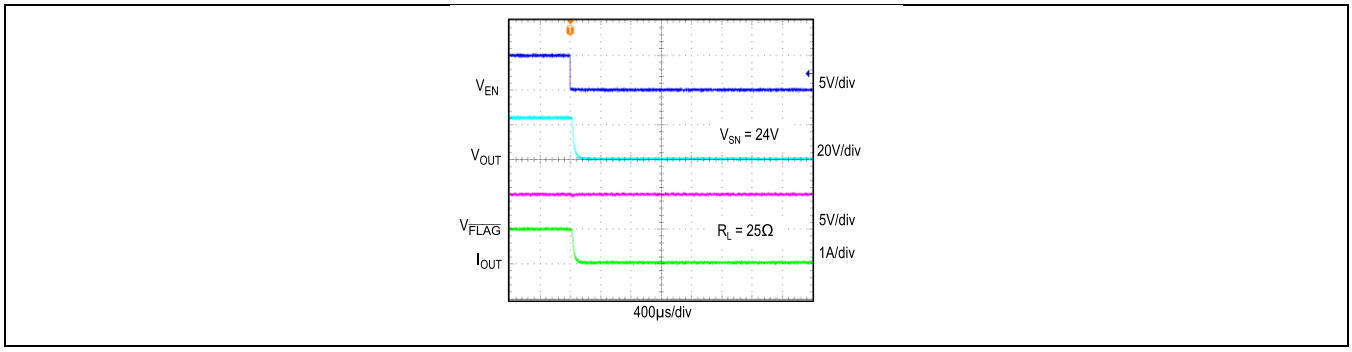


Figure 11. Turn-Off Control Through EN Pin

Startup Control

The device features a startup sequence that continuously limits the current to the set current limit during the startup initial time (t_{STI}), allowing large capacitors present on the output of the switch to be rapidly charged. If the temperature of the device rises to the thermal foldback threshold ($T_{J(FB)}$), the device enters current-limiting mode. In this mode, the device thermally regulates the current through the switch to protect itself while still delivering as much current as possible to the output regardless of the current-limit type selected. If the output is not charged within the startup timeout period (t_{STO}), the switches turn off and IN or EN must be “toggled” to resume normal operation. The t_{STO} timeout period is also applied when there is a restart after a turn-off event caused by UVLO or OVLO. If the output is not charged to the (V_{IN} - V_{FA}) level during this time, the device turns off, and IN or EN must be pulled low for at least 30µs (typ) to resume normal operation.

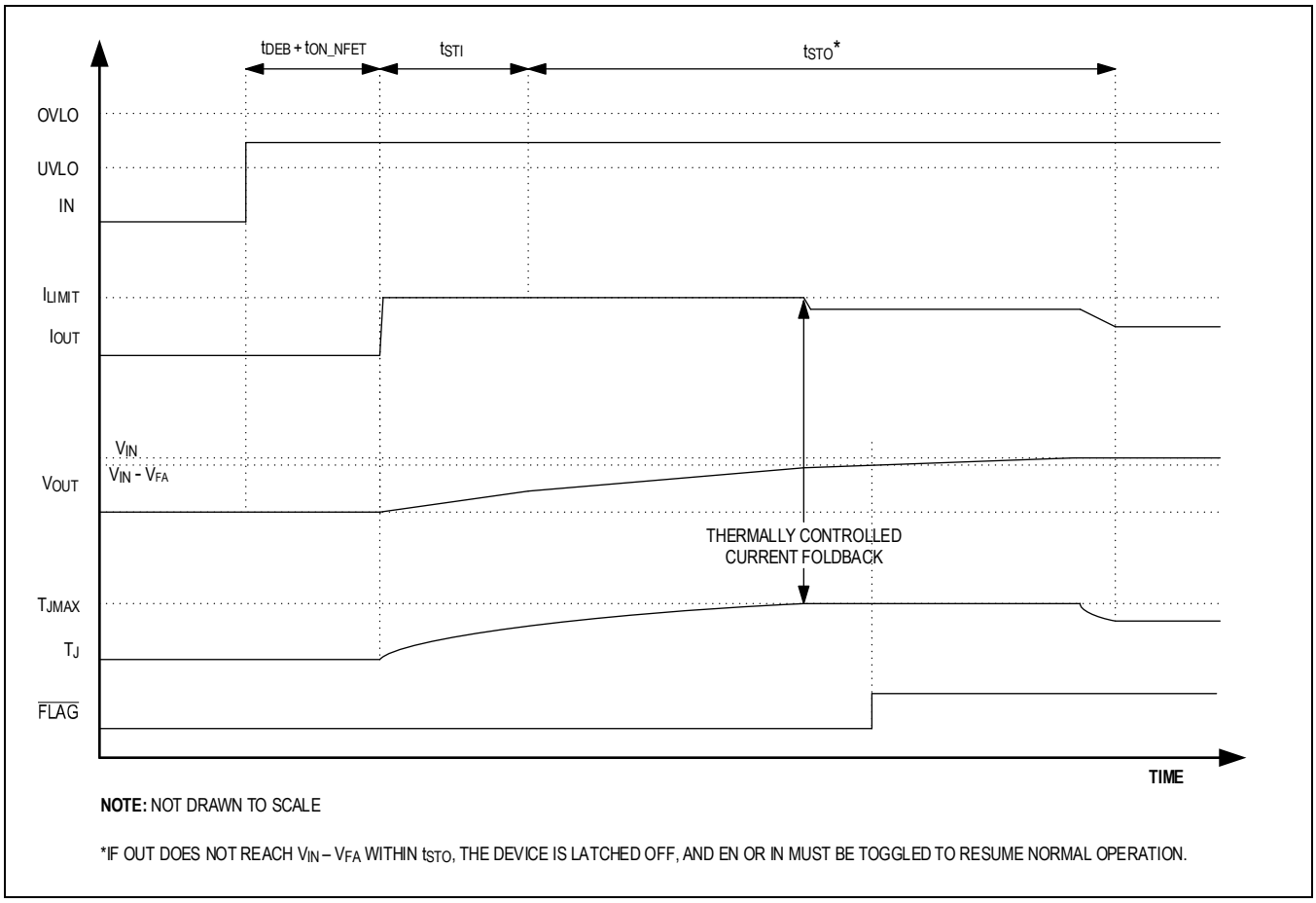


Figure 12. Startup Timing Diagram

Setting the Current-Limit Threshold

Connect a resistor between SETI and GND to program the current-limit threshold in the device. Use the following equation to calculate the current-limit setting resistor:

$$R_{SETI}(k\Omega) = \frac{37500}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current limit in mA.

Do not use an R_{SETI} smaller than 6kΩ. *Table 1* shows current-limit thresholds for different resistor values.

The device offers a read-out of the current flowing into the IN pin on the SETI pin. A current mirror with a ratio of C_{IRATIO} is implemented using a current-sense auto-zero operational amplifier. The mirrored current flows out through the SETI pin into the external current-limit resistor. The voltage on the SETI pin provides information about the IN current with the following relationship:

$$I_{IN-OUT}(mA) = \frac{V_{SETI}(V)}{R_{SETI}(k\Omega)} \times C_{IRATIO}$$

Table 1. Current-Limit Threshold vs. SETI-Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT (A)
62.50	0.6
37.50	1.0
25.00	1.5
18.75	2.0
15.00	2.5
12.50	3.0
10.71	3.5
9.37	4.0
8.33	4.5
7.50	5.0
6.82	5.5
6.25	6.0

If SETI is left unconnected, $V_{SETI} \geq 1.5V$. The current regulator does not allow any current to flow. The device performs a check on the SETI pin for the first time it exits a shutdown condition. If the resistor placed on SETI is below 3.2kΩ, the switch remains off and the $\overline{FLAG}$ asserts. *Figure 13* shows the SETI response during a load step event. For best damped measurement, the capacitance on the SETI pin shall be limited to 30pF.

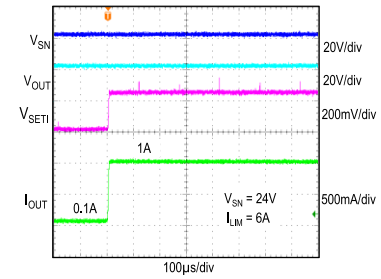


Figure 13. SETI Response During a Load Step Event

Current-Limit Feature

The MAX17527A features precise current limiting during overload and short-circuit faults. When the device's current exceeds the current limit set by R_{SETI} resistance, it regulates the current to the I_{LIM} value for t_{BLANK} time. Thereafter, the device operation depends on the current-limit type selected. *Figure 14* shows the performance of the MAX17527A with an overload condition, and *Figure 15* shows recovery from an overload condition in autoretry mode.

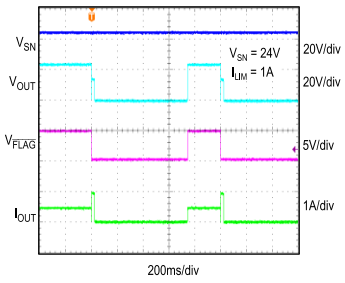


Figure 14. Overload Fault Response in Autoretry Mode

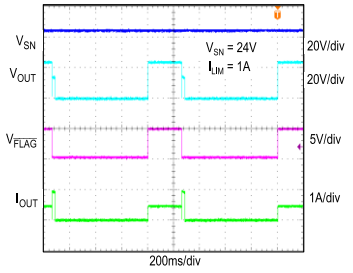


Figure 15. Recovery Response During Coming Out of an Overload Fault in Autoretry Mode

Current-Limit Type Select

The device features three selectable current-limiting modes. During power-up, the device defaults to continuous mode and follows the procedure defined in the *Startup Control* section. Once the device is successfully powered on and t_{STO} has expired, the device senses the condition of the CLMODE pin. The CLMODE pin is used to program the overcurrent response of the device in one of the following three modes:

- Continuous mode: CLMODE is left unconnected
- Autoretry mode: CLMODE is connected to GND
- Latch-Off mode: a 220kΩ resistor is connected between CLMODE and GND

Continuous Current Limit

In continuous current-limit mode, when current through the device reaches the current-limit threshold, the device limits the current to the programmed current limit. The $\overline{FLAG}$ pin asserts when the voltage drop across the internal switch rises above V_{FA}, and deasserts when it falls below V_{FA}. *Figure 16* depicts typical behavior in continuous current-limit mode.

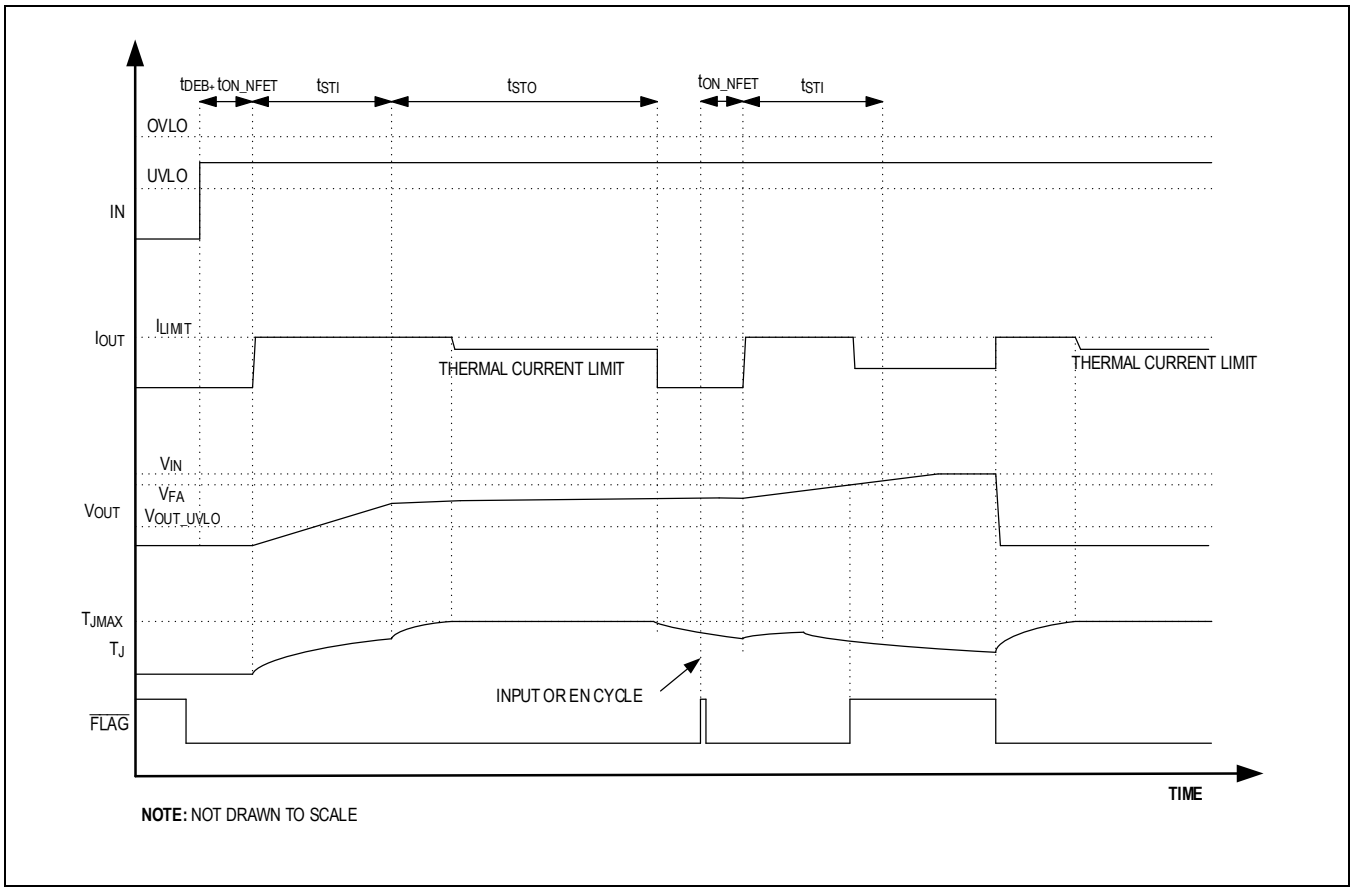


Figure 16. Continuous-Fault Timing Diagram

Autoretry Current Limit

In autoretry current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts when the voltage drop across the internal switch rises above V_{FA} and deasserts when it falls below V_{FA}. The timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed. If the overcurrent condition remains for the t_{BLANK} period, a retry time delay (t_{RETRY}) starts immediately after t_{BLANK} has elapsed. During t_{RETRY} time, the switch remains off. Once t_{RETRY} has elapsed, the switch is turned back on again. If the fault still exists, the cycle repeats and the $\overline{FLAG}$ pin remains asserted. If the overcurrent condition is resolved, the switch stays on.

The autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is on during t_{BLANK} time, the supply current is held at the current-limit. During t_{RETRY} time, there is no current through the switch. Thus, the average output current is much less than the programmed current-limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK} + t_{STI}}{t_{BLANK} + t_{STI} + t_{RETRY}}\right]$$

With a 24ms (typ) t_{BLANK}, 24ms (typ) t_{STI}, and 720ms (typ) t_{RETRY}, the duty cycle is 6.25% resulting in 93.75% power reduction when compared to the switch being on the entire time. *Figure 17* depicts typical behavior in the autoretry current-limit mode.

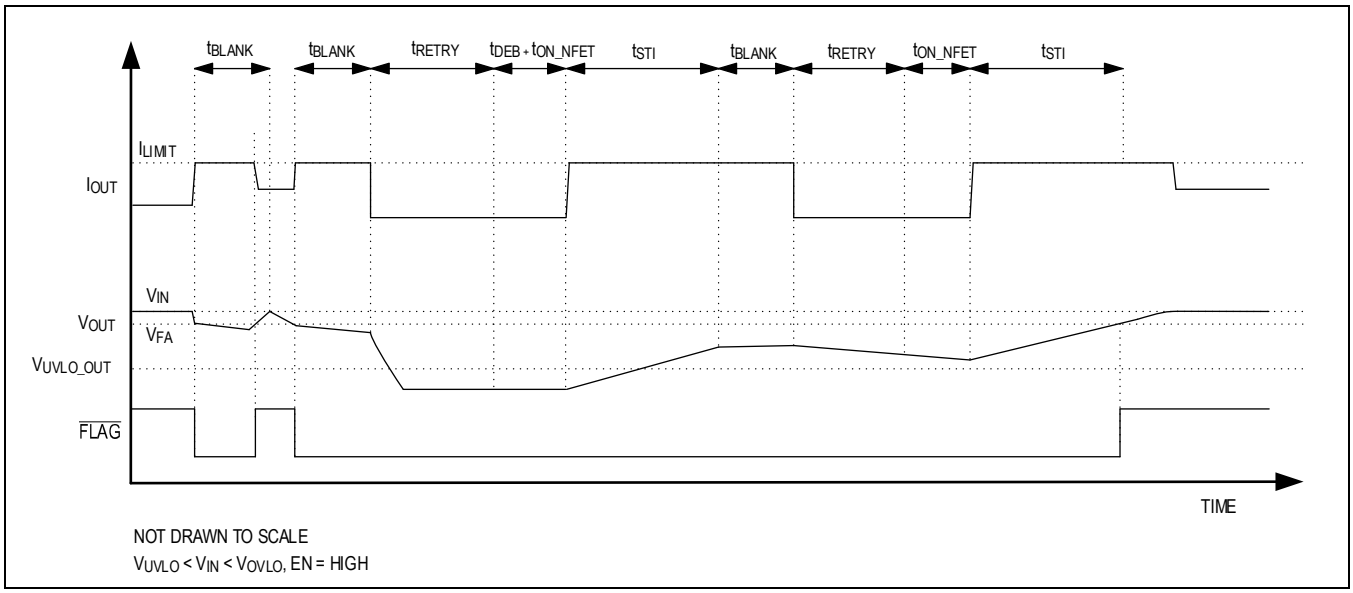


Figure 17. Fault Timing Diagram

Latch-Off Current Limit

In latch-off current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts when the voltage drop across the internal switch rises above V_{FA} and deasserts when it falls below V_{FA}. The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond t_{BLANK}. To reset the switch, either by holding the control logic (EN) below 0.4V for at least 30µs (typ) or cycle the input voltage. *Figure 18* depicts typical behavior in latch-off current-limit mode.

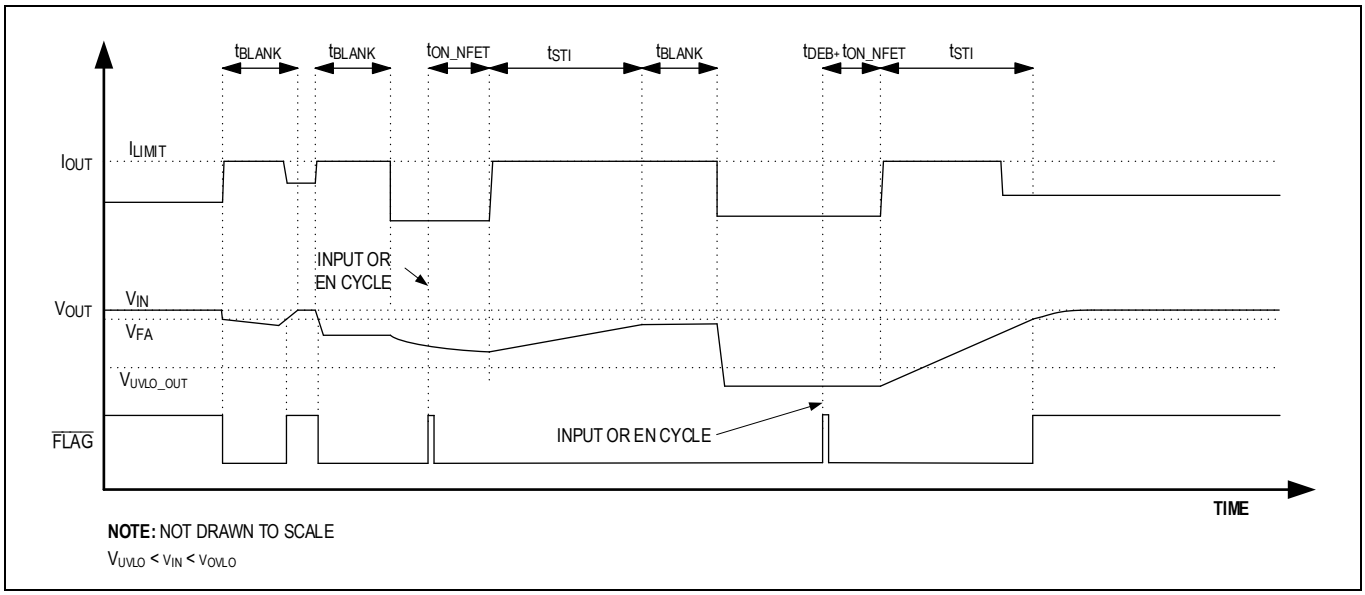


Figure 18. Latchoff-Fault Timing Diagram

Short Circuit Protection

During an output short circuit event, the current through the device increases very rapidly. The device incorporates a fast-trip current comparator to limit the output short circuit peak current. The fast-trip current comparator turns off the internal nFET within 3µs (t_{DELAY1}), when the current through the internal nFET exceeds the overcurrent protection threshold (I_{OCP}). The I_{OCP} is internally set to 24A(typ). After a time delay of 200µs (t_{DELAY2}), the internal nFET turns back on and limits the output current to the programmed current limit and operates as described in earlier current limit mode sections. The external nFET remains on during the short-circuit event. *Figure 19* and *Figure 20* illustrate the behavior of the system when the current exceeds the I_{OCP} threshold.

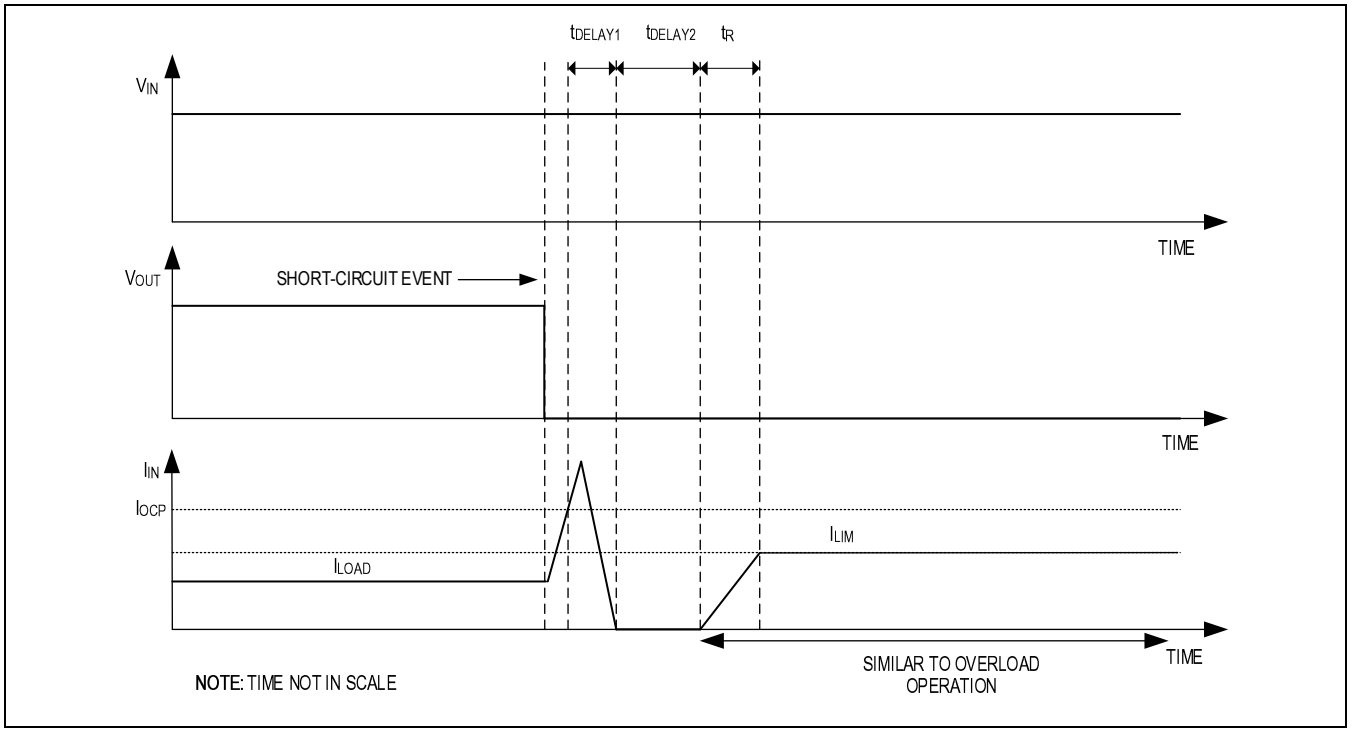


Figure 19. Fast Overcurrent Trip Timing Diagram

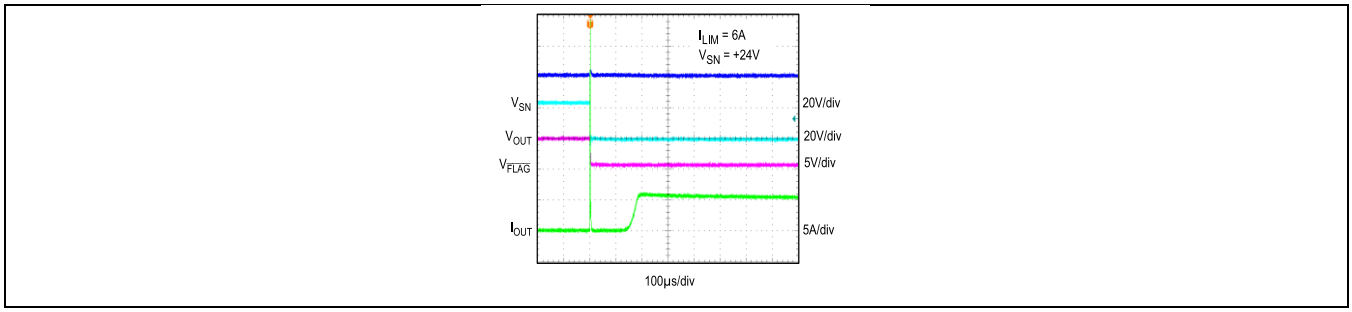


Figure 20. Short Circuit Response

Reverse Current Protection

The reverse current-protection feature is enabled when used with external nFET. The device prevents reverse current flow from OUT to IN pins.

If a reverse current condition is detected ((V_{IN} - V_{OUT}) < $V_{RIB\_}$), the external nFET is turned off. When the reverse current condition no longer exists ((V_{SN} - V_{OUT}) > V_{RIB_RISING}), the external nFET is turned back ON after $t_{ON\_EXTNFET}$. If the reverse current condition is the only fault (no UVLO, no OVLO, no thermal fault, no forward overcurrent fault), then the internal nFET is kept on, otherwise the internal nFET is also turned off. *Figure 21* depicts typical behavior in a slow or fast reverse current condition.

The device contains two reverse-current thresholds with slow (Typ 17µs) and fast (Typ 108ns) response time for reverse-current protection. The threshold value for slow reverse is 5.4mV (typ) whereas for fast reverse, it is 100mV (typ). This feature results in robust operation in a noisy environment, while still delivering fast protection for a severe fault, such as input short-circuit or hot plug-in at the OUT pins. The $\overline{FLAG}$ pin does not assert during a reverse current condition.

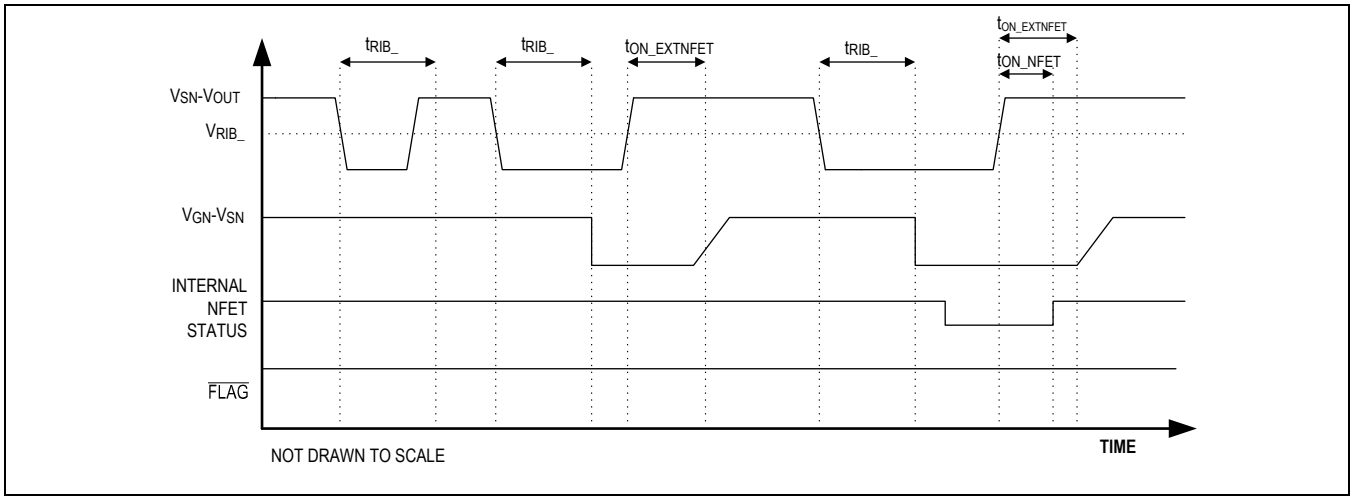


Figure 21. Reverse-Current-Fault Timing Diagram

Power Limit

The MAX17527A features a unique power limit feature that allows the set current limit to be modified automatically based on an external voltage (V_{EXT}). The MAX17527A monitors a fraction of this external voltage on the PLIM pin and dynamically adjusts the current limit set by the SETI pin resistor based on the following relationship:

When $V_{PLIM} \leq V_{PLIM\_TH}$,

Current is limited to I_{LIM} value set by R_{SETI}

When $V_{PLIM} > V_{PLIM\_TH}$,

Current is limited to $\frac{I_{LIM} \times V_{PLIM\_TH}}{V_{PLIM}}$

Assuming the resistor-divider ratio of K for the resistors R5, R6 configured as shown in the *Typical Operating Circuit*, the above algorithm limits the power (P) delivered by the external voltage source as shown below:

$$V_{PLIM} = V_{EXT} \times K$$

$$P = \frac{V_{EXT} \times I_{LIM} \times V_{PLIM\_TH}}{V_{PLIM}}$$

Hence, $P = \frac{I_{LIM} \times V_{PLIM\_TH}}{K}$

where I_{LIM}, K and V_{PLIM_TH} are essentially constants with tolerances dictated by the design. The device is designed for ±7% power limit accuracy for the range $V_{PLIM\_TH} < V_{PLIM} < 3 \times V_{PLIM\_TH}$, which covers a 3x variation of external voltage (V_{EXT}).

Consider the design requirement of the output power limit (P) is 100W and the current limit is 4A.

The resistor-divider ratio K is calculated as:

$$K = \frac{R6}{R6 + R5} = \frac{I_{LIM} \times V_{PLIM\_TH}}{P}$$

where V_{PLIM_TH} = 0.8. Assuming R6 is 10kΩ, R5 is calculated to be 301kΩ.

In an input power limit application V_{IN} is equal to V_{EXT}, and the PLIM resistor divider is set to determine the input voltage at which the current limit starts decreasing. By setting this voltage and setting the maximum current limit, the maximum "input-power limit" for the application is set. The current limit can also be dynamically modified based on the output voltage by using V_{OUT} equal to V_{EXT}. This feature implements an "output-power limit" function that potentially allows larger output currents to be delivered to charge the output reservoir capacitors at low output voltage conditions experienced after input power returns after an "outage," provided there are no thermal limitations due to excessive power dissipation. The power limit feature is disabled by connecting the PLIM pin to GND. A simplified block diagram of the PLIM feature is shown in *Figure 22*. *Figure 23* shows 100W class 2 output-power limit response.

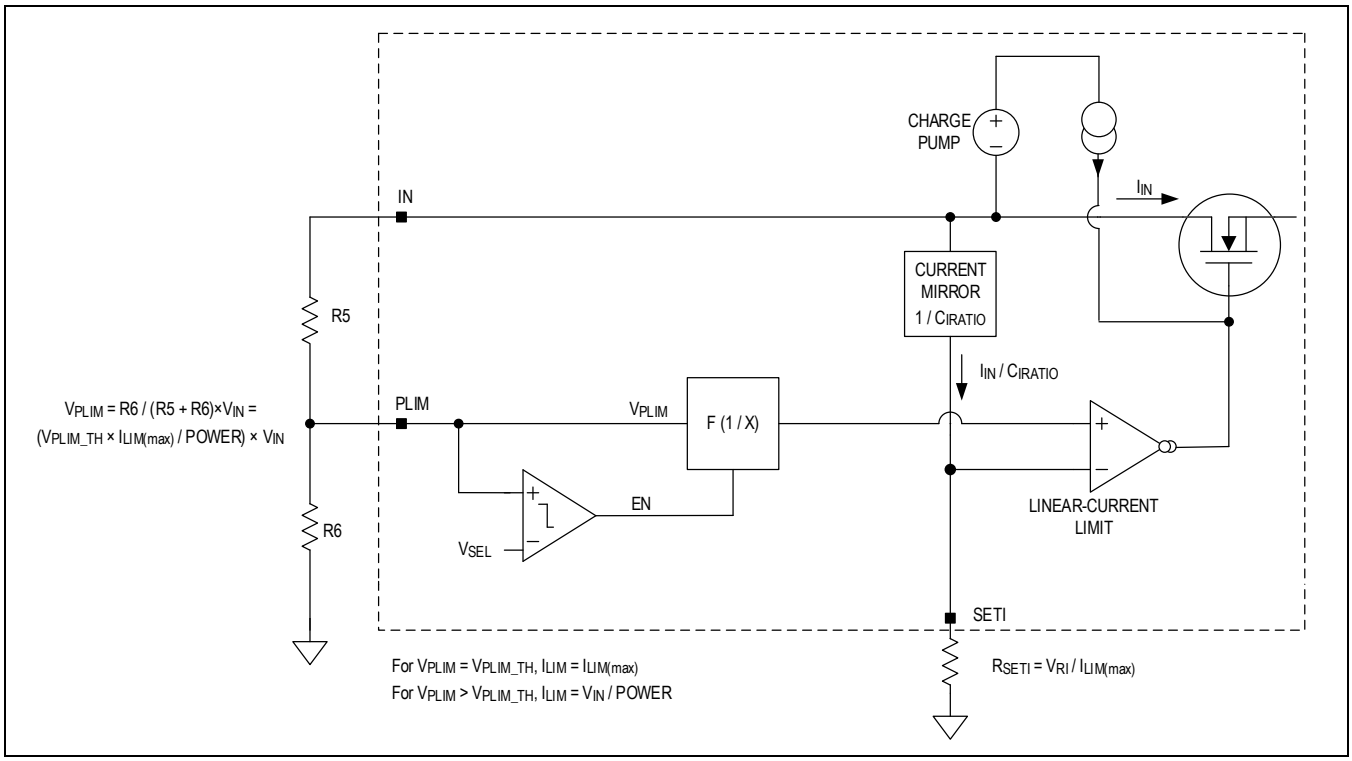


Figure 22. Power Limit Circuit

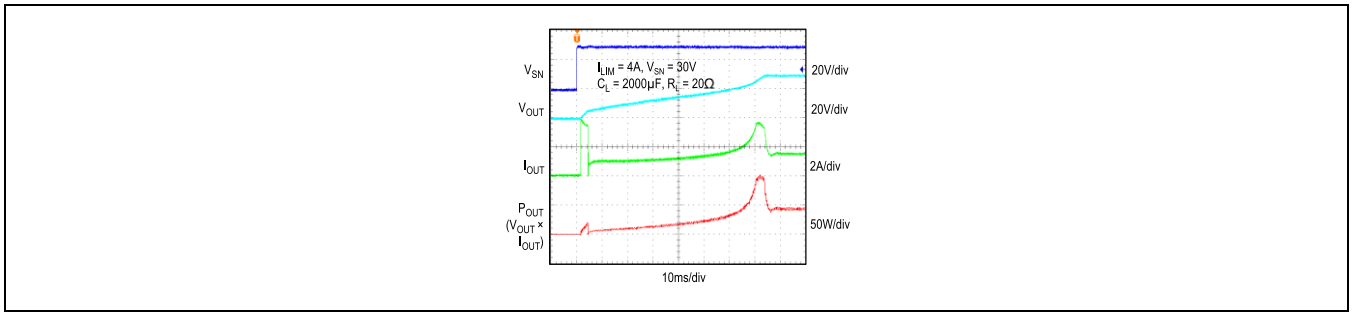


Figure 23. 100W Class 2 Output Power Limit

Fault Output

The device offers an open-drain fault-indicator output ($\overline{FLAG}$). It requires an external pullup resistor to a DC supply. $\overline{FLAG}$ is held low when any of the following conditions occur:

- V_{IN} - V_{OUT} > V_{FA}
- Die temperature exceeds +165°C
- R_{SETI} is less than 3.2kΩ (max)
- Input voltage falls below the UVLO threshold
- Input voltage rises above the OVLO threshold

Table 2 below describes the status of the nFETs along with various fault conditions. $\overline{FLAG}$ pin is also 60V tolerant and when the open drain is on, it has a current protection that turns off the open drain if the current exceeds 4mA. The open drain is then turned back on if the fault condition is cycled.

Table 2. nFETs Status During Faults

CONDITION	INTERNAL nFET STATUS	EXTERNAL nFET STATUS	$\overline{FLAG}$ STATUS
No Fault	ON	ON	HIGH
UVLO	OFF	OFF	LOW
OVLO	OFF	OFF	LOW
Reverse Current with No Other Fault	ON	OFF	HIGH
Overcurrent Protection (I_{OCP}, 24A)	OFF	OFF	LOW
Thermal Shutdown	OFF	OFF	LOW
SETI Grounded*	OFF	OFF	LOW
V_{IN} - V_{OUT} > V_{FA}	X**	X**	LOW

**This condition is checked only at the first power on.*

***The status of the nFETs in this condition depends on the timing and the current limit mode selected.*

Loss of Ground

The device protects loads by turning off the internal and external nFETs in a loss-of-ground event. A loss-of-ground event can be caused by a break in connectivity between the ground reference of the system control and the IC ground net around MAX17527A. This feature eliminates the requirement for additional external circuits for protection from loss-of-ground events. Additional components are required for the protection of signal pins (EN, SETI, $\overline{FLAG}$). *Figure 24* shows the typical behavior during a loss-of-ground event.

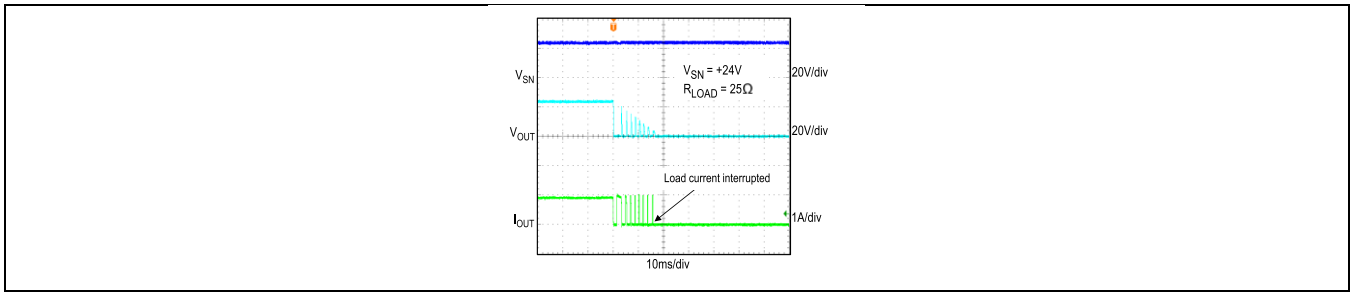


Figure 24. Load Current Interruption During a Loss-of-Ground Event

Thermal Shutdown Protection

The device has a thermal-shutdown feature to protect against overheating, in addition to a thermal foldback current limit control. When the junction temperature reaches 150°C (typ), the current limit is internally lowered to reduce the power dissipation on the internal nFET, and regulate the junction temperature at around 150°C. In extreme conditions, the device turns off and asserts the $\overline{FLAG}$ pin when the junction temperature exceeds +165°C (typ). The device exits thermal shutdown and resumes normal operation after the junction temperature cools by 10°C (typ), except when in latch-off mode when the device remains latched off.

The thermal shutdown behaves similarly to the current limit. In mode, the thermal shutdown works with the autoretry timer. When the junction temperature falls below the falling thermal shutdown threshold, the device turns on after the t_{RETRY}. In latch-off mode, the device latches off until either the input power is cycled or the EN pin is toggled. In continuous mode, the device is only turned off when the temperature is over the limit and turns back on after t_{DEB} when the temperature reaches the falling thermal-shutdown threshold. There is no blanking time for thermal protection. *Figure 16*, *Figure 17* and *Figure 18* depict typical behavior under different current limit modes.

Applications Information

IN Capacitor

A 1µF capacitor from the IN pin to GND is recommended to hold input voltage during sudden load-current changes.

Hot Plug-In at IN Terminal

In many powering applications, an input-filtering capacitor is required to lower the radiated emission and enhance the ESD capability. In hot plug-in applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to a maximum 60V shall be placed close to the input terminals for enhanced protection.

Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The device detects reverse current entering at the OUT pin and flowing out of the IN pin and turns off the external nFET. The magnitude of the reverse current depends on the inductance of input circuitry and any capacitance installed near the IN pins.

Voltage Interruption Response

The MAX17527A features fast recovery after voltage interruption during input-supply brownout tests. The device takes 200µs (typ) to turn on the internal nFET and 1.2ms (typ) to turn on the external nFET when recovering from a brownout fault. *Figure 25* illustrates the performance of voltage interruption and recovery response of the MAX17527A.

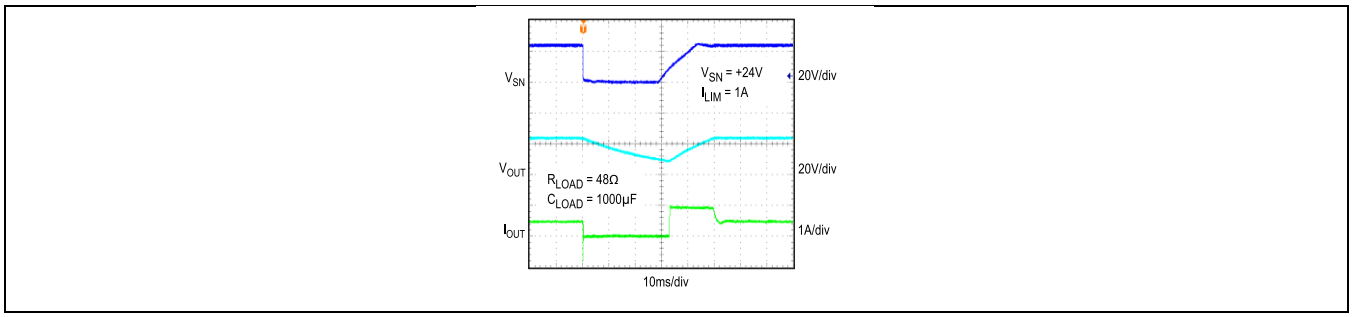


Figure 25. Voltage Interruption and Recovery Response

OUT Capacitor

The maximum capacitive load (C_{MAX}) that can be connected is a function of the current-limit setting (I_{LIM} in A), the startup initial time (t_{STI} in ms) and startup timeout (t_{STO} in ms), and the input voltage. The C_{MAX} is calculated using the following relationship:

$$C_{MAX}(mF) = I_{LIM}(A) \times \left(\frac{t_{STI}(ms) + t_{STO}(ms)}{V_{IN}(V)}\right)$$

For example, for V_{IN} = 24V, t_{STO} (typ) = 1200ms, t_{STI} (typ) = 24ms, and I_{LIM} = 3A, C_{MAX} is 153mF.

Output capacitor values in excess of C_{MAX} can trigger false overcurrent conditions. Note that above expression assumes no load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current resulting in a large charging period; hence, the possibility of a false overcurrent condition.

In practical applications, the C_{MAX} value is limited by the thermal performance of the PCB. Poor thermal design can cause the thermal foldback current-limiting function of the device to kick in too early, which can further limit the maximum capacitance that can be charged. Therefore, good thermal PCB design is imperative to charge large capacitor banks.

Hot Plug-In at OUT Terminal

In some applications, there might be a possibility of applying an external voltage at the OUT terminal of the device with or without the presence of an input voltage. During these conditions, the device detects any reverse current entering the OUT pin and flowing out of the IN pin and turns off the external nFET. Parasitic cable inductance along with input and output capacitors cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection device to see up to twice the applied voltage, which can damage the device. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the absolute maximum ratings.

OUT Clamping Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, an output clamp is recommended. This clamp can be implemented with a TVS and a diode as shown in the *Typical Operating Circuit*. This is required to clamp a negative spike on the OUT pin due to the inductive kickback during an output short-circuit event within the safe operating region. Maximum negative clamping voltage of the TVS for a maximum input voltage of the V_{INMAX} is limited to $(60\text{-}V_{INMAX})V$ in order to ensure the IN to OUT pin voltage does not exceed 60V.

Layout and Thermal Dissipation

To optimize the switch response to output short-circuit conditions, it is important to reduce the effect of undesirable parasitic inductance by keeping all traces as short as possible. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During steady-state operation, the power dissipation is typically low, and the package temperature change is usually minimal. PCB layout designs need to meet two challenges: (a) high current in input and output paths; and (b) heat dissipation. It is recommended to use 70µm copper on an FR4 isolator in a four-layer configuration. The layer stack needs to be Top (routing), GND (plane), Power (plane, connected to V_{OUT}), and Bottom (routing), in this order from top to bottom. Install the IC on an exposed pad landing of minimum 2.54mm x 2.54mm with at least five through vias to the GND plane. The vias should be 0.8128mm in diameter with a 0.4064mm plated hole. The hole plating needs to be at least 17.5µm copper. Provide a minimum of 25.4mm x 25.4mm area of copper plane on all four layers. It is important to remember that the inner planes do not contribute much to heat dissipation due to FR4 isolation, but they are important from an electrical point of view. If possible, keep the top and bottom copper areas clear of solder mask as this greatly improves heat dissipation. Use a similarly large copper area connected directly to the OUT pins. A dimension of 25.4mm x 25.4mm is also recommended. This might look oversized for current path requirements, but it is essential for heat dissipation. Keep in mind that heat is generated at the drain junction of the internal nMOS pass FET, which is then eliminated through the five OUT pins and needs to be dissipated on this same copper area.

Connect all five IN pins to a copper area that is at least 3.8mm wide. Using 70µm copper can reduce this requirement to 2.54mm. Remember to provide the same copper trace width on the source connection, when using the external nMOS pass FET (with the source connected to the IN pins). Use extreme caution when placing the decoupling capacitors to the IN and OUT pins. The tendency to go as close as possible to the IC pins might interfere with the minimum requirement of the trace width above. It is important to note that the return load current does not flow through the IC; therefore, it is important to provide an external ground trace of at least the same width as the input/output one. Use of a GND plane is recommended. Connect the input and output grounds to this plane using at least four plated vias each. The vias should be 2.1336mm in diameter (or 1.524mm x 1.524mm, if square) with a 0.889mm plated hole.

ESD Protection

No capacitor is required for ±2kV (type) (HBM) ESD on IN. All pins have ±2kV (HBM) ESD protection. In applications in which an external nFET is used, see the *IN Capacitor* section.

Figure 26 shows the Human Body Model and *Figure 27* shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

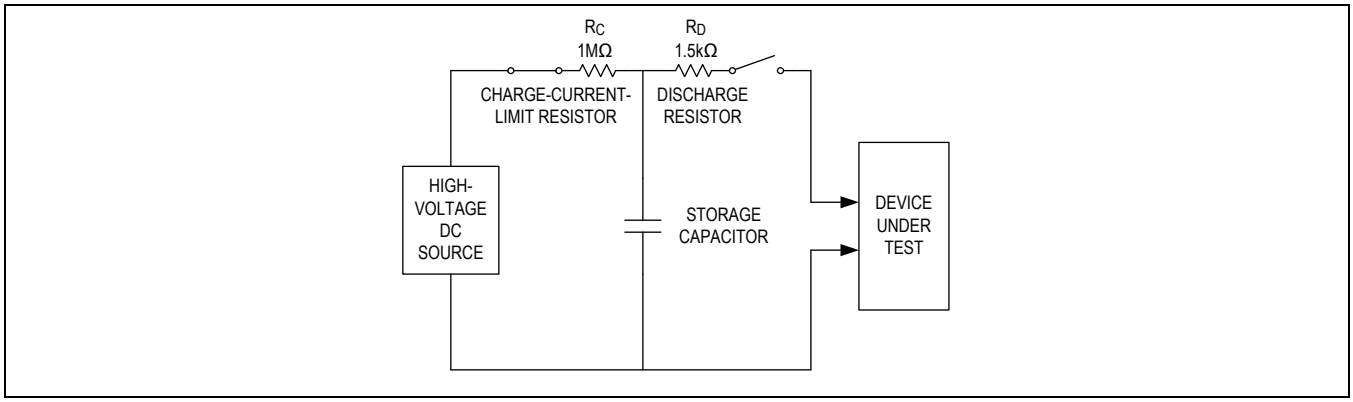


Figure 26. Human Body ESD Test Model

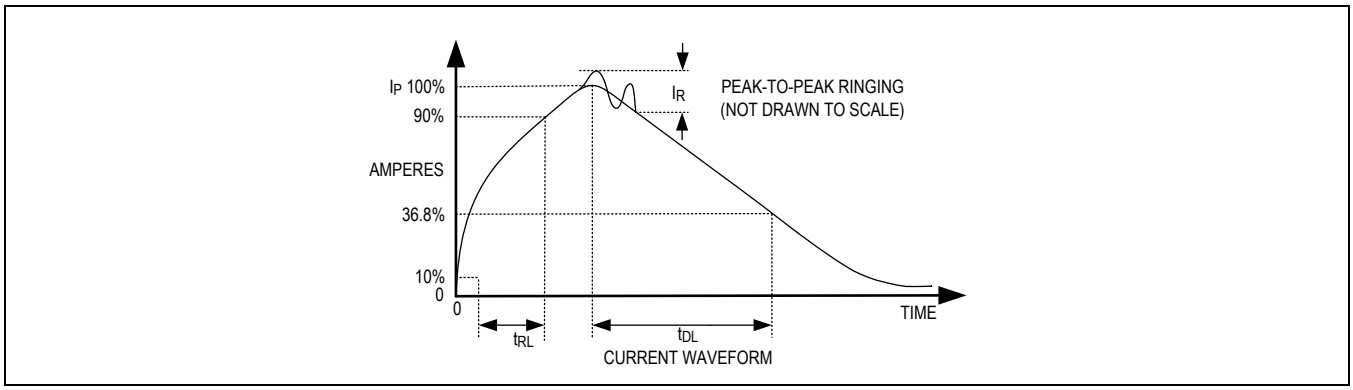
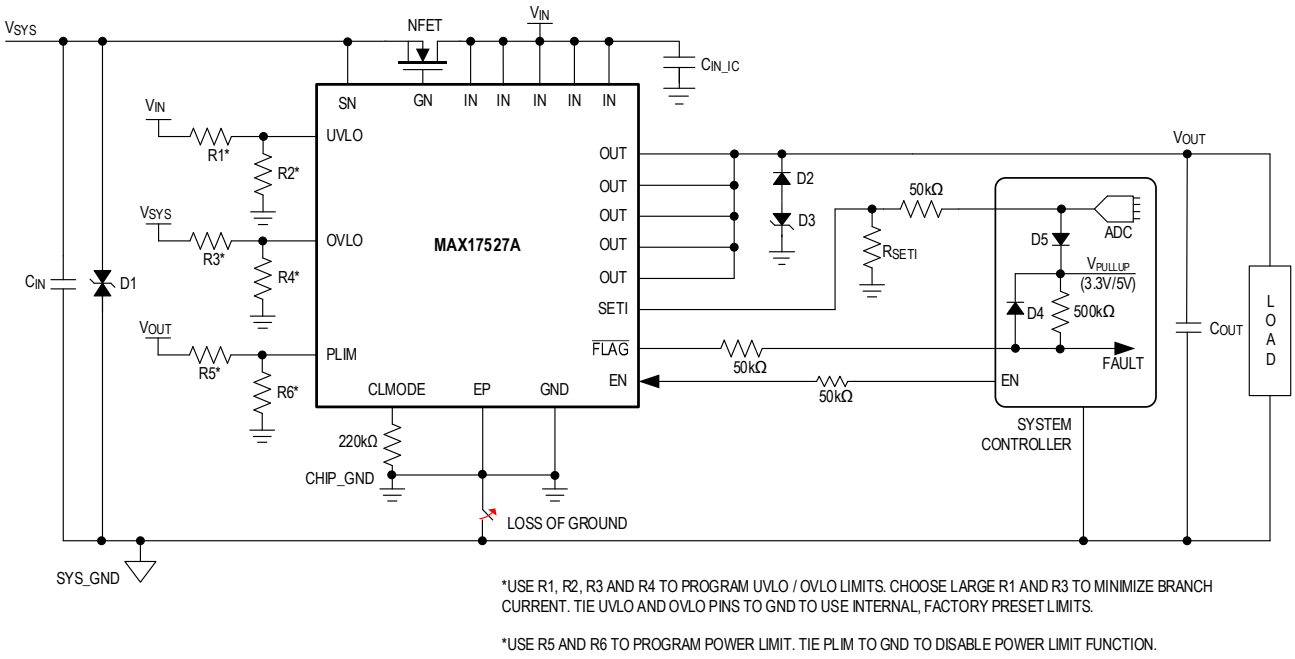


Figure 27. Human Body Current Waveform

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17527AATP+	-40°C to +125°C	20 TQFN-EP*
MAX17527AATP+T	-40°C to +125°C	20 TQFN-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*