MAX17542G

42V, 1A, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The MAX17542G high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over 4.5V to 42V input. The converter can deliver up to 1A and generates output voltages from 0.9V up to 0.92 x V_{IN}. The feedback (FB) voltage is accurate to within ±1.7% over -40°C to +125°C.

The MAX17542G uses peak-current-mode control with pulse-width modulation (PWM) and operates with fixed 600kHz switching frequency at any load. The device is available in a 10-pin (3mm x 2mm) TDFN package. Simulation models are available.

Applications

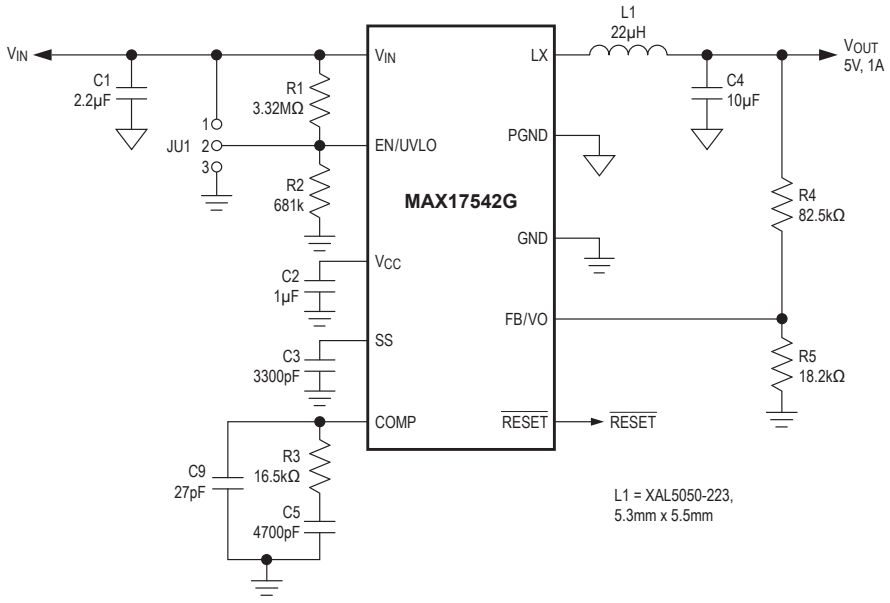
- Industrial Process Control
- HVAC and Building Control
- Base Station, VOIP, Telecom
- Home Theatre
- Battery-Powered Equipment
- General-Purpose Point of Load

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 42V Input
  - Adjustable 0.9V to 92%V_{IN} Output
  - Delivers up to 1A
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - Shutdown Current = 0.9µA (typ)
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Current Limit, Sink Current Limit, and Autoretry Startup
  - Built-In Output-Voltage Monitoring ($\overline{RESET}$ Pin)
  - Programmable EN/UVLO Threshold
  - Adjustable Soft-Start and Prebiased Power-Up
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range / -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

MAX17542G Application Circuit (5V Output, 1A Maximum Load Current)



maxim integrated™

Absolute Maximum Ratings (Note 1)

V_{IN} to GND.....-0.3V to +48V
EN/UVLO to GND.....-0.3V to (V_{IN} + 0.3V)
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
FB, $\overline{RESET}$, COMP, SS to GND .....-0.3V to +6V
V_{CC} to GND.....-0.3V to +6V
GND to PGND.....-0.3V to +0.3V
LX Total RMS Current..... ±1.6A
Output Short-Circuit Duration.....Continuous
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Package Thermal Characteristics

10 TDFN
Continuous Power Dissipation (T_A = +70°C)
(derate 14.9mW/°C above +70°C) (multilayer board).1188.7mW
Junction-to-Ambient Thermal Resistance (θ_{JA}).....67.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....18.2°C/W

Package Information

PACKAGE TYPE: 10-PIN TDFN	
Package Code	T1032N+1
Outline Number	21-0429
Land Pattern Number	90-0082

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		42	V
Input Supply Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode		0.9	3.5	µA
	I_{IN-SW}	Normal switching mode, no load		4.75	6.75	mA
ENABLE/UVLO (EN/UVLO)						
EN Threshold	V_{ENR}	V_{EN} rising	1.194	1.218	1.236	V
	V_{ENF}	V_{EN} falling	1.114	1.135	1.156	
	$V_{EN-TRUESD}$	V_{EN} falling, true shutdown		0.7		
EN Input Leakage Current	I_{EN}	V_{EN} = V_{IN} = 42V, T_A = +25°C		8	200	nA

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO							
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 12V, 0mA < I_{VCC} < 10mA, 12V < V_{IN} < 42V, 0mA < I_{VCC} < 2mA		4.65	5	5.35	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V		15	40	80	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA		4.1			V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising		3.85	4	4.15	V
	V_{CC-UVF}	V_{CC} falling		3.55	3.7	3.85	
POWER MOSFETs							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.5A (sourcing)	T_A = +25°C		0.55	0.85	Ω
			T_A = T_J = +125°C (Note 3)			1.2	
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.5A (sinking)	T_A = +25°C		0.2	0.35	Ω
			T_A = T_J = +125°C (Note 3)			0.47	
LX Leakage Current	I_{LX_LKG}	V_{EN} = 0V, T_A = +25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} - 1V)				1	µA
SOFT-START (SS)							
Charging Current	I_{SS}	V_{SS} = 0.5V		4.7	5	5.3	µA
FEEDBACK (FB/VO)							
FB Regulation Voltage	V_{FB_REG}			0.884	0.9	0.916	V
FB Input Bias Current	I_{FB}	V_{FB} = 0.9V				100	nA
OUTPUT VOLTAGE (V_{OUT})							
Output Voltage Range	V_{OUT}			0.9		0.92 x V_{IN}	V
TRANSCONDUCTANCE AMPLIFIER (COMP)							
Transconductance	G_M	I_{COMP} = ±2.5µA		510	590	650	µS
COMP Source Current	I_{COMP_SRC}			19	32	55	µA
COMP Sink Current	I_{COMP_SINK}			19	32	55	µA
Current-Sense Transresistance	R_{CS}			0.45	0.5	0.55	V/A
CURRENT LIMIT							
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$			1.4	1.65	1.9	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$			1.45	1.7	2	A
Sink Current-Limit Threshold	$I_{SINK-LIMIT}$			0.56	0.65	0.74	A

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

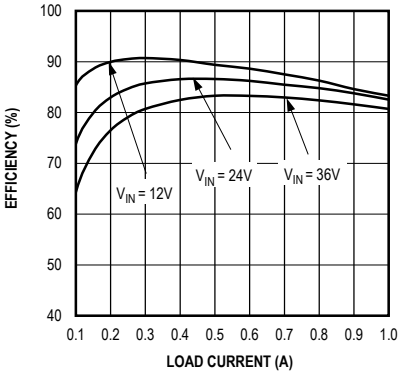
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMINGS						
Switching Frequency	f_{SW}	V_{FB} > $V_{OUT-HICF}$	560	600	640	kHz
		V_{FB} < $V_{OUT-HICF}$	280	300	320	
Events to Hiccup after Crossing Runaway Current Limit				1		Event
V_{OUT} Undervoltage Trip Level to Cause Hiccup	$V_{OUT-HICF}$	V_{SS} > 0.95V (soft-start is done)	69.14	71.14	73.14	%
HICCUP Timeout				32,768		Cycles
Minimum On-Time	t_{ON_MIN}			75	120	ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.98 x V_{FB-REG}	92	94	96	%
LX Dead Time				5		ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 1mA			0.02	V
$\overline{RESET}$ Output Leakage Current High		V_{FB} = 1.01 x V_{FB-REG}, T_A = +25°C			0.45	µA
V_{OUT} Threshold for $\overline{RESET}$ Falling	$V_{OUT-OKF}$	V_{FB} falling	90.5	92.5	94.5	%
V_{OUT} Threshold for $\overline{RESET}$ Rising	$V_{OUT-OKR}$	V_{FB} rising	93.5	95.5	97.5	%
$\overline{RESET}$ Delay After FB Reaches 95% Regulation		V_{FB} rising		1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

Note 2: All limits are 100% tested at +25°C. Limits over temperature are guaranteed by design.
Note 3: Guaranteed by design, not production tested.

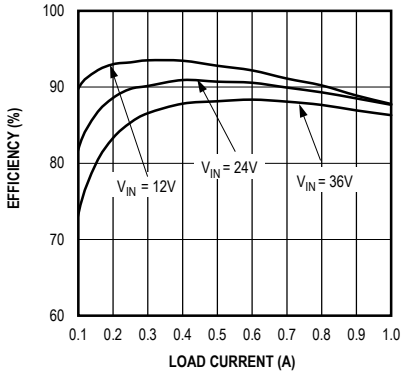
Typical Operating Characteristics

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

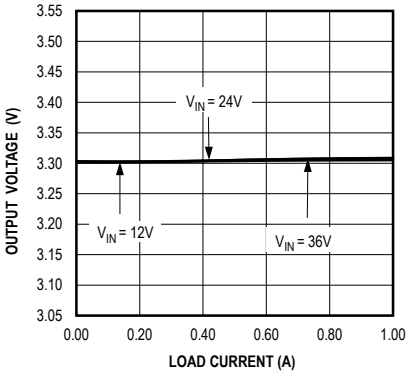
3.3V OUTPUT
EFFICIENCY VS. LOAD CURRENT
FIGURE 5 CIRCUIT



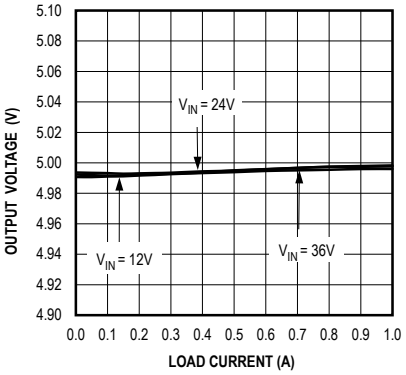
5V OUTPUT
EFFICIENCY VS. LOAD CURRENT
FIGURE 6 CIRCUIT



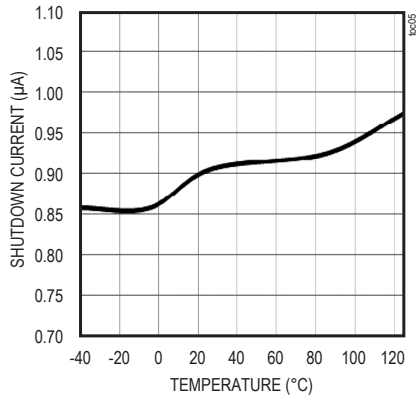
3.3V OUTPUT
LOAD AND LINE REGULATION
FIGURE 5 CIRCUIT



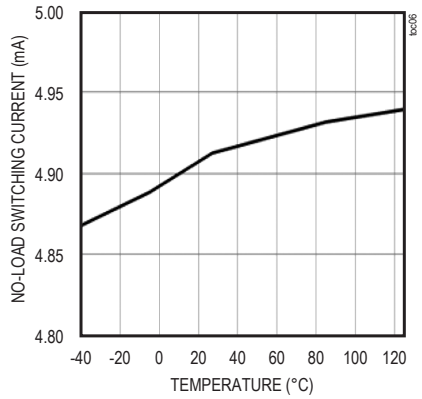
5V OUTPUT
LOAD AND LINE REGULATION
FIGURE 6 CIRCUIT



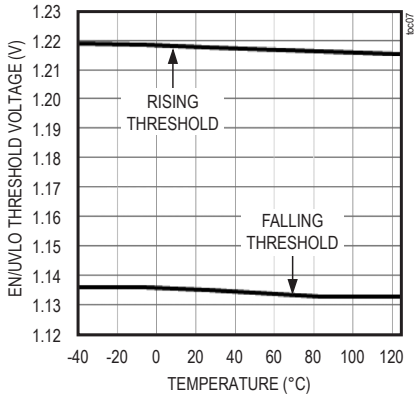
SHUTDOWN CURRENT
vs. TEMPERATURE



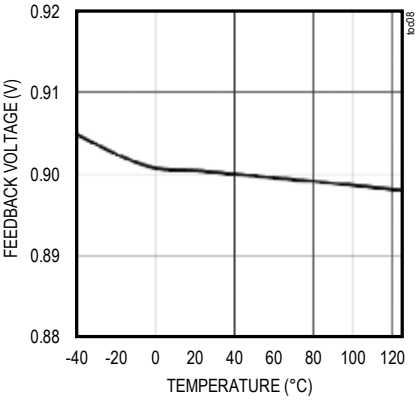
NO-LOAD SWITCHING CURRENT
vs. TEMPERATURE



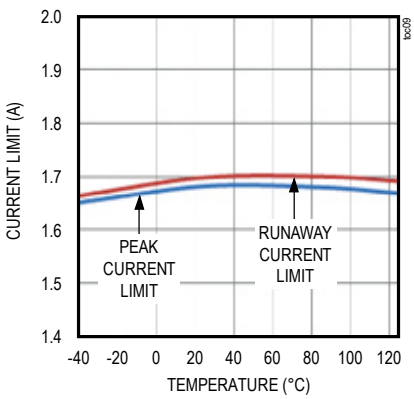
EN/UVLO THRESHOLD
vs. TEMPERATURE



FEEDBACK VOLTAGE
vs. TEMPERATURE



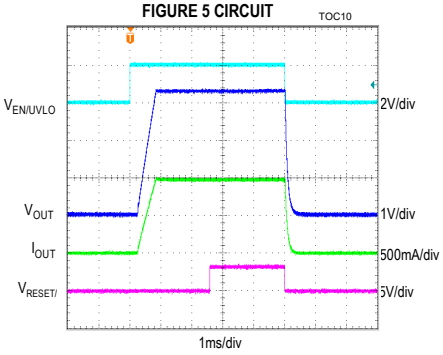
PEAK AND RUNAWAY CURRENT LIMIT
vs. TEMPERATURE



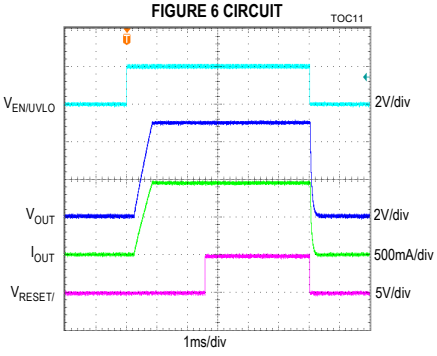
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

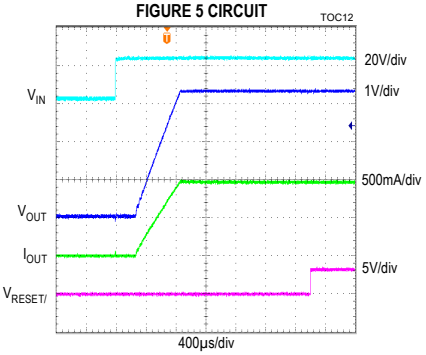
SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, 1A LOAD CURRENT, FIGURE 5 CIRCUIT



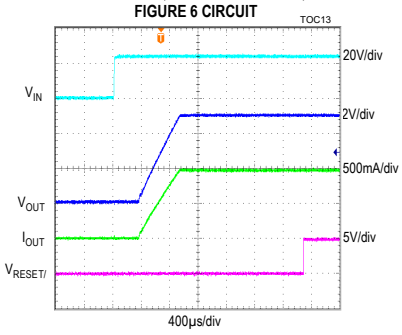
SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, 1A LOAD CURRENT, FIGURE 6 CIRCUIT



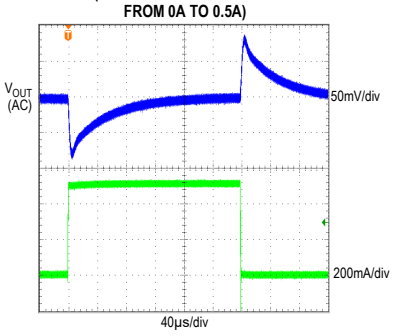
SOFT-START FROM VIN, 3.3V OUTPUT, 1A LOAD CURRENT, FIGURE 5 CIRCUIT



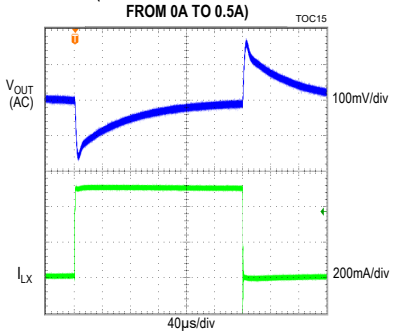
SOFT-START FROM VIN, 5V OUTPUT, 1A LOAD CURRENT, FIGURE 6 CIRCUIT



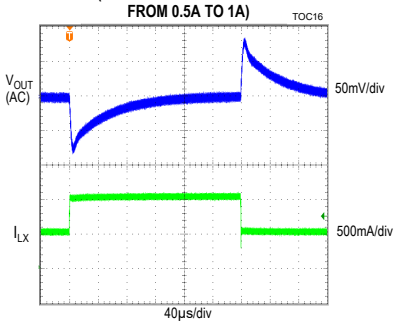
3.3V OUTPUT, FIGURE 5 CIRCUIT (LOAD CURRENT STEPPED FROM 0A TO 0.5A)



5V OUTPUT, FIGURE 6 CIRCUIT (LOAD CURRENT STEPPED FROM 0A TO 0.5A)



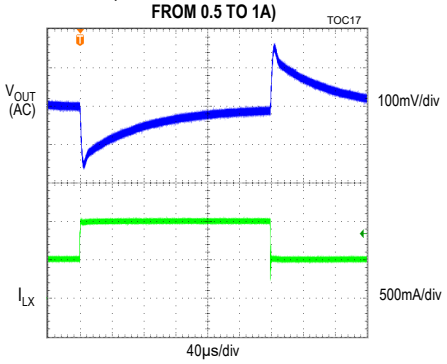
3.3V OUTPUT, FIGURE 5 CIRCUIT (LOAD CURRENT STEPPED FROM 0.5A TO 1A)



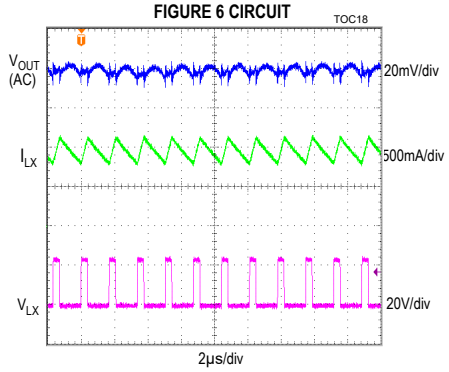
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, LX = unconnected, $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

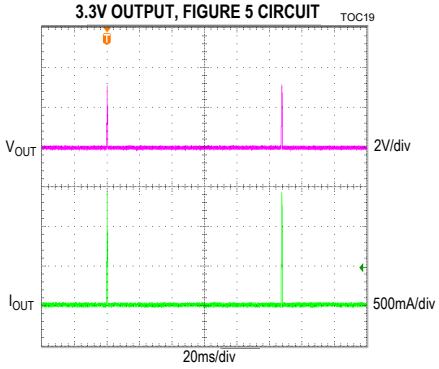
5V OUTPUT, FIGURE 6 CIRCUIT (LOAD CURRENT STEPPED FROM 0.5 TO 1A)



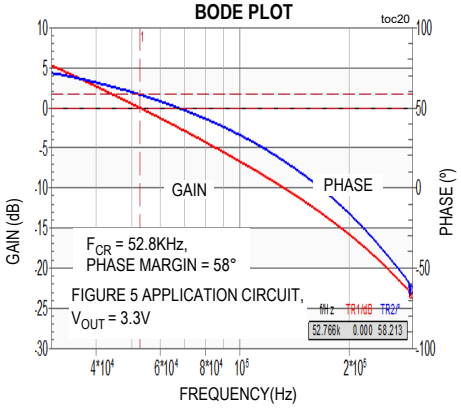
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 1A LOAD CURRENT, FIGURE 6 CIRCUIT



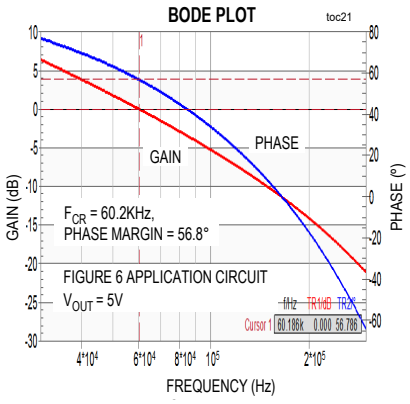
OVERLOAD PROTECTION 3.3V OUTPUT, FIGURE 5 CIRCUIT



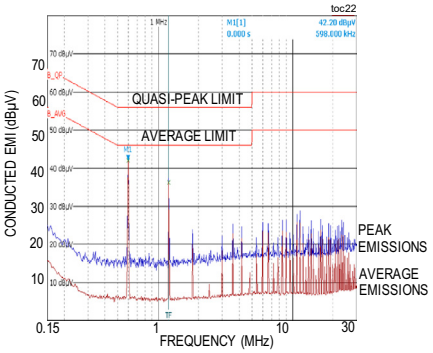
BODE PLOT



BODE PLOT

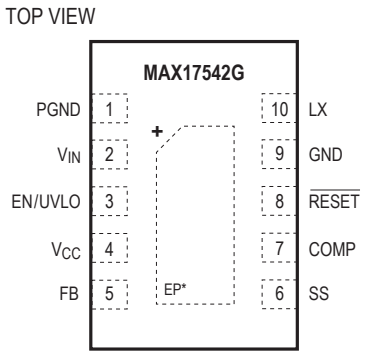


CONDUCTED EMI CURVE (5V OUTPUT, 1A LOAD CURRENT, FIGURE6 CIRCUIT)



MEASURED ON THE MAX17542GTEVKIT WITH INPUT FILTER (C_{IN} = 2.2µF, L_{IN} = 10µH

Pin Configurations



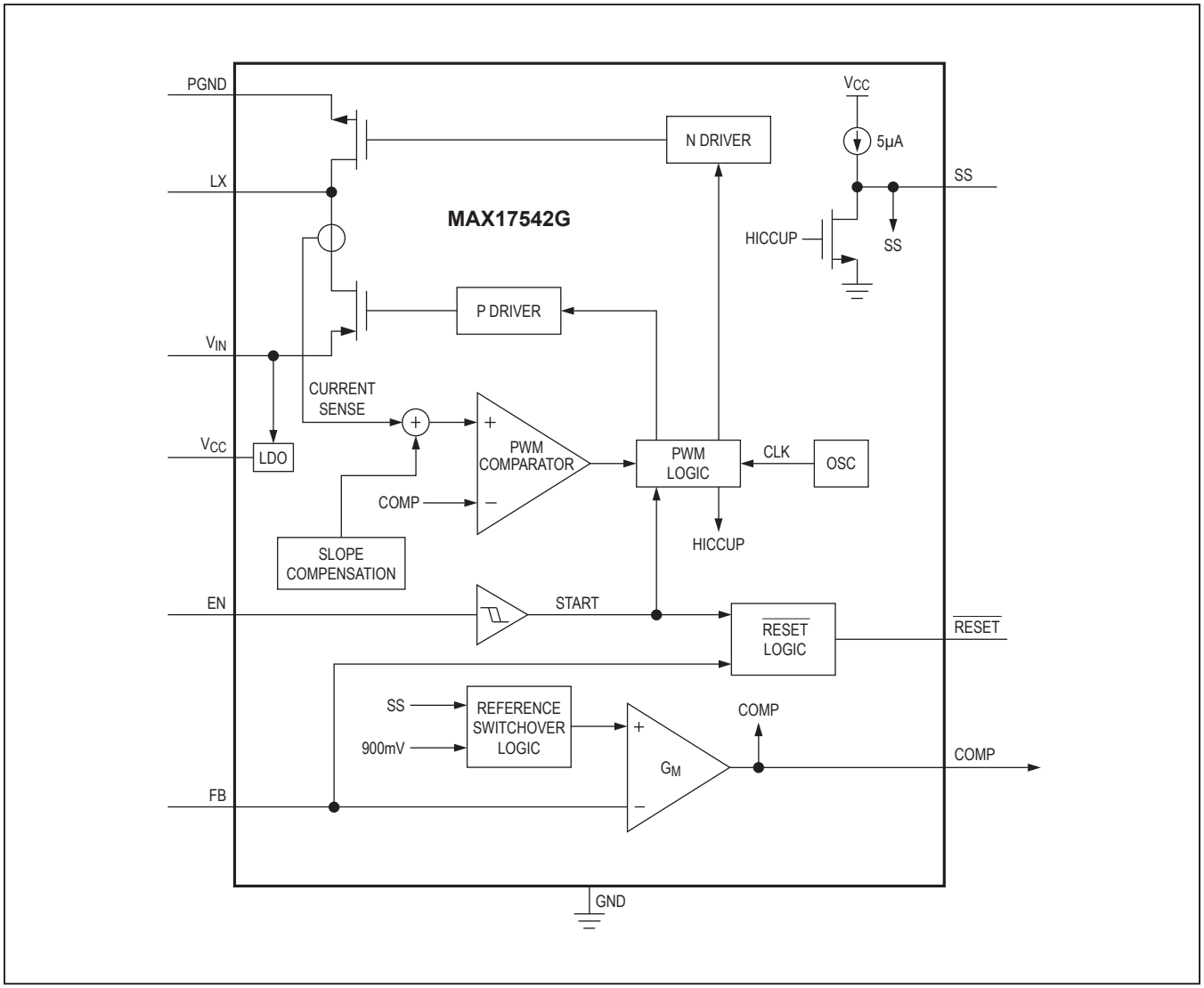
TDFN
(3mm x 2mm)

*EP = EXPOSED PAD. CONNECT TO GND

Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
2	V_{IN}	Power Supply Input. The input supply range is from 4.5V to 42V.
3	EN/UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the center of the resistive divider between V_{IN} and GND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to V_{IN} for always on.
4	V_{CC}	5V LDO Output. Bypass V_{CC} with 1µF ceramic capacitance to GND.
5	FB	Feedback Input. Connect FB to the center of the resistive divider between V_{OUT} and GND.
6	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time.
7	COMP	External Loop Compensation. Connect an RC network from COMP to GND. See External Loop Compensation for Adjustable Output Versions section for more details.
8	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92.5% of its set value. $\overline{\text{RESET}}$ goes high 1024 clock cycles after FB rises above 95.5% of its set value. $\overline{\text{RESET}}$ is valid when the device is enabled and V_{IN} is above 4.5V.
9	GND	Analog Ground
10	LX	Switching Node. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
—	EP	Exposed Pad. Connect to the GND pin of the IC. Connect to a large copper plane below the IC to improve heat dissipation capability.

Block Diagram



Detailed Description

The MAX17542G synchronous step-down regulator operates from 4.5V to 42V and delivers up to 1A load current. Output voltage regulation accuracy meets ±1.7% over temperature.

The device uses a peak-current-mode control scheme. An internal transconductance error amplifier generates an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side pMOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side nMOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down, and provides current to the output (the internal low R_{DSON} pMOS/nMOS switches ensure high efficiency at full load).

This device also integrates enable/undervoltage lockout (EN/UVLO), adjustable soft-start time (SS), and open-drain reset output ($\overline{RESET}$) functionality.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal blocks and the low-side MOSFET driver. The output of the V_{CC} linear regulator should be bypassed with a 1µF ceramic capacitor to GND. The device employs an undervoltage-lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.7V (typical). The internal V_{CC} linear regulator can source up to 40mA (typical) to supply the device and to power the low-side gate driver.

Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.47))}{0.92} + (I_{OUT(MAX)} \times 0.73)$$

$$V_{IN(MAX)} = 13 \times V_{OUT}$$

where V_{OUT} is the steady-state output voltage, $I_{OUT(MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor

Overcurrent Protection/HICCUP Mode

The device is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 1.65A (typ). A runaway current limit on the high-side switch current at 1.7A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 71.14% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. This operation results in minimal power dissipation under overload fault conditions.

$\overline{RESET}$ Output

The device includes a $\overline{RESET}$ comparator to monitor the output voltage. The open-drain $\overline{RESET}$ output requires an external pullup resistor. $\overline{RESET}$ can sink 2mA of current while low. $\overline{RESET}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95.5% of the designated nominal regulated voltage. $\overline{RESET}$ goes low when the regulator output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{RESET}$ also goes low during thermal shutdown. $\overline{RESET}$ is valid when the device is enabled and V_{IN} is above 4.5V.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences first with the high-side switch. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

Applications Information

Input Capacitor Selection

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple that reflects back to the source dictate the capacitance requirement. The device's high switching frequency allows the use of smaller value input capacitors. X7R capacitors are recommended in industrial applications for their temperature stability. A minimum value of 2.2µF should be used for the input capacitor. Higher values help reduce the ripple on the input DC bus further. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the 2.2µF ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The output voltage determines the inductor value as follows:

$$L = 4 \times V_{OUT}$$

where L is in µH.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value ($I_{PEAK-LIMIT}$ (typ) = 1.65A for the device).

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to ±3% of the output-voltage change.

The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency (600kHz). Select f_C to be 1/12th of f_{SW}. Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 19 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

Adjusting Output Voltage

The MAX17542G offers an adjustable output voltage from 0.9V to 92%V_{IN}. Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to GND (see Figure 1). Connect the center node of the divider to FB. To optimize efficiency and output accuracy, use the following procedure to choose the values of R4 and R5:

$$R4 = 16 \times V_{OUT}$$

where R4 is in kΩ.

Calculate R5 as follows:

$$R5 = \frac{R4 \times 0.9}{(V_{OUT} - 0.9)}$$

Setting the Input Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see Figure 2). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ, and then calculate R2 as:

$$R2 = \frac{R1 \times 1.218}{(V_{INU} - 1.218)}$$

where V_{INU} is the voltage at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

If the EN/UVLO pin is driven from an external signal source, it is recommended to place a series resistance of minimum 1kΩ between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

External Loop Compensation

The MAX17542G uses peak current-mode control scheme and needs only a simple RC network to have a stable, high-bandwidth control loop for the adjustable output voltage versions. The basic regulator loop is modeled as a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain $G_{MOD(dc)}$, with a pole and zero pair. The following equation defines the power modulator DC gain:

$$G_{MOD(dc)} = \frac{2}{\frac{1}{R_{LOAD}} + \frac{0.4}{V_{IN}} + \left(\frac{0.5 - D}{f_{SW} \times L_{SEL}}\right)}$$

where R_{LOAD} = $V_{OUT}/I_{OUT(MAX)}$, f_{SW} is the switching frequency (600kHz), L_{SEL} is the selected output inductance, D is the duty ratio, D = V_{OUT}/V_{IN}.

The compensation network is shown in Figure 3.

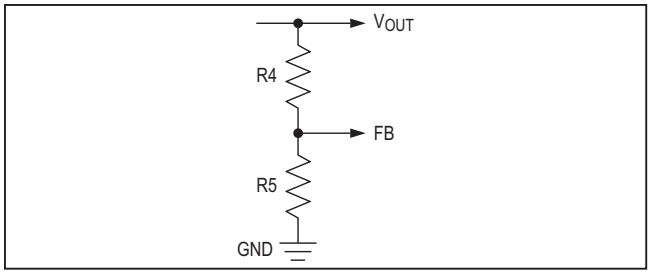


Figure 1. Setting the Output Voltage

R_Z can be calculated as:

$$R_Z = 6000 \times f_C \times C_{SEL} \times V_{OUT}$$

where R_Z is in Ω. Choose f_C to be 1/12th of the switching frequency.

C_Z can be calculated as follows:

$$C_Z = \frac{C_{SEL} \times G_{MOD(dc)}}{2 \times R_Z}$$

C_P can be calculated as follows:

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

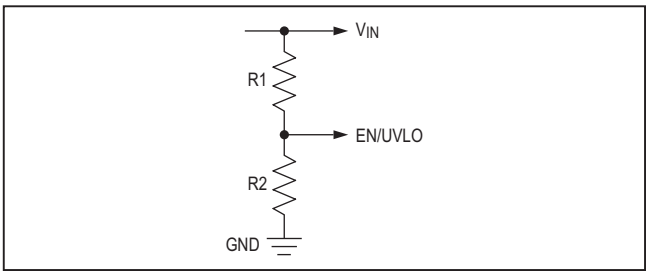


Figure 2. Adjustable EN/UVLO Network

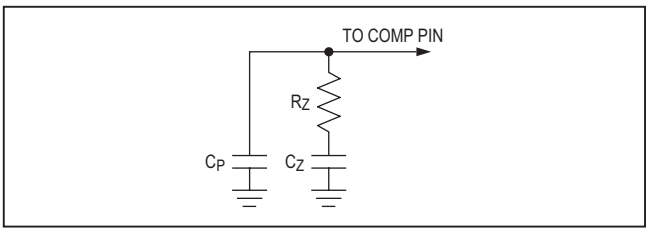


Figure 3. External Compensation Network

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is is the efficiency of the device, and R_{DCR} is the DC resistance of the output inductor (refer to the T*ypical Operating Characteristics* in the evaluation kit data sheet for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given as:

$$\theta_{JA} = 67.3°C/W$$

$$\theta_{JC} = 18.2°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17542G evaluation kit layouts available at **www.maximintegrated.com**. Follow these guidelines for good PCB layout:

1) All connections carrying pulsed currents must be very short and as wide as possible. The loop area of these connections must be made very small to reduce stray inductance and radiated EMI.
2) A ceramic input filter capacitor should be placed close to the V_{IN} pin of the device. The bypass capacitor for the V_{CC} pin should also be placed close to the V_{CC} pin. External compensation components should be placed close to the IC and far from the inductor. The feedback trace should be routed as far as possible from the inductor.
3) The analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at minimum, typically the return terminal of the V_{CC} bypass capacitor. The ground plane should be kept continuous as much as possible.
4) A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device, for efficient heat dissipation.

Figure 4 shows the recommended component placement for the MAX17542G.

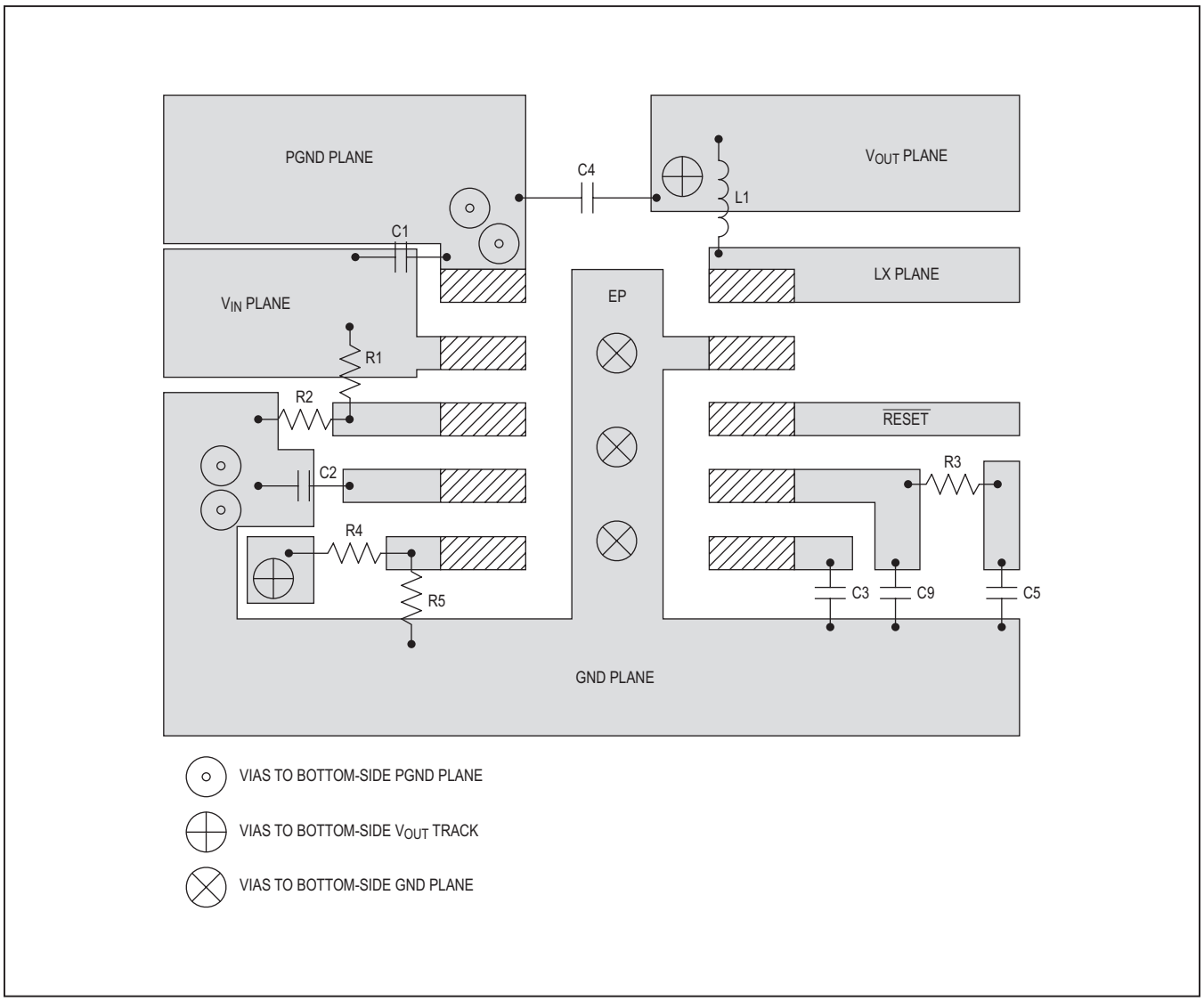


Figure 4. Recommended Component Placement for MAX17542G

Typical Applications Circuits

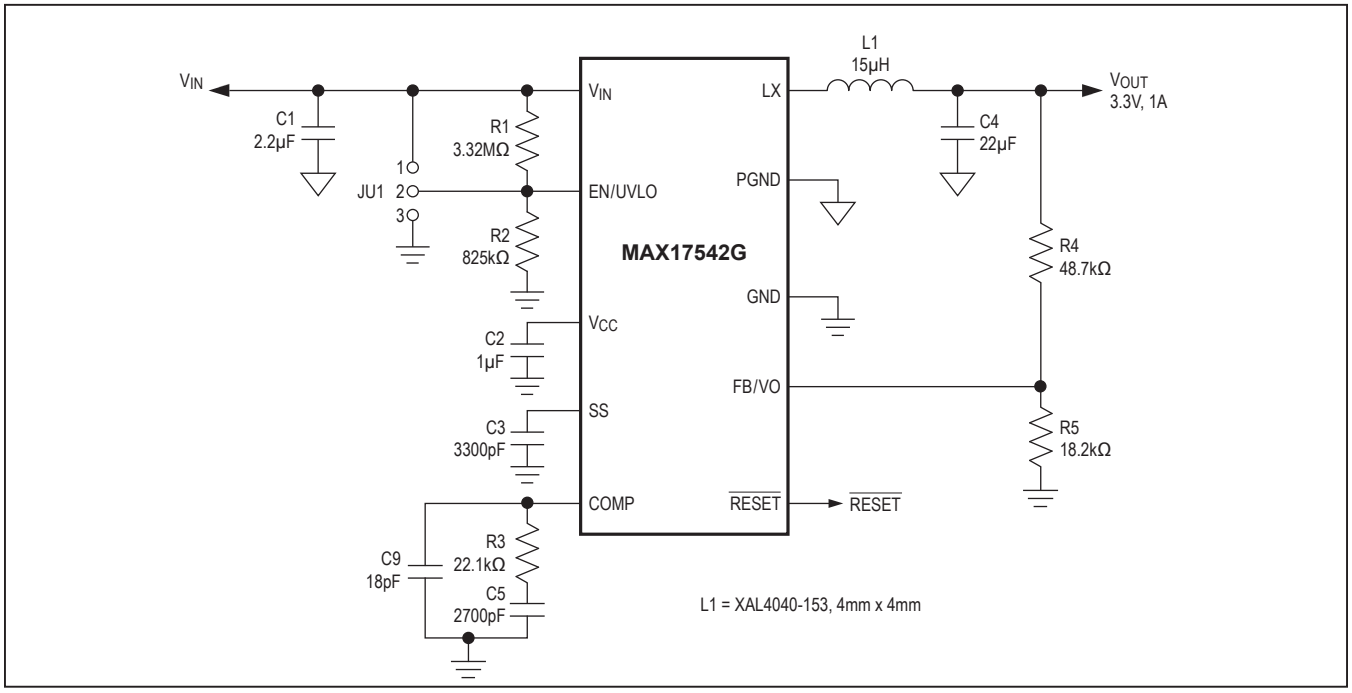


Figure 5. MAX17542G Application Circuit (3.3V Output, 1A Maximum Load Current)

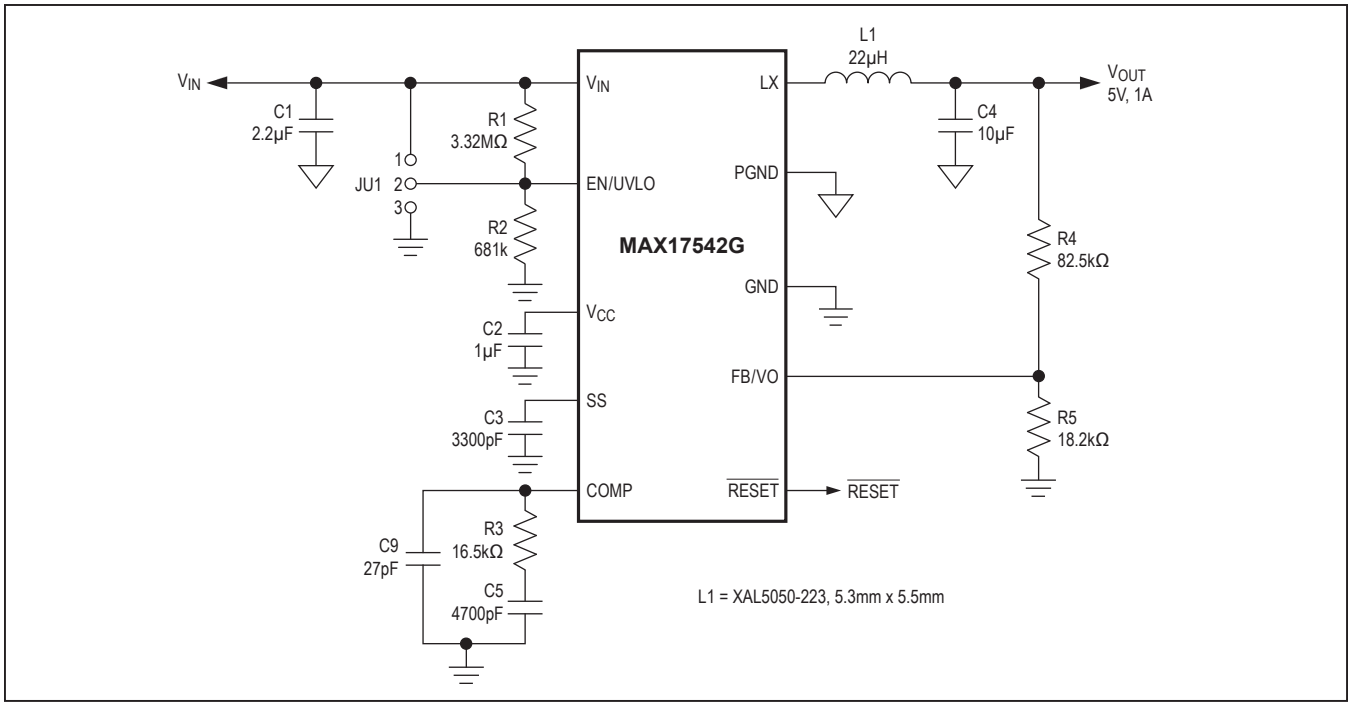


Figure 6. MAX17542G Application Circuit (5V Output, 1A Maximum Load Current)

Ordering Information

PART	PIN-PACKAGE
MAX17542GATB+	10 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS