Click here for production status of specific part numbers.

MAX17634A/MAX17634B/ MAX17634C

4.5V to 36V, 4.25A, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The MAX17634x is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 4.5V to 36V. It can deliver up to 4.25A current. The MAX17634 is available in three variants: MAX17634A, MAX17634B, and MAX17634C. The MAX17634A and MAX17634B are fixed 3.3V and fixed 5V output voltage parts, respectively. The MAX17634C is an adjustable output voltage (from 0.9V up to 90% of V_{IN}) part. Built-in compensation across the output voltage range eliminates the need for external components.

The MAX17634x features peak-current-mode control architecture. The device can be operated in forced pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and lightload conditions. The MAX17634x offers a low minimum on time that allows high switching frequencies and a smaller solution size.

The feedback voltage regulation accuracy over -40°C to +125°C for the MAX17634x is ±1.3%.The device is available in a compact 20-pin (4mm x 4mm) TQFN package. Simulation models are available.

Applications

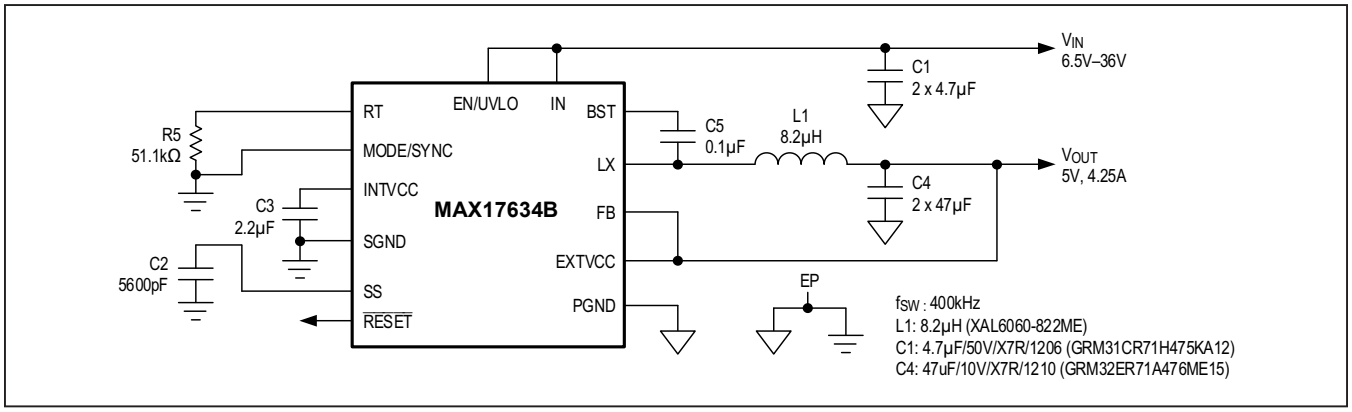
- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky–Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 36V Input
  - Adjustable Output Range from 0.9V up to 90% of V_{IN}
  - 400kHz to 2.2MHz Adjustable Frequency with External Synchronization
  - Available in a 20-Pin, 4mm x 4mm TQFN Package
- Reduces Power Dissipation
  - Peak Efficiency of 94%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap Supply (EXTVCC) for Improved Efficiency
  - 2.8µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable and Monotonic Startup with Prebiased Output Voltage
  - Built-in Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

Ordering Information *appears at end of data sheet.*

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

IN to PGND .....-0.3V to +40V
EN/UVLO to SGND .....-0.3V to (V_{IN} + 0.3V)
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
EXTVCC to SGND .....-5.5V to +6.5V
BST to PGND .....-0.3V to +46.5V
BST to LX .....-0.3V to +6.5V
BST to INTVCC .....-0.3V to +40V
FB to SGND (MAX17634A and MAX17634B) .....-5.5V to +6.5V
FB to SGND (MAX17634C) .....-0.3V to +6.5V
SS, MODE/SYNC, $\overline{\text{RESET}}$, INTVCC, RT to SGND ....-0.3V to +6.5V
PGND to SGND.....-0.3V to +0.3V
LX Total RMS Current .....±4.7A
Output Short-circuit duration .....Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 38.5mW/°C above +70°C.).....3076.9mW
Operating Temperature Range (Note1).....-40°C to 125°C
Junction Temperature..... -40°C to +150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

PACKAGE CODE	T2044+4C
Outline Number	21-100172
Land Pattern Number	90-0409
Thermal Resistance, Four-Layer Board (Note 2)	
Junction to Ambient (θ_{JA})	26°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 2: Package thermal resistances were obtained using the MAX17634 evaluation kit with no airflow

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 500 kHz), C_{INTVCC} = 2.2uF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V; V_{FB} = 3.67V (MAX17634A), V_{FB} = 5.5V (MAX17634B), V_{FB} = 1V (MAX17634C), LX = SS = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		36	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		2.8	4.5	µA
Input Quiescent Current	I_{Q_PFM}	MODE/SYNC = OPEN, V_{EXTVCC} = 5V		96		µA
		R_{RT} = 40.2kΩ, MODE/SYNC = OPEN, V_{EXTVCC} = 5V		106		
	I_{Q_DCM}	DCM Mode, V_{LX} = 0.1V		1.2	1.8	mA
	I_{Q_PWM}	Normal switching mode; V_{EXTVCC} = 5V		11		
ENABLE/UVLO (EN/UVLO)						
EN Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	
EN Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	-50	0	+50	nA
INTVCC (LDO)						
INTVCC Output Voltage Range	V_{INTVCC}	1mA ≤ I_{INTVCC} ≤ 25mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 36V, I_{INTVCC} = 1mA	4.75	5	5.25	
INTVCC Current Limit	$I_{INTVCC-MAX}$	V_{INTVCC} = 4.5V, V_{IN} = 7.5V	30			mA
INTVCC Dropout	$V_{INTVCC-DO}$	V_{IN} = 4.5V, I_{INTVCC} = 10mA			0.3	V
INTVCC UVLO	V_{INTVCC_UVR}	V_{INTVCC} rising	4.05	4.2	4.3	V
	V_{INTVCC_UVF}	V_{INTVCC} falling	3.65	3.8	3.9	
EXTVCC						
EXTVCC Switchover Threshold		V_{EXTVCC} rising	4.56	4.7	4.84	V
		V_{EXTVCC} falling	4.3	4.43	4.6	
POWER MOSFET						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		60	115	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A, sinking		37	73	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = (V_{PGND}+1) V to (V_{IN} -1) V, T_A = +25°C	-2		3	µA
SOFT-START (SS)						
Charging Current	I_{SS}		4.7	5	5.3	µA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 500 kHz), C_{INTVCC} = 2.2uF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V; V_{FB} = 3.67V (MAX17634A), V_{FB} = 5.5V (MAX17634B), V_{FB} = 1V (MAX17634C), LX = SS = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	MODE/SYNC = SGND or MODE/SYNC = INTVCC, for MAX17634A	3.256	3.3	3.344	V
		MODE/SYNC = SGND or MODE/SYNC = INTVCC, for MAX17634B	4.94	5	5.06	
		MODE/SYNC = SGND or MODE/SYNC = INTVCC, for MAX17634C	0.888	0.9	0.912	
		MODE/SYNC = OPEN, for MAX17634A	3.256	3.36	3.44	
		MODE/SYNC = OPEN, for MAX17634B	4.94	5.09	5.21	
		MODE/SYNC = OPEN, for MAX17634C	0.889	0.915	0.938	
FB Input Bias Current	I_{FB}	For MAX17634A		23		µA
		For MAX17634B		33		
		For MAX17634C, T_A = +25°C	-50		+50	nA
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE/SYNC = INTVCC (DCM mode)	V_{INTVCC} - 0.65			V
	V_{M-PFM}	MODE/SYNC = OPEN (PFM mode)	V_{INTVCC}/2			
	V_{M-PWM}	MODE/SYNC = SGND (PWM mode)			0.75	
SYNC Frequency Capture Range	F_{SYNC}	f_{SW} set by R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		5.7	6.7	7.7	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		6.7	7.8	9	A
PFM Current-Limit Threshold	I_{PFM}	MODE/SYNC = OPEN		1.6		A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	MODE/SYNC = OPEN or MODE/SYNC = INTVCC	-0.28	0	+0.28	A
		MODE/SYNC = SGND		2.5		

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 500 kHz), C_{INTVCC} = 2.2uF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V; V_{FB} = 3.67V (MAX17634A), V_{FB} = 5.5V (MAX17634B), V_{FB} = 1V (MAX17634C), LX = SS = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RT						
Switching Frequency	f_{SW}	R_{RT} = 50.8kΩ	380	400	420	kHz
		R_{RT} = 40.2kΩ	475	500	525	
		R_{RT} = OPEN	460	500	540	
		R_{RT} = 8.06kΩ	1950	2200	2450	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$	For MAX17634A	2.03	2.13	2.22	V
		For MAX17634B	3.07	3.22	3.37	
	$V_{FB-HICF}$	For MAX17634C	0.55	0.58	0.605	
HICCUP Timeout		(Note 4)		32768		Cycles
Minimum On-Time	t_{ON-MIN}			52	80	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		160	ns
LX Dead TIme	LX_{DT}			5		ns
$\overline{RESET}$						
$\overline{RESET}$Output Level Low	V_{RESETL}	$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$Output Leakage Current	$I_{RESETLKG}$	T_A = T_J = 25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} Rising, % of V_{FB-REG}	93.8	95	97.8	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} Falling, % of V_{FB-REG}	90.5	92	94.6	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN (TEMP)						
Thermal Shutdown Threshold		Temperature rising		165		°C
Thermal Shutdown Hysteresis				10		°C

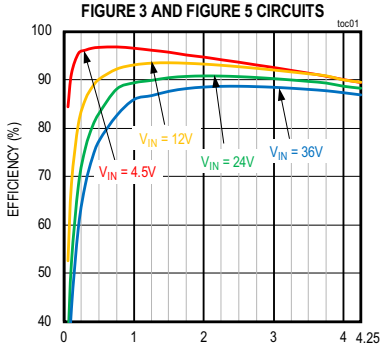
Note 3: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 4: See the *Overcurrent Protection/Hiccup Mode* Section for more details

Typical Operating Characteristics

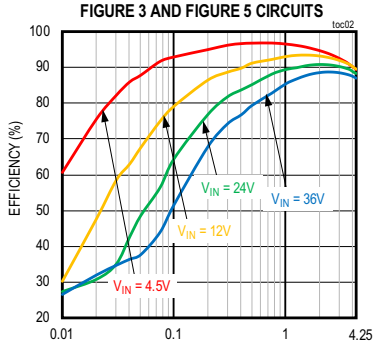
(($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{INTVCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.))

EFFICIENCY vs. LOAD CURRENT
FIGURE 3 AND FIGURE 5 CIRCUITS



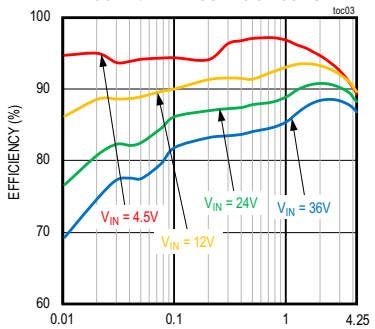
CONDITIONS: 3.3V OUTPUT, PWM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 3 AND FIGURE 5 CIRCUITS



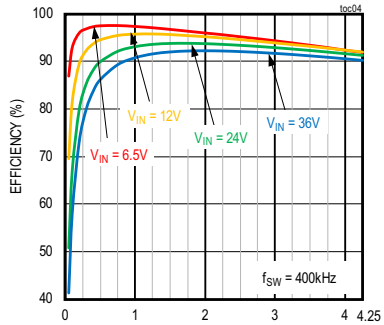
CONDITIONS: 3.3V OUTPUT, DCM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 3 AND FIGURE 5 CIRCUITS



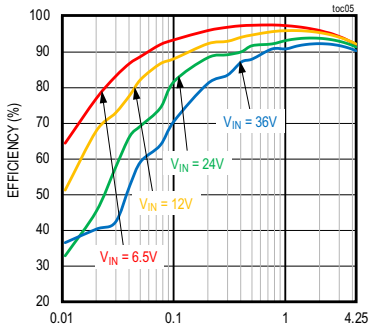
CONDITIONS: 3.3V OUTPUT, PFM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 AND FIGURE 6 CIRCUITS



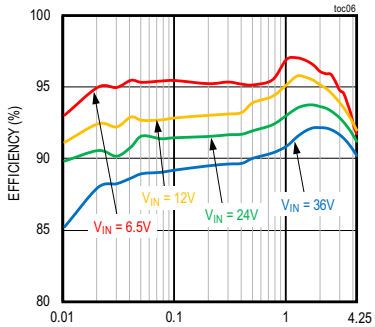
CONDITIONS: 5V OUTPUT, PWM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 AND FIGURE 6 CIRCUIT



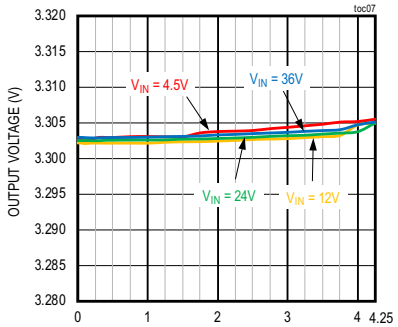
CONDITIONS: 5V OUTPUT, DCM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 AND FIGURE 6 CIRCUIT



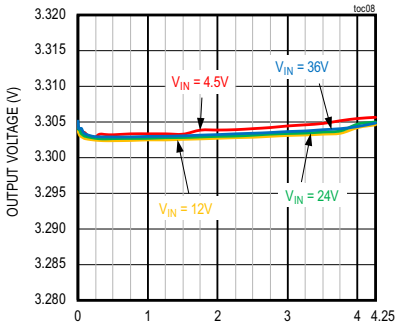
CONDITIONS: 5V OUTPUT, PFM MODE

LINE AND LOAD REGULATION
FIGURE 3 AND FIGURE 5 CIRCUITS



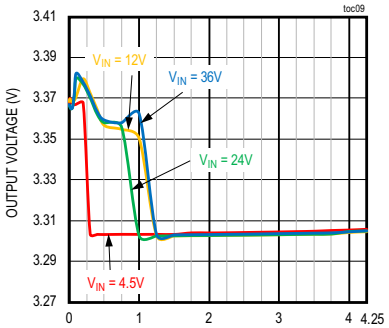
CONDITIONS: 3.3V OUTPUT, PWM MODE

LINE AND LOAD REGULATION
FIGURE 3 AND FIGURE 5 CIRCUITS



CONDITIONS: 3.3V OUTPUT, DCM MODE

LINE AND LOAD REGULATION
FIGURE 3 AND FIGURE 5 CIRCUITS

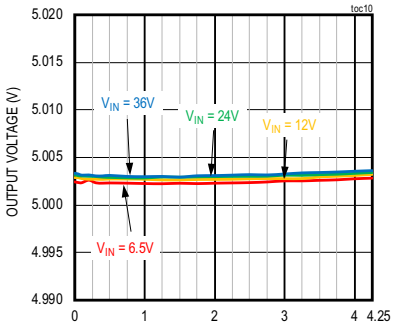


CONDITIONS: 3.3V OUTPUT, PFM MODE

Typical Operating Characteristics (continued)

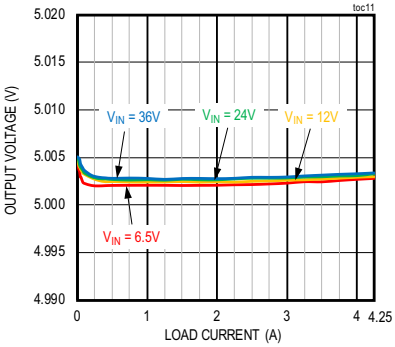
(($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{INTVCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.))

LINE AND LOAD REGULATION
FIGURE 4 AND FIGURE 6 CIRCUITS



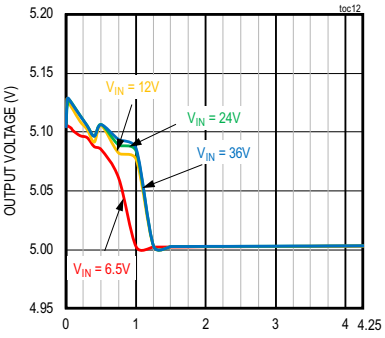
CONDITIONS: 5V OUTPUT, PWM MODE

LINE AND LOAD REGULATION
FIGURE 4 AND FIGURE 6 CIRCUITS



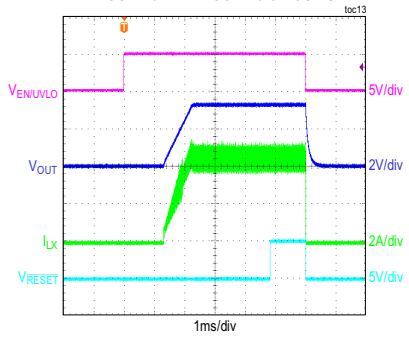
CONDITIONS: 5V OUTPUT, DCM MODE

LINE AND LOAD REGULATION
FIGURE 4 AND FIGURE 6 CIRCUITS



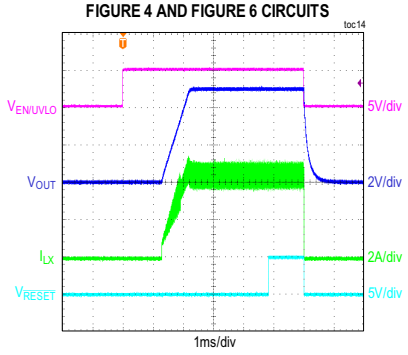
CONDITIONS: 5V OUTPUT, PFM MODE

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 3 AND FIGURE 5 CIRCUITS



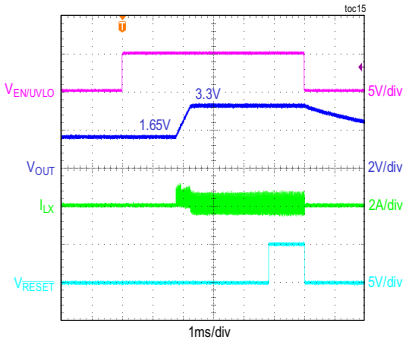
CONDITIONS: 3.3V OUTPUT, PWM MODE, 0.776Ω LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 AND FIGURE 6 CIRCUITS



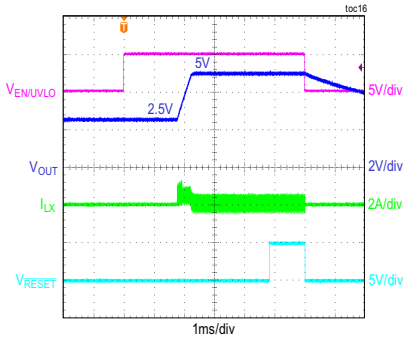
CONDITIONS: 5V OUTPUT, PWM MODE, 1.176Ω LOAD

SOFT-START WITH PREBIAS OF VOLTAGE 1.65V
FIGURE 3 AND FIGURE 5 CIRCUITS



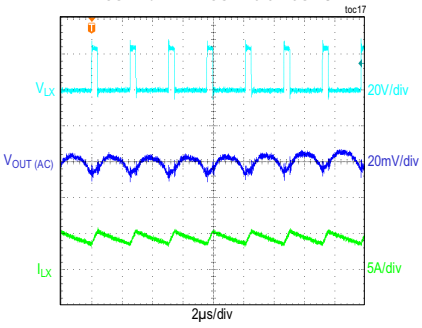
CONDITIONS: 3.3V OUTPUT, PWM MODE, 66Ω LOAD

SOFT-START WITH PREBIAS OF VOLTAGE 2.5V
FIGURE 4 AND FIGURE 6 CIRCUITS



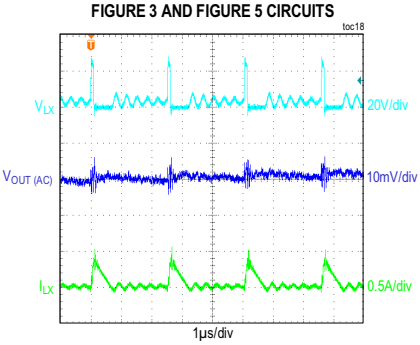
CONDITIONS: 5V OUTPUT, PWM MODE, 100Ω LOAD

STEADY-STATE PERFORMANCE
FIGURE 3 AND FIGURE 5 CIRCUITS



CONDITIONS: 3.3V OUTPUT, PWM MODE, 4.25A LOAD

STEADY-STATE PERFORMANCE
FIGURE 3 AND FIGURE 5 CIRCUITS

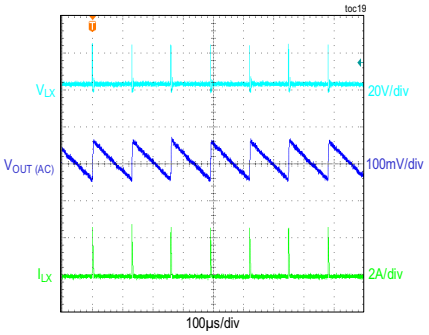


CONDITIONS: 3.3V OUTPUT, DCM MODE, 50mA LOAD

Typical Operating Characteristics (continued)

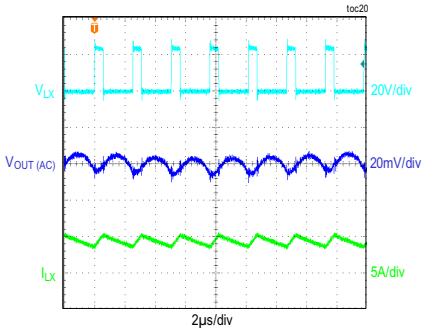
(($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{INTVCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.))

**STEADY-STATE PERFORMANCE
FIGURE 3 AND FIGURE 5 CIRCUITS**



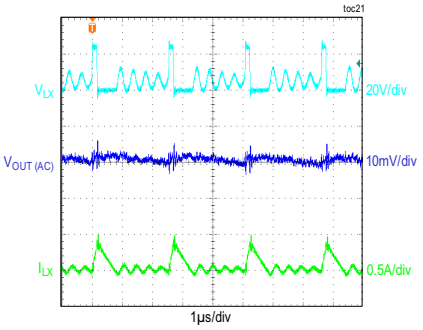
CONDITIONS: 3.3V OUTPUT, PFM MODE, 50mA LOAD

**STEADY-STATE PERFORMANCE
FIGURE 4 AND FIGURE 6 CIRCUITS**



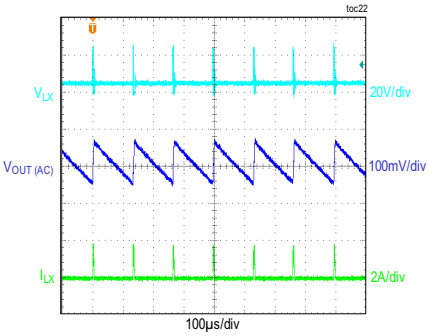
CONDITIONS: 5V OUTPUT, PWM MODE, 4.25A LOAD

**STEADY-STATE PERFORMANCE
FIGURE 4 AND FIGURE 6 CIRCUITS**



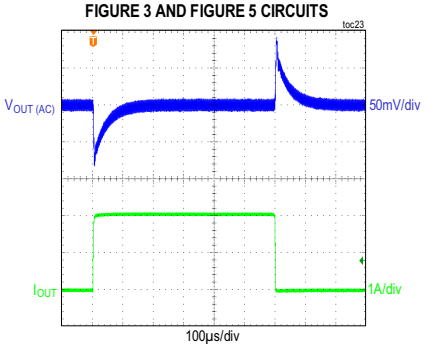
CONDITIONS: 5V OUTPUT, DCM MODE, 50mA LOAD

**STEADY-STATE PERFORMANCE
FIGURE 4 AND FIGURE 6 CIRCUITS**



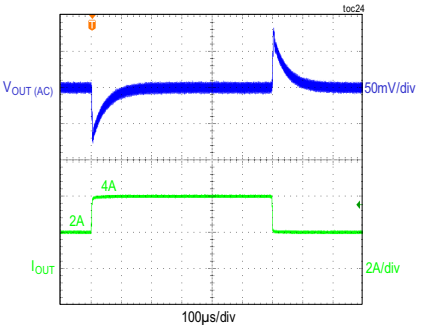
CONDITIONS: 5V OUTPUT, PFM MODE, 50mA LOAD

**LOAD TRANSIENT BETWEEN 0A AND 2A
FIGURE 3 AND FIGURE 5 CIRCUITS**



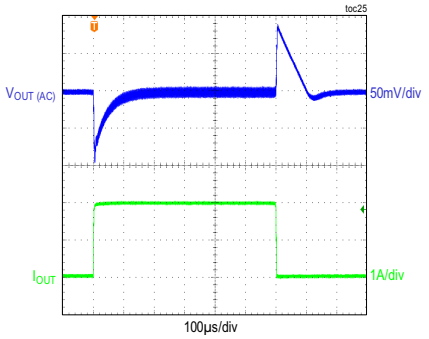
CONDITIONS: 3.3V OUTPUT, PWM MODE

**LOAD TRANSIENT BETWEEN 2A AND 4A
FIGURE 3 AND FIGURE 5 CIRCUITS**



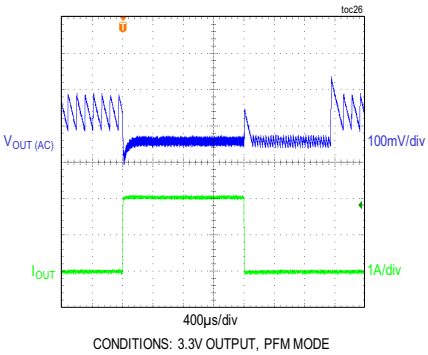
CONDITIONS: 3.3V OUTPUT, PWM/PFM/DCM MODE

**LOAD TRANSIENT BETWEEN 0.05A AND 2A
FIGURE 3 AND FIGURE 5 CIRCUITS**



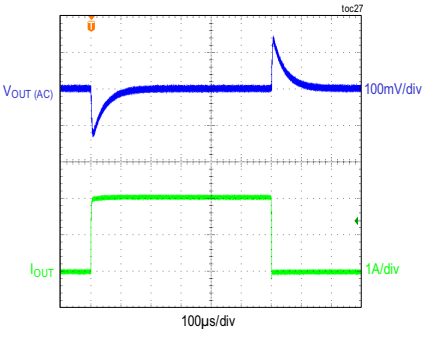
CONDITIONS: 3.3V OUTPUT, DCM MODE

**LOAD TRANSIENT BETWEEN 0.05A AND 2A
FIGURE 3 AND FIGURE 5 CIRCUITS**



CONDITIONS: 3.3V OUTPUT, PFM MODE

**LOAD TRANSIENT BETWEEN 0A AND 2A
FIGURE 4 AND FIGURE 6 CIRCUITS**

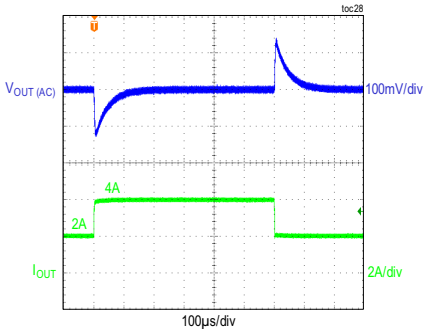


CONDITIONS: 5V OUTPUT, PWM MODE

Typical Operating Characteristics (continued)

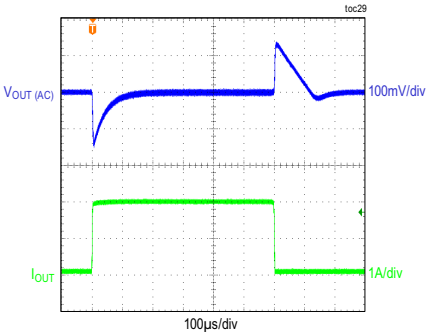
(($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{INTVCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.))

LOAD TRANSIENT BETWEEN 2A AND 4A
FIGURE 4 AND FIGURE 6 CIRCUITS



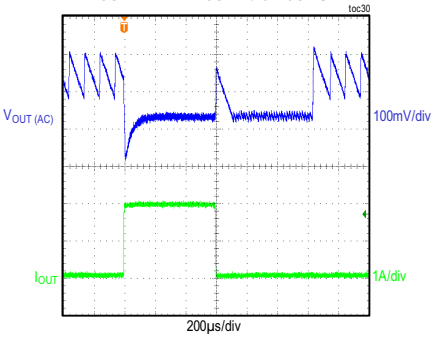
CONDITIONS: 5V OUTPUT, PWM/PFM/DCM MODE

LOAD TRANSIENT BETWEEN 0.05A AND 2A
FIGURE 4 AND FIGURE 6 CIRCUITS



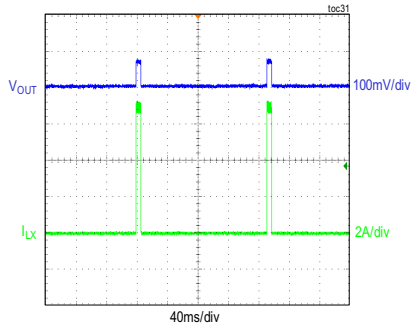
CONDITIONS: 5V OUTPUT, DCM MODE

LOAD TRANSIENT BETWEEN 0.05A AND 2A
FIGURE 4 AND FIGURE 6 CIRCUITS



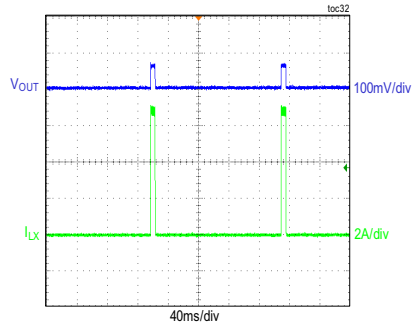
CONDITIONS: 5V OUTPUT, PFM MODE

SHORT-CIRCUIT PROTECTION
FIGURE 3 AND FIGURE 5 CIRCUITS



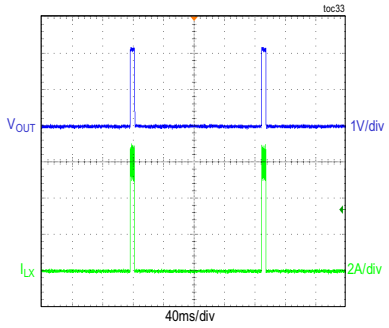
CONDITIONS: 3.3V OUTPUT, PWM MODE, R_LOAD = 0.01Ω

SHORT-CIRCUIT PROTECTION
FIGURE 4 AND FIGURE 6 CIRCUITS



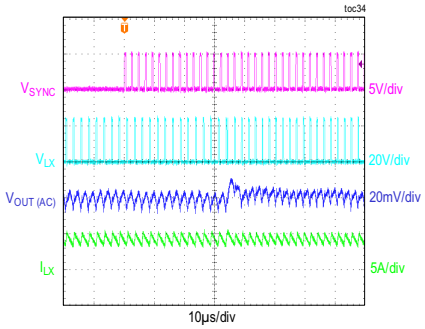
CONDITIONS: 5V OUTPUT, PWM MODE, R_LOAD = 0.01Ω

OVERLOAD PROTECTION
FIGURE 4 AND FIGURE 6 CIRCUITS



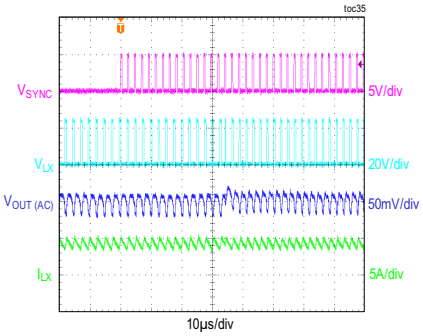
CONDITIONS: 5V OUTPUT, PWM MODE, R_LOAD = 0.35Ω

EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 3 AND FIGURE 5 CIRCUITS



CONDITIONS: 3.3V OUTPUT, PWM MODE, 4.25A LOAD
f_{SW} = 400kHz, EXTERNAL CLOCK FREQUENCY = 440kHz

EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 4 AND FIGURE 6 CIRCUITS

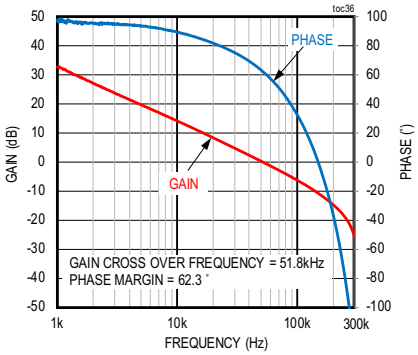


CONDITIONS: 5V OUTPUT, PWM MODE, 4.25A LOAD
f_{SW} = 400kHz, EXTERNAL CLOCK FREQUENCY = 440kHz

Typical Operating Characteristics (continued)

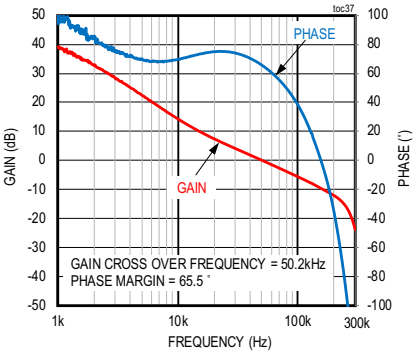
(($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{INTVCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.))

MAX17634A BODE PLOT
FIGURE 5 CIRCUIT



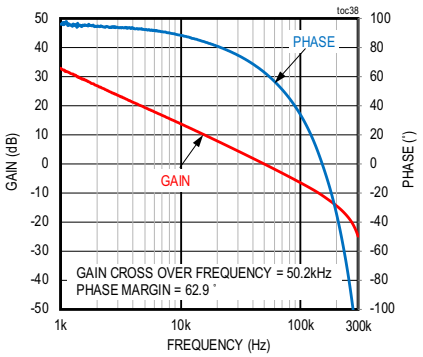
CONDITIONS: FIXED 3.3V OUTPUT, 4.25A LOAD, PWM MODE

MAX17634B BODE PLOT
FIGURE 6 CIRCUIT



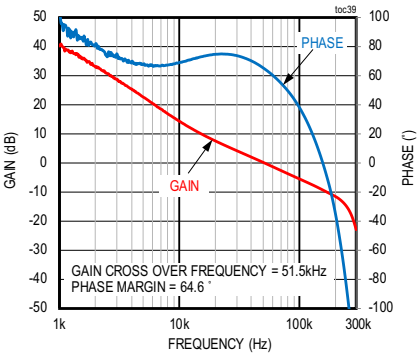
CONDITIONS: FIXED 5V OUTPUT, 4.25A LOAD, PWM MODE

MAX17634C BODE PLOT
FIGURE 3 CIRCUIT



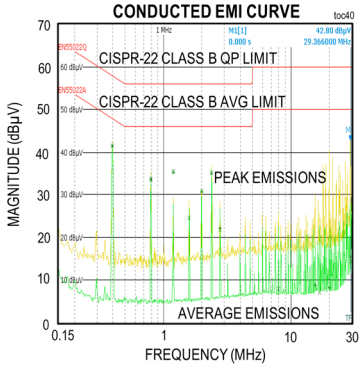
CONDITIONS: ADJUSTABLE 3.3V OUTPUT, 4.25A LOAD, PWM MODE

MAX17634C BODE PLOT
FIGURE 4 CIRCUIT



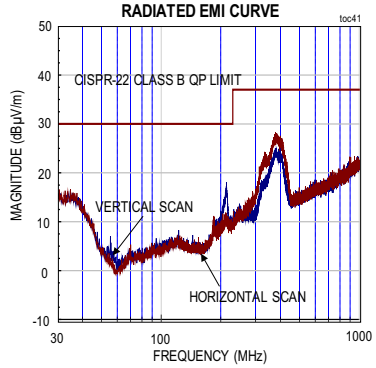
CONDITIONS: ADJUSTABLE 5V OUTPUT, 4.25A LOAD, PWM MODE

MAX17634C, 5V OUTPUT, 4.25A LOAD CURRENT
CONDUCTED EMI CURVE



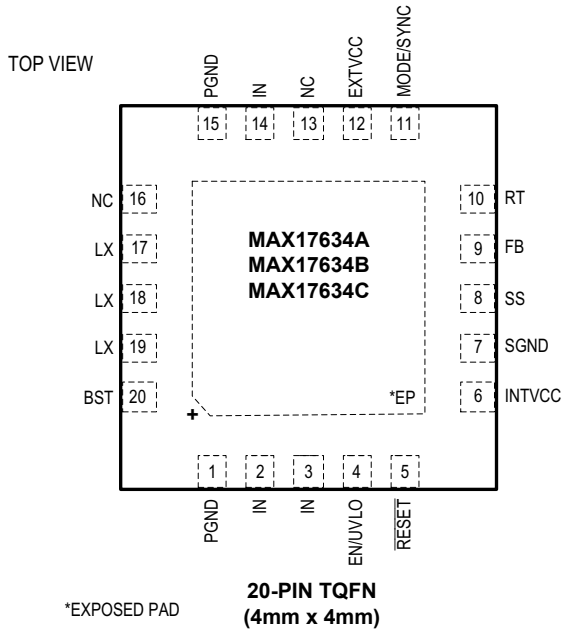
CONDITIONS: MEASURED ON THE MAX17634CEVKIT WITH L2 = 22µH, C12 = C13 = 2.2µF/50V/X7R/1206, C14 = C19 = 4.7µF/50V/X7R/1210

MAX17634C, 5V OUTPUT, 4.25A LOAD CURRENT
RADIATED EMI CURVE



CONDITIONS: MEASURED ON THE MAX17634CEVKIT

Pin Configuration



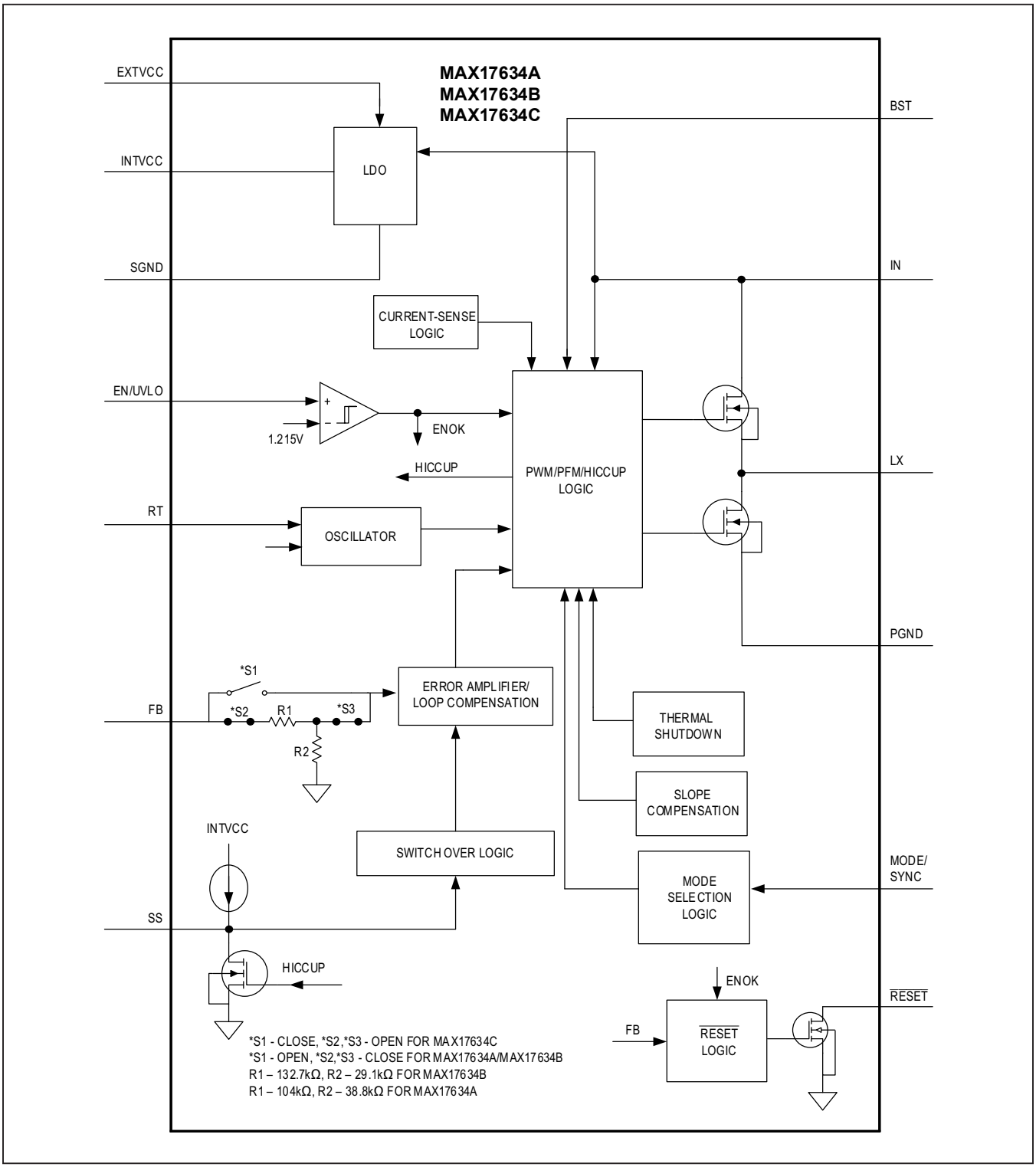
Pin Description

PIN	NAME	FUNCTION
1, 15	PGND	Power Ground Pins of the Converter. Connect externally to the power ground plane. Refer to the *MAX17634 EV kit* data sheet for a layout example.
2,3,14	IN	Power-Supply Input Pins. 4.5V to 36V input supply range. Decouple to PGND with a minimum of 4.7µF capacitor; place the capacitor close to the IN and PGND pins.
4	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high (greater than V_{ENR}) to enable the output. Connect to the center of the resistor-divider between IN and SGND to set the input voltage at which the part turns on. Connect to IN pin for always on operation. Pull low (lower than V_{ENF}) for disabling the device.
5	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$output is driven low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above 95% of its set value
6	INTVCC	5V LDO Output of the Part. Bypass INTVCC with a 2.2µF ceramic capacitance to SGND. LDO doesn't support the external loading on INTVCC.
7	SGND	Analog Ground
8	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.

Pin Description (continued)

PIN	NAME	FUNCTION
9	FB	Feedback Input. Connect the output voltage node (V_{OUT}) to FB for MAX17634A and MAX17634B. Connect FB to the center node of an external resistor-divider from the output to SGND to set the output voltage for MAX17634C. See the *Adjusting Output Voltage* section for more details.
10	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the regulator's switching frequency between 400kHz and 2.2MHz. Leave RT open for the default 500kHz frequency. See the *Setting the Switching Frequency (RT)* for more details.
11	MODE/SYNC	MODE/SYNC Pin Configures the Device to Operate in PWM, PFM, or DCM Modes of Operation. Leave MODE/SYNC open for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to INTVCC for DCM operation at light loads.The device can be synchronized to an external clock using this pin. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
12	EXTVCC	External Power Supply Input Reduces the Internal-LDO loss. Connect it to buck output when it is programmed to 5V only. When EXTVCC is not used, connect it to SGND.
13,16	NC	No Connection
17-19	LX	Switching Node Pins. Connect LX pins to the switching side of the inductor.
20	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
—	EP	Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large SGND plane with several thermal vias for best thermal performance. Refer to the MAX17634 EV kit data sheet for an example of the correct method for EP connection and thermal vias.

Functional Diagram



Detailed Description

The MAX17634x is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input voltage range of 4.5V to 36V. It can deliver up to 4.25A current. The MAX17634A and MAX17634B are the fixed 3.3V and fixed 5V output parts, respectively. The MAX17634C is an adjustable output voltage (from 0.9V upto 90% of V_{IN}) part. Built-in compensation across the output voltage range eliminates the need for external compensation components. The feedback (FB) voltage regulation accuracy over -40°C to +125°C is ±1.3% for MAX17634x.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the highside MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE/SYNC pin that can be used to operate the device in PWM, PFM, or DCM control schemes. The device also features adjustable-input undervoltage lockout, adjustable soft-start, open drain $\overline{RESET}$, and external frequency synchronization features. The MAX17634x offers a low minimum on time that enables to design converter at higher switching frequencies and a small solution size.

Mode Selection and External Clock Synchronization (MODE/SYNC):

The MAX17634x supports the PWM, PFM, and DCM modes of operation. The device enters the required mode of operation based on the setting of the MODE/SYNC pin as detected within 1.5ms after INTVCC and EN/UVLO voltages exceed their respective UVLO rising thresholds ($V_{INTVCC-UVR}$, V_{ENR}). If the MODE/SYNC pin is open, the device operates in PFM mode at light loads. If the state of the MODE/SYNC pin is low (< V_{M-PWM}), the device operates in constant-frequency PWM mode at all loads. If the state of the MODE/SYNC pin is high (>V_{M-DCM}), the device operates in DCM mode at light loads.

During external clock synchronization the device operates in PWM mode, irrespective of whether PWM or DCM mode is set. When 16 external clock rising edges are detected on the MODE/SYNC pin, the internal oscillator frequency set by RT pin (f_{SW}) changes to external clock frequency. The device remains in PWM mode until EN/UVLO or input power is cycled. The external clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}. The minimum external clock pulse width should be greater than 50ns. The off-time duration of the external clock should be at least 160ns.

If PFM mode of operation is set, the device ignores the external clock pulses and remains in PFM mode. Thus, external clock synchronization is not supported in PFM mode.

See the MODE/SYNC section of the *Electrical Characteristics* table for details.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation irrespective of loading, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of I_{PFM} (1.6A, typ) every clock cycle until the output rises to 102.3% of the set nominal output voltage. Once the output reaches 102.3% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the set nominal output voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the set nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from the supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The output voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode.

Linear Regulator (INTVCC and EXTVCC)

The MAX17634x has an internal LDO (low dropout) regulator that powers INTVCC from IN. This LDO is enabled during power-up or when EN/UVLO is above 0.75V (typ). An internal switch connects the EXTVCC to INTVCC. The switch is open during power up. If INTVCC is above its UVLO threshold and, if EXTVCC is greater than 4.7V (typ), the internal LDO is disabled and INTVCC is powered from EXTVCC. Powering INTVCC from EXTVCC increases efficiency at higher input voltages. Typical INTVCC output voltage is 5V. Bypass INTVCC to SGND with a 2.2µF low-ESR ceramic capacitor. INTVCC powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor.

The MAX17634x employs an undervoltage lockout circuit that forces the buck converter off when INTVCC falls below $V_{INTVCC-UVF}$ (3.8, typ). The buck converter can be immediately enabled again when INTVCC > $V_{INTVCC-UVR}$ (4.2, typ). The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to EXTVCC pin, if the output is shorted to ground then the transfer from EXTVCC to internal LDO happens seamlessly without any impact on the normal functionality. Connect the EXTVCC pin to SGND, when not in use.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor (R_{RT}) connected at the RT pin by the following equation:

$$R_{RT} \cong \frac{21000}{f_{SW}} - 1.7$$

Where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open will force the device to operate at default switching frequency of 500kHz. See Table 1 for R_{RT} resistor values for a few common switching frequencies.

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS-ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF-MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS-ONH(MAX)} - R_{DS-ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON-MIN(MAX)}}$$

Where

V_{OUT} = Steady-state output voltage,

$I_{OUT(MAX)}$ = Maximum load current,

R_{DCR} = Worst-case DC resistance of the inductor,

$f_{SW(MAX)}$ = Maximum switching frequency,

$t_{OFF-MIN(MAX)}$ = Worst-case minimum switch off-time (160ns),

$t_{ON-MIN(MAX)}$ =Worst-case minimum switch on-time (80ns),

$R_{DS-ONL(MAX)}$ and $R_{DS-ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side internal MOSFETs, respectively.

Table 1. Switching Frequency vs. R_{RT} Resistor

SWITCHING FREQUENCY (kHz)	R_{RT} RESISTOR (kΩ)
400	50.8
500	OPEN
500	40.2
2200	8.06

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ (6.7A, typ). A runaway current limit on the high-side switch current at $I_{RUNAWAY-LIMIT}$ (7.8A, typ) protects the device under high input voltage, output short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if feedback voltage drops to $V_{FB-HICF}$ due to a fault condition, hiccup mode is triggered 1024 clock cycles after soft-start time is completed. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed $V_{FB-HICF}$, the device continues to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the status of output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) with a delay of 1024 switching cycles after the regulator output increases above 95% (V_{FB-OKR}) of V_{FB-REG}. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% (V_{FB-OKF}) of V_{FB-REG}. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the device starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Shutdown Protection

Thermal-shutdown protection limits junction temperature in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on with soft-start after the junction temperature reduces by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times \left(1 - D\right)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where,

D = V_{OUT}/V_{IN} is the duty ratio of the converter,

f_{SW} = Switching frequency,

ΔV_{IN} = Allowable input voltage ripple,

η = Efficiency.

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{0.7 \times V_{OUT}}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula. Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of $I_{PEAK-LIMIT}$ (6.7A, typ).

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. Output capacitor is calculated and sized to support a 50% of maximum output current as the dynamic step load, and to contain the output voltage deviation to within ±3% of the output voltage. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where,

I_{STEP} = Load current step,

$t_{RESPONSE}$ = Response time of the controller,

ΔV_{OUT} = Allowable output-voltage deviation,

f_C = Target closed-loop crossover frequency,

f_{SW} = Switching frequency.

Select f_C to be 1/10th of f_{SW} for the switching frequencies less than or equal to 800 kHz. If the switching frequency is more than 800 kHz, select f_C to be 80kHz. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that, during startup, the device operates at half the programmed switching frequency until the output voltage reaches 64.4% of set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from INto SGND (see Figure 1). Connect the center node of the divider to EN/UVLO. Choose R_{TOP} to be 3.3MΩ and then calculate R_{BOTTOM} as follows:

$$R_{BOTTOM} = \frac{R_{TOP} \times 1.215}{\left(V_{INU} - 1.215\right)}$$

where V_{INU} is the voltage at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power-up (slower than soft-start)/ power-down. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin, to reduce voltage ringing on the line.

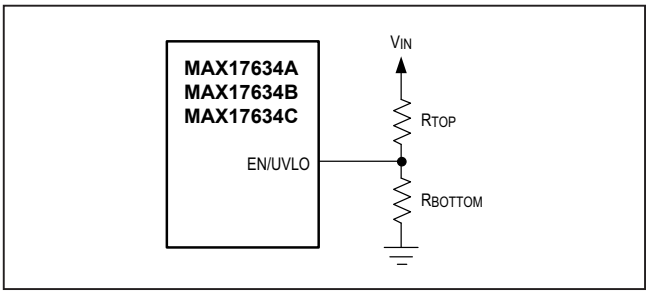


Figure 1. Setting the Input Undervoltage Lockout

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin for MAX17634C. Connect the output voltage node (V_{OUT}) to the FB pin for MAX17634A and MAX17634B. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_U from the output to the FB pin as follows:

$$R_U = \frac{320}{f_C \times C_{OUT\_SEL}}$$

where,

R_U is in kΩ,

f_C = Crossover frequency is in Hz,

C_{OUT_SEL} = Actual capacitance of selected output capacitor at DC-bias voltage in F.

Calculate resistor R_B connected from the FB pin to SGND as follows:

$$R_B = \frac{R_U \times 0.9}{\left(V_{OUT} - 0.9\right)}$$

R_B is in kΩ.

Select an appropriate f_C and C_{OUT}, so that the parallel combination of R_B and R_U is less than 50kΩ.

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where,

P_{OUT} = Output power,

η = Efficiency of the converter.

R_{DCR} = DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

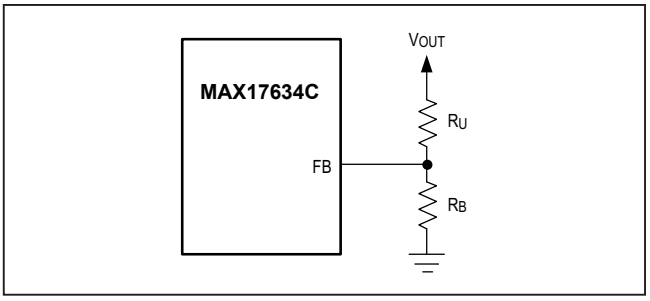


Figure 2. Setting the Output Voltage

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 26^{\circ}C/W$$

$$\theta_{JC} = 2^{\circ}C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + \left(\theta_{JC} \times P_{LOSS}\right)$$

Note: *Junction temperatures greater than +125°C degrades operating lifetimes.*

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the INTVCC pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17634 evaluation kit layout available at **www.maximintegrated.com**.

Typical Application Circuits

Adjustable 3.3V Output Typical Application Circuit

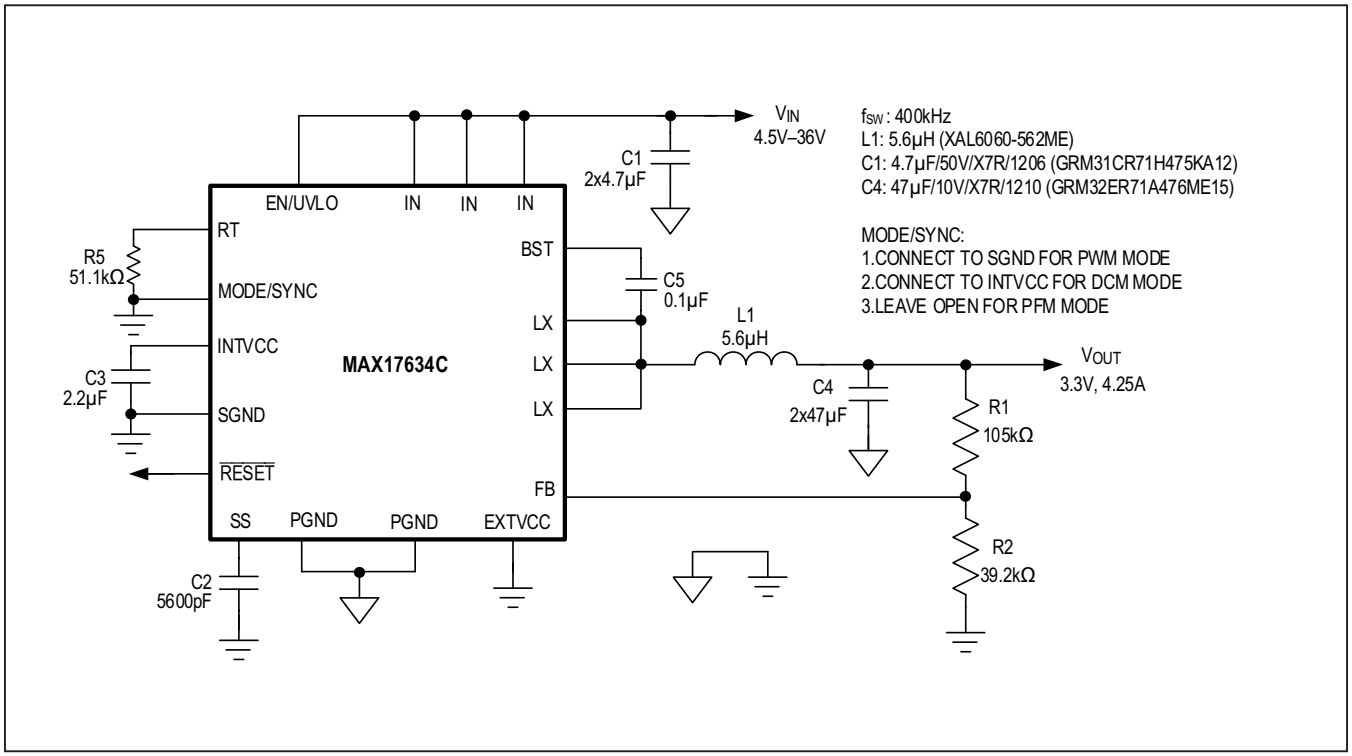


Figure 3. Adjustable 3.3V Output with 400kHz Switching Frequency

Typical Application Circuits (continued)

Adjustable 5V Output Typical Application Circuit

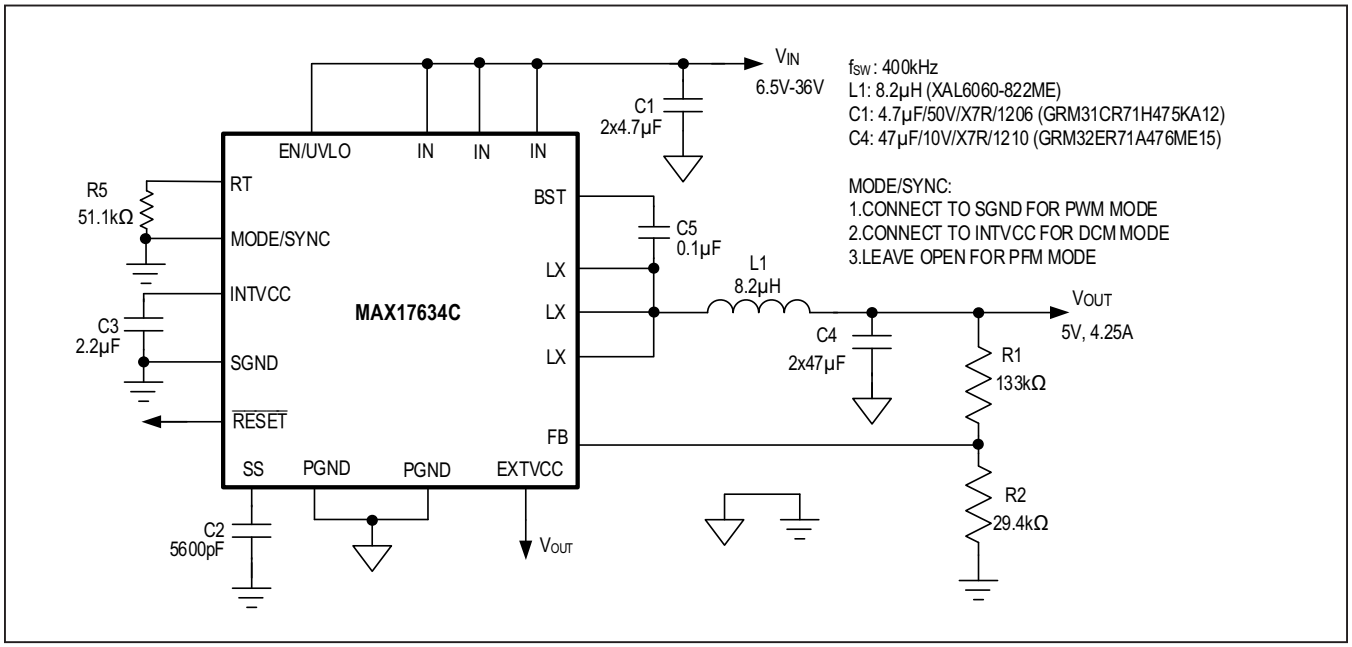


Figure 4. Adjustable 5V Output with 400kHz Switching Frequency

Fixed 3.3V Output Typical Application Circuit

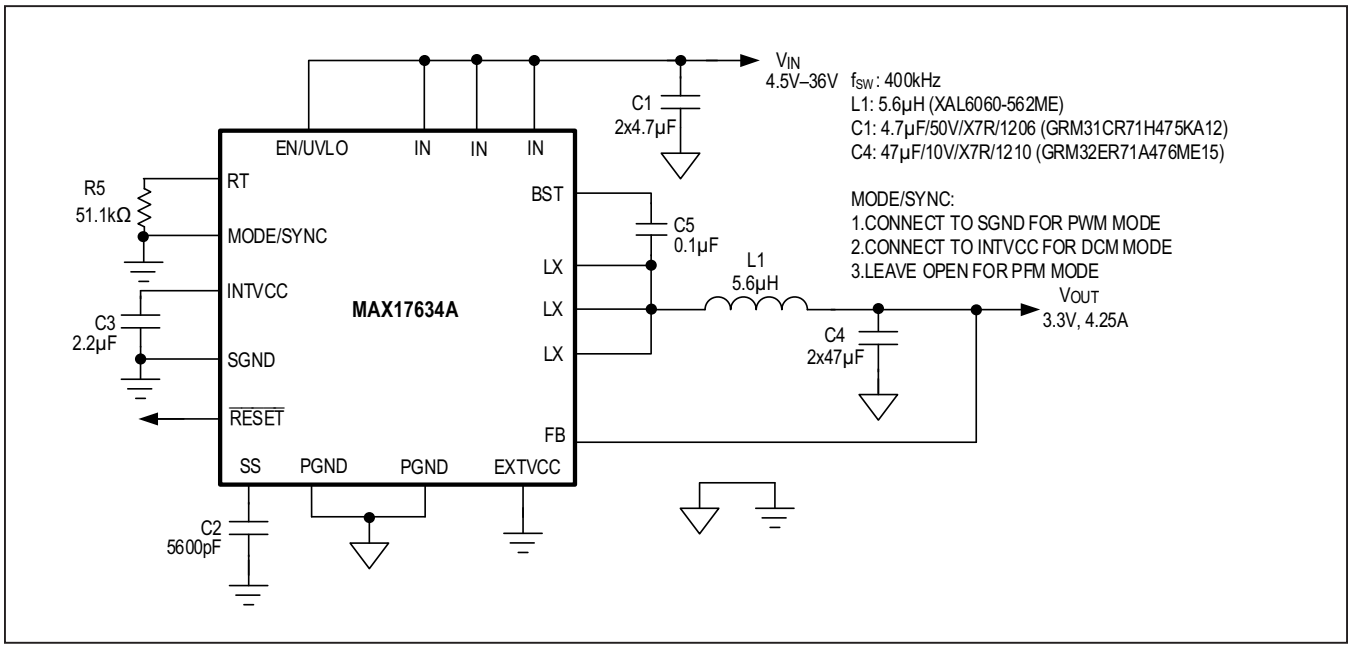


Figure 5. Fixed 3.3V Output with 400kHz Switching Frequency

Typical Application Circuits (continued)

Fixed 5V Output Typical Application Circuit

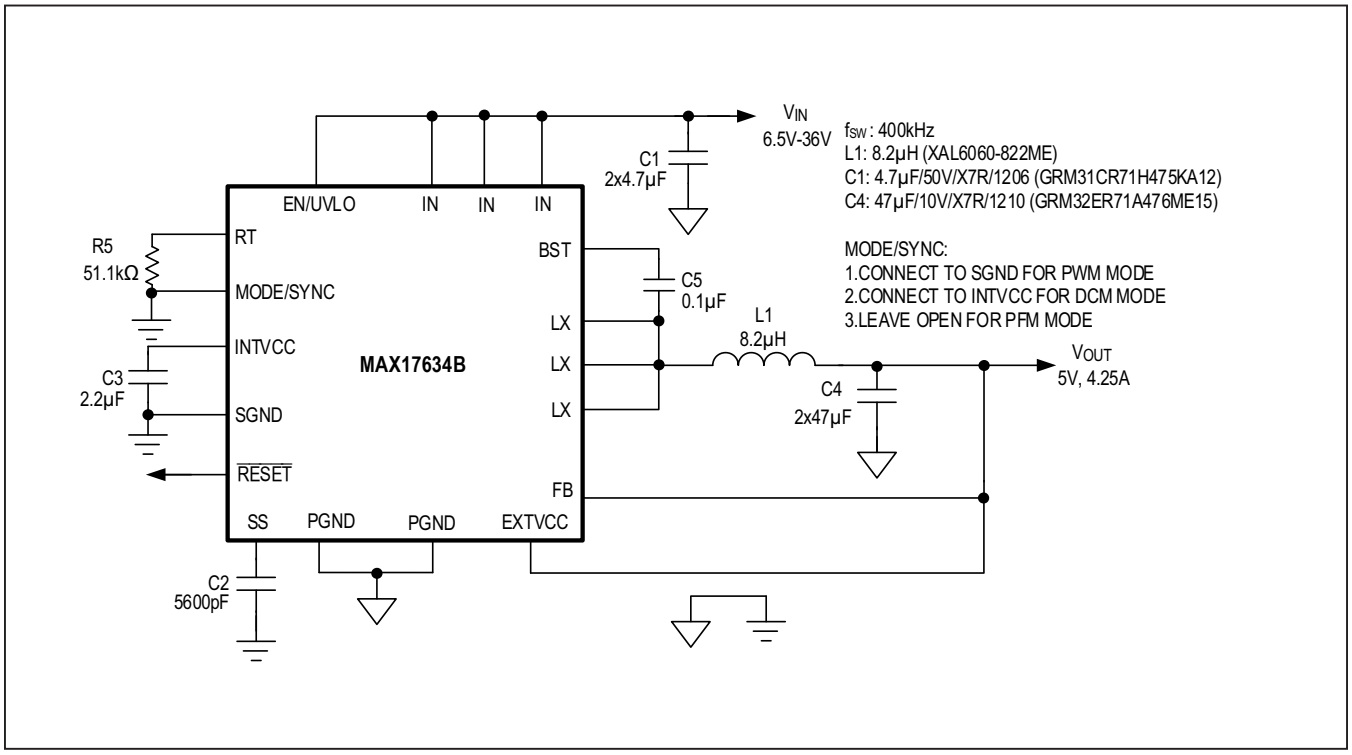


Figure 6. Fixed 5V Output with 400kHz Switching Frequency

Ordering Information

PART NUMBER	OUTPUT VOLTAGE(V)	PIN-PACKAGE
MAX17634AATP+	3.3	20 TQFN 4mm x 4mm
MAX17634BATP+	5	20 TQFN 4mm x 4mm
MAX17634CATP+	Adjustable	20 TQFN 4mm x 4mm

+Denotes a lead(Pb)-free/RoHS compliant package.