Click here to ask about the production status of specific part numbers.

MAX17670, MAX17671, MAX17672

Integrated 4V-60V, 150mA, High-Efficiency, Synchronous Step-Down DC-DC Converter with 50mA Linear Regulator

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power-supply solutions. MAX17670, MAX17671, and MAX17672 are dual-output regulators integrating a 4V to 60V, 150mA high-voltage, high-efficiency, Himalaya synchronous step-down converter with internal MOSFETs and a high-PSRR, low-noise, 2.35V to 5.5V, 50mA linear regulator. The MAX17670 and MAX17671 provide fixed step-down converter output voltages of 3.3V and 5V, respectively. The output voltage of the MAX17672 step-down converter is adjustable (0.8V up to 90% of V_{IN}). 3.3V (MAX17671 and MAX17672 only), 3.0V, 2.5V, 1.8V, 1.5V, and 1.2V linear regulator output voltage options are supported. See the *Ordering Information* for details.

The feedback-voltage regulation accuracy over -40°C to +125°C temperature range for the linear regulator is ±1.3% and for the step-down converter is ±2%. The devices are available in a compact 10-pin (3mm x 3mm) TDFN package. Simulation models are available.

Applications

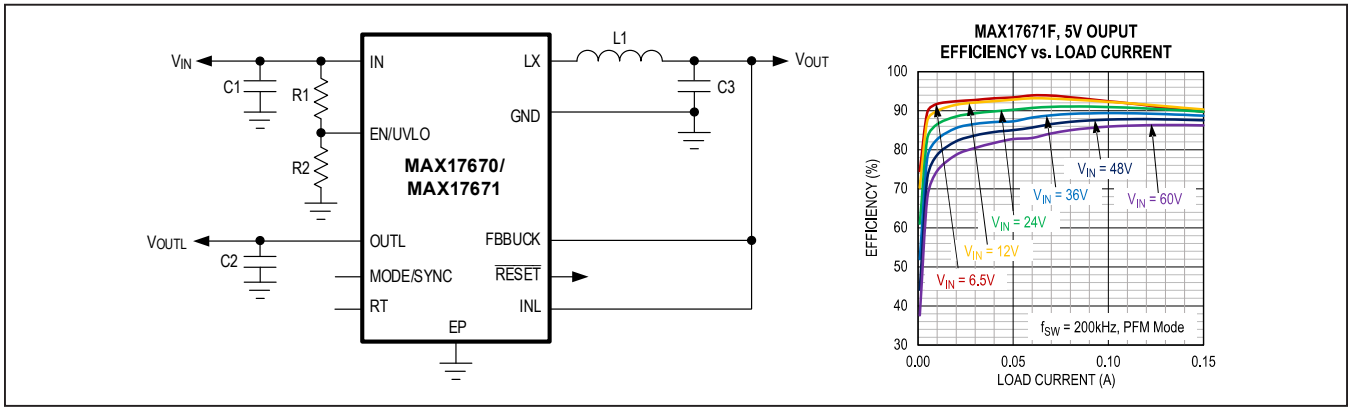
- Industrial Sensors and Process Control
- High-Voltage Linear Regulator Replacement
- Battery-Powered Equipment
- HVAC and Building Control

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky–Synchronous Operation
  - Internal Compensation
  - Built-In Soft-Start
  - All-Ceramic Capacitors, Compact Layout
  - Protection against Inductive Short at Step-Down Converter Output
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4V to 60V Input Range for the Step-Down Converter Regulator
  - Up to 98% Duty-Cycle Step-Down Operation
  - 200kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization for Step-down Converter
  - 2.35V to 5.5V, Input Range for the Linear Regulator
  - Linear Regulator with up to 50mA Load Current Capability
- Reduces Power Dissipation
  - 50µA No-Load Supply Current
  - PFM Enables Enhanced Light-Load Efficiency
  - 2.5µA Shutdown Current
  - Bootstrap Bias Input for Improved Efficiency
- Reliable Operation in Adverse Environments
  - Peak Current-Limit Protection
  - Built-In Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Resistor Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range / -40°C to +150°C Junction Temperature Range

Simplified Application Circuit



Absolute Maximum Ratings

IN to GND .....-0.3V to +70V
LX, EN/UVLO to GND .....-0.3V to IN + 0.3V
RT, OUTL, MODE/SYNC, $\overline{\text{RESET}}$ to GND .....-0.3V to +6V
INL to GND .....-5.5V to lower of (V_{IN} + 0.6V) or +6V
FBBUCK to GND (MAX17670, MAX17671).....-5.5V to +6V
FBBUCK to GND (MAX17672) .....-0.3V to +6V
INL to FBBUCK .....-5V to +6V

Linear Regulator and Step-Down Converter
Output Short-Circuit Duration .....Continuous
Continuous Power Dissipation
(T_A = +70°C, derate 24.4mW/°C above +70°C.).....1952mW
Operating Temperature Range (Note 1)..... -40°C to +125°C
Junction Temperature..... -40°C to +150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Package Information

PACKAGE TYPE: 10-PIN TDFN	
Package Code	T1033+1C
Outline Number	**21-0137**
Land Pattern Number	**90-0003**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{INL}= 5V, V_{FBBUCK} = 1.05 x $V_{FBBUCK-REG}$, C_{OUTL} = 2.2µF to GND, V_{GND} = 0V, RT = LX = MODE/SYNC = $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input-Voltage Range	V_{IN}		4		60	V
Input-Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V, T_A = +25°C		2.5	4.5	µA
Input-Quiescent Current	I_{Q-PFM}			70		µA
	I_{Q-PWM}	V_{FBBUCK} = 0.95 x $V_{FBBUCK-REG}$, Normal switching mode, V_{INL} = 0V		1336		
		V_{FBBUCK} = 0.95 x $V_{FBBUCK-REG}$, Normal switching mode, V_{INL} = 5V		1000		
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.112	
EN/UVLO Input-Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 1.3V, T_A = 25°C	-100		100	nA
EXTERNAL BIAS (INL)						
INL Switch Over Voltage	V_{INL_TH}	INL rising	2.725	3	3.21	V
INL Switch Over Hysteresis	V_{INL_HYS}			0.17		V
INL Operating Voltage Range			3.21		5.5	V
HIGH-SIDE MOSFET AND LOW-SIDE MOSFET DRIVER						
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.1A (Sourcing)		2.7	5.1	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.1A (Sinking)		1.33	2.7	Ω
LX-Leakage Current	I_{LX_LKG}	V_{EN} = 0V, V_{LX} = (V_{GND} +1V) to (V_{IN} - 1V), T_A = 25°C	-1		+1	µA
SOFT-START						
Soft-Start Time	t_{SS1}		4.4	5.1	5.8	ms
STEP-DOWN CONVERTER FEEDBACK (FBBUCK)						
FBBUCK Regulation Voltage	$V_{FBBUCK-REG}$	MODE/SYNC = GND, MAX17670	3.216	3.3	3.365	V
		MODE/SYNC = unconnected, MAX17670	3.216	3.35	3.425	
		MODE/SYNC = GND, MAX17671	4.887	5	5.087	
		MODE/SYNC = unconnected, MAX17671	4.887	5.075	5.188	
		MODE/SYNC = GND, MAX17672	0.782	0.8	0.814	
		MODE/SYNC = unconnected, MAX17672	0.782	0.812	0.830	
FBBUCK Input-Bias Current	I_{FBBUCK}	MAX17670, MAX17671		10		µA
		MAX17672	-100		100	nA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{INL}= 5V, V_{FBBUCK} = 1.05 x $V_{FBBUCK-REG}$, C_{OUTL} = 2.2µF to GND, V_{GND} = 0V, RT = LX = MODE/SYNC = $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		245	295	345	mA
Sink Current-Limit Threshold	$I_{SINK-LIMIT}$	MODE/SYNC = GND	65	105	145	mA
				1		
PFM Current-Limit Threshold	I_{PFM}		55	92	120	mA
OSCILLATOR (RT)						
Switching Frequency Accuracy		f_{SW} = 200kHz to 2.2MHz	-11		+11	%
Switching Frequency	f_{SW}		536	610	680	kHz
Switching Frequency Adjustable Range		See the *Switching Frequency (RT)* section for details	200		2200	
TIMING						
Minimum On-Time	t_{ON_MIN}			75	128	ns
Minimum Off-Time	t_{OFF_MIN}		40	55	75	ns
Minimum Off-Time during SYNC Mode of Operation	$t_{OFF\_MIN(SYNC)}$		48	75	100	ns
HICCUP Timeout				51		ms
MODE/SYNC						
MODE/SYNC Internal Pullup Resistor	R_{MODE}	Mode = PFM		32		kΩ
		Mode = PWM		1100		
SYNC Input Frequency			1.1 x f_{SW}		1.4 x f_{SW}	
Minimum SYNC Pulse Width			100			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
$\overline{RESET}$						
$\overline{RESET}$ Output-Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output-Leakage Current		T_A = +25°C, $V_{\overline{RESET}}$ = 5.5V	-100		100	nA
FBBUCK Threshold for $\overline{RESET}$ Rising	$V_{FBBUCKR}$	FBBUCK rising (Note 3)	92	95	98	%
FBBUCK Threshold for $\overline{RESET}$ Falling	$V_{FBBUCKF}$	FBBUCK falling (Note 3)	89	92	95	
OUTL Threshold for $\overline{RESET}$ Rising	V_{OUTLR}	OUTL rising (Note 3)	91.5	94.5	97.5	
OUTL Threshold for $\overline{RESET}$ Falling	V_{OUTLF}	OUTL falling (Note 3)	88	91	94	

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{INL}= 5V, V_{FBBUCK} = 1.05 x $V_{FBBUCK-REG}$, C_{OUTL} = 2.2µF to GND, V_{GND} = 0V, RT = LX = MODE/SYNC = $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ Delay after FBBUCK and V_{OUTL} Reach 95% Regulation	t_D	See *Reset Output ($\overline{RESET}$)* section for details		2.1		ms
LINEAR REGULATOR INPUT SUPPLY (INL)						
Linear Regulator Input-Voltage Range	V_{INL}		2.35		5.5	V
Linear Regulator Input-Quiescent Current	I_{INL}	I_{OUTL} = 0A, V_{INL} = 5, V_{FFBUCK} = 0.95 × $V_{FFBUCK-REG}$, Normal Switching mode.		710		µA
		I_{OUTL} = 0A, V_{INL} = 2.5		35		
Linear Regulator UVLO	V_{INL_UVLO}		2.11	2.18	2.25	V
Linear Regulator UVLO Hysteresis	$V_{INL\_UVLO(HYS)}$			50		mV
LINEAR REGULATOR OUTPUT VOLTAGE (OUTL)						
OUTL Accuracy		V_{INL} = 2.8V, I_{OUTL} = 10mA, V_{OUTL} = 1.2V, 1.5V, 1.8V	-1.5		+1.5	%
		V_{INL} = V_{OUTL} + 0.8V, I_{OUTL} = 10mA, V_{OUTL} = 2.5V, 3.0V, 3.3V	-1.33		+1.33	
Load Regulation		0.1mA < I_{OUTL} < 50mA. V_{INL} = 2.8V for V_{OUTL} = 1.2V, 1.5V, 1.8V; V_{INL} = V_{OUTL} +0.8V for V_{OUTL} = 2.5V, 3.0V, 3.3V		0.5	0.9	%
Dropout Voltage	V_{DO}	V_{INL} = V_{OUTL}, I_{OUTL} = 50mA (Note 4)		200	400	mV
Linear Regulator Current Limit	I_{LDO_LIM}	V_{OUTL} = 70% of nominal value, V_{INL} = V_{OUTL} + 2V	55	84		mA
Soft-Start Time	t_{SS2}			1.1		ms
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		160		°C
Thermal-Shutdown Hysteresis				20		°C

Note 2: All the Electrical Specifications are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

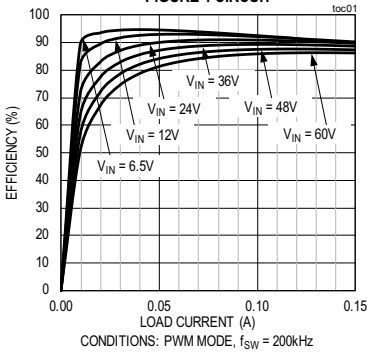
Note 3: Specifications are in respect to regulation voltage.

Note 4: Applicable for linear regulators with nominal output voltages of 2.5V, 3.0V, and 3.3V.

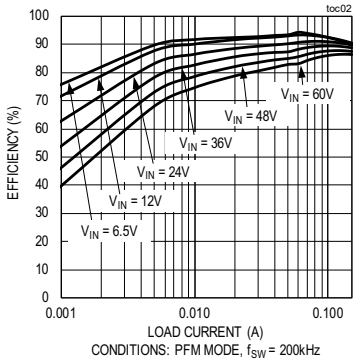
Typical Operating Characteristics

(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

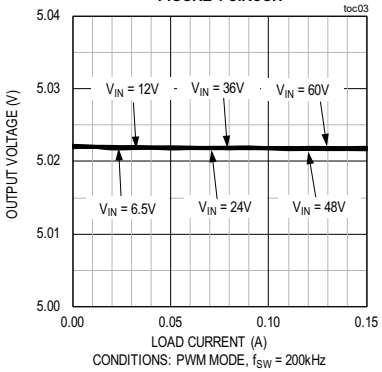
MAX17671F, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



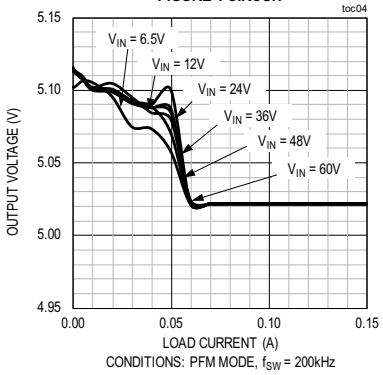
MAX17671F, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



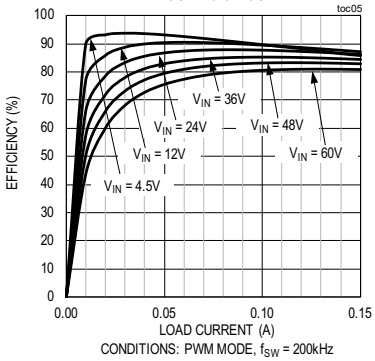
MAX17671F, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 4 CIRCUIT



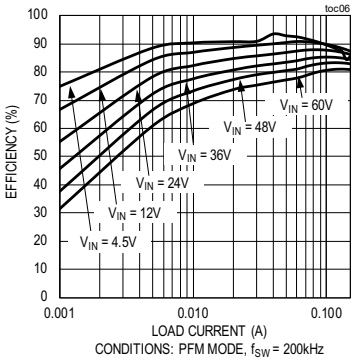
MAX17671F, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 4 CIRCUIT



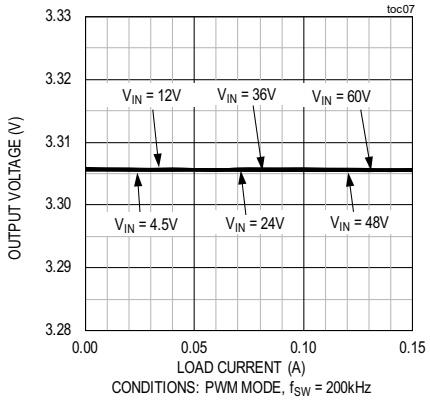
MAX17670E, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 5 CIRCUIT



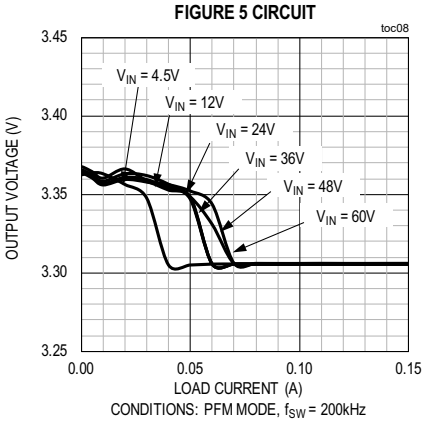
MAX17670E, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 5 CIRCUIT



MAX17670E, 3.3V OUTPUT LOAD AND LINE REGULATION FIGURE 5 CIRCUIT



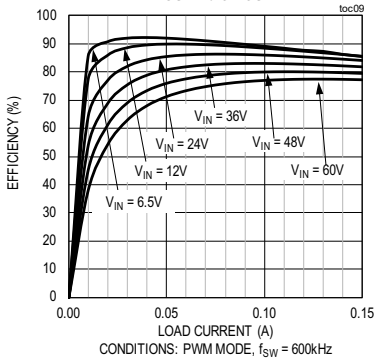
MAX17670E, 3.3V OUTPUT LOAD AND LINE REGULATION FIGURE 5 CIRCUIT



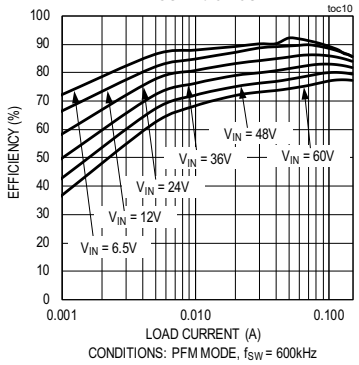
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

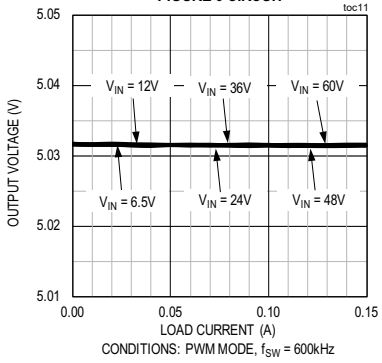
MAX17671F, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 6 CIRCUIT



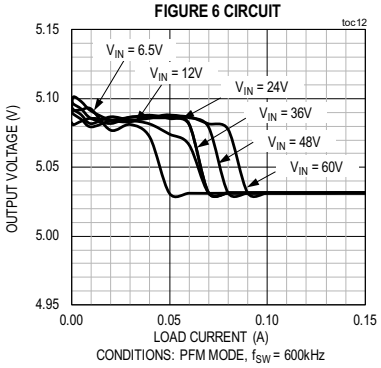
MAX17671F, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 6 CIRCUIT



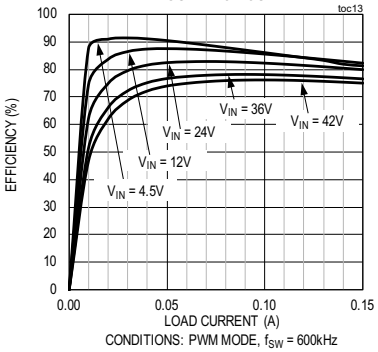
MAX17671F, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 6 CIRCUIT



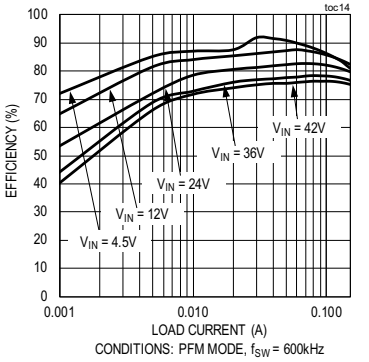
MAX17671F, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 6 CIRCUIT



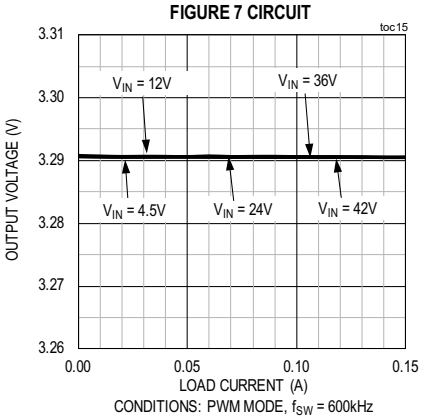
MAX17670E, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 7 CIRCUIT



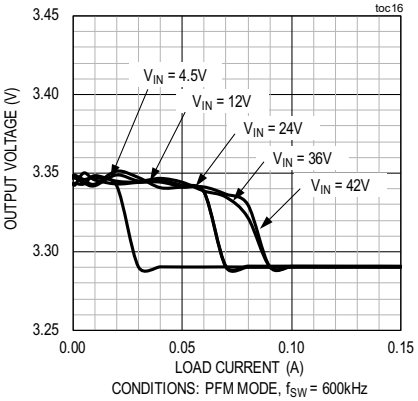
MAX17670E, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 7 CIRCUIT



MAX17670E, 3.3V OUTPUT LOAD AND LINE REGULATION FIGURE 7 CIRCUIT



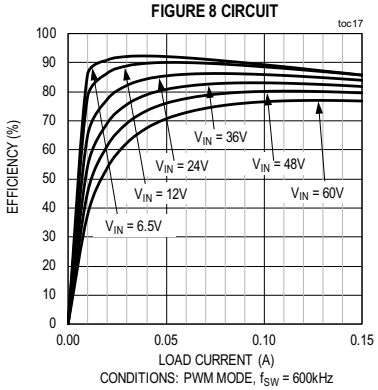
MAX17670E, 3.3V OUTPUT LOAD AND LINE REGULATION FIGURE 7 CIRCUIT



Typical Operating Characteristics (continued)

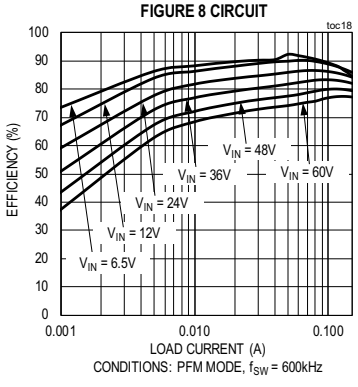
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17672C, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 8 CIRCUIT



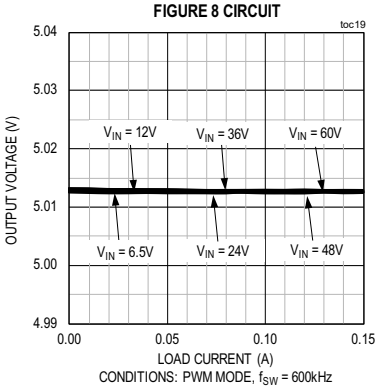
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 8 CIRCUIT



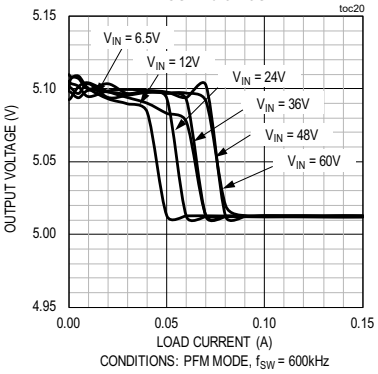
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 8 CIRCUIT



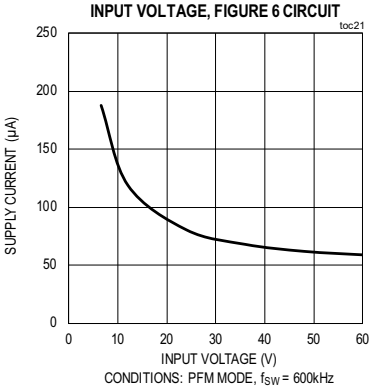
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 8 CIRCUIT



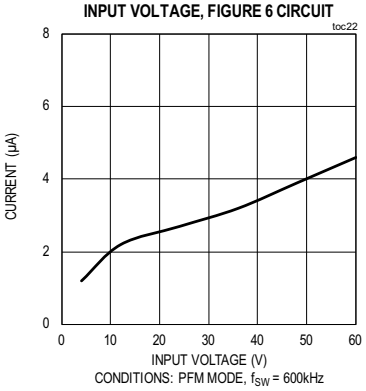
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE, FIGURE 6 CIRCUIT



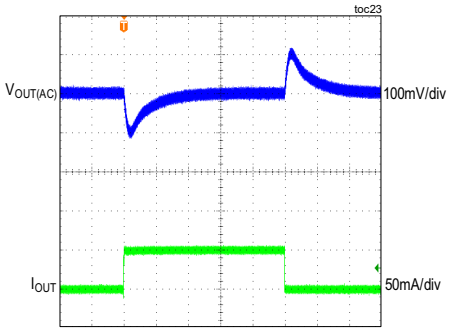
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT SHUTDOWN CURRENT vs. INPUT VOLTAGE, FIGURE 6 CIRCUIT



CONDITIONS: PFM MODE, f_{SW} = 600kHz

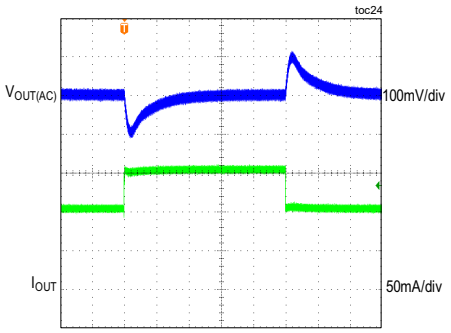
MAX17671F, 5V OUTPUT LOAD TRANSIENT BETWEEN 0mA AND 50mA FIGURE 4 CIRCUIT



100µs/div

CONDITIONS: PWM MODE, f_{SW} = 200kHz

MAX17671F, 5V OUTPUT LOAD TRANSIENT BETWEEN 100mA AND 150mA FIGURE 4 CIRCUIT



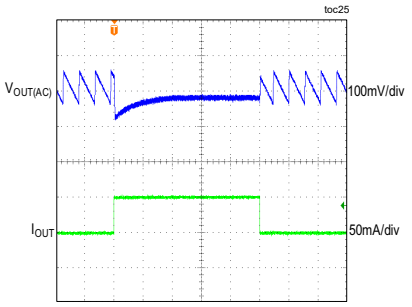
100µs/div

CONDITIONS: PWM MODE, f_{SW} = 200kHz

Typical Operating Characteristics (continued)

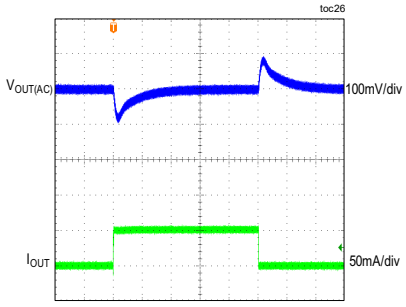
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17671F, 5V OUTPUT
LOAD TRANSIENT BETWEEN 1mA AND 50mA
FIGURE 4 CIRCUIT



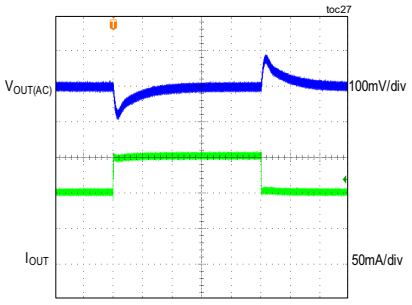
CONDITIONS: PFM MODE, f_{SW} = 200kHz

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0mA AND 50mA
FIGURE 5 CIRCUIT



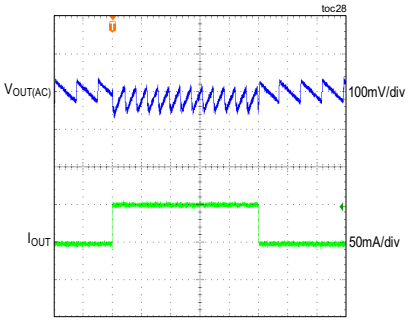
CONDITIONS: PWM MODE, f_{SW} = 200kHz

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 100mA AND 150mA
FIGURE 5 CIRCUIT



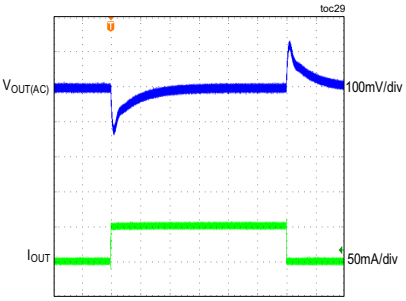
CONDITIONS: PWM MODE, f_{SW} = 200kHz

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 1mA AND 50mA
FIGURE 5 CIRCUIT



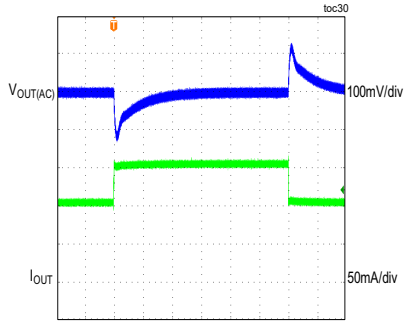
CONDITIONS: PFM MODE, f_{SW} = 200kHz

MAX17671F, 5V OUTPUT
LOAD TRANSIENT BETWEEN 0mA AND 50mA
FIGURE 6 CIRCUIT



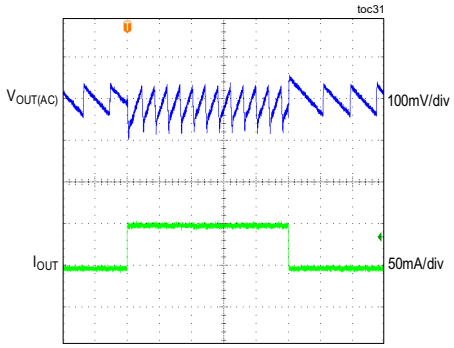
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT
LOAD TRANSIENT BETWEEN 100mA AND 150mA
FIGURE 6 CIRCUIT



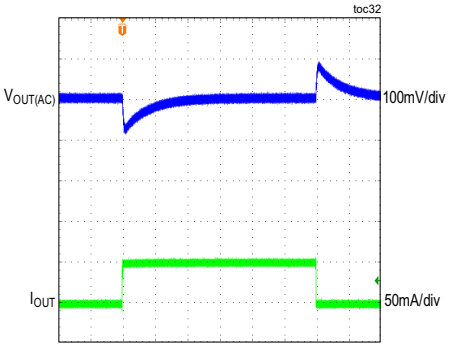
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT
LOAD TRANSIENT BETWEEN 1mA AND 50mA
FIGURE 6 CIRCUIT



CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0mA AND 50mA
FIGURE 7 CIRCUIT

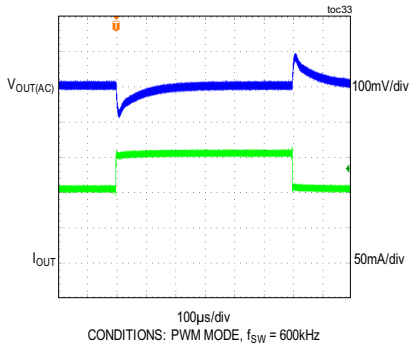


CONDITIONS: PWM MODE, f_{SW} = 600kHz

Typical Operating Characteristics (continued)

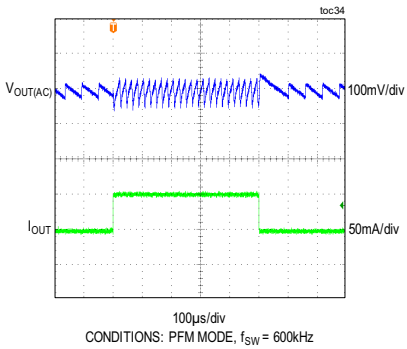
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 100mA AND 150mA
FIGURE 7 CIRCUIT



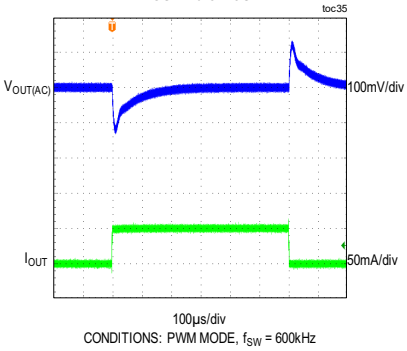
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17670E, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 1mA AND 50mA
FIGURE 7 CIRCUIT



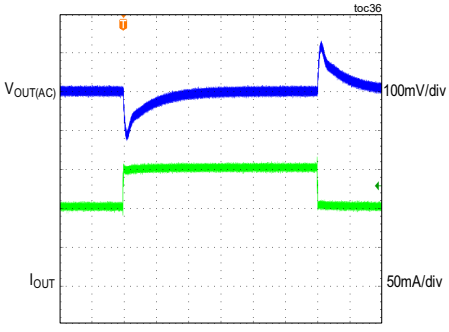
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT
LOAD TRANSIENT BETWEEN 0mA AND 50mA
FIGURE 8 CIRCUIT



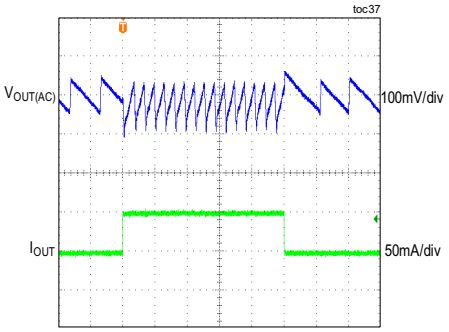
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT
LOAD TRANSIENT BETWEEN 100mA AND 150mA
FIGURE 8 CIRCUIT



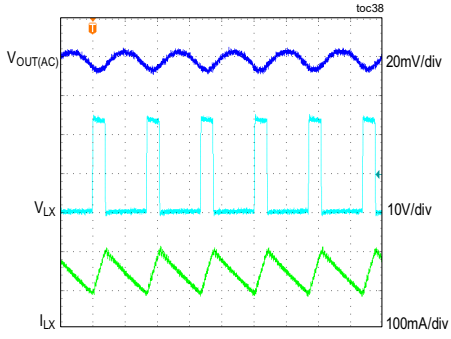
CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17672C, 5V OUTPUT
LOAD TRANSIENT BETWEEN 1mA AND 50mA
FIGURE 8 CIRCUIT



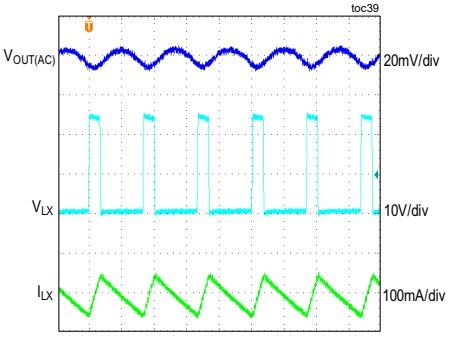
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT
STEADY STATE AT 150mA LOAD
FIGURE 6 CIRCUIT



CONDITIONS: PWM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT
STEADY STATE AT 0mA LOAD
FIGURE 6 CIRCUIT

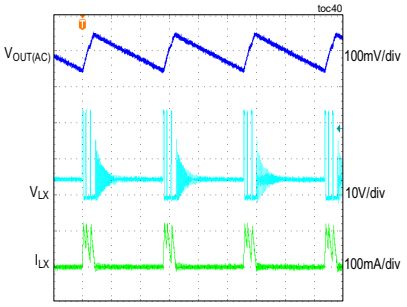


CONDITIONS: PWM MODE, f_{SW} = 600kHz

Typical Operating Characteristics (continued)

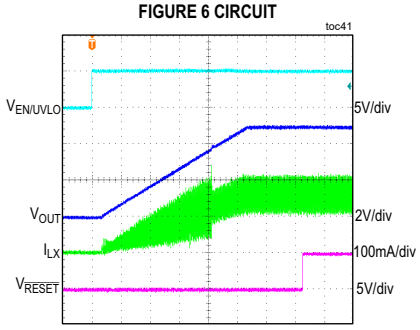
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17671F, 5V OUTPUT
STEADY STATE AT 10mA LOAD
FIGURE 6 CIRCUIT



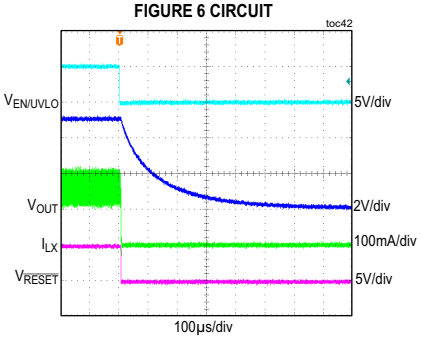
CONDITIONS: PFM MODE, f_{SW} = 600kHz

MAX17671F, 5V OUTPUT
SOFT-START THROUGH EN/UVLO
FIGURE 6 CIRCUIT



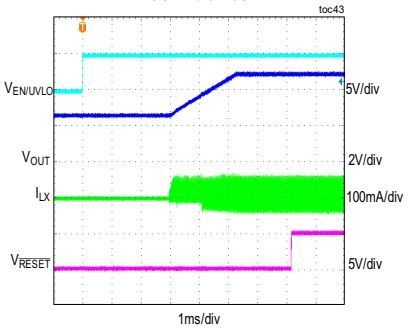
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 33Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{OUT} WITH A 10kΩ RESISTOR

MAX17671F, 5V OUTPUT
SHUTDOWN THROUGH EN/UVLO
FIGURE 6 CIRCUIT



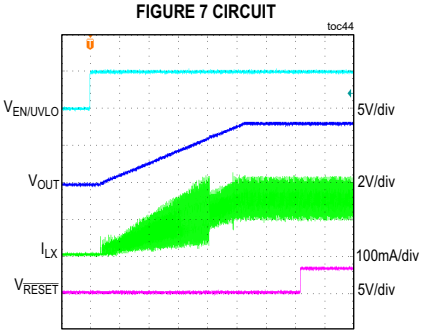
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 33Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{OUT} WITH A 10kΩ RESISTOR

MAX17671F, 5V OUTPUT
SOFT-START WITH PREBIAS VOLTAGE OF 2.5V
FIGURE 6 CIRCUIT



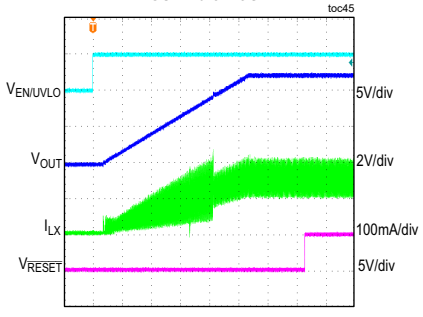
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 1kΩ RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{OUT} WITH A 10kΩ RESISTOR

MAX17670E, 3.3V OUTPUT
SOFT-START THROUGH EN/UVLO
FIGURE 7 CIRCUIT



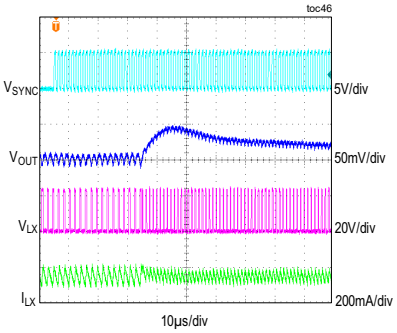
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 22Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{OUT} WITH A 10kΩ RESISTOR

MAX17672C, 5V OUTPUT
SOFT-START THROUGH EN/UVLO
FIGURE 8 CIRCUIT



CONDITIONS: PWM MODE, f_{SW} = 600kHz, 33Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{OUT} WITH A 10kΩ RESISTOR

MAX17671F, 5V OUTPUT
EXTERNAL CLOCK SYNCHRONIZATION
WITH 840kHz, FIGURE 6 CIRCUIT

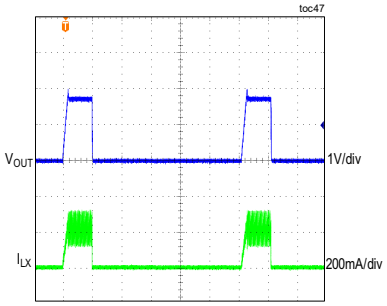


CONDITIONS: f_{SW} = 600kHz, 150mA LOAD

Typical Operating Characteristics (continued)

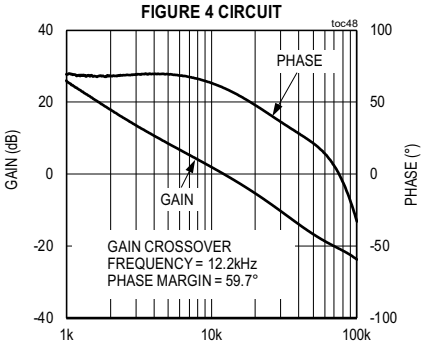
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17671F, 5V OUTPUT OVERLOAD PROTECTION FIGURE 6 CIRCUIT



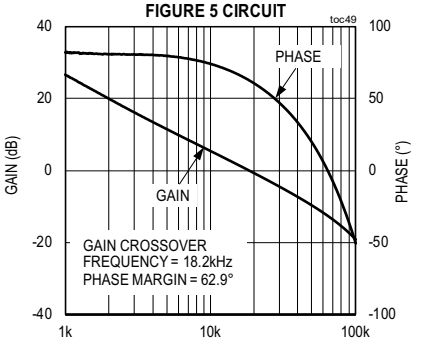
CONDITIONS: f_{SW} = 600kHz

MAX17671F, 5V OUTPUT CLOSED LOOP BODE PLOT FIGURE 4 CIRCUIT



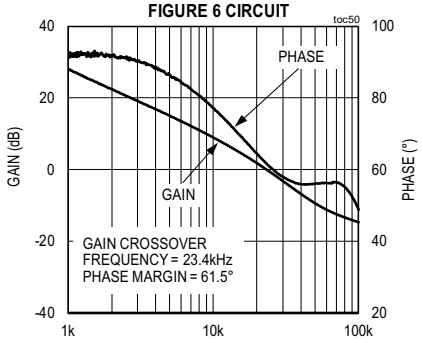
CONDITIONS: PWM MODE, f_{SW} = 200kHz, 150mA LOAD

MAX17670E, 3.3V OUTPUT CLOSED LOOP BODE PLOT FIGURE 5 CIRCUIT



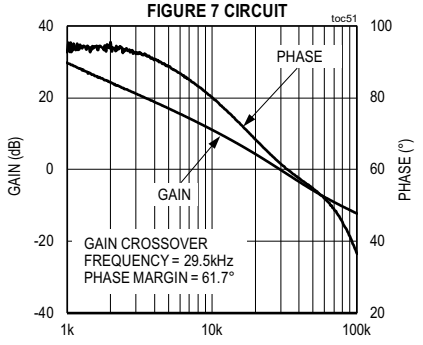
CONDITIONS: PWM MODE, f_{SW} = 200kHz, 150mA LOAD

MAX17671F, 5V OUTPUT CLOSED LOOP BODE PLOT FIGURE 6 CIRCUIT



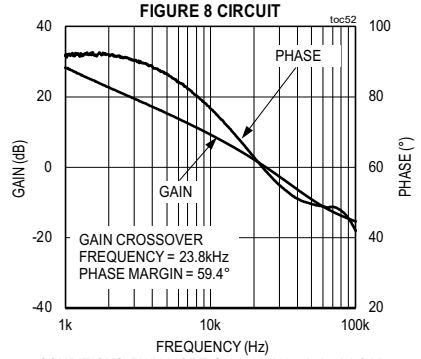
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 150mA LOAD

MAX17670E, 3.3V OUTPUT CLOSED LOOP BODE PLOT FIGURE 7 CIRCUIT



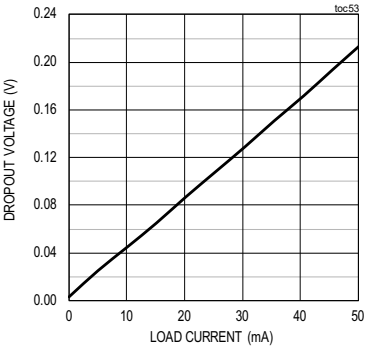
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 150mA LOAD

MAX17672C, 5V OUTPUT CLOSED LOOP BODE PLOT FIGURE 8 CIRCUIT



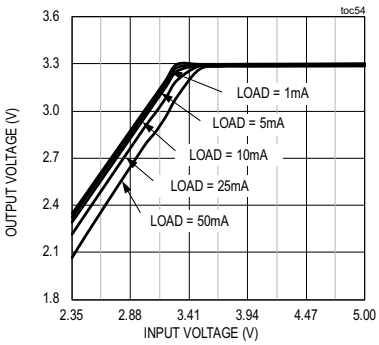
CONDITIONS: PWM MODE, f_{SW} = 600kHz, 150mA LOAD

MAX17671F, 3.3V LINEAR REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT



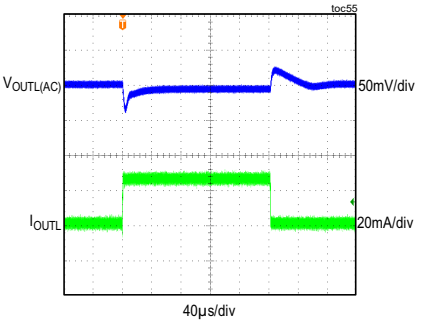
CONDITIONS: INL CONNECTED TO EXTERNAL SUPPLY

MAX17671F, 3.3V LINEAR REGULATOR OUTPUT VOLTAGE vs. INPUT VOLTAGE



CONDITIONS: INL CONNECTED TO EXTERNAL SUPPLY

MAX17671F, 3.3V LINEAR REGULATOR LOAD TRANSIENT BETWEEN 1mA AND 25mA FIGURE 6 CIRCUIT

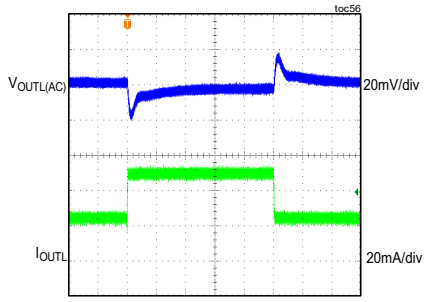


CONDITIONS: INL CONNECTED TO V_{OUT}, PWM MODE

Typical Operating Characteristics (continued)

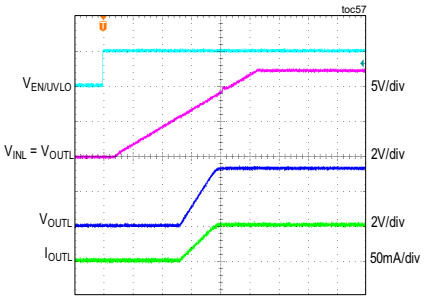
(V_{IN} = 24V, V_{GND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17671F, 3.3V LINEAR REGULATOR LOAD TRANSIENT BETWEEN 25mA AND 50mA FIGURE 6 CIRCUIT



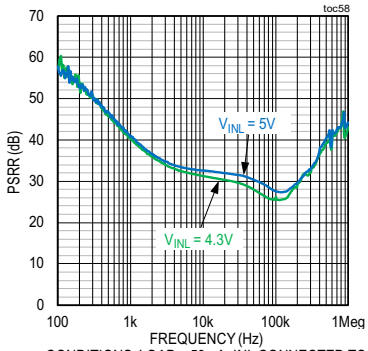
CONDITIONS: INL CONNECTED TO V_{OUT}, PWM MODE

MAX17671F, 3.3V LINEAR REGULATOR START-UP FROM EN/UVLO FIGURE 6 CIRCUIT



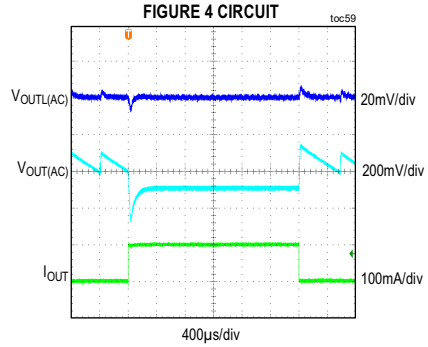
CONDITIONS: f_{SW} = 600kHz, 66Ω RESISTIVE LOAD, INL CONNECTED TO V_{OUT}

MAX17671F, 3.3V OUTPUT LINEAR REGULATOR, POWER SUPPLY REJECTION RATIO vs. FREQUENCY



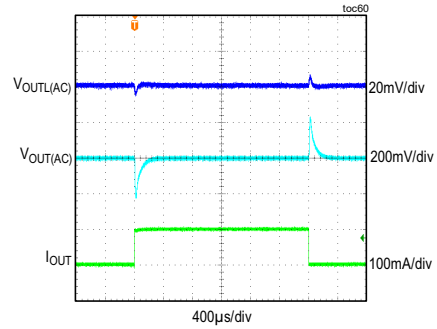
CONDITIONS: LOAD = 50mA, INL CONNECTED TO EXTERNAL SUPPLY

MAX17671F, STEP-DOWN CONVERTER LOAD TRANSIENT ON 3.3V LINEAR REGULATOR OUTPUT, FIGURE 4 CIRCUIT



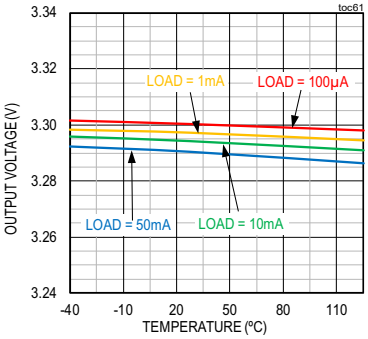
CONDITIONS: f_{SW} = 200kHz, PFM MODE, I_{OUTL} = 1mA, STEP-DOWN CONVERTER LOAD STEP BETWEEN 0mA AND 100mA

MAX17671F, STEP-DOWN CONVERTER LOAD TRANSIENT ON 3.3V LINEAR REGULATOR OUTPUT, FIGURE 4 CIRCUIT



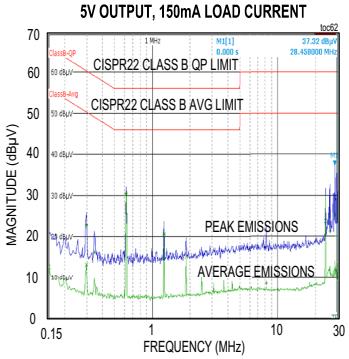
CONDITIONS: f_{SW} = 200kHz, PWM MODE, I_{OUTL} = 50mA, STEP-DOWN CONVERTER LOAD STEP BETWEEN 0mA AND 100mA

MAX17671F, 3.3V LINEAR REGULATOR OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE, FIGURE 4 CIRCUIT



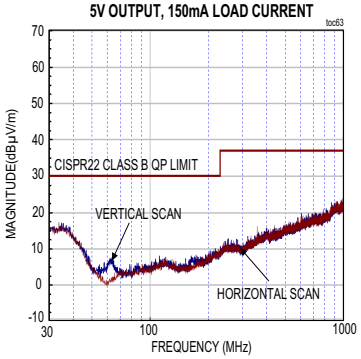
CONDITIONS: PWM MODE, INL CONNECTED TO V_{OUT}

CONDUCTED EMISSIONS PLOT 5V OUTPUT, 150mA LOAD CURRENT



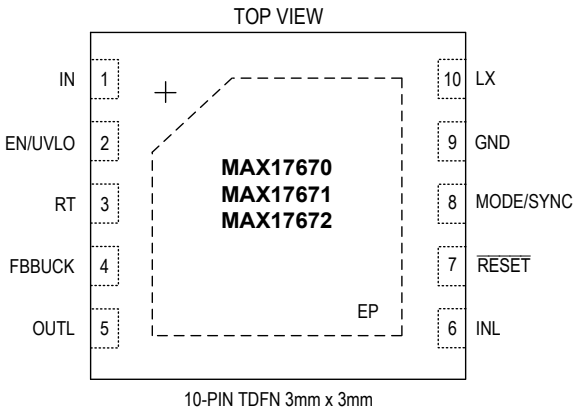
MEASURED ON MAX17672CEVKIT# with L2 = 8.2µH, C10 = 1µF/100V/X7R/1206

RADIATED EMISSIONS PLOT 5V OUTPUT, 150mA LOAD CURRENT



MEASURED ON MAX17672CEVKIT# with L2 = SHORT, C10 = OPEN

Pin Configuration



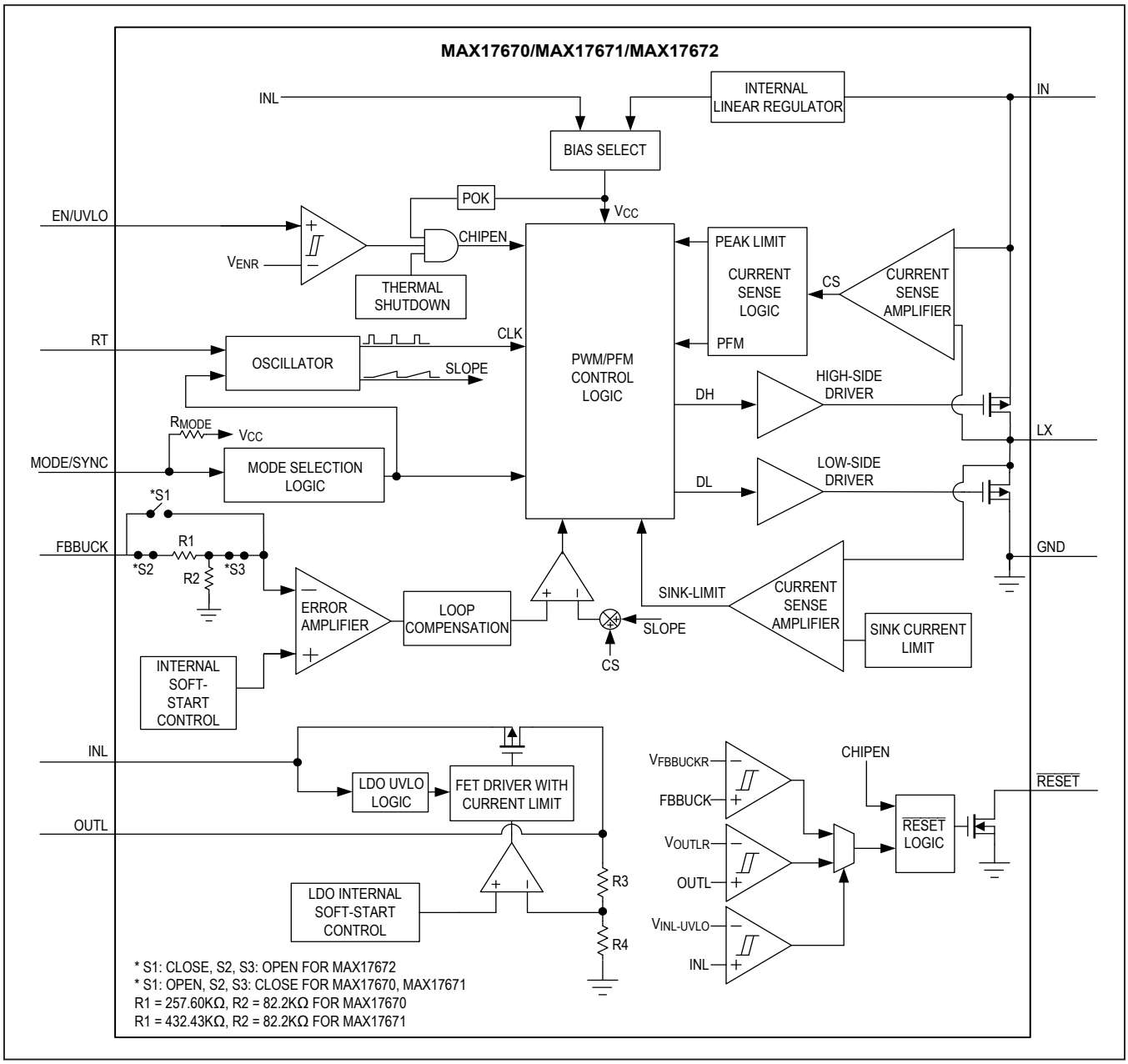
Pin Description

PIN	NAME	FUNCTION
1	IN	Power Supply Input of the Step-Down Converter. Decouple the IN pin to GND with an X7R 1µF ceramic capacitor.
2	EN/ UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the midpoint of a resistor divider from IN to GND to set the input voltage at which the device turns ON. The allowed minimum turn ON input voltage is 4V. Pull low to GND for disabling the device. See *Setting the Input Undervoltage-Lock-out Level* section for more details.
3	RT	Programmable Switching Frequency Input. Connect a resistor from RT to GND to program the switching frequency from 200kHz to 2.2MHz. Leave the RT pin unconnected for a default 600kHz switching frequency. See the *Switching Frequency (RT)* section for details.
4	FBBUCK	Step-down Converter Feedback Input. For MAX17670 and MAX17671, connect FBBUCK directly to the output node of the step-down converter. For the MAX17672, connect FBBUCK to a resistor-divider between the regulated buck-voltage node and GND. See the *Adjusting the Output Voltage* section for details.
5	OUTL	Linear Regulator Output Pin. Connect at least 2.2µF, 0603 capacitor across OUTL and GND.
6	INL	Linear Regulator Power-Supply Input. Connect this pin to the Step-down converter's output capacitor for output voltages up to 5.5V. Otherwise, the INL pin should be grounded. INL also acts as a bootstrap input to power up internal blocks for improved efficiency. INL switchover occurs only for INL voltages between 3.3V and 5.5V. See the *Linear Regulator Power-Supply Input (INL)* section for details.
7	$\overline{\text{RESET}}$	Open-Drain Reset Output. Pull up $\overline{\text{RESET}}$ to an external power supply with a resistor. The $\overline{\text{RESET}}$ pin is driven low if either FBBUCK voltage or OUTL voltage drops below 92% of their set value and also when EN/UVLO voltage falls below its threshold value. $\overline{\text{RESET}}$ goes high 2.1ms after FBBUCK and OUTL voltages rise above 95% of their set value if INL is above V_{INL_UVLO}. Else, $\overline{\text{RESET}}$ considers only FBBUCK voltage for its high impedance state.
8	MODE/ SYNC	Mode Selection and External Clock Synchronization Input. Connect the MODE/SYNC pin to the GND pin to enable the fixed-frequency PWM operation. Leave MODE/SYNC unconnected for PFM operation. An external clock can be applied to the MODE/SYNC pin to synchronize the internal clock to the external clock. See the *Mode Selection and External Synchronization (MODE/SYNC)* section for details.
9	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines Layout Guidelines* section.

Pin Description (continued)

PIN	NAME	FUNCTION
10	LX	Switching Node of the Step-Down Converter. Connect LX to the switching side of the inductor. LX is high impedance when the device is shut down.
—	EP	Exposed Pad. Always connect EP to the GND pin of the IC. Also, connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17670, MAX17671, and MAX17672 EV kit datasheet for an example of the correct method for EP connection and thermal vias.

Functional Diagrams



Detailed Description

MAX17670, MAX17671, and MAX17672 are dual-output regulators integrating a 4V to 60V, 150mA high voltage, high efficiency, Himalaya synchronous step-down converter with internal MOSFETs and a high PSRR, low noise, 2.35V to 5.5V, 50mA linear regulator. MAX17670 and MAX17671 are the fixed 3.3V and 5V step-down converter output voltage devices, respectively. MAX17672 is the adjustable step-down converter output voltage (0.8V to 90%V_{IN}) device. All three devices feature internal compensation. The feedback-voltage regulation accuracy over -40°C to +125°C temperature range for the linear regulator is ±1.3% for 3.3V, 3.0V, 2.5V linear regulator outputs; ±1.5% for 1.8V, 1.5V, 1.2V linear regulator outputs; and, ±2% for the step-down converter.

The step-down converter uses an internally compensated, peak-current mode control architecture. On the rising edge of the internal clock, the high-side p-MOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the p-MOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the p-MOSFET is kept off and the low-side n-MOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output.

The step-down converter has a 5.1ms fixed internal soft-start to reduce the inrush currents. An EN/UVLO pin allows the user to turn the device on/off at the desired input-voltage level greater than 4V. An open-drain $\overline{RESET}$ pin allows output-voltage monitoring.

Mode Selection and External Synchronization (MODE/SYNC)

The device features a MODE/SYNC pin for selecting either forced PWM or PFM mode of operation. If the MODE/SYNC pin is grounded, the device operates in a constant-frequency PWM mode at all loads. If the MODE/SYNC pin is unconnected, the device operates in PFM mode at light load. When a rising edge is detected at the MODE/SYNC pin, the internal logic changes the mode from PWM to PFM after 16 internal clock cycles. When a falling edge is detected, the change from PFM to PWM mode is instantaneous.

PWM operation is useful in frequency-sensitive applications and provides fixed switching frequency at all loads. However, PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation.

PFM mode disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak (I_{PFM}) of 92mA (typ) every clock cycle until the output rises to 102% (typ) of the nominal voltage. Once the output reaches 102% (typ) of the nominal voltage, both high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% (typ) of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to reduce quiescent current. After the output falls below 101% (typ) of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102% (typ) of the nominal output voltage. The advantage of PFM mode is higher efficiency at light loads due to the lower quiescent currents in PFM mode.

The device naturally exits PFM mode when the load current demands inductor peak current above I_{PFM} (92mA typ). The device enters PFM mode when the load current is less than half the peak-to-peak inductor ripple current.

The internal oscillator of the device can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the switching frequency programmed by the resistor connected to the RT pin. When an external clock is applied to the MODE/SYNC pin, the internal clock synchronizes to the external clock frequency (from original frequency based on the RT pin setting) after 8 external pulses are detected within 16 internal clock cycles. Mode of operation can be reset with a V_{IN} power cycle or EN/UVLO cycle. The minimum external clock on-time and off-time pulse-widths should be greater than 100ns. See the *Mode Selection and External Synchronization (MODE/SYNC)* section in the *Electrical Characteristics* table for details.

Linear Regulator Power-Supply Input (INL)

The INL pin can be tied to the step-down converter output node for voltages up to 5.5V. Otherwise, INL should be connected to GND.

The linear regulator operates from 2.35V to 5.5V input-voltage range and the linear regulator is enabled when V_{INL} is more than V_{INL_UVLO}.

The INL pin also functions as bootstrap input to power up the internal blocks. Switchover to bootstrap input occurs when V_{INL} is above V_{INL_TH}. This improves the overall efficiency, since the internal blocks are being powered from the step-down converter output which has the voltage less than the input voltage.

Enable/Undervoltage-Lockout Input (EN/UVLO) and Soft-Start

When EN/UVLO voltage increases above V_{ENR} (1.215V typ), the device initiates a built-in 5.1ms (typ) soft-start period after an internal delay of 400µs (t_1), allowing a monotonic increase of the output voltage to the final set value.

EN/UVLO can be used as an input-voltage UVLO adjustment input, to set the turn-on/off input-voltage level. The allowed minimum turn-on/off input voltage is 4V. See the *Setting the Input Undervoltage-Lockout Level* section for details. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces quiescent current to around 2.5µA. If the EN/UVLO pin is driven from an external signal source, a series resistance of 1kΩ (min) is recommended to be placed between the output of the signal source and the EN/UVLO pin to reduce voltage ringing on the line.

Startup Into a Prebiased Step-Down Converter Output

The device supports monotonic startup into a prebiased step-down converter output. When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

$\overline{\text{RESET}}$ Output

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor step-down converter output voltage and linear regulator output voltage. The $\overline{\text{RESET}}$ pin should be pulled up with an external resistor to the desired external power supply.

$\overline{\text{RESET}}$ goes to high impedance 2.1ms after both step-down converter and linear regulator outputs rise above 95% of their nominal set value, if V_{INL} is above V_{INL_UVLO}. Otherwise, $\overline{\text{RESET}}$ only considers step-down converter output voltage for its high impedance state.

$\overline{\text{RESET}}$ pulls low after 4µs (t_2) if one of the either output voltages fall below 92% of their set value. $\overline{\text{RESET}}$ is also driven low when EN/UVLO voltage falls below its threshold value. Figure 1 shows the $\overline{\text{RESET}}$ output timing diagram.

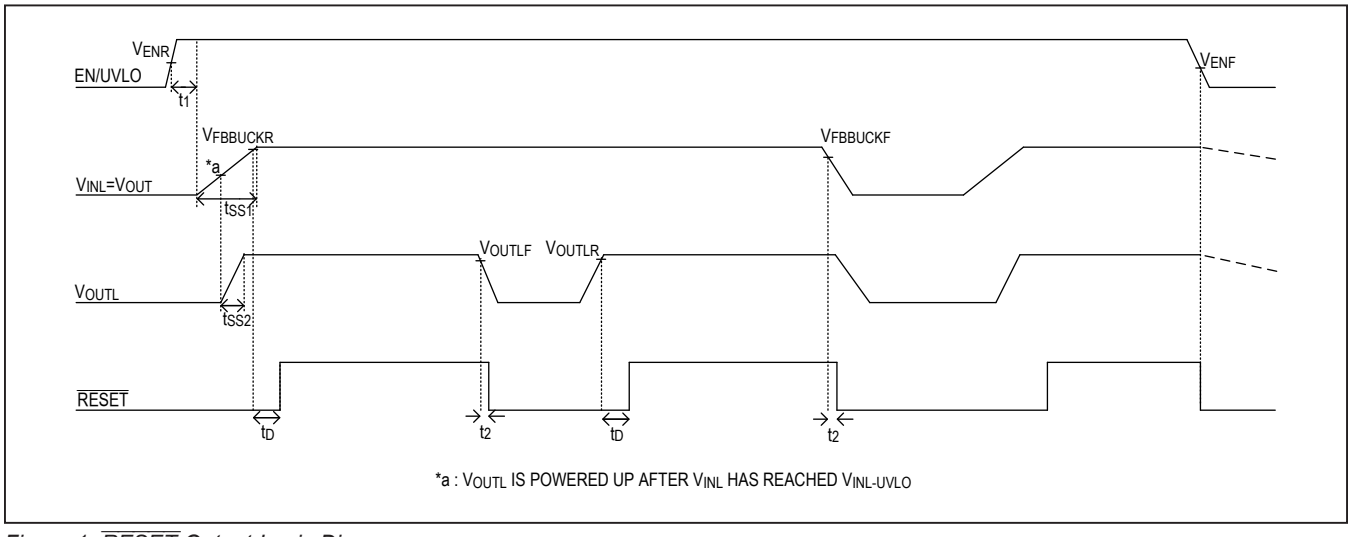


Figure 1. $\overline{\text{RESET}}$ Output Logic Diagram

Switching Frequency (RT)

Switching frequency of the device can be programmed from 200kHz to 2.2MHz by using a resistor connected from RT to GND. The switching frequency (f_{SW}) is related to the resistor (R_{RT}) connected at the RT pin by the following equation:

$$R_{RT} \approx \frac{500}{\left(\frac{11.6}{t_{SW} - 0.045}\right) - 0.5}$$

$$t_{SW} = \frac{1}{f_{SW}}$$

Where R_{RT} is in kΩ and t_{SW} is in µs. Leave the RT pin unconnected for the default 600kHz switching frequency. The value of R_{RT} in the range of 165kΩ (308kHz) and 248kΩ (215kHz) is not allowed for user programming to ensure proper configuration of the internal adaptive-loop compensation scheme. The maximum allowable switching frequency for PFM mode of operation is 900kHz.

Operating Input-Voltage Range

The maximum operating input voltage is determined by the minimum on-time, and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}))}{1 - t_{OFF\_MIN(MAX)} \times f_{SW(MAX)}} + (I_{OUT(MAX)} \times (R_{DS\text{-}ONH(MAX)} - R_{DS-ONL(MAX)}))$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\_MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage,

$I_{OUT(MAX)}$ = Maximum load current,

$R_{DCR(MAX)}$ = Maximum DC resistance of the inductor,

$f_{SW(MAX)}$ = Maximum switching frequency,

$t_{OFF\_MIN(MAX)}$ = Worst case minimum switch off-time (75ns),

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (128ns),

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Maximum on-state resistances of the low-side and high-side MOSFETs, respectively.

Overcurrent Protection

The device implements a hysteretic peak current-limit protection scheme to protect the internal FETs and inductor under output short-circuit conditions. When the inductor peak current exceeds $I_{PEAK\text{-}LIMIT}$ (0.295A typ), the high-side switch is turned off and the low-side switch is turned on to reduce the inductor current. After the current is reduced to 150mA (typ), the high-side switch is turned on at the rising edge of the next clock pulse. The device enters hiccup mode if the inductor current hits $I_{PEAK\text{-}LIMIT}$ for 16 consecutive times. After the hiccup time-out period, the device auto retries to startup and the same operation continues until the short is removed and the inductor peak current goes below $I_{PEAK\text{-}LIMIT}$. Since the inductor current is bounded between the two values, the inductor current runaway never happens in this scheme.

Low Side-Switch Protection

Hysteretic-sink current limit controls the low-side switch sink current to $I_{SINK\text{-}LIMIT}$ (105mA typ) with a ripple of 50mA.

Thermal-Shutdown Protection

Thermal-shutdown protection limits the junction temperature in the IC. This feature is present in PWM mode. When the junction temperature exceeds +160°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs and the linear regulator, allowing the device to cool down. The device turns on with soft-start after the junction temperature reduced by 20°C.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{8150 \times V_{OUT}}{f_{SW}}$$

where:

L = Inductance in µH,

V_{OUT} = Output voltage

f_{SW} = Switching frequency in kHz

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit ($I_{PEAK-LIMIT}$).

Input Capacitor Selection

The input-filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}$/1.414. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

D = V_{OUT}/V_{IN} is the duty ratio of the controller,

f_{SW} = Switching frequency,

ΔV_{IN} = Allowable input voltage ripple,

η = Efficiency

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Output Capacitor Selection for Step-Down Converter

X7R ceramic output capacitors are recommended for the device due to their stability over the temperature in industrial applications. The output capacitor has two functions. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. The output capacitor is sized to support a step load of 50mA such that the output-voltage deviation is less than 3%. The minimum required output capacitance can be calculated as shown in Table 1.

It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels. It should be that the derated value of the selected capacitance meets the minimum required output capacitance.

Linear Regulator Output Capacitor Selection

For stable operation over the full temperature range, use a low-ESR 2.2µF X7R ceramic capacitor at the OUTL pin. Ceramic capacitors exhibit capacitance and ESR variations over temperature. Ensure that the minimum capacitance under worst-case conditions does not drop below 1µF for linear regulator output stability.

Table 1. Output Capacitor Selection

FREQUENCY RANGE (KHZ)	MINIMUM OUTPUT CAPACITANCE (µF)
200 to 215	$\frac{20}{V_{OUT}}$
308 to 2200	$\frac{13}{V_{OUT}}$

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to GND (see Figure 2). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ (max) and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage greater than 4V above which the device is required to turn on.

Adjusting the Output Voltage

For MAX17670 and MAX17671, connect FBBUCK directly to the output node of the step-down converter. The output voltage of MAX17672 can be programmed from 0.8V to 0.9 x V_{IN}. Set the output voltage by connecting a resistor divider from output node to FBBUCK to GND (see Figure 3). Choose R2 less than or equal to 100kΩ and calculate R1 with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{0.8} - 1\right]$$

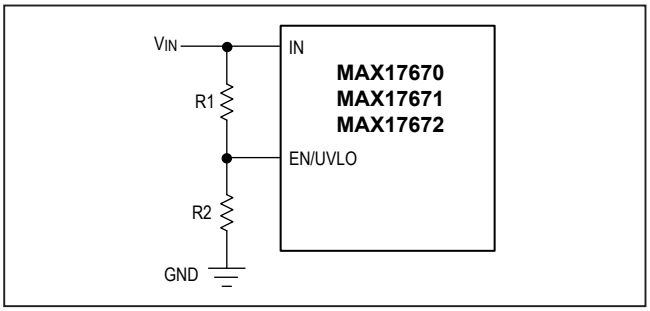


Figure 2. Adjustable EN/UVLO Network

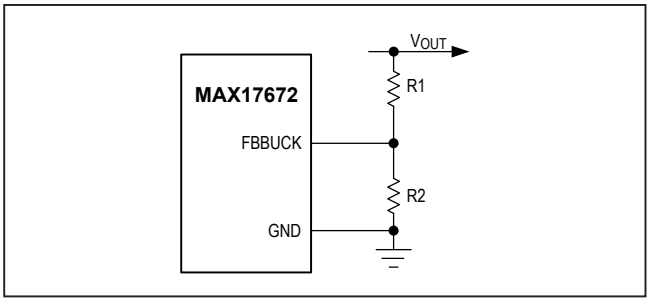


Figure 3. Setting the Output Voltage

Linear Regulator Output Voltage Options

3.3V (MAX17671 and MAX17672 only), 3.0V, 2.5V, 1.8V, 1.5V, and 1.2V linear regulator output voltage options are supported. See *Ordering Information* for details.

Power Dissipation

At a particular operating condition, the power losses that lead to the temperature rise of the device are estimated as follows:

$$P_{LOSS} = P_{BUCK} + P_{LDO}$$

$$P_{BUCK} = \left(V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{LDO} = (V_{INL} - V_{OUTL}) \times I_{OUTL}$$

where:

V_{OUT} = Step-down converter output voltage,

I_{OUT} = Step-down converter load current,

η = Efficiency of step-down converter power conversion,

V_{INL} = LDO-input voltage,

V_{OUTL} = LDO-output voltage,

I_{OUTL} = LDO load current

R_{DCR} = DC resistance of the output inductor.

See the *Typical Operating Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation. For a typical multi-layer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 41^{\circ}C/W$$

$$\theta_{JC} = 9^{\circ}C/W$$

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JC} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as

$$T_{J(MAX)} = T_{EP(MAX)} + (\theta_{JC} \times P_{LOSS})$$

Note: Junction Temperature greater than +125°C degrades operating lifetimes

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention.

The following are the guidelines for a good PCB layout:

- Place the input ceramic capacitor as close as possible to the IN and GND pins
- Minimize the area formed by the LX pin and inductor connection to reduce the radiated EMI
- Ensure that all feedback connections are short and direct
- Route the high-speed switching node (LX) away from the signal pins
- Place the linear regulator output capacitor close to the OUTL pin
- A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the device for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17670, MAX17671 and MAX17672 evaluation kit PCB layout available at **www.maximintegrated.com**.

Typical Application Circuits

MAX17671 High-Efficiency 5V Output

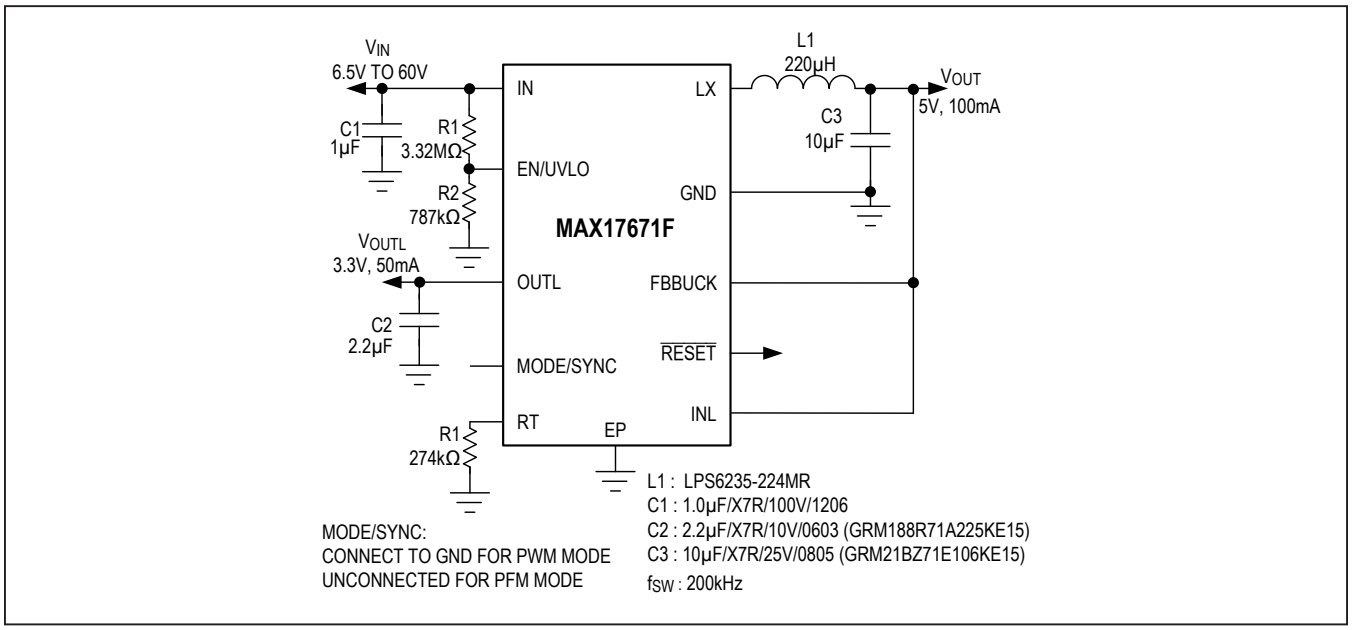


Figure 4. Fixed 5V Step-Down Converter Output at 200kHz Switching Frequency and 3.3V Linear Regulator Output

Typical Application Circuits (continued)

MAX17670 High-Efficiency 3.3V Output

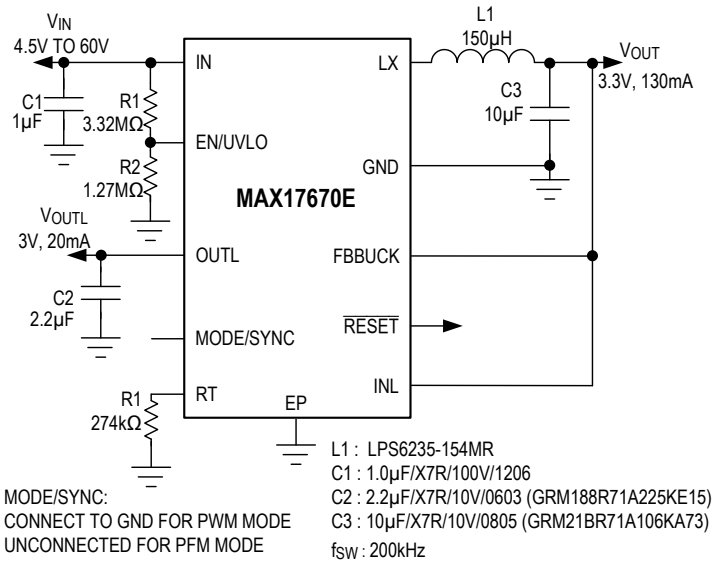


Figure 5. Fixed 3.3V Step-Down Converter Output at 200kHz Switching Frequency and 3.0V Linear Regulator Output

MAX17671 Small-Footprint 5V Output

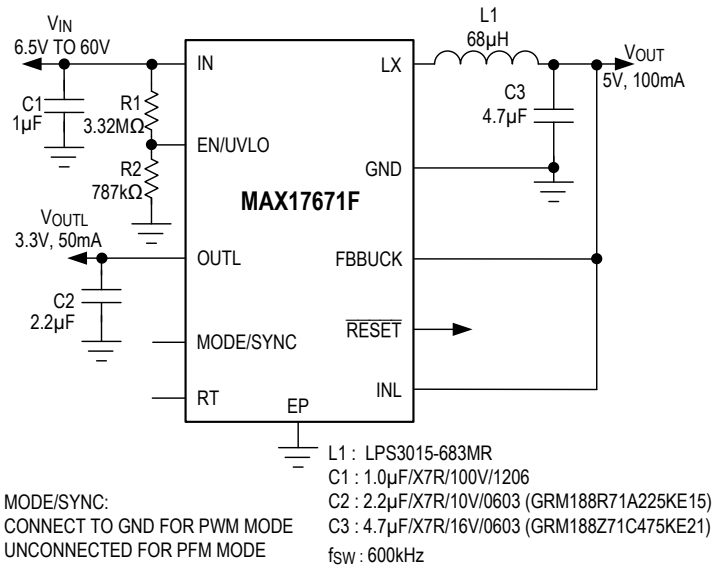


Figure 6. Fixed 5.0V Step-Down Converter Output at 600kHz Switching Frequency and 3.3V Linear Regulator Output

Typical Application Circuits (continued)

MAX17670 Small-Footprint 3.3V Output

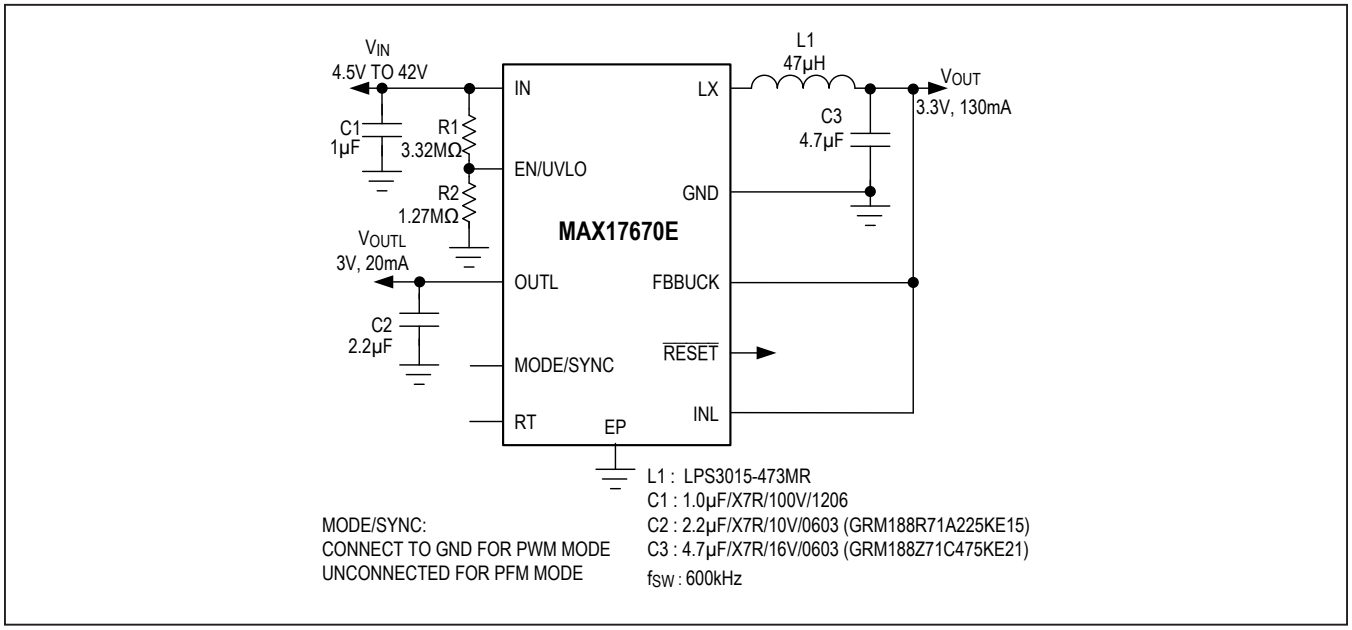


Figure 7. Fixed 3.3V Step-Down Converter Output at 600kHz Switching Frequency and 3.0V Linear Regulator Output

MAX17672 Small-Footprint 5V Output

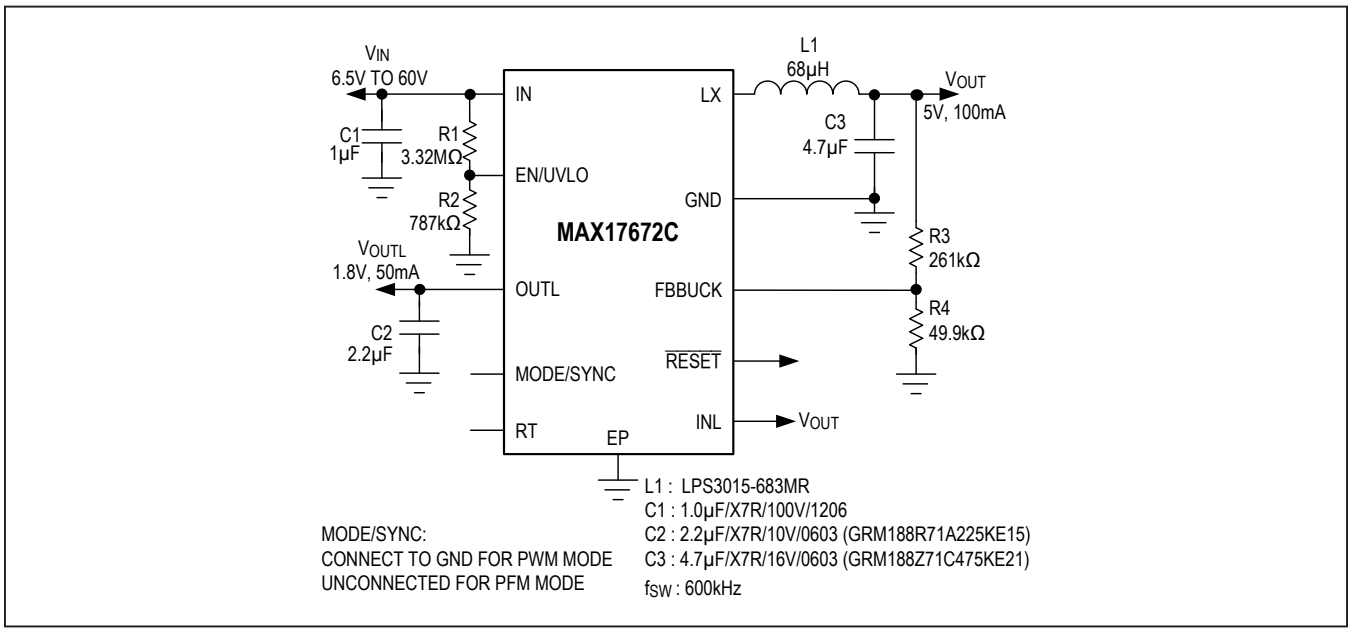


Figure 8. Adjustable 5.0V Step-Down Converter Output at 600kHz Switching Frequency and 1.8V Linear Regulator Output

Ordering Information

PART NUMBER	BUCK OUTPUT VOLTAGE (V)	LINEAR REGULATOR OUTPUT VOLTAGE (V)	PIN PACKAGE
MAX17670AATB+*	3.3	1.2	10-Pin TDFN
MAX17670BATB+*	3.3	1.5	10-Pin TDFN
MAX17670CATB+*	3.3	1.8	10-Pin TDFN
MAX17670DATB+*	3.3	2.5	10-Pin TDFN
MAX17670EATB+	3.3	3.0	10-Pin TDFN
MAX17670EATB+T	3.3	3.0	10-Pin TDFN
MAX17671AATB+*	5	1.2	10-Pin TDFN
MAX17671BATB+*	5	1.5	10-Pin TDFN
MAX17671CATB+*	5	1.8	10-Pin TDFN
MAX17671DATB+*	5	2.5	10-Pin TDFN
MAX17671EATB+*	5	3.0	10-Pin TDFN
MAX17671FATB+	5	3.3	10-Pin TDFN
MAX17671FATB+T	5	3.3	10-Pin TDFN
MAX17672AATB+*	Adjustable	1.2	10-Pin TDFN
MAX17672BATB+*	Adjustable	1.5	10-Pin TDFN
MAX17672CATB+	Adjustable	1.8	10-Pin TDFN
MAX17672CATB+T	Adjustable	1.8	10-Pin TDFN
MAX17672DATB+*	Adjustable	2.5	10-Pin TDFN
MAX17672EATB+*	Adjustable	3.0	10-Pin TDFN
MAX17672FATB+	Adjustable	3.3	10-Pin TDFN
MAX17672FATB+T	Adjustable	3.3	10-Pin TDFN

**Future product—contact factory for availability.*
+Denotes a lead(Pb)-free/RoHS compliant package.
T=Tape-and-reel.