19-2198; Rev 0; 10/01

EVALUATION KIT AVAILABLE

3A, 1MHz, Low-Voltage, Step-Down Regulators with Synchronous Rectification and Internal Switches

General Description

The MAX1830/MAX1831 constant-off-time, pulse-width-modulated (PWM) step-down DC-DC converters are ideal for use in 5V and 3.3V to low-voltage conversion necessary in notebook and subnotebook computers. These devices feature internal synchronous rectification for high efficiency and reduced component count. They require no external Schottky diode. The internal 45mΩ PMOS power switch and 55mΩ NMOS synchronous-rectifier switch easily deliver continuous load currents up to 3A. The MAX1830 produces preset +2.5V, +1.8V, or +1.5V output voltage or an adjustable output from +1.1V to V_{IN}. The MAX1831 produces preset +3.3V, +2.5V, and +1.5V output voltages and an adjustable output from +1.1V to V_{IN}. They achieve efficiencies as high as 94%.

The MAX1830/MAX1831 use a unique current-mode, constant-off-time, PWM control scheme, which includes Idle Mode™ to maintain high efficiency during light-load operation. The programmable constant-off-time architecture sets switching frequencies up to 1MHz, allowing the user to optimize performance trade-offs between efficiency, output switching noise, component size, and cost. Both devices are designed for continuous output currents up to 3A, an internal digital soft-start to limit surge currents during startup, a 100% duty cycle mode for low-dropout operation, and a low-power shutdown mode that disconnects the input from the output and reduces supply current below 1µA.The MAX1830/MAX1831 are available in 16-pin QSOP packages.

For similar devices that provide continuous output currents of 1A to 3A, refer to the MAX1644, MAX1623, and MAX1742/MAX1842/MAX1843 data sheets.

Applications

5V or 3.3V to Low-Voltage Conversion

CPU I/O Supplies

Chipset Supplies

Notebook and Subnotebook Computers

Pin Configuration appears at end of data sheet.

Idle Mode is a trademark of Maxim Integrated Products, Inc.

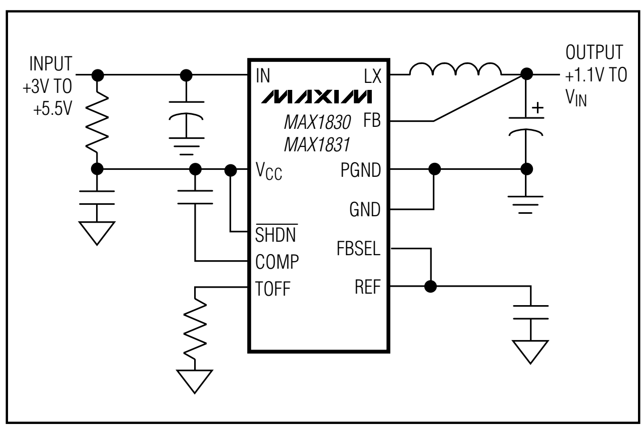
Features

- ♦ ±1.5% Output Accuracy
- ♦ 94% Efficiency
- ♦ Internal PMOS/NMOS Switches
  - 45mΩ/55mΩ On-Resistance at V_{IN} = +4.5V
  - 50mΩ/55mΩ On-Resistance at V_{IN} = +3V
- ♦ Output Voltages
  - +3.3V, +2.5V, or +1.5V Pin Selectable (MAX1831)
  - +2.5V, +1.8V, or +1.5V Pin Selectable (MAX1830)
  - +1.1V to V_{IN} Adjustable (Both Devices)
- ♦ +3V to +5.5V Input Voltage Range
- ♦ 750µA (max) Operating Supply Current
- ♦ <1µA Shutdown Supply Current
- ♦ Programmable Constant-Off-Time Operation
- ♦ Up to 1MHz Switching Frequency
- ♦ Idle Mode Operation at Light Loads
- ♦ Thermal Shutdown
- ♦ Internal Digital Soft-Start Inrush Current Limiting
- ♦ 100% Duty Cycle During Low-Dropout Operation
- ♦ Output Short-Circuit Protection
- ♦ 16-Pin QSOP Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1830EEE	-40°C to +85°C	16 QSOP
MAX1831EEE	-40°C to +85°C	16 QSOP

Typical Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN, $\overline{SHDN}$ to GND ....-0.3V to +6V
IN to V_{CC} ....±0.3V
GND to PGND ....±0.3V
COMP, FB, TOFF, FBSEL, REF to GND .....-0.3V to (V_{CC} + 0.3V)
LX Current (Note 1) 5.1A
REF Short Circuit to GND Duration ....Continuous
ESD Protection ....±2kV

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 14mW/°C above +70°C; part mounted on 1in^2 of 1oz copper) 1.12W
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) .... +300°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias the diode should take care not to exceed the IC's package power dissipation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Preset Output Voltage	V_{OUT}	V_{IN} = +3V to +5.5V, I_{LOAD} = 0 to 3A, V_{FB} = V_{OUT}	FBSEL = V_{CC}	2.487	2.525	2.563	V
			FBSEL = unconnected	1.492	1.515	1.538	
			FBSEL = REF (MAX1830)	1.791	1.818	1.845	
			FBSEL = GND	1.084	1.100	1.117	
		V_{IN} = +3.7V to +5.5V, I_{LOAD} = 0 to 3A, V_{FB} = V_{OUT}	FBSEL = REF (MAX1831)	3.283	3.333	3.383	
Adjustable Output Voltage Range		V_{CC} = V_{IN} = +3V to +5.5V, I_{LOAD} = 0, FBSEL = GND		V_{REF}		V_{IN}	V
AC Load Regulation Error					2		%
DC Load Regulation Error					0.4		%
Dropout Voltage	V_{DO}	V_{CC} = V_{IN} = +3V, I_{LOAD} = 3A			150	330	mV
Reference Voltage	V_{REF}			1.089	1.100	1.111	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -1µA to +10µA			0.5	2	mV
Current-Limit Threshold	I_{LIMIT}			4.0	4.8	5.4	A
Maximum Output RMS Current	$I_{OUT(RMS)}$	(Note 4)				3.4	A
Idle Mode Current Threshold	I_{IM}			0.2	0.6	1.0	A
PMOS Switch On-Resistance	$R_{ON, P}$	I_{LX} = 0.5A	V_{IN} = 4.5V		45	90	mΩ
			V_{IN} = 3V		50	110	
NMOS Switch On-Resistance	$R_{ON, N}$	I_{LX} = 0.5A	V_{IN} = 4.5V		55	95	
			V_{IN} = 3V		55	100	
Switching Frequency	f	(Note 2)				1	MHz
No-Load Supply Current	I_{IN} + I_{CC}	V_{FB} = 1.2V			325	750	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current		$\overline{SHDN}$ = GND, into V_{CC} and IN pins; LX = 0 or 3.3V		0.2	20	µA
		$\overline{SHDN}$ = GND, into IN with LX = 0		0.2	20	
		$\overline{SHDN}$ = GND, into IN with LX = 3.3V		0.1	20	
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C		165		°C
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling, hysteresis = 90mV	1.8	2.6	2.8	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V	0	70	300	nA
Off-Time	t_{OFF}	R_{TOFF} = 110kΩ	0.85	1.00	1.15	µs
		R_{TOFF} = 44kΩ	0.3	0.4	0.5	µs
		R_{TOFF} = 440kΩ	3.0	3.9	5.0	µs
Startup Off-Time				4 × t_{OFF}		µs
Minimum On-Time	t_{ON}	(Note 2)	0.40			µs
Soft-Start Time (Note 3)				3 × 256		cycles
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = 0 or V_{CC}	-0.5		0.5	µA
$\overline{SHDN}$ Logic Input Low Voltage	V_{IL}				0.8	V
$\overline{SHDN}$ Logic Input High Voltage	V_{IH}		2.0			V
FBSEL Input Current			-5		5	µA
FBSEL Logic Thresholds		FBSEL = GND			0.2	V
		FBSEL = REF	0.9		1.3	V
		FBSEL = unconnected	0.7 × V_{CC} - 0.2		0.7 × V_{CC} + 0.2	V
		FBSEL = V_{CC}	V_{CC} - 0.2		V_{CC} + 0.2	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Preset Output Voltage	V_{OUT}	V_{IN} = +3V to +5.5V, I_{LOAD} = 0 to 3A, V_{FB} = V_{OUT}	FBSEL = V_{CC}	2.475		2.575	V
			FBSEL = unconnected	1.485		1.545	
			FBSEL = REF (MAX1830)	1.782		1.854	
			FBSEL = GND	1.078		1.122	
		V_{IN} = +3.7V to +5.5V, I_{LOAD} = 0 to 3A, V_{FB} = V_{OUT}	FBSEL = REF (MAX1831)	3.267		3.399	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

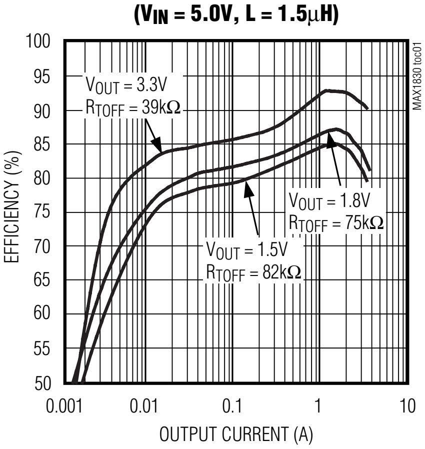
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Adjustable Output Voltage Range		V_{CC} = V_{IN} = +3V to +5.5V, I_{LOAD} = 0, FBSEL = GND		V_{REF}		V_{IN}	V
Reference Voltage	V_{REF}			1.078		1.122	V
Current-Limit Threshold	I_{LIMIT}			3.9		5.4	A
Idle Mode Current Threshold	I_{IM}			0.14		1.0	A
PMOS Switch On-Resistance	$R_{ON, P}$	I_{LX} = 0.5A	V_{IN} = 4.5V			90	mΩ
			V_{IN} = +3V			110	
NMOS Switch On-Resistance	$R_{ON, N}$	I_{LX} = 0.5A	V_{IN} = 4.5V			95	
			V_{IN} = +3V			100	
No-Load Supply Current	I_{IN} + I_{CC}	V_{FB} = 1.2V				750	µA
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V		0		360	nA
Off-Time	t_{OFF}	R_{TOFF} = 110kΩ		0.8		1.2	µs

Note 2: Not production tested.
Note 3: Soft-start time is measured with respect to the number of cycles on LX.
Note 4: This is a metal migration limit. Maximum output current may be limited by thermal capability to a lower value than this.
Note 5: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

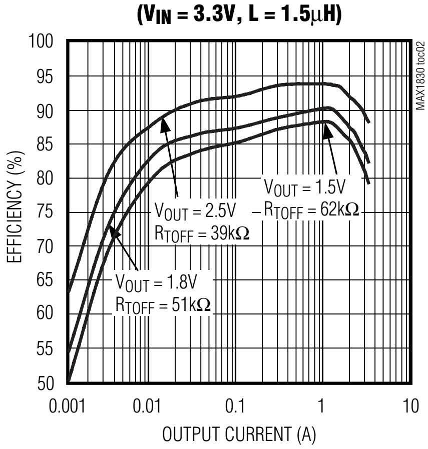
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

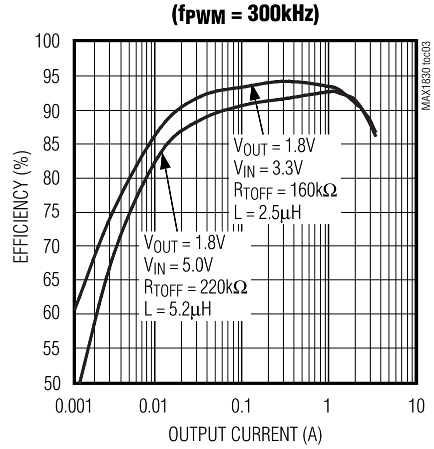
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5.0V, L = 1.5µH)



EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V, L = 1.5µH)



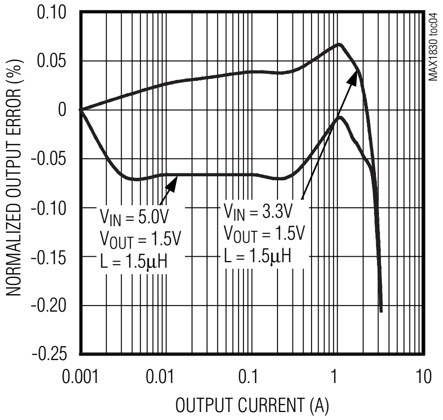
EFFICIENCY vs. OUTPUT CURRENT (f_{PWM} = 300kHz)



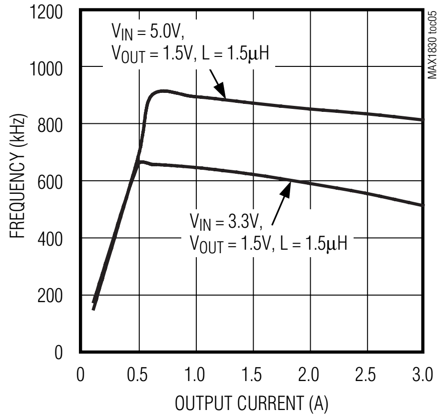
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

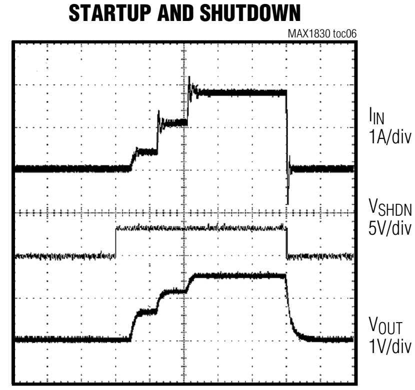
NORMALIZED OUTPUT ERROR vs. OUTPUT CURRENT



SWITCHING FREQUENCY vs. OUTPUT CURRENT

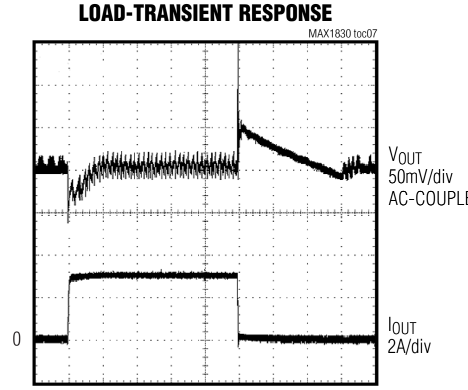


STARTUP AND SHUTDOWN



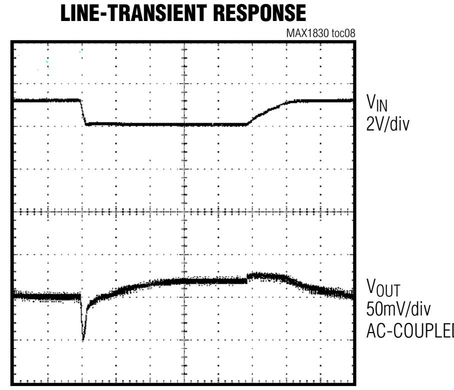
400µs/div
V_{IN} = 3.3V, V_{OUT} = 1.5V,
R_{OUT} = 0.5Ω, R_{TOFF} = 82kΩ, L = 1.5µH

LOAD-TRANSIENT RESPONSE



10µs/div
V_{IN} = 3.3V, V_{OUT} = 1.5V,
R_{TOFF} = 82kΩ, L = 1.5µH, I_{OUT} = 0.1A TO 3A

LINE-TRANSIENT RESPONSE



20µs/div
V_{OUT} = 1.8V, I_{OUT} = 1A,
R_{TOFF} = 75kΩ, L = 1.5µH

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Pin Description

PIN	NAME	FUNCTION
1, 3, 14, 16	LX	Connection for the drains of the PMOS power switch and NMOS synchronous-rectifier switch. Connect the inductor from this node to the output filter capacitor and load.
2, 4	IN	Supply Voltage Input for the internal PMOS power switch
5	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to disable the reference, control circuitry, and internal MOSFETs. Drive high or connect to V_{CC} for normal operation.
6	COMP	Integrator Compensation. Connect a capacitor from COMP to V_{CC} for integrator compensation. See *Integrator Amplifier* section.
7	TOFF	Off-Time Select Input. Sets the PMOS power switch off-time during constant-off-time operation. Connect a resistor from TOFF to GND to adjust the PMOS switch off-time.
8	FB	Feedback Input for both preset-output and adjustable-output operating modes. Connect directly to output for fixed-voltage operation or to a resistive divider for adjustable operating modes.
9	GND	Analog Ground
10	REF	Reference Output. Bypass REF to GND with a 1µF capacitor.
11	FBSEL	Feedback Select Input. Selects output voltage. See Table 3 for programming instructions.
12	V_{CC}	Analog Supply Voltage Input. Supplies internal analog circuitry. Bypass V_{CC} with a 10Ω and 2.2µF lowpass filter (Figure 1).
13, 15	PGND	Power Ground. Internally connected to the internal NMOS synchronous-rectifier switch.

Detailed Description

The MAX1830/MAX1831 synchronous, current-mode, constant-off-time, PWM DC-DC converters step down input voltages of +3V to +5.5V to preset output voltages, or to an adjustable output voltage from +1.1V to V_{IN}. The MAX1830 has preset outputs +2.5V, +1.8V, and +1.5V. The MAX1831 has preset outputs of +3.3V, +2.5V or +1.5V. Both devices deliver up to 3A of continuous output current. Internal switches composed of a 45mΩ PMOS power switch and a 55mΩ NMOS synchronous rectifier switch improve efficiency, reduce component count, and eliminate the need for an external Schottky diode.

The MAX1830/MAX1831 optimize efficiency by operating in constant-off-time mode under heavy loads and in Maxim's proprietary Idle Mode under light loads. A single resistor-programmable constant-off-time control sets switching frequencies up to 1MHz, allowing the user to optimize performance trade-offs in efficiency, switching noise, component size, and cost. Under low-dropout conditions, the device operates in a 100% duty-cycle mode, where the PMOS switch remains continuously on. Idle Mode enhances light-load efficiency by skipping cycles, thus reducing transition and gate-charge losses.

When power is drawn from a regulated supply, constant-off-time PWM architecture essentially provides constant-frequency operation. This architecture has the inherent advantage of quick response to line and load transients.

The MAX1830/MAX1831 current-mode, constant-off-time PWM architecture regulates the output voltage by changing the PMOS switch on-time relative to the constant off-time. Increasing the on-time increases the peak inductor current and the amount of energy transferred to the load per pulse.

Modes of Operation

The current through the PMOS switch determines the mode of operation: constant-off-time mode (for load currents greater than half the Idle Mode threshold), or Idle Mode (for load currents less than half the Idle Mode threshold). Current sense is achieved through a proprietary architecture that eliminates current-sensing I^2R losses.

Constant-Off-Time Mode

Constant-off-time operation occurs when the current through the PMOS switch is greater than the Idle Mode threshold current (which corresponds to a load current of half the Idle Mode threshold). In this mode, the regu-

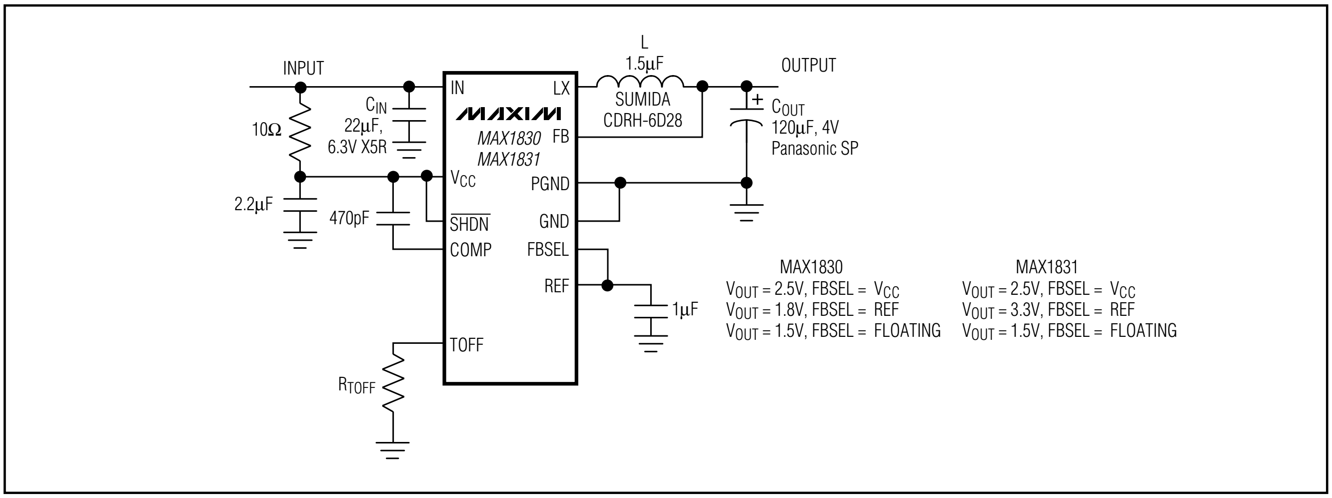

Figure 1. Typical Circuit

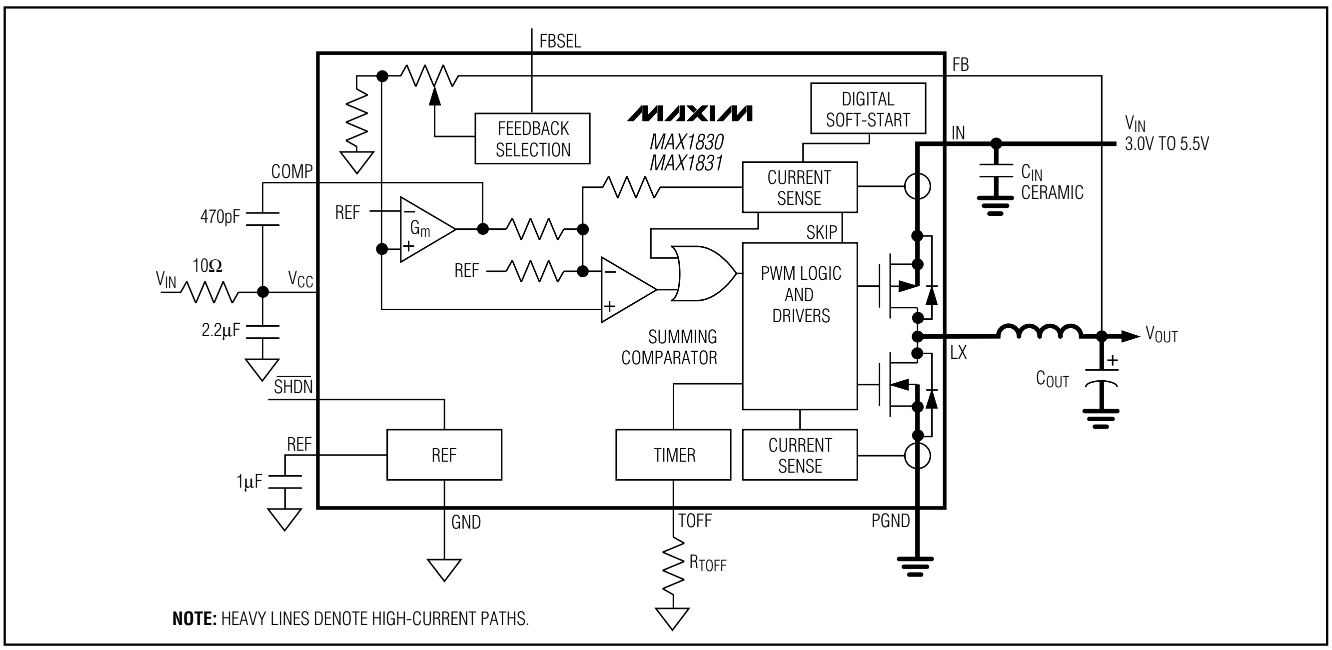

Figure 2. Functional Diagram

lation comparator turns the PMOS switch on at the end of each off-time, keeping the device in continuous-conduction mode. The PMOS switch remains on until the output is in regulation or the current limit is reached. When the PMOS switch turns off, it remains off for the programmed off-time (t_{OFF}). To control the current under short-circuit conditions, the PMOS switch remains off for approximately 4 x t_{OFF} when $V_{OUT} < V_{OUT(NOM)}$ / 4.

Idle Mode

Under light loads, the devices improve efficiency by switching to a pulse-skipping Idle Mode. Idle Mode operation occurs when the current through the PMOS switch is less than the Idle Mode threshold current. Idle Mode forces the PMOS to remain on until the current through the switch reaches the Idle Mode threshold, thus minimizing the unnecessary switching that degrades efficiency under light loads. In Idle Mode, the

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Table 1. Recommended Component Values (I_{OUT} = 3.0A)

V_{IN} (V)	V_{OUT} (V)	f_{PWM} (kHz)	L (µH)	R_{TOFF} (kΩ)
5	3.3	800	2.2	39
5	2.5	865	2.2	56
5	1.8	850	2.2	75
5	1.5	860	2.2	82
5	1.1	625	2.2	130
3.3	2.5	570	1.5	39
3.3	1.8	850	1.5	51
3.3	1.5	860	1.5	62
3.3	1.1	680	1.5	100

device operates in discontinuous conduction. Current-sense circuitry monitors the current through the NMOS synchronous switch, turning it off before the current reverses. This prevents current from being pulled from the output filter through the inductor and NMOS switch to ground. As the device switches between operating modes, no major shift in circuit behavior occurs.

100% Duty-Cycle Operation

When the input voltage drops near the output voltage, the duty cycle increases until the PMOS MOSFET is on continuously. The dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal PMOS switch and parasitic resistance in the inductor. The PMOS switch remains on continuously as long as the current limit is not reached.

Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the current-limit level at startup to reduce input-surge currents. The MAX1830/MAX1831 contain internal digital soft-start circuits, controlled by a counter, a digital-to-analog converter (DAC), and the current-limit comparator. At power-on or in shutdown mode, the soft-start counter is reset to zero. When the MAX1830/MAX1831 are enabled or powered up, its counter starts counting LX switching cycles, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC ramps up the internal current limit in four 25% steps, as the count increases to 256 cycles. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on nominal switching frequency, output capacitance, and the load current, and is typically 1ms.

Shutdown

Drive $\overline{SHDN}$ to a logic-level low to place the MAX1830/MAX1831 in low-power shutdown mode and reduce supply current to less than 1µA. In shutdown, all circuitry and internal MOSFETs turn off, and the LX node becomes high impedance. Drive $\overline{SHDN}$ to a logic-level high or connect to V_{CC} for normal operation.

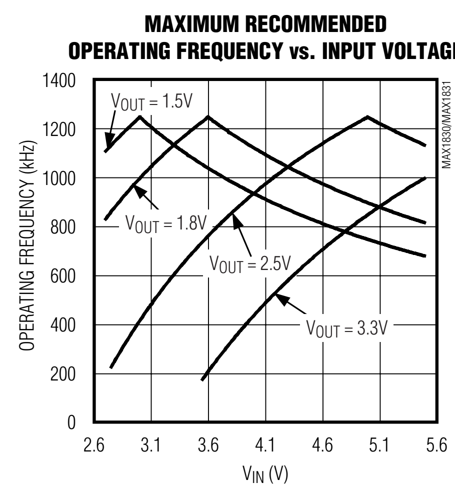


Figure 3. Maximum Recommended Operating Frequency vs. Input Voltage

Summing Comparator

Three signals are added together at the input of the summing comparator (Figure 2): an output-voltage error signal relative to the reference voltage, an integrated output-voltage error correction signal, and the sensed PMOS switch current. The integrated error signal is provided by a transconductance amplifier with an external capacitor at COMP. This integrator provides high DC accuracy without the need for a high-gain amplifier. Connecting a capacitor at COMP modifies the overall loop response (see *Integrator Amplifier*).

Table 2. Output Voltage Programming

PIN		OUTPUT VOLTAGE (V)	
FBSEL	**FB**	**MAX1830**	**MAX1831**
V_{CC}	Output voltage	2.5	2.5
Unconnected	Output voltage	1.5	1.5
REF	Output voltage	1.8	3.3
GND	Resistive divider	Adjustable	

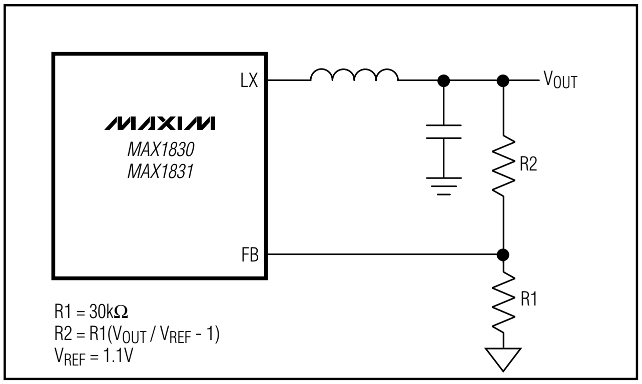


Figure 4. Adjustable Output Voltage

Synchronous Rectification

In a step-down regulator without synchronous rectification, an external Schottky diode provides a path for current to flow when the inductor is discharging. Replacing the Schottky diode with a low-resistance NMOS synchronous switch reduces conduction losses and improves efficiency.

The NMOS synchronous-rectifier switch turns on following a short delay after the PMOS power switch turns off, thus preventing cross conduction or "shoot through." In constant-off-time mode, the synchronous-rectifier switch turns off just prior to the PMOS power switch turning on. While both switches are off, inductor current flows through the internal-body diode of the NMOS switch. The internal-body diode's forward voltage is relatively high. An external Schottky diode from PGND to LX can improve efficiency.

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area immediately surrounding the IC leads. The MAX1830/MAX1831 evaluation kit has 0.7in^2 of copper area and a thermal resistance of +71°C/W with no forced airflow. Airflow over the board significantly reduces the junction-to-ambient thermal resistance. For heatsinking purposes, evenly distribute the copper area connected at the IC among the high-current pins.

Power Dissipation

Power dissipation in the MAX1830/MAX1831 is dominated by conduction losses in the two internal power switches. Power dissipation due to supply current in the control section and average current used to charge and discharge the gate capacitance of the internal switches (i.e., switching losses) is approximately:

$$P_{DS} = C \times V_{IN}^2 \times f_{PWM}$$

where C = 5nF and f_{PWM} is the switching frequency in PWM mode.

This number is reduced when the switching frequency decreases as the part enters Idle Mode. Combined conduction losses in the two power switches are approximated by:

$$P_D = I_{OUT}^2 \times R_{PMOS}$$

where R_{PMOS} is the on-resistance of the PMOS switch.

The junction-to-ambient thermal resistance required to dissipate this amount of power is calculated by:

$$\theta_{JA} = (T_{J,MAX} - T_{A,MAX}) / P_{D(TOT)}$$

where:

θ_{JA} = junction-to-ambient thermal resistance

$T_{J,MAX}$ = maximum junction temperature

$T_{A,MAX}$ = maximum ambient temperature

$P_{D(TOT)}$ = total losses

Design Procedure

For typical applications, use the recommended component values in Table 1. For other applications, take the following steps:

1) Select the desired PWM-mode switching frequency; 1MHz is a good starting point. See Figure 3 for maximum operating frequency.
2) Select the constant off-time as a function of input voltage, output voltage, and switching frequency.
3) Select R_{TOFF} as a function of off-time.
4) Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

Setting the Output Voltage

The output of the MAX1830/MAX1831 is selectable between one of three preset output voltages. For a preset output voltage, connect FB to the output voltage and connect FBSEL as indicated in Table 2. For an adjustable output voltage, connect FBSEL to GND and connect FB to a resistive divider between the output voltage and ground (Figure 4). Regulation is maintained for adjustable output voltages when $V_{FB} = V_{REF}$. Use 30kΩ for R1. R2 is given by the equation:

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} is typically 1.1V.

Programming the Switching Frequency and Off-Time

The MAX1830/MAX1831 feature a programmable PWM mode-switching frequency, which is set by the input and output voltage and the value of R_{TOFF}, connected from TOFF to GND. R_{TOFF} sets the PMOS power switch off-time in PWM mode. Use the following equation to select the off-time according to your desired switching frequency in PWM mode:

$$t_{OFF} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{f_{PWM}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

where:

t_{OFF} = the programmed off-time

V_{IN} = the input voltage

V_{OUT} = the output voltage

V_{PMOS} = the voltage drop across the internal PMOS power switch

V_{NMOS} = the voltage drop across the internal NMOS synchronous-rectifier switch

f_{PWM} = switching frequency in PWM mode

Select R_{TOFF} according to the formula:

$$R_{TOFF} = (t_{OFF} - 0.07\mu s)(110k\Omega / 1.00\mu s)$$

Recommended values for R_{TOFF} range from 36kΩ to 430kΩ for off-times of 0.4µs to 4µs.

Inductor Selection

The key inductor parameters must be specified: inductor value (L) and peak current (I_{PEAK}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC current (ripple current) to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple-current to load-current ratio (LIR = 0.25), which corresponds to a peak-inductor current 1.125 times the DC load current:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{OUT} \times LIR}$$

where:

I_{OUT} = maximum DC load current

LIR = ratio of peak-to-peak AC inductor current to DC load current, typically 0.25

The peak-inductor current at full load is 1.125 x I_{OUT} if the above equation is used; otherwise, the peak current is calculated by:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT} \times t_{OFF}}{2 \times L}$$

Choose an inductor with a saturation current at least as high as the peak-inductor current. The inductor you select should exhibit low losses at your chosen operating frequency.

Capacitor Selection

The input-filter capacitor reduces peak currents and noise at the voltage source. Use a low-ESR and low-ESL capacitor located no further than 5mm from IN. Select the input capacitor according to the RMS input ripple-current requirements and voltage rating:

$$I_{RIPPLE} = I_{LOAD}\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} = input RMS current ripple.

The output-filter capacitor affects the output-voltage ripple, output load-transient response, and feedback-loop stability. For stable operation, the MAX1830/MAX1831 require a minimum output ripple voltage of $V_{RIPPLE} \geq 1\% \times V_{OUT}$.

The minimum ESR of the output capacitor should be:

$$ESR > 1\% \times \frac{L}{t_{OFF}}$$

Stable operation requires the correct output-filter capacitor. When choosing the output capacitor, ensure that:

$$C_{OUT} \geq \frac{t_{OFF}}{V_{OUT}} 79\mu FV/\mu s$$

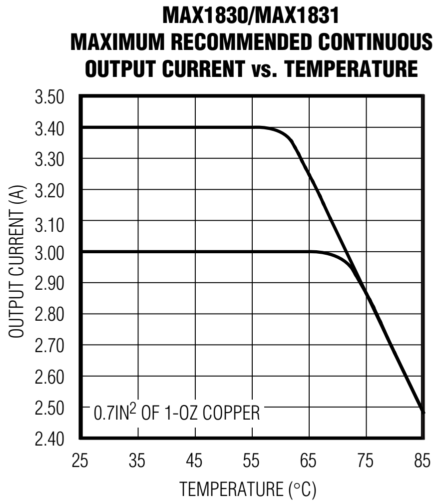


Figure 5. Maximum Recommended Continuous Output Current vs. Temperature

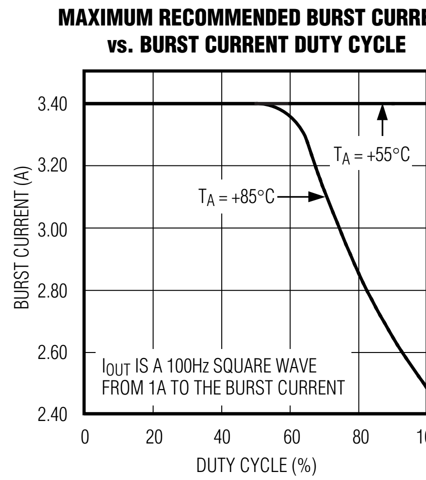


Figure 6. Maximum Recommended Burst Current vs. Burst Current Duty Cycle

Integrator Amplifier

An internal transconductance amplifier fine tunes the output DC accuracy. A capacitor, C_{COMP}, from COMP to V_{CC} compensates the transconductance amplifier. For stability, choose C_{COMP} = 470pF.

A large capacitor value maintains a constant average output voltage but slows the loop response to changes in output voltage. A small capacitor value speeds up the loop response to changes in output voltage but decreases stability.

High-Current Thermal Considerations

High ambient temperatures can limit the maximum current or duty factor of the output current, depending on the total copper, are connected to the MAX1830/ MAX1831 and available airflow.

Figure 5 shows the maximum recommended continuous output current vs. ambient temperature. Figure 6 shows the maximum recommended output current vs. the output current duty cycle at high temperatures. These figures are based on $0.7in^2$ of 1oz copper in free air.

Figure 6 assumes that the output current is a square wave with a 100Hz frequency. The duty cycle is defined as the duration of the burst current divided by the period of the square wave. This figure shows the limitations for continuous bursts of output current.

Note that if the thermal limitations of the MAX1830/ MAX1831 are exceeded, it enters thermal shutdown to prevent destructive failure.

Frequency Variation with Output Current

The operating frequency of the MAX1830/MAX1831 is determined primarily by t_{OFF} (set by R_{TOFF}), V_{IN}, and V_{OUT} as shown in the following formula:

$$f_{PWM} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{\left[t_{OFF}(V_{IN} - V_{PMOS} + V_{NMOS})\right]}$$

However, as the output current increases, the voltage drop across the NMOS and PMOS switches increases and the voltage across the inductor decreases. This causes the frequency to drop. The change in frequency can be approximated with the following formula:

$$\Delta f_{PWM} = -I_{OUT} \times R_{PMOS} / (V_{IN} \times t_{OFF})$$

where R_{PMOS} is the resistance of the internal MOSFETs (50mΩ typ).

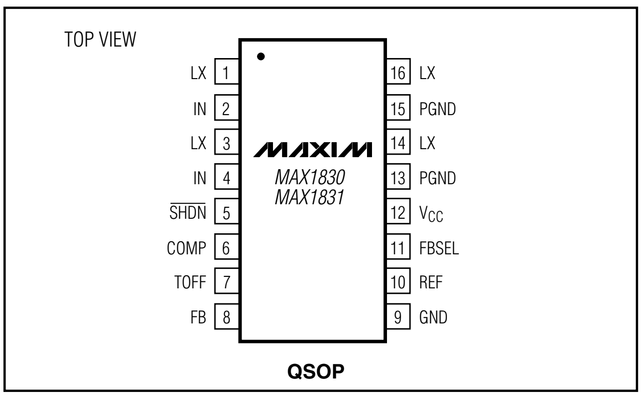
Circuit Layout and Grounding

Good layout is necessary to achieve the MAX1830/ MAX1831s' intended output power level, high efficiency, and low noise. Good layout includes the use of a ground plane, careful component placement, and correct routing of traces using appropriate trace widths.

The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND. Connect the resulting island to GND at only one point.
2) Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
3) Place the LX node components as close together and as near to the device as possible. This reduces resistive and switching losses as well as noise.
4) A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane. Avoid large AC currents through the ground plane.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3662