*Click **here** for production status of specific part numbers.*

MAX20037/MAX20038 Automotive High-Current Step-Down Converter with USB Protection/Host Charger Adapter Emulation

General Description

The MAX20037/MAX20038 ICs combine a 3.5A automotive-grade step-down converter, USB host charger adapter emulator, and USB protection switches for automotive USB host applications. The device family also includes a USB load current-sense amplifier and configurable feedback-adjustment circuit, designed to provide automatic USB voltage compensation for voltage drops in captive cables often found in automotive applications. The ICs limit the USB load current using both a fixed internal peak-current threshold of the DC-DC converter and a user-configurable external USB load current-sense amplifier threshold.

The ICs allow flexible configuration options for both stand-alone and supervised applications, and can be programmed for desired operation using both external programming resistors and/or internal I^2C registers through the I^2C bus.

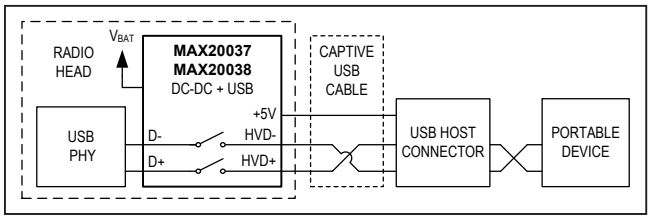
The ICs are optimized for high-frequency operation and include programmable frequency selection from 310kHz to 2.2MHz, allowing optimization of efficiency, noise, and board space based on application requirements. The fully synchronous DC-DC converters feature integrated high-side and low-side MOSFETs, an external SYNC input/output, and can be configured for spread-spectrum operation.

The MAX20037/MAX20038 are available in a small (5mm x 5mm) 28-pin TQFN package (side-wettable available) designed to minimize required components and layout area.

Applications

- Automotive Radio and Navigation
- USB Port for Host and Hub Applications
- Automotive Connectivity/Telematics
- Dedicated USB Charging Port (DCP)

Simplified Typical Operating Circuit



Benefits and Features

- One-Chip Solution Directly from Car Battery to Portable Device
  - 4.5V to 28V (40V Load Dump) Input Voltage
  - 5V, 3.5A Output Current Capability
  - Device-Attach Detection Output
  - Low-Q Current Skip and Shutdown Modes
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 275kHz to 2.2MHz Operation
  - Fixed-PWM Option at No Load
  - Spread Spectrum for EMI Reduction
  - SYNC Input/Output for Frequency Parking
- Optimal USB Power and Communication for Portable Devices
  - User-Programmable Voltage Gain Adjusts Output for Up to 600mΩ Cable Resistance
  - User-Programmable USB Current Limit
  - USB 480Mbps/12Mbps/1.5Mbps Data Switches
  - Integrated iPod®/iPhone®/iPad® and Samsung® Charge-Detection Termination Resistors
  - Supports USB BC1.2 CDP and DCP Modes
  - Supports China YD/T 1591-2009
  - Compatible with USB On-the-Go Specification
- Robust Design Keeps Vehicle System and Portable Devices Safe in Automotive Environment
  - Short-to-Battery Protection on DC-DC Converter Pins
  - Short-to-VBUS Protection on USB Pins (MAX20037)
  - Short-to-Battery Protection on USB Pins (MAX20038)
  - ±15kV Air/±8kV Contact ISO 10605*
  - ±15kV Air/±8kV Contact IEC 61000-4-2*
  - Reduced Inrush Current with Soft-Start
  - Overtemperature Protection
  - -40°C to +125°C Operating Temperature Range

**Tested in Typical Operating Circuit, as used on the MAX20037/MAX20038 Evaluation Kit.*

***Ordering Information* and *Typical Operating Circuit* appear at the end of data sheet.**

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Samsung is a registered trademark of Samsung Electronics Co., Ltd.

19-100104; Rev 8; 7/18

maxim integrated™

Absolute Maximum Ratings

SUPSW to PGND .....-0.3V to +40V
LX, HVEN to PGND (Note 1) ..... -0.3V to (V_{SUPSW} + 0.3V)
BIAS to SUPSW ..... V_{SUPSW} + 0.3V
DRV to PGND .....-0.3V to (V_{BIAS} + 0.3V)
FBCAP, SYNC to AGND.....-0.3V to (V_{BIAS} + 0.3V)
SENSN, SENSP, INT to AGND ..... -0.3V to (V_{SUPSW} + 0.3V)
AGND to PGND.....-0.3V to +0.3V
BST to PGND .....-0.3V to +46V
BST to LX .....-0.3V to +6V
IN, CONFIG1, ENBUCK, SDA, SCL, to AGND .....-0.3V to +6V
BIAS, CDP/DCP, $\overline{FAULT}$, SHIELD to AGND .....-0.3V to +6V
HVD+, HVD- to AGND (MAX20037) .....-0.3V to +6V
HVD+, HVD- to AGND (MAX20038) .....-0.3V to +18V
LX Continuous RMS Current 3.5A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-pin TQFN (derate 34.5mW/°C > 70°C) ..... 2759 mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Package Information

PACKAGE TYPE: 28 TQFN	
Package Code	T2855+6C
Outline Number	**21-0140**
Land Pattern Number	**90-0026**
PACKAGE TYPE: 28 SWTQFN	
Package Code	T2855Y+6C
Outline Number	**21-100041**
Land Pattern Number	**90-0026**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY AND ENABLE						
Supply Voltage Range	V_{SUP}	(Note 2)	4.5		28	V
Load-Dump Event Supply Voltage Range	V_{SUPSW_LD}	t < 1s, inferred by leakage test			40	V
Supply Current	I_{SUPSW}	Powered enabled no load skip mode; (Note 3)		2.3		mA
		Powered, enabled, no load FPWM mode (Note 3)		32		
		V_{SUPSW} = 18V, V_{HVEN} = 0V, V_{IN} = 0V; off state		4	20	µA
Standby Supply Current	I_{SUPSW}	V_{HVEN} = 3.3V,V_{ENBUCK} = 0, high-speed or CDP mode		1.18		mA
		V_{HVEN} = 3.3V, V_{ENBUCK} = 0, DCP mode		1.3		
BIAS Voltage	V_{BIAS}	5.75V ≤ V_{SUPSW} ≤ 28V	4.75	5	5.25	V
		In switchover mode		4.7		V
BIAS Current Limit			50		160	mA
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} rising	3.7		3.9	V
BIAS Undervoltage-Lockout Hysteresis				0.09		V
SUPSW Undervoltage Lockout	V_{UV_SUPSW}	V_{UV_SUPSW} rising	3.850		4.43	V
SUPSW Undervoltage-Lockout Hysteresis			0.15		0.25	V
IN Voltage Range	V_{IN}		3		3.6	V
IN Overvoltage Lockout	V_{IN_OVLO}	V_{IN} rising	3.8		4.3	V
IN Input Current	I_{IN}				10	µA
HVEN Rising Threshold	V_{HVEN_R}		0.6	1.5	2.4	V
HVEN Falling Threshold	V_{HVEN_F}				0.4	V
HVEN Hysteresis	V_{HVEN}			0.08		V
HVEN Debounce (Rising)	t_{HVEN_R}			6		µs
HVEN Debounce (Falling)	t_{HVEN_F}			12		µs
HVEN Input Leakage Current					10	µA

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D+, D- ANALOG USB SWITCHES						
Analog Signal Range		Guaranteed by R_{ON} measurement	0		3.6	V
Protection Trip Threshold	V_{OV_D}		3.65	3.9	4.1	V
Protection Response Time	t_{FP_D}	V_{IN} = 4.0V, $V_{HVD\pm}$ = 3.3V to 4.3V step, R_L = 15kΩ on D±, delay to $V_{D\pm}$ < 3V		3		µs
Overvoltage Blanking Timeout Period	t_{B,OV_D}	From overvoltage condition to $\overline{FAULT}$ asserted.		15.6		ms
D+, D- ANALOG USB SWITCHES (MAX20038 ONLY)						
On-Resistance Switch A	R_{ON_SA}	I_L = 10mA, $V_{D_}$ = 0 to V_{IN}, V_{IN} = 3.0V to 3.6V		4	8	Ω
On-Resistance Match Between Channels, Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D_}$ = 1.5V or 3.0V		0.03	.2	Ω
On-Resistance Flatness, Switch A	$R_{FLAT(ON)A}$	I_L = 10mA, $V_{D_}$ = 0V or 0.4V		.02		Ω
On-Resistance of HVD+/HVD- Short	R_{SHORT}	V_{D+} = 1V, I_{D-} = 500uA		90	180	Ω
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD\pm}$ = 3.6V or 0V	-7		+7	µA
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	$V_{HVD\pm}$ =18V, $V_{D\pm}$ = 0V			50	µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD\pm}$ =18V, $V_{D\pm}$ = 0V	-1		+1	µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance 50Ω		480		MHz
Crosstalk	V_{CT}	R_L = 50Ω, frequency = 480MHz		-14		dB
On-Capacitance, Switch A	C_{ON}	Frequency = 240MHz, V_{BIAS} = 250mV, Voltage = 500mV_{P-P}		15		pF
Rise-Time Propagation Delay	t_{PLH}	R_S = R_L = 50Ω		200		ps
Fall-Time Propagation Delay	t_{PHL}	R_S = R_L = 50Ω		200		ps
Output Skew Between Switches	$t_{SK(O)}$	Skew between D+ and D- switch, R_L = 50Ω		50		ps
Output Skew Same Switch	$t_{SK(P)}$	Skew between opposite transitions in same switch, R_L = 50Ω		50		ps
D+, D- ANALOG USB SWITCHES (MAX20037 ONLY)						
On-Resistance, Switch A	R_{ON_SA}	I_L = 10mA, I_L = 10mA, $V_{D_}$ = 0V to V_{IN}, V_{IN} = 3.0V to 3.6V		2.5	4	Ω
On-Resistance Match Between Channels, Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D_}$ = 1.5V or 3.0V		0.03	0.2	Ω
On-Resistance Flatness, Switch A	$R_{FLAT(ON)A}$	I_L = 10mA,$V_{D_}$ =0V or 0.4V		0.02		Ω
On-Resistance of HVD+/HVD- Short	R_{SHORT}	V_{D+} = 1V, I_{D-} = 500µA		90	180	Ω

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD±}$ = 3.6V or 0V	-7		+7	µA
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	$V_{HVD±}$ = 6V, $V_{D±}$ = 0V			10	µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD±}$ = 6V, $V_{D±}$ = 0V	-1		+1	µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance 50Ω		640		MHz
Crosstalk	V_{CT}	R_L = 50Ω, f = 480MHz		-14		dB
On-Capacitance, Switch A	C_{ON}	Frequency = 240MHz, V_{BIAS} = 250mV, voltage = 500mV_{P-P}		15		pF
Rise-Time Propagation Delay	t_{PLH}	R_S = R_L = 50Ω		200		ps
Fall-Time Propagation Delay	t_{PHL}	R_S = R_L = 50Ω		200		ps
Output Skew, Between Switches	$t_{SK(O)}$	Skew between D+ and D- switch, R_L = 50Ω		50		ps
Output Skew, Same Switch	$t_{SK(P)}$	Skew between opposite transitions in same switch, R_L = 50Ω		50		ps
CURRENT-SENSE AMPLIFIER (SENSP, SENSN)						
Feedback-Adjustment Gain		V_{ADJUST}/V_{SENSE}, GAIN[4:0] = 11110 V_{SENSP} - V_{SENSN} = 80mV		19.4		V/V
Output-Voltage Accuracy		V_{SENSP} - V_{SENSN} = 79.2mV, GAIN[4:0] = 11110, T_A = -40°C to +105°C (Note 3)	6.33		6.68	V
Overcurrent Threshold		ILIM[2:0] = 111	3.06	3.18	3.30	A
		ILIM[2:0] = 110	2.57	2.69	2.80	
		ILIM[2:0] = 101	2.06	2.14	2.23	
		ILIM[2:0] = 100	1.56	1.63	1.69	
		ILIM[2:0] = 011	1.04	1.09	1.14	
		ILIM[2:0] = 010	0.79	0.83	0.87	
		ILIM[2:0] = 001	0.54	0.57	0.60	
		ILIM[2:0] = 000	0.28	0.31	0.34	
Attach Comparator Input-Voltage Threshold			230	560	850	µV
CSA Attach Deglitch				1		ms
SENSN Discharge Threshold (Falling)	V_{SENSN_DIS}	V_{SENSN} falling	0.48	0.51	0.55	V
SENSN Discharge Current	I_{SENSN_DIS}		11		32	mA

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSN Discharge Timeout	$t_{SENSN_DIS_TIMEOUT}$			1		s
SENSN Discharge Time Upon CD1 Bit Toggle	$t_{SENSN_DIS_CD}$	CD1 bit toggle or CDP/DCP pin toggle; going in to or out of dedicated charging mode		2		s
SENSN Undervoltage Threshold (Falling)	V_{UV_SENSN}		4	4.375	4.75	V
SENSN Overvoltage Threshold (Rising)	V_{OV_SENSN}		7	7.46	7.9	V
SENSN Undervoltage-Fault Blanking Time			8	16		ms
SENSN Overvoltage-Fault Blanking Time	t_{B,OV_SENSN}	From overvoltage condition to fault notification	1	3	5	µs
REMOTE FEEDBACK ADJUSTMENT						
SHIELD Input Voltage Range			0.1		0.75	V
Gain		V_{ADJUST}/V_{SHIELD}, CSA attach = true	1.935	2	2.065	V/V
Input-Referred Offset Voltage				±2		mV
SHIELD Input-Leakage Current		0V < V_{SHIELD} < 5.5V	-10		+10	µA
SHIELD Input-Threshold (Rising)			1.23		1.45	V
SHIELD Input Threshold (Falling)			1.07		1.3	V
DIGITAL INPUTS (SDA, SCL, ENBUCK, CDP/DCP)						
Input Leakage Current		V_{PIN} = 5.5V, 0V	-5		+5	µA
Logic-High	V_{IH}		1.6			V
Logic-Low	V_{IL}				0.5	V
USB 2.0 HOST-CHARGER DETECTION (D+/D-)						
Input Logic-High	$V_{IH,HVD}$		2			V
Input Logic-Low	$V_{IL,HVD}$				0.8	V
Data-Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4 V	50	100	150	µA
Data-Detect Voltage High	V_{DAT_REFH}		0.4			V
Data-Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data-Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data-Source Voltage	V_{DAT_SRC}	I_{SOURCE} = 200µA	0.5		0.7	V

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
PWM Output Voltage	V_{SENSP}	8V < V_{SUPSW} ≤ 18V, no load		5.1		V
Skip Mode Output Voltage	V_{SENSP_SKIP}	8V < V_{SUPSW} ≤ 18V, no load, (Note 3)		5.13		V
Load Regulation		8V ≤ V_{SUPSW} ≤18V		50		mΩ
Spread-Spectrum Range		Spread spectrum enabled		6		%
SYNC Switching-Threshold High	V_{SYNC_HI}	Rising	1.4			V
SYNC Switching-Threshold Low	V_{SYNC_LO}	Falling			0.4	V
SYNC Internal Pulldown				200		kΩ
SYNC Input Clock-Acquisition Time	t_{SYNC}	(Note 3)		1		Cycles
High-Side Switch On-Resistance	R_{ONH}	I_{LX} = 1A		54	95	mΩ
Low-Side Switch On-Resistance	R_{ONL}	I_{LX} = 1A		72	135	mΩ
BST Input Current	I_{BST}	V_{BST} - V_{LX} = 5V, high side on		2.2		mA
LX Current-Limit Threshold				5		A
Skip Mode Peak-Current Threshold	I_{SKIP_TH}			1		A
Negative Current Limit				0.9		A
Soft-Start Ramp Time	t_{SS}			8		ms
LX Rise Time		(Note 3)		3		ns
LX Fall Time		(Note 3)		4		ns
OSCILLATOR						
Internal Oscillator Frequency			3.4	4	4.6	MHz
Buck Oscillator Frequency	f_{SW}	FSW[2:0] = 000	1.94	2.2	2.46	MHz
		FSW[2:0] = 101	340	410	480	kHz
Hold Timer			51	60	69	min
ADC						
Resolution				8		bits
Offset Error				±0.4		%FS
Gain Error				±0.3		%FS

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FAULT}$, INT(ATTACH), SYNC OUTPUTS						
Output High-Leakage Current		$V_{\overline{FAULT}}$, $V_{\overline{INT(ATTACH)}}$ = 5.5V	-10		+10	µA
Output Low Level		Sinking 1mA			0.4	V
SYNC Output High Level		Sourcing 1mA, SYNC configured as output	V_{BIAS} - 0.4			V
CONFIG1, CONFIG2, CONFIG3						
CONFIG1–3 Current Leakage		$V_{CONFIG_}$ = 0 to 4V			±5	µA
Minimum Window Amplitude			-3.4		+3.4	%
THERMAL OVERLOAD						
Thermal-Warning Temperature				145		°C
Thermal-Warning Hysteresis				9		°C
Thermal-Shutdown Temperature				165		°C
Thermal-Shutdown Hysteresis				9		°C
I²C INTERFACE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time	t_{BUF}	Between STOP and START condition	1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0		0.6	µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV

Electrical Characteristics (continued)

(V_{SUPSW} = V_{HVEN} = 14V, V_{IN} = V_{ENBUCK} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVD+, HVD- ESD PROTECTION (MAX20037 ONLY—REQUIRES EXTERNAL TVS)						
ESD Protection Level (Note 4)	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		
		IEC 61000-4-2 Air Gap (330pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (330pF, 330Ω)		±8		
HVD+, HVD- ESD PROTECTION (MAX20038 ONLY)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		
		IEC 61000-4-2 Air Gap (330pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (330pF, 330Ω)		±8		

Note 2: Device is designed for use in applications with continuous operation of 14V. Device meets electrical table up to maximum supply voltage.

Note 3: Guaranteed by design and bench characterization; not production tested.

Note 4: Tested in Typical Application Circuit, as shown on the MAX20037 EV kit that utilizes an external ESD array.

Note 5: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Timing Diagrams

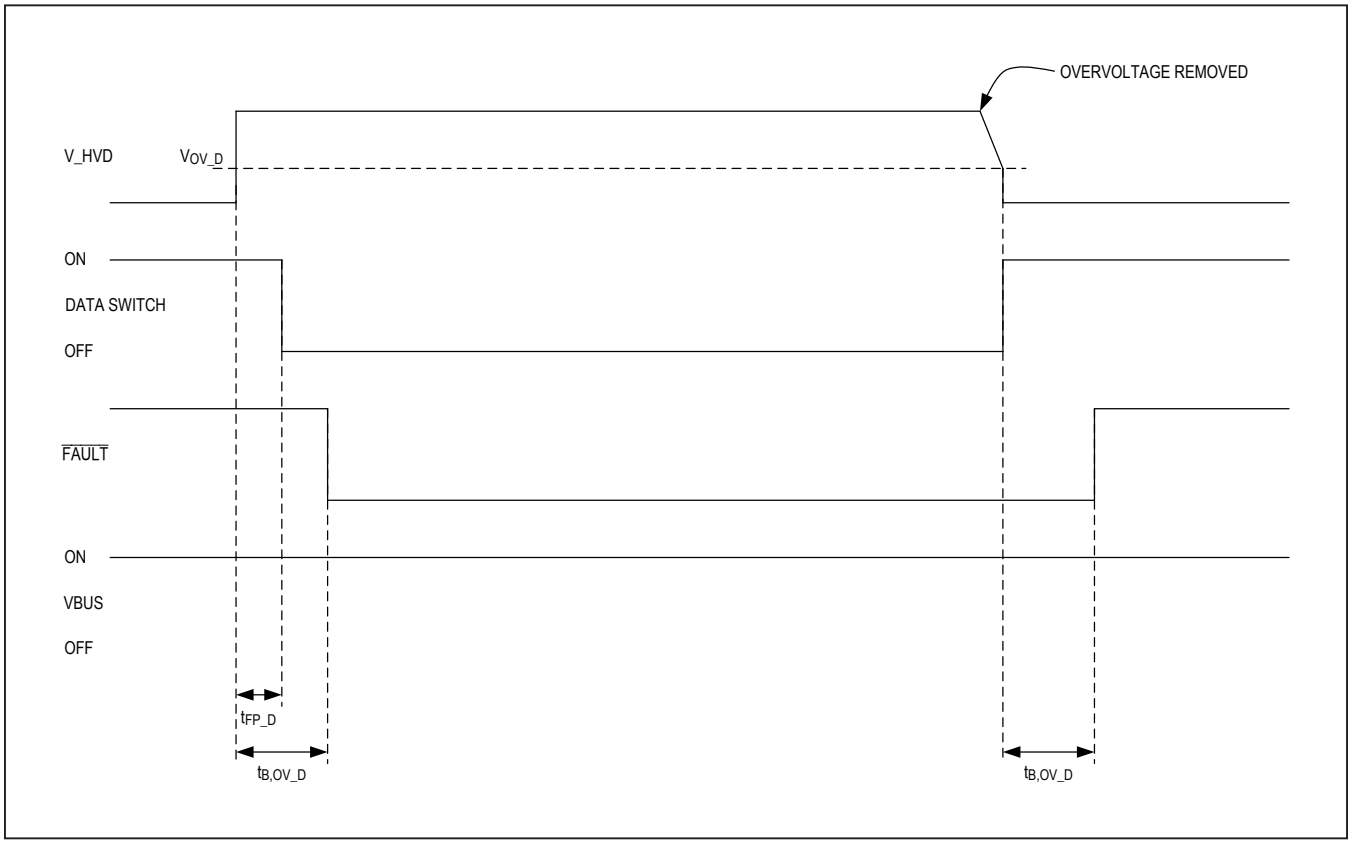


Figure 1. Overvoltage Detection on HVD+, HVD- Timing Diagram

Timing Diagrams (continued)

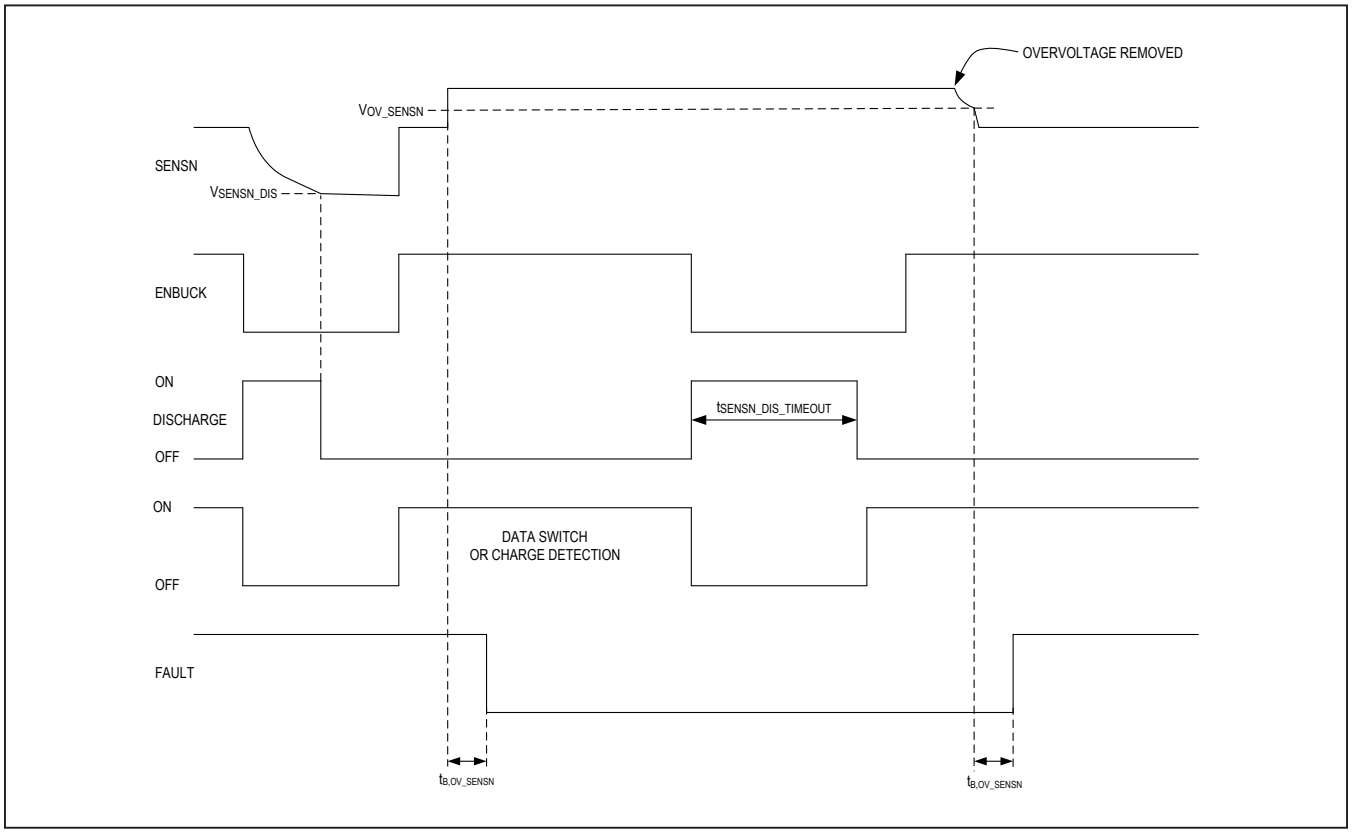


Figure 2. SENSN Discharge and Overvoltage Timing Diagram

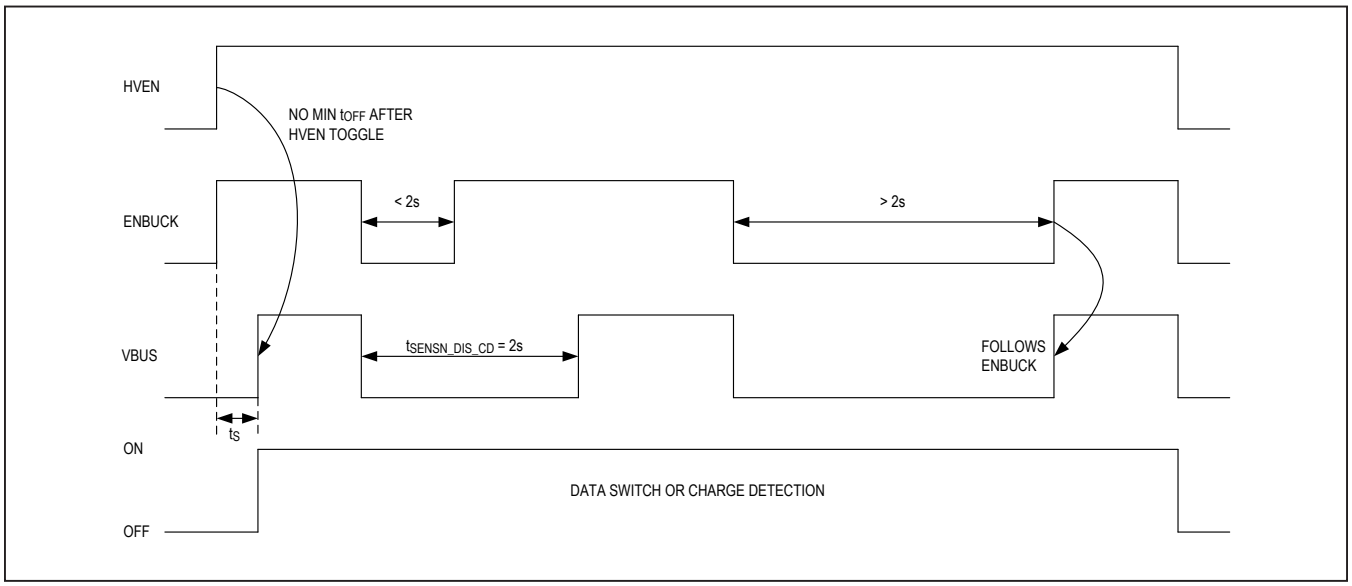


Figure 3a. ENBUCK Reset Behavior and Timing Diagram

Timing Diagrams (continued)

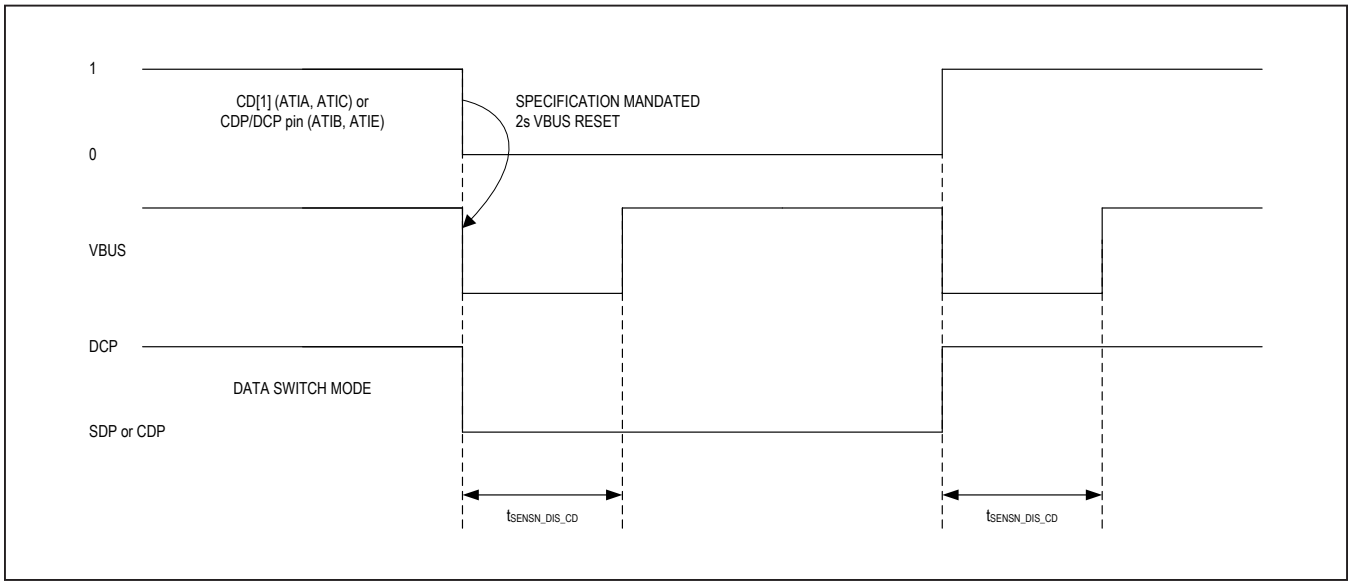


Figure 3b. DCP Reset Behavior and Timing Diagram

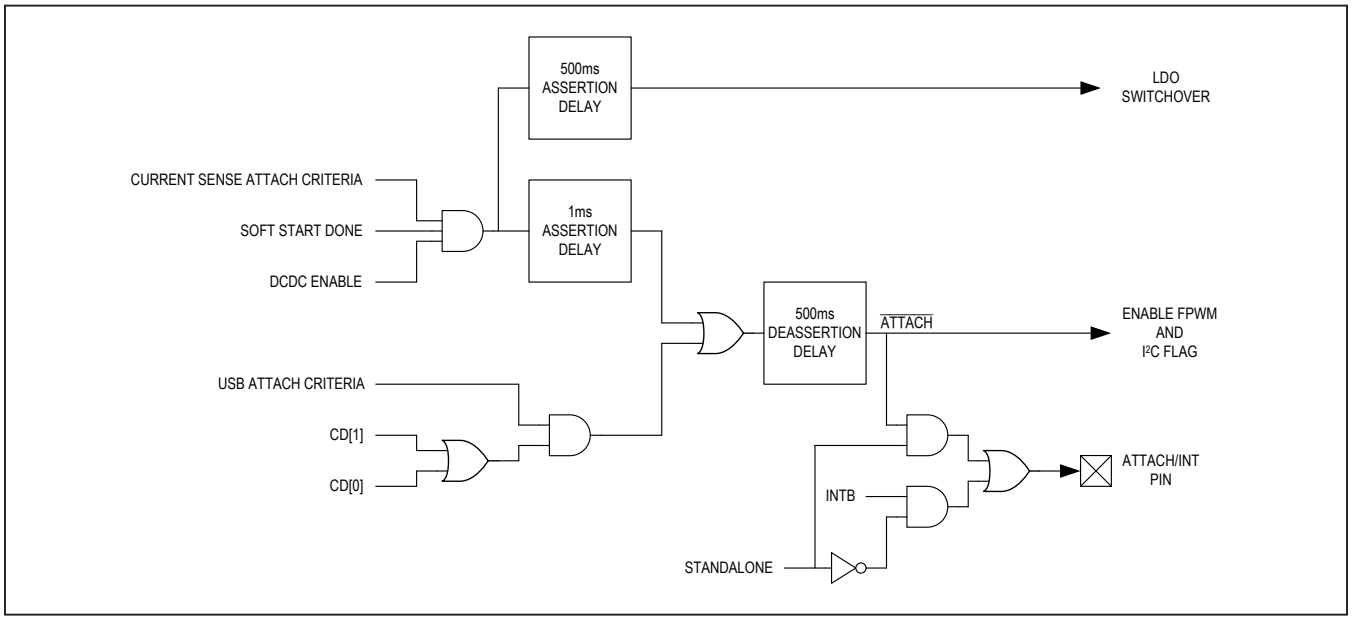


Figure 4. $\overline{ATTACH}$ Logic Diagram

Timing Diagrams (continued)

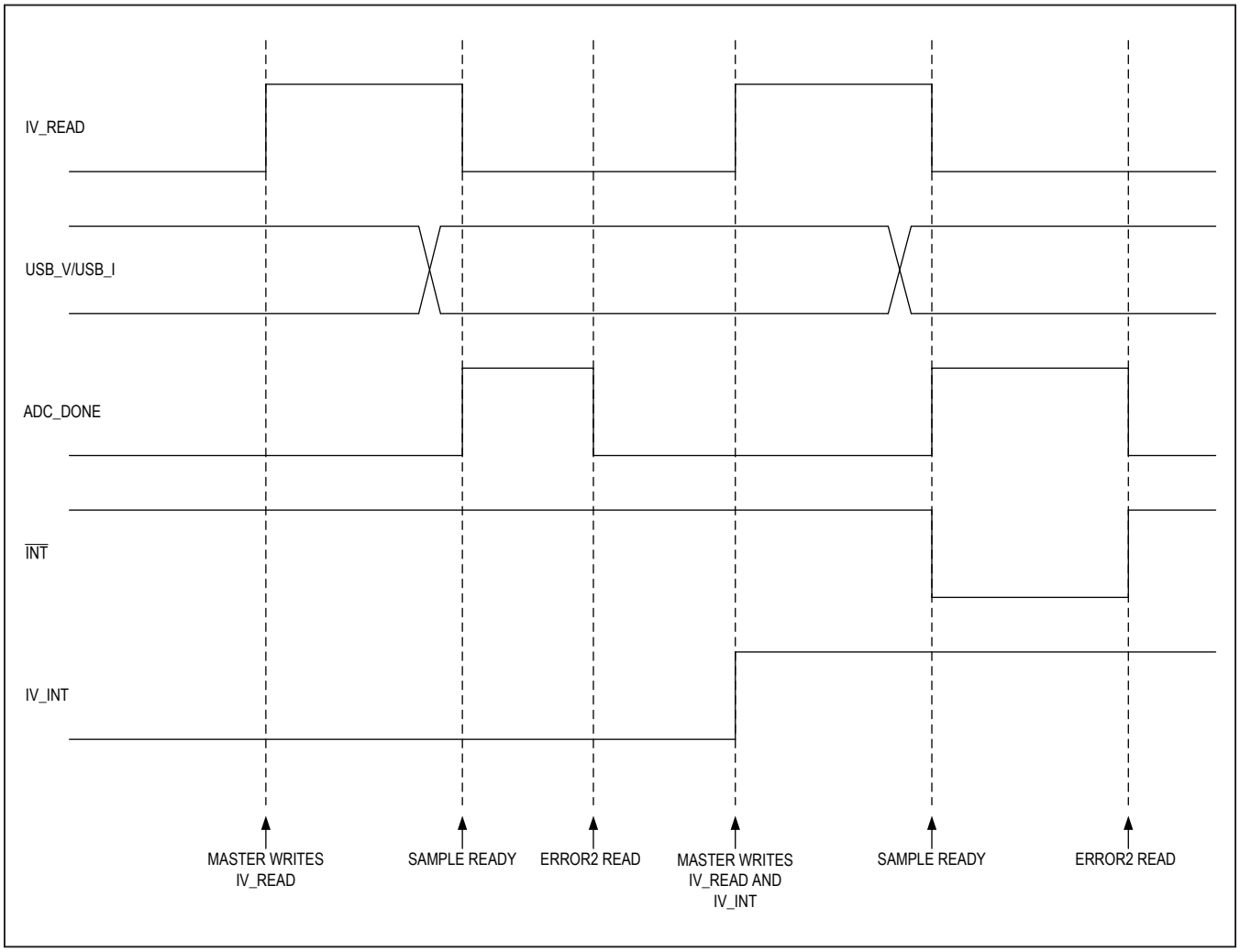


Figure 5. ADC Timing Diagram

Timing Diagrams (continued)

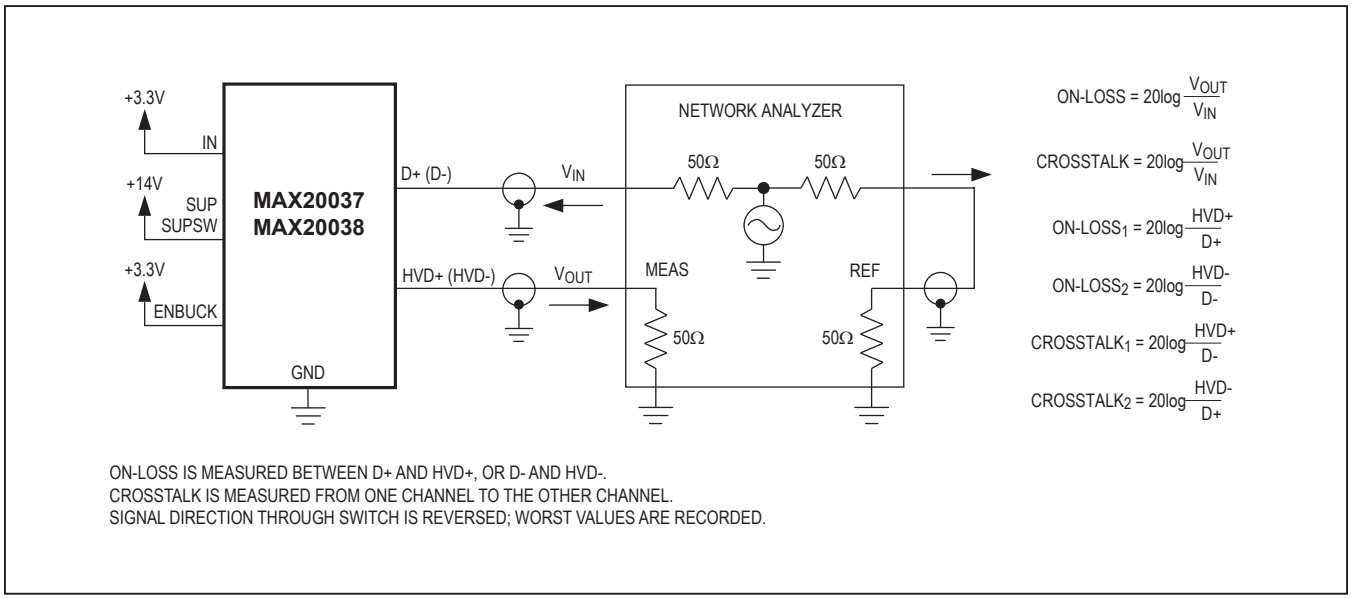


Figure 6. On-Channel -3dB Bandwidth and Crosswalk

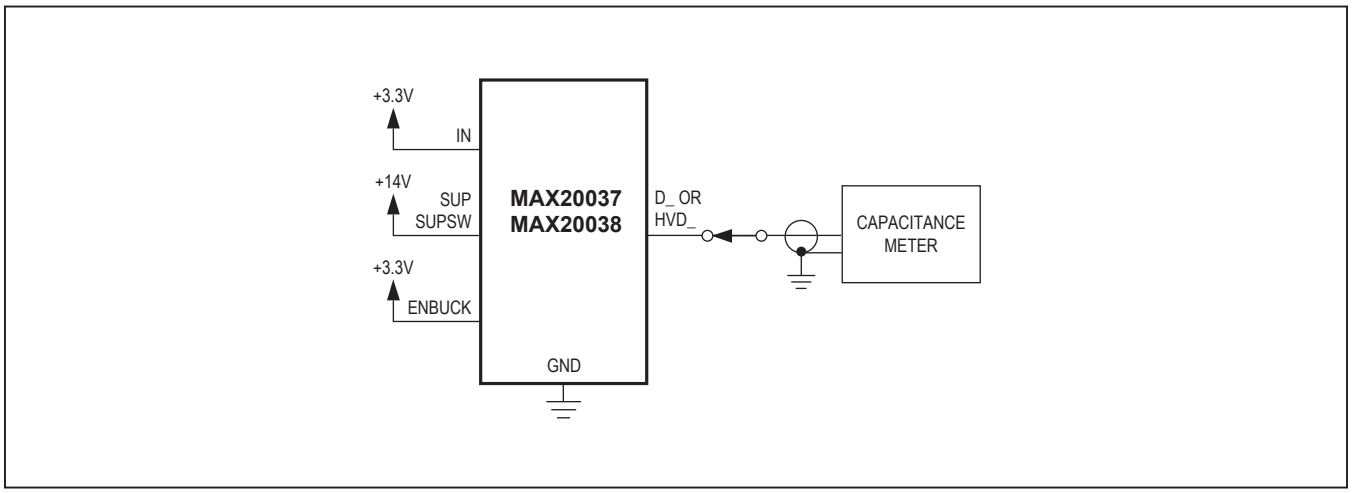
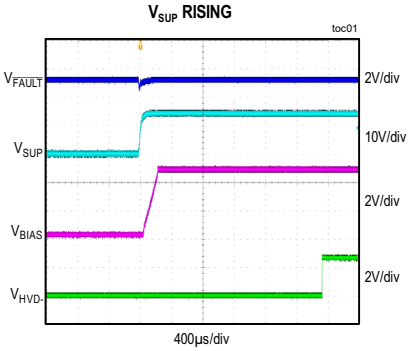


Figure 7. On-Capacitance

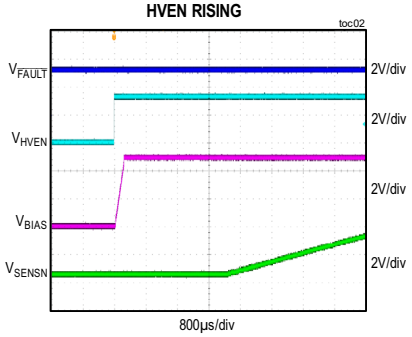
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

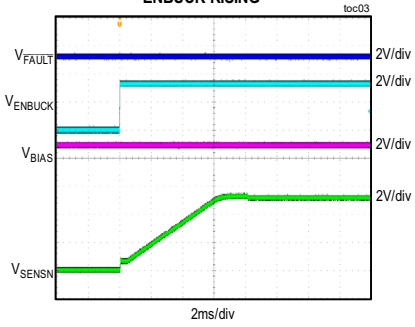
STARTUP
V_{SUP} RISING



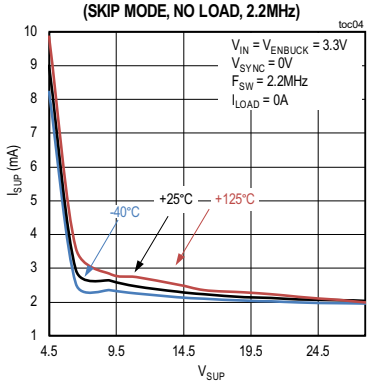
STARTUP
HVEN RISING



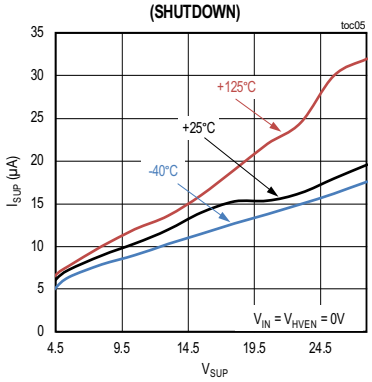
STARTUP
ENBUCK RISING



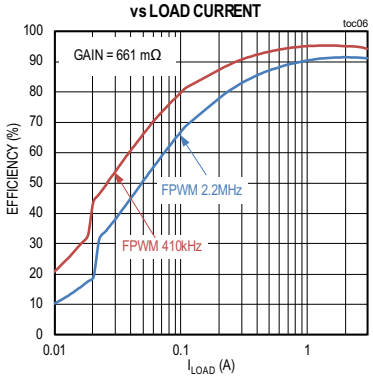
SUPPLY CURRENT vs VOLTAGE
(SKIP MODE, NO LOAD, 2.2MHz)



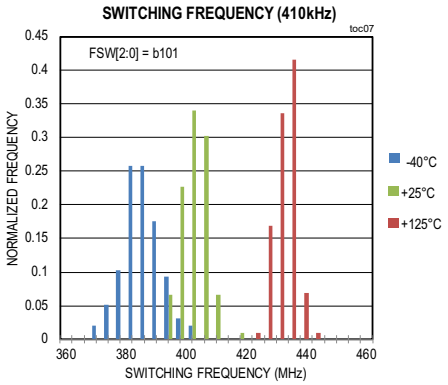
SUPPLY CURRENT vs VOLTAGE
(SHUTDOWN)



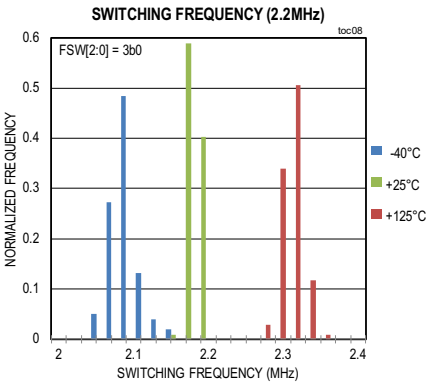
EFFICIENCY
vs LOAD CURRENT



SWITCHING FREQUENCY (410kHz)



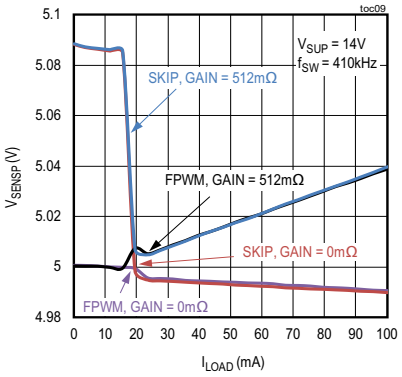
SWITCHING FREQUENCY (2.2MHz)



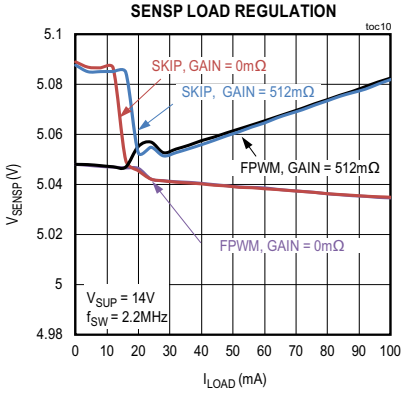
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

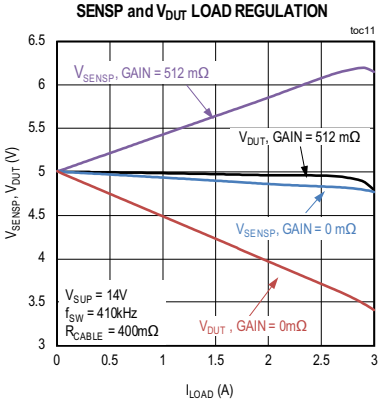
SENSP LOAD REGULATION



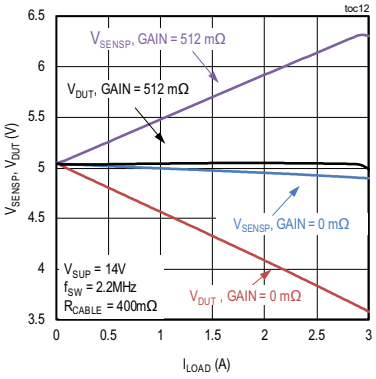
SENSP LOAD REGULATION



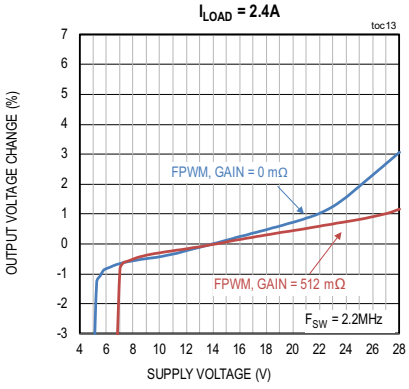
SENSP and V_{DUT} LOAD REGULATION



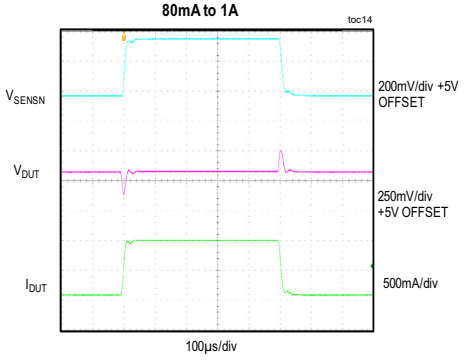
SENSP and V_{DUT} LOAD REGULATION



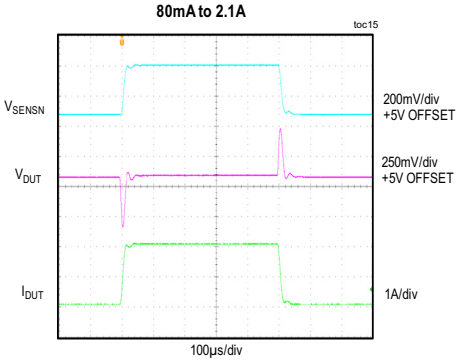
LINE REGULATION
I_{LOAD} = 2.4A



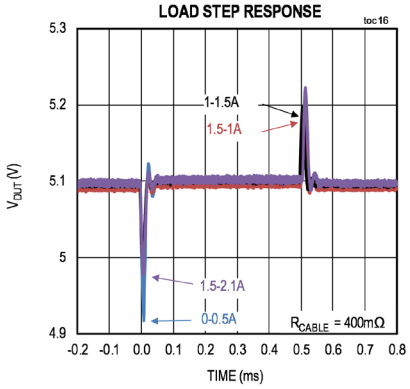
LOAD STEP RESPONSE
80mA to 1A



LOAD STEP RESPONSE
80mA to 2.1A

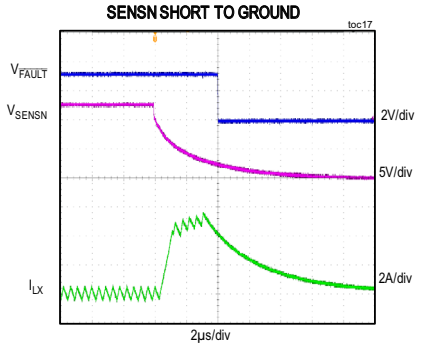


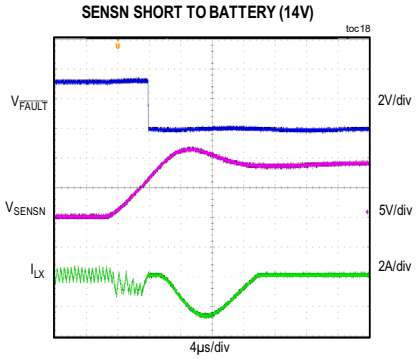
LOAD STEP RESPONSE

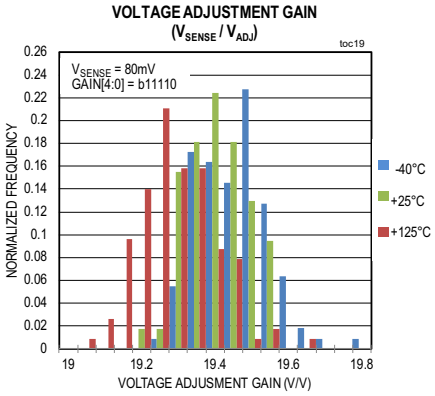


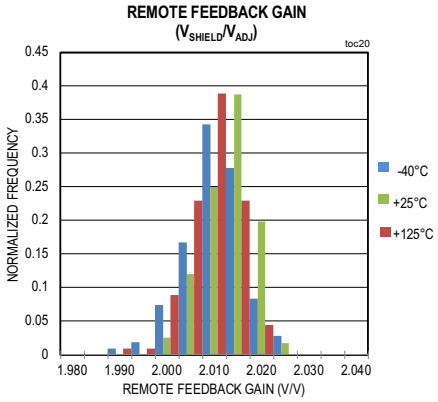
Typical Operating Characteristics (continued)

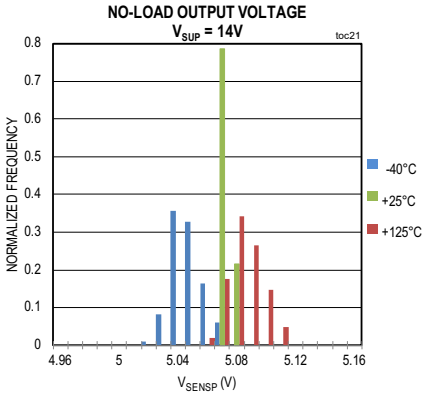
(T_A = +25°C, unless otherwise noted.)

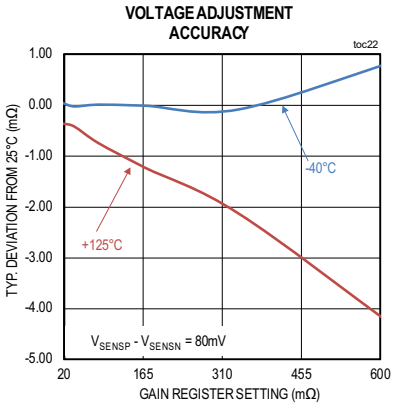








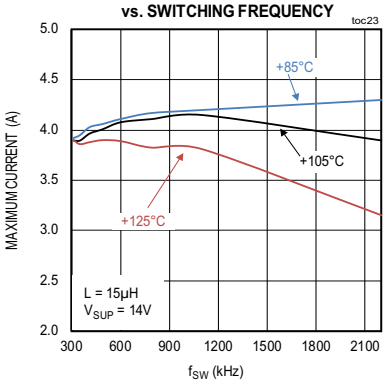




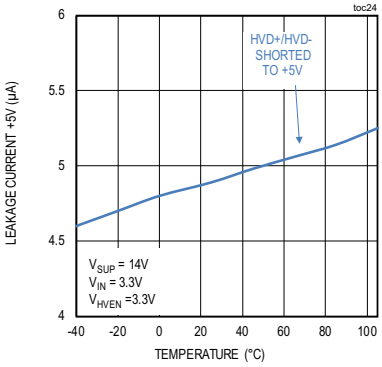
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

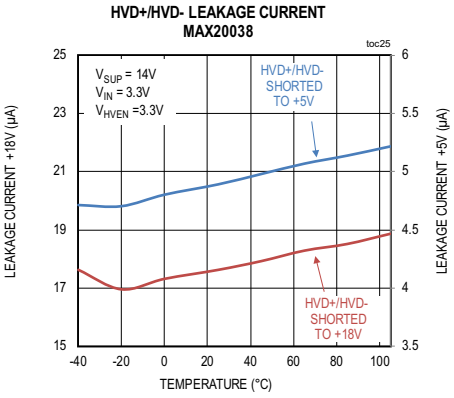
MAXIMUM USB LOAD CURRENT vs. SWITCHING FREQUENCY



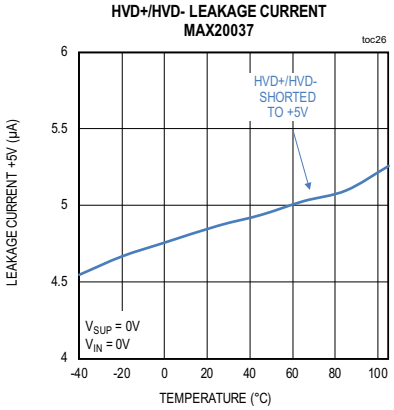
HVD+/HVD- LEAKAGE CURRENT MAX20037



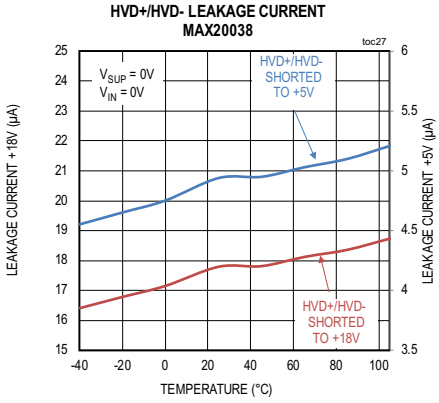
HVD+/HVD- LEAKAGE CURRENT MAX20038



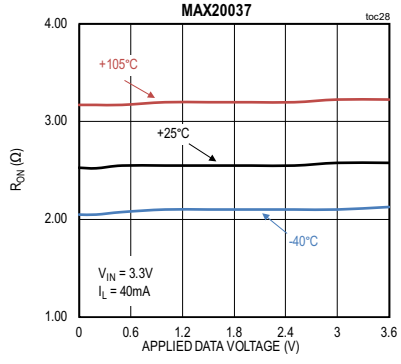
HVD+/HVD- LEAKAGE CURRENT MAX20037



HVD+/HVD- LEAKAGE CURRENT MAX20038

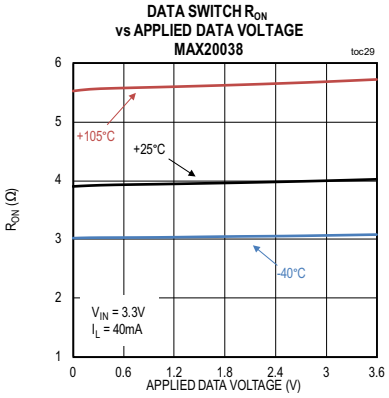


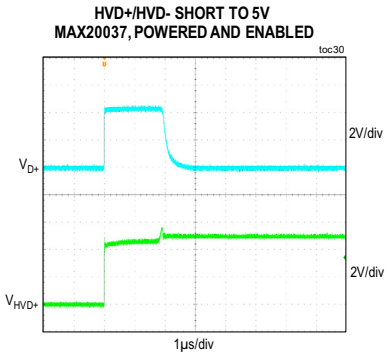
DATA SWITCH R_{ON} vs APPLIED DATA VOLTAGE MAX20037

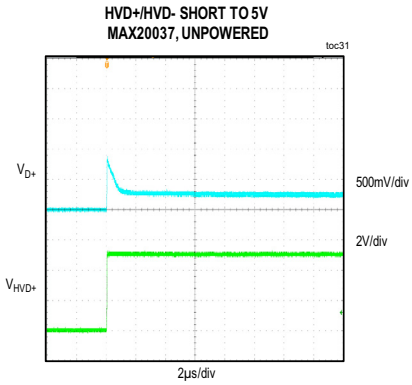


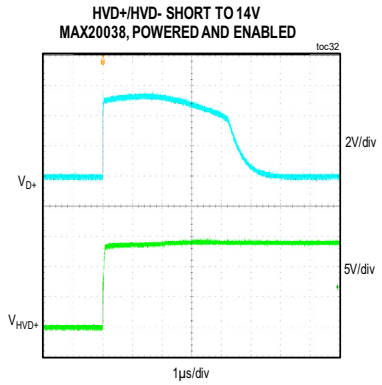
Typical Operating Characteristics (continued)

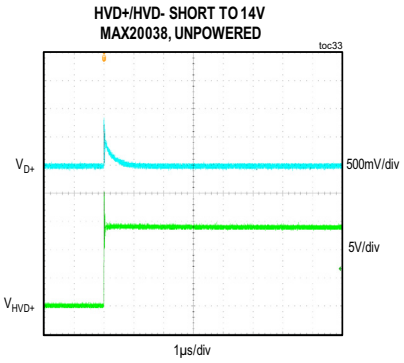
(T_A = +25°C, unless otherwise noted.)

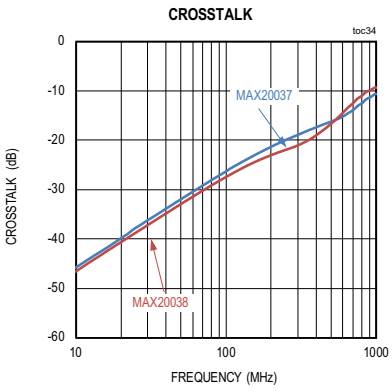




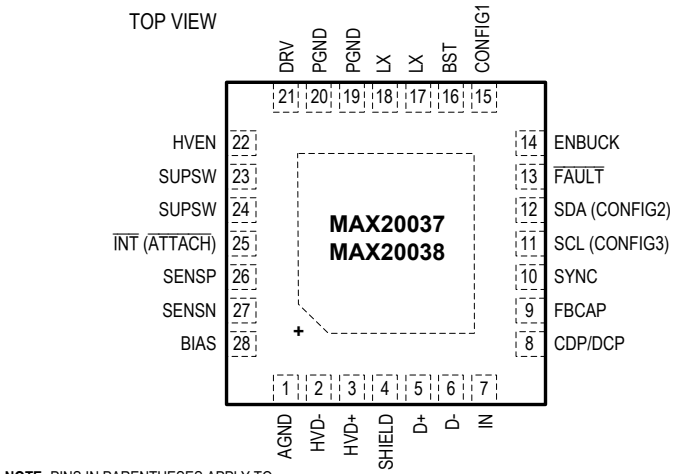








Pin Configuration



NOTE: PINS IN PARENTHESES APPLY TO STAND-ALONE VERSIONS.

TQFN/SWTQFN
(5mm x 5mm)

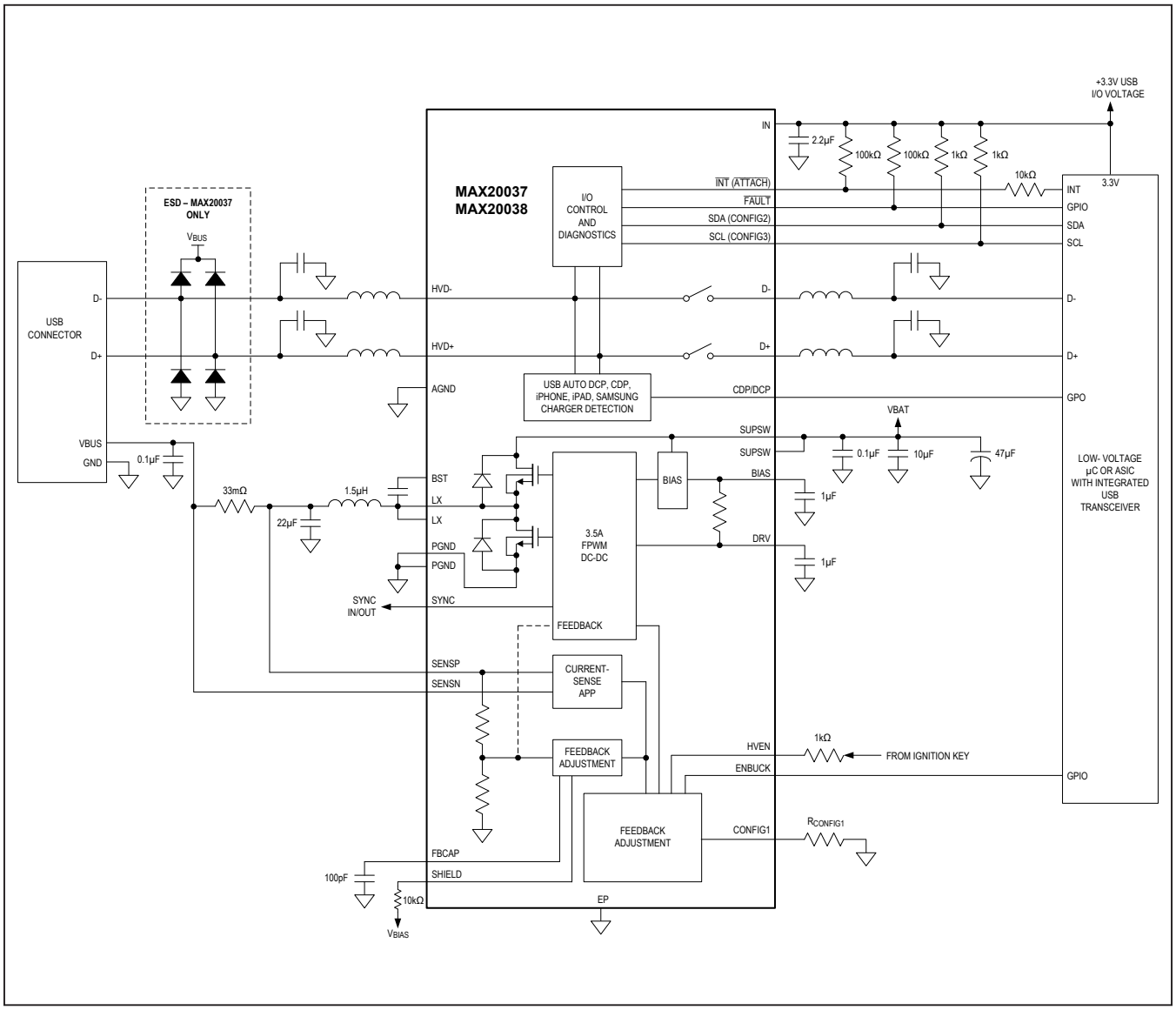
Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	HVD-	Protected USB Differential Data D- Output. Connect HVD- to the downstream-facing USB connector D- pin.
3	HVD+	Protected USB Differential Data D+ Output. Connect HVD+ to the downstream-facing USB connector D+ pin.
4	SHIELD	USB Captive-Cable Shield Input. See the *Applications Information* section.
5	D+	USB Differential Data D+ Input. Connect D+ to the upstream-facing, low-voltage USB transceiver D+ pin.
6	D-	USB Differential Data D+ Input. Connect D+ to the upstream-facing, low-voltage USB transceiver D- pin.
7	IN	Logic Enable Input. Connect to I/O voltage of USB transceiver. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 2.2µF ceramic capacitor from IN to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
8	CDP/DCP	Charger-Detection Configuration Pin. Set low for I²C-mode default to CDP and for stand-alone CDP operation. Set high for stand-alone DCP operation.
9	FBCAP	External Capacitor Connection. Connect a capacitor to GND to set DC current-sense bandwidth.
10	SYNC	Sync Input/Output for Synchronization with Other Supplies. See the *Applications Information* section.
11	SCL (CONFIG3)	I²C Clock (for I²C Variants). For stand-alone variants, connect a resistor to GND and see the *Applications Information* section.for CONFIG3.
12	SDA (CONFIG2)	I²C Data (for I²C Variants). For stand-alone variants, connect a resistor to GND and see the *Applications Information* section. for CONFIG2.
13	$\overline{\text{FAULT}}$	Active-Low, Open-Drain Fault-Indicator Output. Connect a 100kΩ pullup resistor to IN.
14	ENBUCK	DC-DC Enable Input. Drive ENBUCK low/high to disable/enable the switching regulator.
15	CONFIG1	Configuration Pin. See the *Applications Information* section for CONFIG1.
16	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
17, 18	LX	Inductor Connection. Connect an inductor from LX to the DC-DC converter output (SENSP).
19, 20	PGND	Power Ground
21	DRV	External Capacitor Connection. Connect a 1µF capacitor between DRV and PGND.
22	HVEN	Active-High Enable Input for IC. HV_EN is high-voltage compatible. Drive HVEN high for normal operation.
23, 24	SUPSW	Supply Pin for the Internal Linear Regulator and Internal High-Side Switch-Supply Input. SUPSW provides power to the internal switch. Connect a 10µF ceramic capacitor in parallel with a 0.1µF capacitor from SUPSW to PGND. See the *DC-DC Input Capacitor Selection* section.
25	$\overline{\text{INT}}$ ($\overline{\text{ATTACH}}$)	Interrupt Pin (for I²C Variants). Open-drain, active-low attach output (for stand-alone variants).
26	SENSP	DC-DC Converter Feedback Input and Current-Sense Amplifier Positive Input. Connect to positive terminal of current-sense resistor and the main output of the converter. Used for internal voltage-regulation loop.
27	SENSN	Current-Sense Amplifier Negative Input. Connect to negative terminal of current-sense resistor.
28	BIAS	5V Linear Regulator Output. Connect a 1µF ceramic capacitor from BIAS to ground. BIAS powers the internal circuitry.
—	EP	Exposed Pad. Connect EP to multiple ground planes with a 3 x 3 via grid.

Typical Operating Circuit



Detailed Description

The MAX20037/MAX20038 ICs combine a 5V/3.5A automotive-grade step-down converter, a USB host-charger adapter emulator, and USB protection switches. The device variants offer options for both stand-alone/GPIO and I²C configuration and control. This device family is designed for high-power USB ports in automotive radio, navigation, connectivity, USB hub, and dedicated charging applications.

The ICs feature low-voltage, high-bandwidth data switches (MAX20037), and high-voltage, high-ESD data switches (MAX20038). The MAX20037 offers data switch protection for up to 6V, and high-ESD protection with an external ESD array. The MAX20038 offers data switch protection for up to 18V, and high-ESD protection with internal ESD protection circuitry.

The data switches of all device variants protect the sensitive 3.3V pins of the USB transceiver and support USB Low-Speed (1.5Mbps), Full-Speed (12Mbps), and Hi-Speed (480Mbps) communication modes. The internal host-charger port-detection circuitry offer automatic sensing and conformance to multiple standards, including USB-IF BC1.2 CDP/DCP, Apple® 1A/2.4A DCP, Samsung DCP, and China YD/T1591-2009. All variants enable USB-IF OTG, Apple Carplay, and Anroid Auto conformance, while retaining industry-leading protection features and automotive-grade robustness.

The high-efficiency step-down DC-DC converters operate from a voltage up to 28V and are protected from load-dump transients up to 40V. The DC-DC converters can be programmed for, or synced to, switching frequencies from 275kHz to 2.2MHz, and can deliver 3A of continuous current at 105°C.

The ICs feature a high-side current-sense amplifier and programmable feedback-adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications. The precision current sense allows for an accurate DC output current limit that minimizes solution component size and cost.

Power-Up and Enabling

System Enable (HVEN)

HVEN is used as the main enable to the device and initiates system startup and configuration. If HVEN is at a logic-low level, and the system is not configured for hold operation, SUPSW power consumption is reduced and the device enters a standby low-quiescent current level. HVEN is compatible with inputs from automotive battery level down to 3.3V.

DC-DC Enable (ENBUCK)

The buck regulator on the ICs is controlled by the ENBUCK pin for stand-alone variants, and by both the ENBUCK pin and I²C interface for I²C variants. The DC-DC converter is activated by driving ENBUCK high, and disabled by driving ENBUCK low. For I²C variants, setting ENBUCK low overrides an I²C ENBUCK enable command, which allows compatibility with USB hub controllers. For USB hub applications, connect ENBUCK to the enable output of the USB hub controller in a typical application. This allows the USB hub controller to enable and disable the USB power port through software commands. ENBUCK can be directly connected to the BIAS or IN pin for applications that do not require GPIO control of the DC-DC converter enable.

3.3V Input (IN)

IN is used to clamp the D+ and D- pins during an ESD and short-to-BUS/battery event on the HVD+ and HVD- pins. This clamping protects the downstream USB transceiver. Because of this, IN must always be set to 3.3V for USB communication to occur. The IN pin features an overvoltage lockout that disables the data switches if IN is above V_{IN_OVLO}. Bypass IN with a 2.2µF ceramic capacitor, placed close to the IN pin, and connect it to the same 3.3V supply that is shared with the multimedia processor or hub transceiver. For dedicated charging applications, IN can be supplied from a resistive divider off the BIAS pin.

Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal logic and control circuitry for the device. BIAS is internally powered from SUPSW and automatically powers up when HVEN is high and SUPSW voltage exceeds approximately 4.5V. The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when HVEN is low and the device is not configured for hold mode, and a low 4µA (typ) shutdown current mode is entered. Bypass BIAS to GND with a 1µF ceramic capacitor.

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Linear Regulator Output (DRV)

DRV is the output of a 5V linear regulator that powers the high-side and low-side MOSFET drivers for the DC-DC converter. DRV is internally powered from SUPSW and powers up automatically when HVEN is high and SUPSW voltage exceeds ~4.5V. The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when HVEN is low and the device is not configured for hold mode, and a low 4µA (typ) shutdown current mode is entered. Bypass DRV to ground with a 1µF ceramic capacitor.

Power-On Sequencing

HVEN, ENBUCK, and IN do not have a power-up sequence requirement by design; however, the desired system behavior should be considered for the state of these pins at startup. The D+ and D- pins are clamped to IN, so IN should be set to 3.3V before any communication or dedicated charging is required. It is recommended that IN is set to 3.3V before HVEN is set high. ENBUCK acts as the master disable for the DC-DC converter. If ENBUCK is low when HVEN is set high, all variants keep the buck converter in the disabled state until ENBUCK is set high.

Step-Down DC-DC Regulator

Step-Down Regulator

The ICs feature a current-mode step-down converter with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency, forced-PWM (FPWM) operation under light loads. The ICs operate with 4.5V to 28V input voltages, while using only 4µA (typ) at no load. In no-load applications, the device can be operated in either skip mode for reduced current consumption, or fixed-frequency, FPWM mode to eliminate frequency variation and help minimize EMI. The DC-DC converter features a cycle-by-cycle current limit, and intelligent transition from skip mode to FPWM mode, which makes the ICs ideal for automotive applications.

Wide Input Voltage Range

The ICs are specified for a wide 4.5V to 28V input voltage range. SUPSW provides power to the internal BIAS linear regulator and internal power switch. Certain conditions such as cold crank can cause the voltage at the output to drop below the programmed output voltage. Under such conditions, the ICs operate in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The ICs have a maximum duty cycle of 98% (typ). The device monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes for every switching cycle. Once the off-time of 150ns (typ) is detected continuously for 12µs, the low-side FET is forced on for 150ns (typ) every 12µs. The input voltage at which the ICs enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the ICs enter dropout can be approximated, as shown in Equation 1.

Equation 1:

$$V_{SUP} = \frac{V_{OUT} + (I_{OUT} \times R_{ONH})}{0.98}$$

Note: Equation 1 does not take into account the efficiency and switching frequency, but provides a good first-order approximation. Use the R_{ONH} number from the max column in the *Electrical Characteristics* table.

Output Voltage (SENSP)

The ICs feature a precision internal-feedback network connected to SENSP that is used to set the output voltage of the DC-DC converter. The network nominally sets the average DC-DC converter output voltage to the voltage that corresponds to the VOUT[2:0] bits of the SETUP_1 register, with a default of 5.1V.

Soft-Start

When the DC-DC converter is enabled, the regulator soft-starts by gradually ramping up the output voltage from 0 to 5.15V in ~4ms. This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads (see the *USB Loads* section).

Reset Behavior

The ICs implement a discharge function on SENSN any time the DC-DC converter is disabled for any reason, except when a SENSN overvoltage condition is detected. When the discharge function is activated, a reset timer ($t_{SENSN_DIS_CD}$) is also started. The DC-DC converter is internally disallowed from starting up again until after the reset timer has expired. This allows for easy compatibility with USB specifications, and removes the need for long discharge algorithms implemented in system software.

Table 1. $\overline{\text{FAULT}}$ Conditions

EVENT	ERROR_1 REGISTER BITS (I2C ONLY)	ACTION TAKEN
Thermal Fault	T_SHDN	Immediately assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register, and shut down DC-DC converter. After fault no longer exists for 16ms, release $\overline{\text{FAULT}}$ pin and enable DC-DC converter.
Thermal Warning	T_WARN	Immediately assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register. After fault no longer exists for 16ms, release $\overline{\text{FAULT}}$ pin.
HVD± Overvoltage	DATA_OV	Immediately open data switches. Assert $\overline{\text{FAULT}}$ pin and associated bit in ERROR_1 register after fault persists for 16ms. After fault no longer exists for 16ms, release $\overline{\text{FAULT}}$ pin and close data switches.
USB DC Overcurrent	BUS_ILIM	Assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register bit after overcurrent condition persists for 16ms. After overcurrent no longer exists, immediately release $\overline{\text{FAULT}}$ pin.
SENSN < 4.75V	BUS_UV	Assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register after undervoltage condition persists for 16ms. After UV no longer exists, immediately release $\overline{\text{FAULT}}$ pin.
USB DC Overcurrent and SENSN < 4.75V	BUS_ILIM and BUS_UV	Assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register and shut down DC-DC converter after overcurrent and undervoltage conditions persist for 16ms. Release $\overline{\text{FAULT}}$ pin and restart DC-DC converter 16ms after shutdown.
USB DC Overcurrent and SENSN < 2.0V	BUS_STG	Immediately assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 registert and shut down DC-DC converter. Release $\overline{\text{FAULT}}$ pin and restart DC-DC converter 16ms after shutdown.
LX Overcurrent for 4 Consecutive Cycles and SENSN < 2.0V	BUS_STG	Immediately assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register and shut down DC-DC converter. Release $\overline{\text{FAULT}}$ pin and restart DC-DC converter 16ms after shutdown.
SENSN Overvoltage	BUS_OV	Assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register and disable DC-DC converter 3µs after overvoltage condition detected. Release $\overline{\text{FAULT}}$ pin and restart DC-DC converter immediately after overvoltage condition is removed.
IN Overvoltage	IN_OV	Immediately assert $\overline{\text{FAULT}}$ pin/associated bit in ERROR_1 register and disable data switches. Release $\overline{\text{FAULT}}$ pin and close data switches immediately after overvoltage condition is removed.

Reset Criteria

The ICs' DC-DC converter automatically resets for all undervoltage, overvoltage, overcurrent, and overtemperature fault conditions, as well as for any change in the CDP/DCP pin, or the CD1 bit of the SETUP_3 register. See Table 1 for more information.

Switching-Frequency Configuration

The DC-DC switching frequency can be configured by the internal oscillator or by an external clock on the SYNC pin, and the SYNC pin can be configured as either an input or an output. The internal oscillator frequency is set by the FSW[2:0] bits of the SETUP_2 register, which has a POR value corresponding to 2.2MHz. For stand-alone variants, the f_{SW} configuration value is loaded from the CONFIG1 pin at startup. The internal oscillator can be programmed for eight discrete values, from 275kHz to 2.2MHz.

Switching-Frequency Synchronization (SYNC)

When SYNC is configured to operate as an output, skip-mode operation is disallowed, and the internal oscillator frequency is driven out of the SYNC pin, allowing other devices to synchronize with the MAX20037/MAX20038 ICs.

When SYNC is configured as an input, the SYNC pin becomes a logic-level input that can be used for both operating-mode selection and frequency control. Connecting SYNC to a logic-high signal or an external clock enables fixed-frequency, FPWM mode. Connecting SYNC to AGND allows intelligent skip-mode operation. The ICs can be externally synchronized to frequencies within ±20% of the programmed internal oscillator frequency.

Table 2. DC-DC Converter Intelligent Skip Mode Truth Table

SYNC PIN	SYNC_DIR BIT	DATA SWITCH CHARGE-DETECTION MODE	CDP ATTACH DETECTION	DCP ATTACH DETECTION	DC CURRENT SENSE	DC-DC CONVERTER OPERATION
x	1	x	x	x	x	Forced-PWM Mode: Continuous
1	0	x	x	x	x	Forced-PWM Mode: Continuous
Clocked	0	x	x	x	x	Forced-PWM Mode: Continuous
0	0	High-Speed Pass-Through (SDP) Mode	x	x	0	Intelligent Skip Mode: No device attached
0	0	High-Speed Pass-Through (SDP) Mode	x	x	1	Forced-PWM Mode: Device attached
0	0	BC1.2 Auto CDP Mode	0	x	0	Intelligent Skip Mode: No device attached
0	0	BC1.2 Auto CDP Mode	1	x	x	Forced-PWM Mode: Device attached
0	0	BC1.2 Auto CDP Mode	x	x	1	Forced-PWM Mode: Device attached
0	0	1A / 2.4A Auto DCP Modes	x	0	0	Intelligent Skip Mode: No device attached
0	0	1A / 2.4A Auto DCP Modes	x	1	x	Forced-PWM Mode: Device attached
0	0	1A / 2.4A Auto DCP Modes	x	x	1	Forced-PWM Mode: Device Attached

Forced-PWM (FPWM) Operation

In FPWM mode, the ICs maintain fixed-frequency PWM operation over all load conditions, including no-load conditions.

Intelligent Skip-Mode Operation and Device-Attach Detection

When the SYNC pin is configured as an input, but neither a clocked signal nor a logic-high level exists on the SYNC pin, the ICs operate in skip mode at very light load/no-load conditions. Intelligent device-attach detection is used to determine when a device is attached to the USB port. The device intelligently exits skip mode and enters FPWM mode when a device is attached, and remains in FPWM mode as long as the attach signal persists. This minimizes EMI and the concerns caused by automotive captive USB cables and poorly shielded consumer USB cables. The device-attach event is also signaled by the $\overline{\text{ATTACH}}$ pin (stand-alone variants) or ATTACH bit (I^2C variants). The criteria for device-attach detection and intelligent skip-mode operation are shown in Table 2.

Spread-Spectrum Option

Spread-spectrum operation is offered to improve EMI performance of the MAX20037/MAX20038. Spread-spectrum operation is enabled by the SS_EN bit of the SETUP_1 register, which is pre-loaded on startup from the CONFIG1 pin for both stand-alone and I^2C variants. The internal operating frequency modulates up to ±3.25% relative to the internally generated operating frequency, resulting in a total spread-spectrum range of 6.5%. Spread-spectrum mode is only active when operating from the internal oscillator. Spread-spectrum clock dithering is not possible when operating from an external clock.

Current Limit

The ICs limit the USB load current using both a fixed internal peak current threshold of the DC-DC converter and a user-programmable external DC load current-sense amplifier threshold (see the section). This allows the current limit to be adjusted between 300mA to 3A depending on application requirements and protects the DC-DC converter in the event of a fault. Upon exceeding either the DC-DC peak or user-programmable current thresholds, the high-side FET is immediately turned

off and current-limit algorithms are initiated. When the external current limit lasts for longer than 16ms (typ,) the FAULT pin asserts and the BUS_ILIM bit of the ERROR_1 register is set. The ILIM_ITRIP bit of the SETUP_4 register determines the output-voltage droop required to initiate a DC-DC converter reset during current-limit behavior. If both the USB current limit is detected and the output voltage falls below the reset threshold for longer than 16ms (typ), the DC-DC converter resets. Furthermore, if the internal LX peak-current threshold is exceeded for four consecutive switching cycles and the output voltage is less than 2.0V, the DC-DC converter resets.

Output Short-Circuit Protection

The DC-DC converter output (SENSP, SENSN) of all variants is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage condition is encountered, the DC-DC converter immediately resets, asserts the FAULT pin, flags the fault in the ERROR_1 register, and reattempts soft-start after the reset delay. This pattern repeats until the short circuit has been removed.

If a short-to-battery (V_{SENSN} > V_{OV_SENSN}) is encountered, the device stops switching, the FAULT pin is asserted, and the fault is flagged in the ERROR_1 register. This behavior persists as long as the overvoltage condition exists on SENSP.

Thermal-Overload Protection

The thermal-overload protection limits the total power dissipation in the ICs. A thermal-protection circuit monitors the die temperature. If the die temperature exceeds +175°C, the device shuts down, allowing it to cool. Once the device has cooled by 15°C, it is enabled again. This results in a pulsed output during continuous thermal-overload conditions. The thermal-overload protection protects the device in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See the *Package Information* section for more information.

Pre-Thermal Overload Warning

The I²C variants of the ICs feature a thermal-overload warning feature that sets the T_WARN bit of the ERROR_1 register when the die temperature crosses +145°C. This allows system software implementation of thermal-foldback/load-shedding behavior to prevent a thermal-overload condition.

Hold Mode

When hold mode is enabled, the device retains accessory power for the duration of an internal timer. The timer begins when HVEN goes low and hold mode is enabled. When the timer expires, the device transitions into the low-Q shutdown mode. **Note:** Hold mode is not available on part variants with the ATID suffix.

USB Current Limit and Output-Voltage Adjustment

Current-Sense Amplifier (SENSP, SENSN)

The ICs feature an internal USB load current-sense amplifier to monitor the DC load current delivered to the USB port. The (V_{SENSP} - V_{SENSN}) voltage is used internally to provide precision DC current limit and voltage-compensation functionality. A 33mΩ sense resistor should be placed between SENSP and SENSN.

USB DC Current-Limit Configuration

The I²C variants of the ICs allow configuration of the precision DC current limit by the ILIM[2:0] bits of the SETUP_4 register. I²C configuration enables selection of eight discrete DC current-limit values.

Stand-alone variants of the ICs allow a selection of a subset of the eight available current-limit options by use of the CONFIG3 resistor. See the *Control and Diagnostics* section for more information.

Voltage Feedback-Adjustment Configuration

The ICs allow voltage-droop compensation for up to 600mΩ of USB cable in typical USB charging applications. I²C variants of the ICs allow this configuration by the GAIN[4:0] bits of the SETUP_2 register.

Stand-alone variants of the ICs allow configuration by the CONFIG2 resistor, which sets the GAIN[3:0] LSBs, and the CONFIG3 resistor, which sets the GAIN[4] MSB. See the *Control and Diagnostics* section for more information.

High-Voltage Modes Configuration

The I²C variants of the ICs allow high output-voltage-mode configurations for flexibility of use in higher power-charging applications and for load-dump-protected battery output to automotive modules. See Table 9 for configuration information.

USB Protection Switches and Host-Charger Adapter Emulation

HVD+ and HVD- Protection

The ICs provide automotive-grade ESD and short-circuit protection for the low-voltage internal USB data lines of high-integration multimedia processors. HVD+/HVD- protection consists of ESD and overvoltage protection (OVP) for 1.5Mbps, 12Mbps, and 480Mbps USB transceiver applications. This is accomplished with a very low-capacitance FET in series with the D+ and D- data paths.

External ESD diodes are required when using the MAX20037 low-voltage, high-bandwidth variant. With this external protection, the HVD+ and HVD- pins are protected to ±15kV Air Gap/±8kV Contact Discharge with the IEC 61000-4-2 model and 330Ω, 330pF model.

The MAX20038 high-voltage variant does not require an external ESD array and protects the HVD+ and HVD- pins to ±15kV Air Gap/±8kV Contact Discharge with the IEC 61000-4-2 model and 330Ω, 330pF model.

The HVD+ and HVD- short-circuit protection features include protection for short to the USB +5V BUS on all variants, and protection for short to +18V car battery for the MAX20038 high-voltage variant. These protection features prevent damage of the low-voltage USB transceiver when shorts occur in the vehicle harness or customer USB connector/cable. Short-to-ground protection is provided by the upstream USB transceiver.

USB Host Adapter Emulator

The USB protection switches integrate the latest USB-IF Battery Charging Specification Revision 1.2 CDP and DCP circuitry, as well as 1.0A and 2.4A resistor bias options for Apple-compliant devices. Legacy Samsung Galaxy 1.2V divider and China YD/T1591-2009 compatibility are also provided by the DCP modes.

HVD+ and HVD- Modes of Operation

The ICs feature four discrete modes of operation. I²C variants allow selection of all four modes by the CD[1:0] bits of the SETUP_3 register. The CDP/DCP pin should be set low for I²C operation. See Table 3a for configuration information.

Stand-alone variants allow selection of two modes by the CDP/DCP pin. See Table 3b for configuration information. Custom CDP/DCP pin behavior is available; contact Maxim applications support for more information.

Note that for all variants, changing device role between a communication mode (SDP/CDP) and a dedicated charging mode (DCP) initiates a device reset to comply with USB specifications and ensure proper device detection.

USB On-The-Go and Dual-Role Applications

MAX20037 and MAX20038 are fully compatible with USB On-The-Go (OTG) and dual-role applications.

Care must be taken when selecting the IC variant. Ensure compatibility with your specific dual-role application (see Table 3b, Table 3c, and the *Ordering Information* section); contact Maxim applications support for more information.

In instances where there is no host negotiation, and the head-unit SOC is functioning as the initial peripheral, the IC must first be placed into Hi-Speed pass-through (SDP) mode. This has implications on what mode the device should default to upon startup, and the basic functionality of the CDP/DCP pin. If the SOC retains the ability to write registers through the I²C bus before and/or during peripheral mode, then either I²C variant will be successful, with the ATIA variant generally being preferred. If the SOC cannot write to the CD[1:0] register before it enters peripheral mode, the IC must start into SDP mode after an HVEN toggle. This will allow a role swap without microcontroller interaction with the IC. This is necessary if the head unit is booted with an unprogrammed SOC waiting to be programmed through the protected USB port.

In an initial peripheral application that uses a stand-alone version, the IC must have the ability to switch between SDP and BC1.2 Auto-CDP (CDP) modes using the CDP/DCP pin. This is only available on the ATID variant. Similarly, if there is the potential for a peripheral-mode SOC without GPIO control, the CDP/DCP pin should be pulled down to default to Hi-Speed SDP mode.

Control and Diagnostics

I²C Configuration (CONFIG1 and I²C)

The I²C variants of the ICs allow basic device configuration from a resistor placed close to ground on the CONFIG1 pin. The configuration parameters correlating to the chosen resistor are loaded in to their respective I²C registers on startup when HVEN is toggled high, causing a device transition from shutdown to a powered state. After startup, the user is free to change the affected I²C registers as desired. See Table 4 for I²C slave addresses.

For I²C variants, CONFIG1 sets the startup value of the DC-DC spread-spectrum enable bit (SS_EN) and the SYNC direction control bit (SYNC_DIR). CONFIG1 also sets the LSB of the I²C slave address. The configuration table for the I²C variant CONFIG1 pin is shown in Table 5. See Table 7b for resistor value selection. See *Ordering Information* for I²C variant part number information.

Table 3a. Data Switch Mode Truth Table (I²C Version)

DEVICE INPUTS					SA	SB	DATA SWITCH MODE
HVEN	IN	CD1 BIT	CD0 BIT	CDP/DCP PIN			
0	X	X	X	X	0	0	Off
X	0	X	X	X	0	0	Off
1	1	X	X	1	0	1	Invalid mode (CDP/DCP pin = 0 required for I²C variant)
1	1	0	0	0	1	0	Hi-Speed pass-through (SDP) mode
1	1	0	1	0	On if CDP = 0	On if CDP=1	BC1.2 Auto-CDP mode (CDP)
1	1	1	0	0	0	1	Auto BC1.2/SSG/Apple 2.4A (DCP)
1	1	1	1	0	0	1	Auto BC1.2/SSG/Apple 1A (DCP)

Table 3b. Data Switch Mode Truth Table (Stand-Alone)

DEVICE SUFFIX	DEVICE INPUTS			SA	SB	DATA SWITCH MODE
	HVEN	IN	CDP/DCP PIN			
X	0	X	X	0	0	Off
X	1	0	0	0	0	Invalid mode (IN +3.3V required for SDP/CDP)
ATIB	1	1	0	On if CDP = 0	On if CDP=1	BC1.2 auto-CDP mode (CDP)
ATIB	1	X	1	0	1	Auto BC1.2/SSG/Apple 2.4A (DCP)
ATID	1	1	0	1	0	Hi-Speed pass-through mode (SDP)
ATID	1	1	1	On if CDP = 0	On if CDP=1	BC1.2 auto-CDP Mode (CDP)
ATIE	1	1	0	1	0	Hi-Speed pass-through mode (SDP)
ATIE	1	1	1	0	1	Auto BC1.2/SSG/Apple 2.4A (DCP)

Table 3c. Default Data Switch Mode on HVEN Toggle (I²C Version)

DEVICE SUFFIX	DEVICE INPUTS			DATA SWITCH MODE
	HVEN	IN	CDP/DCP PIN	
X	1	X	1	Invalid mode (CDP/DCP pin = 0 required for I²C variant)
ATIA	1	1	0	BC1.2 auto-CDP (CDP) mode
ATIC	1	1	0	Hi-Speed pass-through (SDP) mode

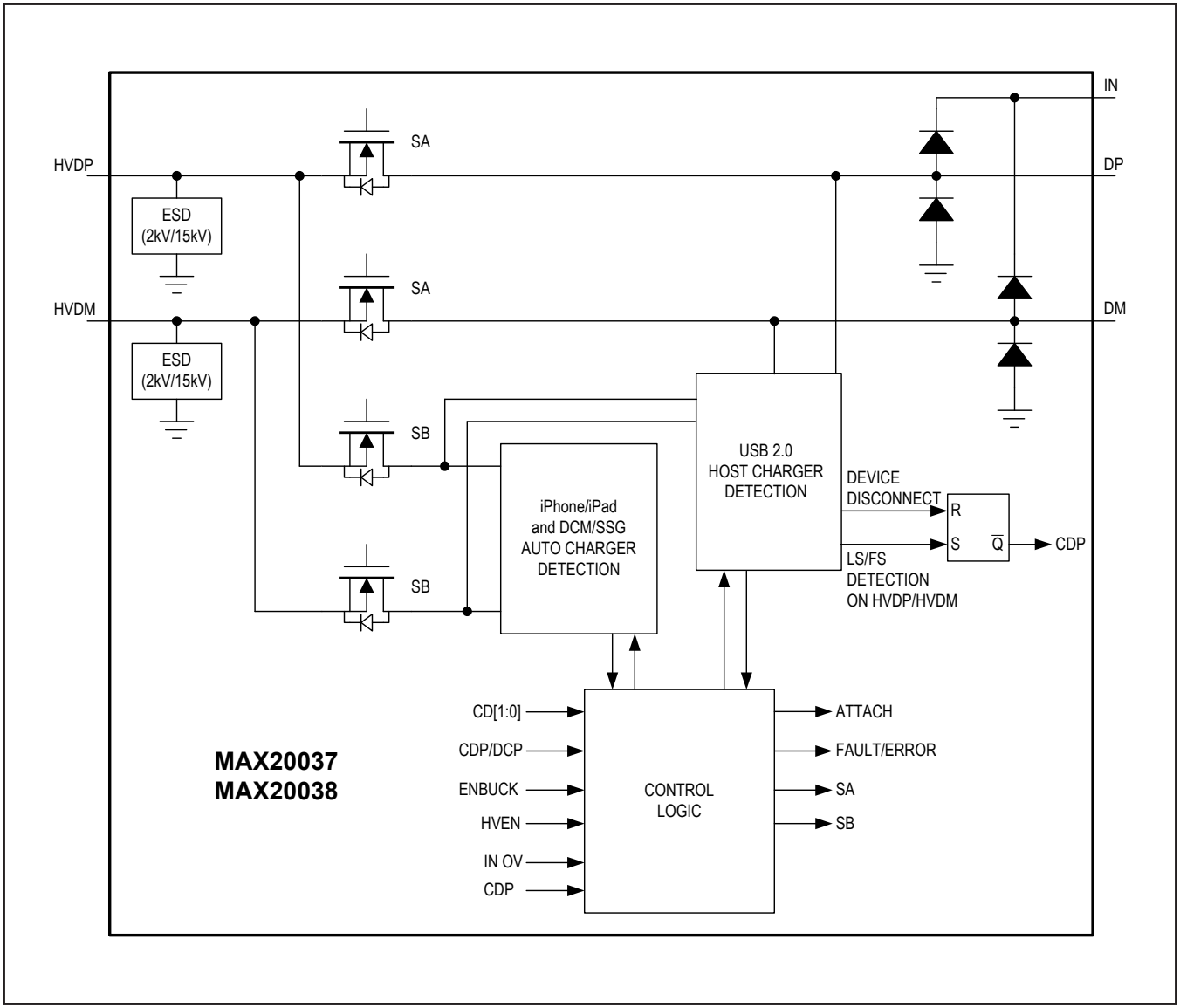

Figure 8. Data Switch and Charge-Detection Block Diagram

Table 4. I²C Slave Addresses

CONFIG1 CODE	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
00	0	1	1	0	0	0	0	0x30	0x60	0x61
01	0	1	1	0	0	0	1	0x31	0x62	0x63
10	0	1	1	0	0	1	0	0x32	0x64	0x65
11	0	1	1	0	0	1	1	0x33	0x66	0x67

Table 5. CONFIG1 Pin Table (I²C Version)

STEP	SPREAD-SPECTRUM ENABLE	I²C ADDRESS LSBs	SYNC PIN DIRECTION
0	Yes	00	Input
1	Yes	01	Input
2	Yes	10	Input
3	Yes	11	Input
4	Yes	00	Output
5	Yes	01	Output
6	Yes	10	Output
7	Yes	11	Output
8	No	00	Input
9	No	01	Input
10	No	10	Input
11	No	11	Input
12	No	00	Output
13	No	01	Output
14	No	10	Output
15	No	11	Output

Table 6. CONFIG1 Pin Table (Stand-Alone Variants)

STEP	SPREAD-SPECTRUM ENABLE	SWITCHING FREQUENCY (kHz)	SYNC PIN DIRECTION
0	Yes	2200	N/A
1	Yes	488	N/A
2	Yes	350	N/A
3	Yes	310	N/A
4	Yes	2200	Output
5	Yes	488	Output
6	Yes	350	Output
7	Yes	310	Output
8	No	2200	Input
9	No	488	Input
10	No	350	Input
11	No	310	Input
12	No	2200	Output
13	No	488	Output
14	No	350	Output
15	No	210	Output

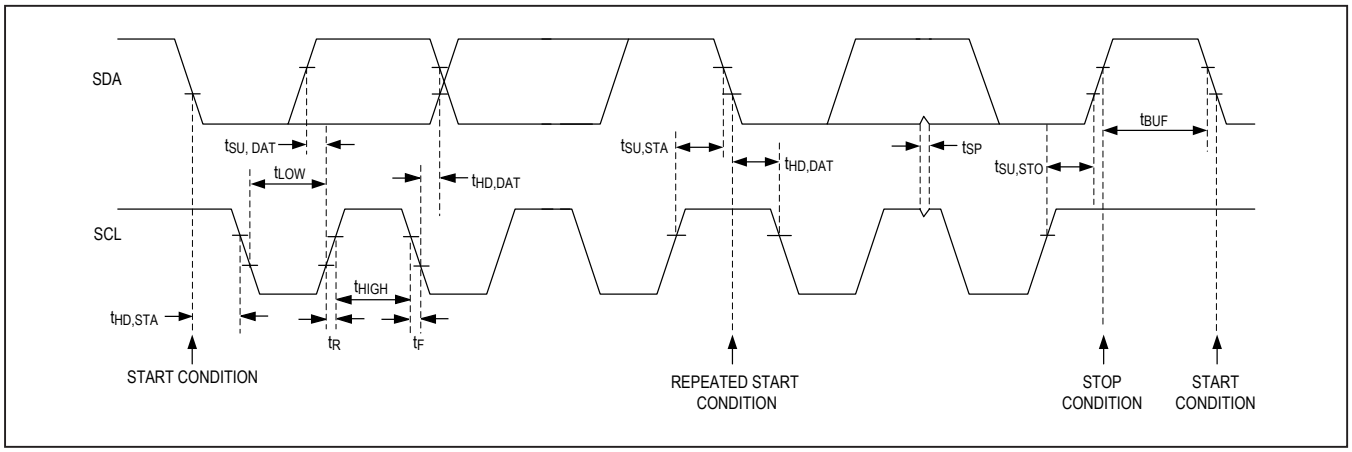

Figure 9. I²C Timing Diagram

Table 7a. CONFIG2 and CONFIG3 Pin Table (Stand-Alone Variants)

STEP	CONFIG2 PIN	CONFIG3 PIN		
	GAIN[3:0] LSBs PROGRAMMED VALUE	GAIN[4] MSB PROGRAMMED VALUE	ILIM (min) PROGRAMMED VALUE	HOLD-MODE ENABLE (ATIB, ATIE ONLY)
0	0000	0	0.57A	No
1	0001	0	1.56A	No
2	0010	0	2.57A	No
3	0011	0	3.06A	No
4	0100	1	0.57A	No
5	0101	1	1.56A	No
6	0110	1	2.57A	No
7	0111	1	3.06A	No
8	1000	0	0.57A	Yes (60min)
9	1001	0	1.56A	Yes (60min)
10	1010	0	2.57A	Yes (60min)
11	1011	0	3.06A	Yes (60min)
12	1100	1	0.57A	Yes (60min)
13	1101	1	1.56A	Yes (60min)
14	1110	1	2.57A	Yes (60min)
15	1111	1	3.06A	Yes (60min)

Table 7b. CONFIG1– CONFIG3 Resistor Selection (All Variants)

STEP	EXTERNAL RESISTOR (E96 1%)
0	Short to ground
1	619Ω
2	953Ω
3	1.33kΩ
4	1.82kΩ
5	2.32kΩ
6	3.01kΩ
7	3.83kΩ
8	4.87kΩ

STEP	EXTERNAL RESISTOR (E96 1%)
9	6.19kΩ
10	8.06kΩ
11	10.7kΩ
12	15kΩ
13	23.2kΩ
14	44.2kΩ
15	Connect to BIAS (or R > 71.5kΩ)

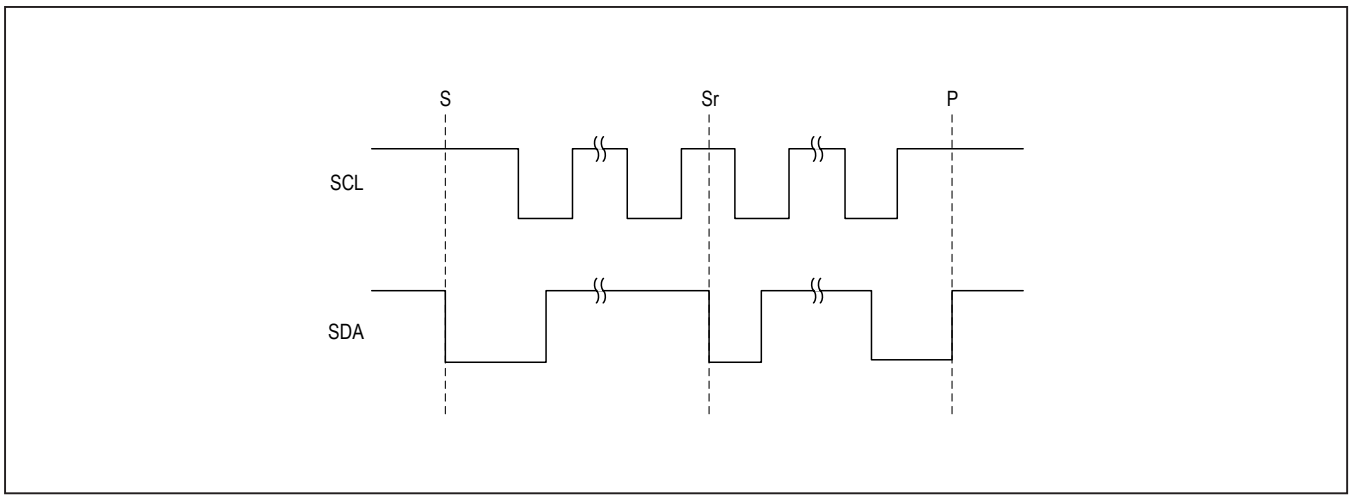

Figure 10. START, STOP, and Repeated START Conditions

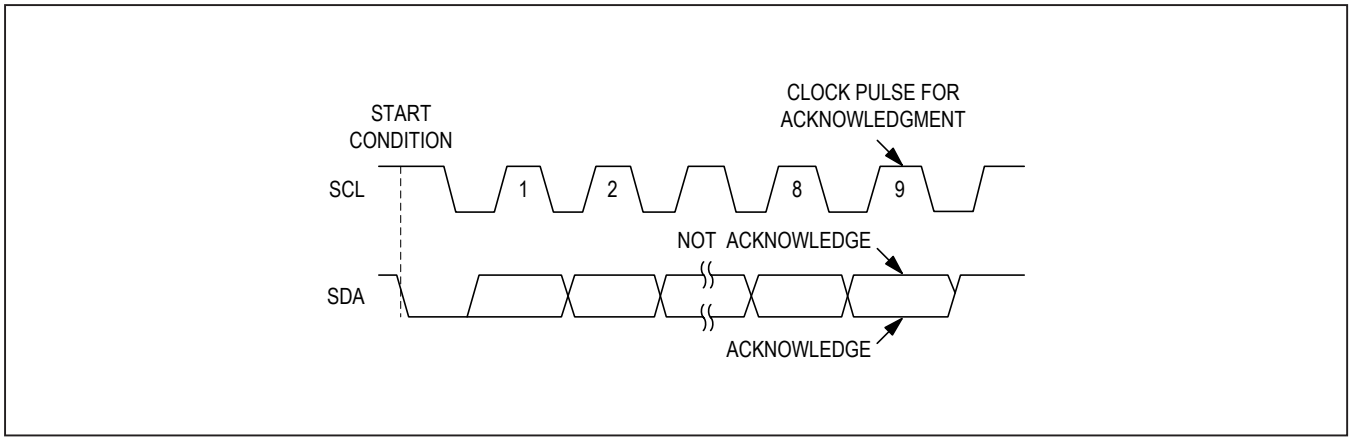

Figure 11. Acknowledge Condition

Stand-Alone Configuration (CONFIG1–CONFIG3)

The stand-alone variants of the ICs allow full device configuration from three resistors placed between the three CONFIG_ pins and ground. For stand-alone variants, SDA and SCL serve as CONFIG2 and CONFIG3, respectively.

For stand-alone variants, CONFIG1 sets the internal oscillator switching frequency, the SYNC pin direction, and enables/disables DC-DC spread-spectrum mode. The configuration table for the stand-alone variant CONFIG1 pin is shown in Table 6.

CONFIG2 sets the four LSBs of the voltage gain configuration GAIN[3:0]. CONFIG3 sets the USB DC current limit, enables/disables Hold mode functionality, and sets the MSB of voltage gain configuration GAIN[4]. **Note:** Hold mode is not available on part variants with the ATID suffix. Enabling hold mode with the CONFIG2 resistor will have no effect on these variants. See Table 7a for stand-alone variants' CONFIG2 and CONFIG3 options. See the *Applications Information* section for resistor value selection.

Note that device configurations are limited for stand-alone variants; full device configuration is available on I²C variants. See the *Applications Information* section for resistor value selection. See *Ordering Information* for I²C vs. stand-alone variant part number information.

Fault Detection and I²C Diagnostics

The ICs feature advanced device-protection features with automatic fault handing and recovery. Table 1 summarizes the conditions that generate a fault, and actions taken by the device. For all variants, the $\overline{FAULT}$ output remains asserted as long as a fault condition persists.

For I²C variants, the ERROR_1/ERROR_2 registers provide detailed information on the source of the fault condition, and the IRQMASK_0/IRQMASK_1 registers allow selection of the criteria for assertion of the I²C interrupt pin ($\overline{INT}$). The ERROR_1/ERROR_2 registers' bits are clear on read; however, the error bits respective to a present fault condition continue to reassert after clear as long as the fault condition persists. If the IRQMASK0/IRQMASK1 registers are configured to assert $\overline{INT}$ for a present fault, the $\overline{INT}$ pin deasserts upon read of the respective ERROR_ register, and subsequently reasserts if the fault condition still persists.

Fault Output Pin ($\overline{FAULT}$)

The ICs feature an open-drain, active-low $\overline{FAULT}$ output and are designed to eliminate false $\overline{FAULT}$ reporting by using an internal deglitch and fault blanking timer. This ensures $\overline{FAULT}$ is not incorrectly asserted during normal operation, such as starting into heavy capacitive loads. The $\overline{FAULT}$ pin is designed such that it can be connected directly to the overcurrent fault input of a hub controller or SoC. See Table 1 for more information.

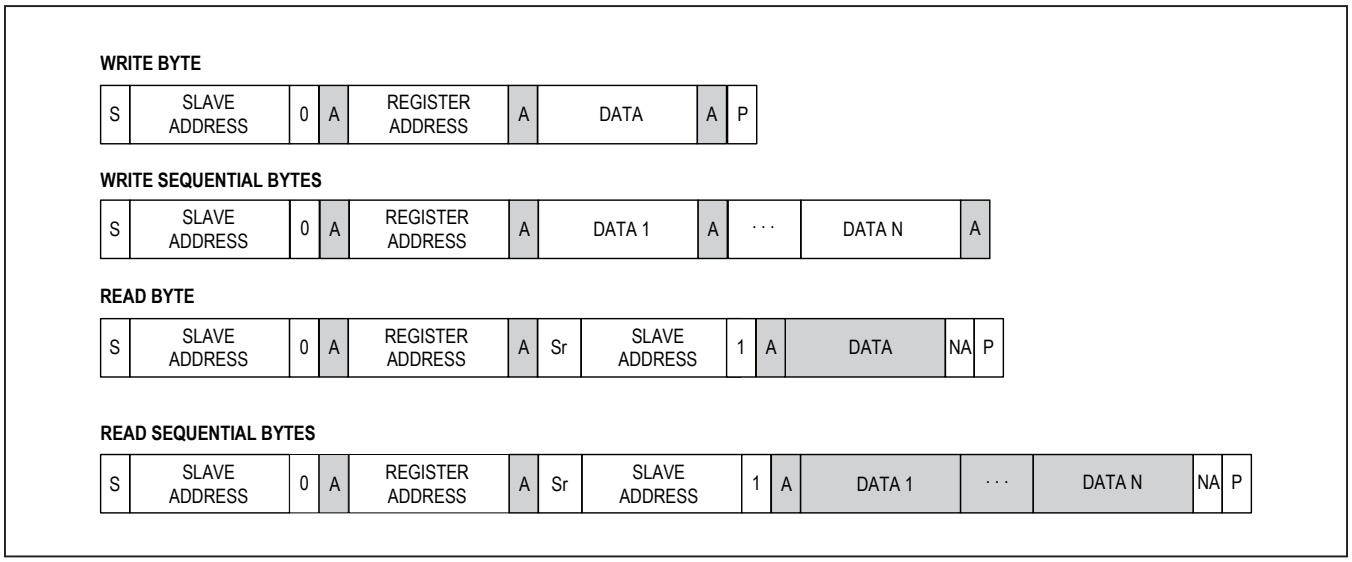

Figure 12. Data Format of I²C Interface

Attach Output Pin ($\overline{ATTACH}$)

The ICs feature an open-drain, active-low output which serves as the Attach Detection pin ($\overline{ATTACH}$) for stand-alone variants, and the Interrupt pin ($\overline{INT}$) for I²C variants. For stand-alone variants, the $\overline{ATTACH}$ pin can be used for GPIO input to a microprocessor, or to drive an LED for attach/charge indication.

I²C Diagnostics and Event Handling

The I²C-based diagnostic functionality of I²C variants is independent of the $\overline{FAULT}$ pin. Setting the IRQMASK bit for a specific fault condition does not mask the $\overline{FAULT}$ pin for the respective fault. IRQMASK register functionality affects only the behavior of the $\overline{INT}$ pin vs. respective ERROR_ register bits. This allows the $\overline{FAULT}$ pin to be tied to overcurrent fault input of a hub controller or SoC, while the I²C interface is simultaneously used by the system software for advanced diagnostic functionality.

I²C Output Voltage and Current Measurement

The I²C variants of the IC allow measurement of the instantaneous SENSP voltage and DC output current. To initiate a measurement, set the IV_READ bit of the SETUP_4 register. The IV_READ bit is cleared when the measurement is complete and the ADC_DONE bit of the ERROR_2 register is set. Additionally, the IV_INT bit of the SETUP_4 register can be set, which forces an interrupt. The completed measurement can be read from the USB_V and USB_I registers. The measured voltage provides 8 bits of resolution. When VOUT[2:0] is set to zero, the range of the ADC is 0 to 7.92V, and the SENSN voltage can be calculated in volts as (7.92/256) x USB_V. When VOUT[2:0] is not set to zero, the range is from 0 to 19.8V and the SENSN voltage can be calculated in volts as (19.8/256) x USB_V. The measured DC current also has 8 bits of resolution and can be calculated in amperes as ((0.1/256) x USB_I)/R_{SENSE}.

I²C Interface Specification

The ICs feature an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the ICs and the master at clock rates up to 400kHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 9 shows the 2-wire interface timing diagram.

A master device communicates to the ICs by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The ICs' SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The ICs' SCL line operates as an input only. A pullup resistor > 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 10). A START (S) condition from the master signals the beginning of a transmission to the ICs. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

Early STOP Condition

The ICs recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock-signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The ICs do not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The ICs do not implement the I²C specifications "general call address." If the ICs see the general call address (0b0000_0000), it does not issue an acknowledge.

Table 8. I²C Register Map

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	CMD	R/W	POR
SETUP_1	—	RSVD	EN_DCDC	VOUT[2:0]			SYNC_DIR	SSEN	0x00	R/W	*
SETUP_2	FSW[2:0]			GAIN[4:0]					0x01	R/W	0x00
SETUP_3	CD[1:0]		HOLD_EN	RSVD	HOLD[1:0]		RSVD		0x02	R/W	**
SETUP_4	AUTOCLR	IV_READ	IV_INT	VOUT_PR	ILIM_ITRIP	ILIM[2:0]			0x03	R/W	0x17
IRQMASK_0	ATTACH	BUS_UV	DATA_OV	BUS_ILIM	BUS_OV	BUS_STG	T_WARN	T_SHDN	0x04	R/W	0x00
IRQMASK_1	—	—	—	—	—	—	—	IN_OV	0x05	R/W	0x00
STATUS	ATTACH	CFG_OK	—	—	—	—	—	—	0x06	R	0x00
ERROR_1	ATTACH	BUS_UV	DATA_OV	BUS_ILIM	BUS_OV	BUS_STG	T_WARN	T_SHDN	0x07	R	0x00
ERROR_2	—	—	—	—	—	CFG_REQ	ADC_ DONE	IN_OV	0x08	R	0x00
USB_V	USB_V[7:0]								0x09	R	0x00
USB_I	USB_I[7:0]								0x0A	R	0x00

**POR dependent on CONFIG1 (see Table 5).*

***POR dependent on part number suffix (see Table 3c).*

Table 9. Setup Register, SETUP_1

SETUP_1								
BIT NO.	7	6	5	4	3	2	1	0
NAME	—	RSVD	EN_DCDC	VOUT[2:0]			SYNC_DIR	SSEN
POR	—	0	1	0	0	0	*	*

BIT	BIT DESCRIPTION
RESERVED	Do Not Modify
EN_DCDC	Buck regulator enable/disable: 0 = Disable buck regulator 1 = Enable buck regulator
VOUT[2:0]	Output-voltage configuration: 000 = 5V W/Voltage compensation 001 = 18V 010 = 9V 011 = 12V 100 = Future use 101 = Future use 110 = Future use 111 = Future use
SYNC_DIR	SYNC pin direction control: 0 = SYNC pin configured as output 1 = SYNC pin configured as input
SS_EN	Spread-spectrum enable/disable: 0 = Spread spectrum disabled 1 = Spread spectrum enabled

**POR dependent on CONFIG1 (see Table 5).*

Table 10. Setup Register, SETUP_2

SETUP_2								
BIT NO.	7	6	5	4	3	2	1	0
NAME	FSW[2:0]			GAIN[4:0]				
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
FSW[2:0]	Buck Regulator Switching-Frequency Configuration: 000 = 2200 kHz 001 = 1200 kHz 010 = 790 kHz 011 = 600 kHz 100 = 488 kHz 101 = 410 kHz 110 = 350 kHz 111 = 310 kHz
GAIN[4:0]	Output Voltage V/I Gain Configuration (in mΩ): 00000 = 0 00001 = 19 00010 = 40 00011 = 61 00100 = 83 00101 = 104 00110 = 125 00111 = 146 01000 = 169 01001 = 190 01010 = 211 01011 = 232 01100 = 255 01101 = 276 01110 = 297 01111 = 318 10000 = 340 10001 = 361 10010 = 382 10011 = 404 10100 = 426 10101 = 447 10110 = 468 10111 = 490 11000 = 512 11001 = 533 11010 = 554 11011 = 576 11100 = 598 11101 = 619 11110 = 640 11111 = 661

Table 11. Setup Register, SETUP_3

SETUP_3								
BIT NO.	7	6	5	4	3	2	1	0
NAME	CD[1:0]		HOLD_EN	RSVD	HOLD[1:0]		RSVD	
POR	**	**	0	0	1	1	0	0

BIT	BIT DESCRIPTION
CD[1:0]	Charge Detection Configuration: 00 = Hi-Speed Pass-Thru (SDP) mode 01 = BC1.2 CDP Mode 10 = iPad 2.4A/BC1.2 Auto DCP/SSG mode 11 = iPhone 1A/BC1.2 Auto DCP/SSG mode
HOLD_EN	Hold Mode Enable/Disable: 0 = Hold mode disabled 1 = Hold mode enabled
RESERVED	Do Not Modify
HOLD[1:0]	Hold Mode Timer Configuration: 00 = 7.5 minutes 01 = 15 minutes 10 = 30 minutes 11 = 60 minutes
RESERVED	Do Not Modify

***POR dependent on part number suffix (see Table 3c).*

Table 12. Setup Register, SETUP_4

SETUP_4								
BIT NO.	7	6	5	4	3	2	1	0
NAME	AUTOCLR	IV_READ	IV_INT	VOUT_PR	ILIM_ITRIP	ILIM[2:0]		
POR	0	0	0	1	0	1	1	1

BIT	BIT DESCRIPTION
AUTOCLR	ERROR Register Read Handling Configuration: 0 = ERROR register flags automatically cleared when fault removed 1 = ERROR register flags latched until read
IV_READ	Initiate Output-Voltage/Current ADC Conversion: 0 = IV_READ cleared to 0 after ADC conversion complete (read) 1 = Initiate ADC conversion (write)
IV_INT	ADC Conversion Interrupt Enable: 0 = Disable interrupt on ADC conversion complete 1 = Enable interrupt on ADC conversion complete
VOUT_PR	Output-Voltage Configuration Protection Bit: 0 = SETUP_1 VOUT[2:0] output-voltage mode change allowed 1 = SETUP_1 VOUT[2:0] output-voltage mode change not allowed
ILIM_ITRIP	Constant-Current Regulation on ILIM Enable/Disable: 0 = Trip and reset T_ILIM_BLANK after ILIM condition when V_{SENSN} < 4.75V 1 = Trip and reset T_ILIM_BLANK after ILIM condition when V_{SENSN} < 2V
ILIM[2:0]	DC Current-LImit (min) Configuration: 000 = 280mA 001 = 540mA 010 = 790mA 011 = 1040mA 100 = 1560mA 101 = 2060mA 110 = 2570mA 111 = 3060mA

Table 13. IRQ Mask Register, IRQMASK_0

IRQMASK_0								
BIT NO.	7	6	5	4	3	2	1	0
NAME	ATTACH	BUS_UV	DATA_OV	BUS_ILIM	BUS_OV	BUS_STG	T_WARN	T_SHDN
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
ATTACH	ATTACH Interrupt Enable/Disable: 0 = Interrupt disabled. 1 = Interrupt enabled.
BUS_UV	SENSN UV Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
DATA_OV	HVD+/- OV Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
BUS_ILIM	DC Current-LImit Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
BUS_OV	SENSN OV Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
BUS_STG	SENSN Short to GND Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
T_WARN	Pre-Thermal-Warning Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled
T_SHDN	Thermal-Shutdown Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled

Table 14. IRQ Mask Register, IRQMASK_1

IRQMASK_1									
BIT NO.	7		6	5	4	3	2	1	0
NAME	—	—	—	—	—	—	—	—	IN_OV
POR	—		—	—	—	—	—	—	0

BIT	BIT DESCRIPTION
IN_OV	IN Pin Overvoltage Interrupt Enable/Disable: 0 = Interrupt disabled 1 = Interrupt enabled

Table 15. Status Register, STATUS

STATUS								
BIT NO.	7	6	5	4	3	2	1	0
NAME	ATTACH	CFG_OK	—	—	—	—	—	—
POR	0	0	—	—	—	—	—	—

BIT	BIT DESCRIPTION
ATTACH	ATTACH event flag. This bit correlates directly to the state of the internal attach detection signal. 0 = No ATTACH event detected. 1 = ATTACH event detected.
CFG_OK	Device configuration status flag. CFG_OK functionality is special-order only and is pre-loaded as a '1' at startup on standard factory variants. 0 = Device is not yet configured; DC-DC is latched off. 1 = Device has been configured, normal operation allowed.

Table 16. Status/Error Register, ERROR_1

ERROR_1								
BIT NO.	7	6	5	4	3	2	1	0
NAME	ATTACH	BUS_UV	DATA_OV	BUS_ILIM	BUS_OV	BUS_STG	T_WARN	T_SHDN
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
ATTACH	ATTACH Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
BUS_UV	SENSN UV Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
DATA_OV	HVD+/HVD- OV Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
BUS_ILIM	USB DC Current-Limit Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
BUS_OV	SENSN OV Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
BUS_STG	SENSN Short to GND Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
T_WARN	Pre-Thermal Shutdown Warning Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected
T_SHDN	Thermal-Shutdown Event Flag (Cleared on Read): 0 = No event detected 1 = Event detected

Table 17. Status/Error Register, ERROR_2

ERROR_2								
BIT NO.	7	6	5	4	3	2	1	0
NAME	—	—	—	—	—	CFG_REQ	ADC_DONE	IN_OV
POR	—	—	—	—	—	0	0	0

BIT	BIT DESCRIPTION
CFG_REQ	Configuration Request Flag (Cleared on Read); CFG_REQ functionality is special-order only and does not assert on standard factory variants: 0 = No POR event detected 1 = POR event detected (system must configure device I^2C registers as desired and set CFG_OK bit in STATUS register)
ADC_DONE	Indicates ADC Conversion Complete (Cleared on Read): 0 = Conversion not complete or not in progress 1 = Conversion complete (measurements stored in USB_V and USB_I registers)
IN_OV	IN pin over-voltage event flag (Cleared on read): 0 = No event detected 1 = Event detected

Table 18. USB Output Voltage Register, USB_V

USB_V								
BIT NO.	7	6	5	4	3	2	1	0
NAME	USB_V[7:0]							
POR	0							

BIT	BIT DESCRIPTION
USB_V[7:0]	SENSN Output-Voltage Value Sampled by ADC Upon Request. V_{SENSN} = (7.92/256) x USB_V (volts), when VOUT[2:0] = 000

Table 19. USB Output Current Register, USB_I

USB_I								
BIT NO.	7	6	5	4	3	2	1	0
NAME	USB_I[7:0]							
POR	0							

BIT	BIT DESCRIPTION
USB_I[7:0]	DC Output Current value sampled by ADC upon request. DC Current = ((0.1/256) x USB_I)/R_{SENSE} (amperes)

Slave Address

Once the device is enabled, the I2C slave address is set by the CONFIG1 pin.

The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the devices after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 11). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to register address, one byte of data to the command register, and a STOP condition. Figure 12 illustrates the proper format for one frame.

Read Data Format

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to register address, restart condition, the slave address with read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 12 illustrates the proper format for one frame.

I2C Configuration and Control

Interrupt Handling

The ICs' $\overline{\text{ATTACH}}$ pin functions as an interrupt ($\overline{\text{INT}}$) for I2C variants. The $\overline{\text{INT}}$ pin asserts on interrupts based on the configuration of the IRQMASK_0 and IRQMASK_1 registers. Interrupt configuration allows the $\overline{\text{INT}}$ pin to assert any of the featured fault detections, as well as on device attach/detach, and for USB voltage/current ADC conversion completion.

Register Map

The I2C variants of the ICs allow full control of device features through the use of 11 8-bit registers. Stand-alone variants preload the SETUP_ registers from the resistors populated on the CONFIG1—CONFIG3 pins as detailed in the *Applications Information* section.

Applications Information

DC-DC Switching-Frequency Configuration and Synchronization

The I2C variant allows for digital programming of the switching frequency using the SETUP_2 register (see Table 10). The stand-alone version offers similar frequnecy selection using the CONFIG1 resistor. See Table 6 for resistor selection.

The device can be syncronized with other devices by connecting an external clock to the SYNC pin. Alternatively, the device can be configured so that the SYNC pin outputs the internal clock, making the ICs the master clock.

The choice of switching frequency dominates the efficiency, component selection, thermal performance, and EMI. A high switching frequency allows for smaller compo-nents and solution size, but increases switching losses and decreases overall efficiency. Operation between 500kHz and 1.8MHz is not recommended to avoid AM band interference.

DC-DC Input Capacitor Selection

The input capacitor reduces the peak currents drawn from the upstream power source and is a determining factor in the input-voltage ripple. The input capacitor RMS current requirement (I_{RMS}) is defined by Equation 2.

Equation 2:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{SENSP}\left(V_{SUPSW} - V_{SENSP}\right)}}{V_{SUPSW}}$$

I_{RMS} has a maximimum value when the input voltage equals twice the output voltage (V_{SUPSW} = 2 x V_{SENSP} so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$

For long-term reliability, select an input capacitor that exhibits less than 10°C self-heating temperature rise at the RMS current.

The input-voltage ripple is determined by the input capacitance (V_C), and the input capacitor ESR (V_{ESR}). Use low-ESR ceramic capacitors with high ripple-current capabil-

ity. Input voltage ripple can be estimated by the equations shown in Equation 3.

Equation 3:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta IL}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUPSW} - V_{SENSP}) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ where } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

Bypass SUPSW with 10µF of ceramic capacitance close to the SUPSW and PGND pins. Minimize the PCB current loop area to reduce EMI. Bypass SUPSW with 47µF of bulk electrolytic capacitance to dampen line transients.

DC-DC Output Capacitor Selection

The minimum required output capacitance depends on the maximum operating output voltage, the maximum device current capability, as well as the error-amplifier voltage gain. The output filter capacitor determines the output-voltage ripple, load-transient response, and the converter's stability margin.

To ensure stability and compliance with the USB and Apple specifications, follow the recommended output filters listed in Table 20. For proper functionality, a minimum amount of ceramic capacitance must be used regardless of f_{SW}. Additional capacitance for lower switching frequencies can be low-ESR electrolytic types (< 0.25Ω).

DC-DC Inductor Selection

Three key parameters must be considered when selecting an inductor: inductance value (L), saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select an inductor value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A small LIR will reduce the RMS current in the output capacitor and results in a small output-voltage ripple, but requires a larger inductor. A good compromise between size and loss is a 35% LIR. Determine the inductor value using Equation 4

Equation 4:

$$L = \frac{V_{SENSP} \times (V_{SUPSW} - V_{SENSP})}{V_{SUPSW} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{SUPSW}, V_{SENSP}, and I_{OUT} are typical values (such that efficiency is optimum for nominal operating conditions.) Table 20 shows the recommended inductor values for various switching frequencies.

Ensure the inductor I_{SAT} is well above the buck converter's cycle-by-cycle peak current limit over all operating conditions.

Layout Considerations

Proper PCB layout is critical for robust system performance. See the MAX20037/MAX20038 EV kit data sheet for a recommended layout. Minimize the current-loop area and the parasitics of the DC-DC conversion cicuitry to reduce EMI. Place the input capacitor, power inductor, and output capacitor as close as possible to the IC. Shorter traces should be prioritized over wider traces.

A low-impedance ground connection between the input and output capacitor is required (route through the ground pour on the exposed pad). Connect the exposed pad to ground. Place multiple vias in the pad to connect to all other ground layers for proper heat dissipation (failure to do so may result in the IC repeatedly reaching thermal shutdown). Do not use separate power and analog grounds; use a single common ground. High-frequency return current flows through the path of least impedence (through the ground pour directly underneath the corresponding traces).

USB traces must be routed as a 90Ω differential pair with an appropriate keep-out area. Avoid routing USB traces near clocks and high-frequency switching nodes. The length of the routing should be minimized and avoid 90° turns, excessive vias, and RF stubs.

Table 20. Recommended Output Filters

f_{SW} (kHz)	L (µH)	RECOMMENDED C_{OUT}
2200	1.5	22µF ceramic
410	8.2	3 x 22µF ceramic
410	8.2	22µF ceramic + low-ESR 150µF electrolytic < 0.25Ω

Determining USB System Requirements

The nominal cable resistance (with tolerance) for both the USB power wire (BUS) and return GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from any inline or PCB connectors. Determin the desired operating temperatur range for the application, and consider the change in resistance over temperature.

A typical application presents a 200mΩ BUS resistance with a matching 200mΩ resistance in the ground path. In this application, the voltage drop at the far end of the captive cable is 800mV when the load current is 2A. This voltage drop requires the voltage-adjustment curcuitry of the ICs to increase the output voltage to comply with the USB and Apple specifications.

USB Loads

The ICs are compatible with both USB-compliant and non-compliant loads. A compliant USB device is not allowed to sink more then 30mA and must not present more then 10µF of capacitance when initially attached to the port. The device then begins its D+/D- connection and enumeration process. After completion of the “connect” process, the device can pull 100mA/150mA and must not present a capacitance > 10µF. This is considered the hot-inserted, USB-compliant load of 44Ω||10µF.

For non-compliant USB loads, the ICs can also support both a hot insertion and soft-start into a USB load of 2Ω||330µF.

USB Output Current Limit

The USB load current is monitored by the internal current-sense amplifier through the voltage created across R_{SENSE}. The ICs offer a digitally adjustable USB current-limit threshold. See Table 7a or Table 7b to select an appropriate register or resistor value for the desired current limit.

USB Voltage Adjustment

The DC-DC output voltage increases linearly as the voltage across R_{SENSE} increases. The slope of the output voltage increases as the GAIN[4:0] register value is incre-mented (see Figure 13). Gain refers to the bit-weight of the GAIN[4:0] register in mΩ, as listed in Table 10. Gain should be selected such that it compensates for the total system resistance in addition to the buck converter’s load regulation.

The ideal gain bit-weight for an application is given by the equation below. Select a register setting that most closely matches the ideal gain.

$$GAIN = R_{CABLE} + R_{SENSE} + R_{PCB} + R_{LR}$$

where R_{CABLE} is the round-trip resistance of the USB cable, R_{LR} is the buck converter’s load regulation expressed in mΩ, and R_{PCB} is the resistance of any additional VBUS parasitics (i.e., VBUS PCB trace, USB connector, and any VBUS ferrites).

The device has a maximum amount of allowable voltage adjustment which occurs when V_{SENSE} exceeds the threshold. The load current at which this occurs will depend on the value of R_{SENSE}. When R_{SENSE} is 33mΩ, max adjustment will be reached as I_{LOAD} exceeds 2.9A (as in Figure 13). When the load current increases beyond that threshold, the output voltage begins to drop per the load-regulation specification.

Selecting a Current-Sense Resistor

The external current-sense resistor (R_{SENSE}) is critical for accurate current-limit, voltage-adjustment, attach-detection, and ADC measurement. Select a resistor with high precision and low temperature variation (ppm). It is highly recommended that designs use a resistor with an exact value of 33mΩ. Since the current limit and voltage adjustment are selected digitally (there are a discrete number of levels), changing this value also changes the possible current-limit thresholds, the voltage-adjustment compensation, and the attach threshold. The specifications in the register and resistor tables will need to be scaled accordingly.

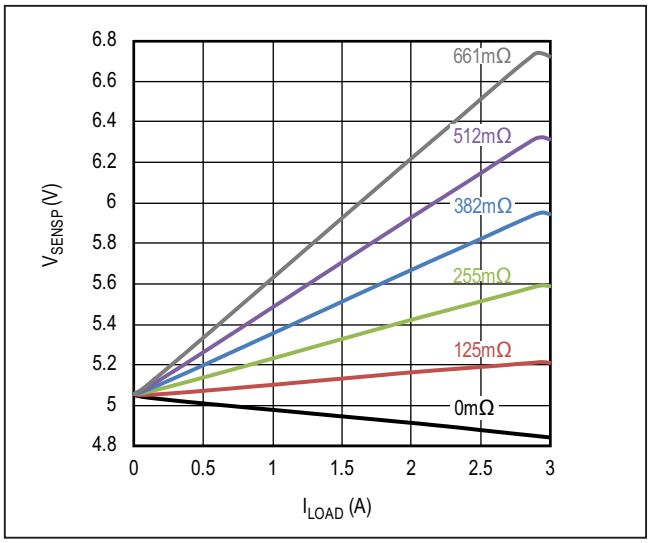

Figure 13. Increase in SENSP vs. USB Current

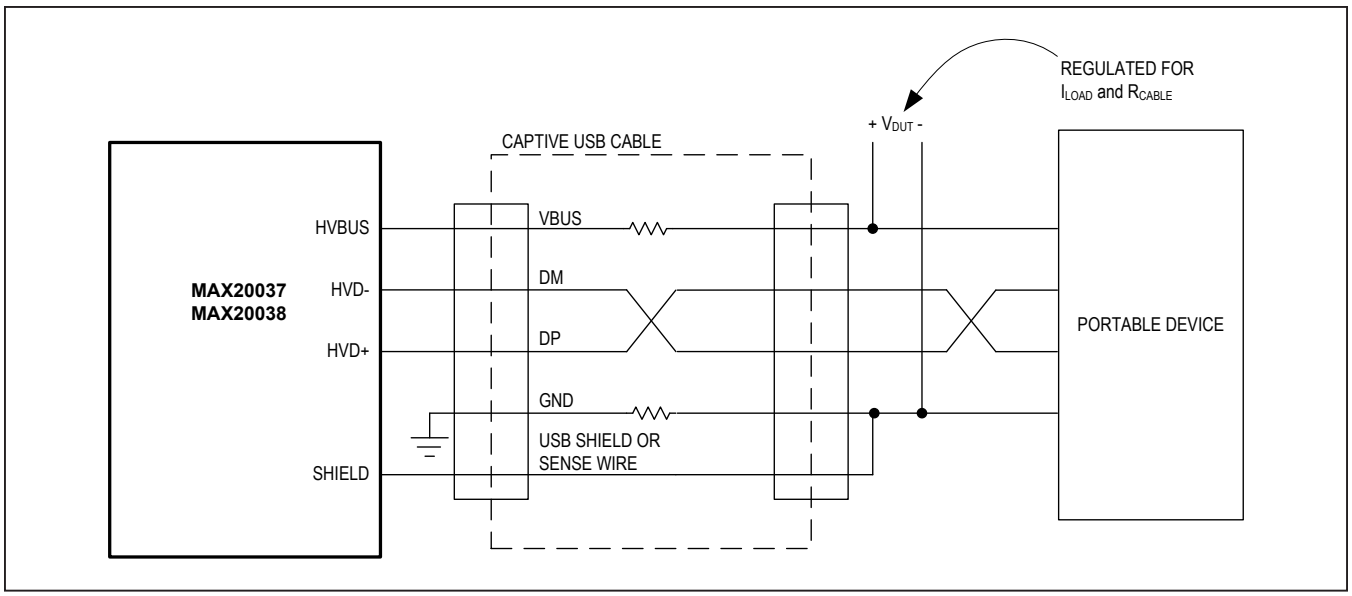

Figure 14. Remote Cable-Sense Diagram

Remote Cable Sense (Shield Function)

The ICs have the ability to automatically set the required voltage adjustment, regardless of the cable resistance. This allows for the use of multiple cables, without any difference in the circuit design. This functionality requires the ability to sense the voltage at the remote ground pin of the captive cable. This can be accomplished by tying the cable shield to the remote ground, then connecting the cable shield to the SHIELD pin of the IC. Alternatively, an additional SENSE wire can be used to connect to the remote ground. See Figure 14 for a system diagram.

When using the shield function, additional voltage adjustment must be set using the GAIN[4:0] register. The ideal GAIN bit weight should be set such that the buck's load regulation, PCB resistances, and differences between the cable's V_{BUS} and GND resistances are compensated for. Select a register setting that most closely matches the ideal GAIN.

$$GAIN = R_{SENSE} + R_{LR} + R_{PCB} + (R_{VBUS} - R_{GND})$$

Where R_{LR} is the buck converter's load regulation expressed in mΩ and R_{PCB} is the resistance of the V_{BUS} PCB trace, the USB connector, and any V_{BUS} ferrites. R_{VBUS} and R_{GND} refer to the resistance of the individual current-carrying paths through the captive cable.

The signal on the SHIELD pin must be bandwidth-limited to support load transients with capacitive loads. If overvoltage protection above the absolute maximum rating is required, it should be achieved with an external clamp. Contact the Maxim applications team for support.

Connect the SHIELD pin high to disable the remote feedback functionality.

Tuning of USB Data Lines

USB HS mode requires careful PCB layout with 90 controlled differential impedance-matched traces of equal lengths with no stubs or test points. Tuning components may not be necessary for the low-voltage, high-bandwidth MAX20037 variant; however, it is important to include these components for the MAX20038 high-voltage variant. All PCB designs are recommended to include pads that allow LC components to be mounted on the data lines, so tuning can easily be performed later if required. Tuning components should be placed as close as possible to the device's data pins, on the same layer of the PCB as the device. The proper configuration of the tuning components is shown in Figure 15; Figure 16 shows the reference eye diagram used in the test setup. Figure 17 shows the MAX20037 low-voltage eye diagram on the standard EV kit, with no tuning components; Figure 19 shows the MAX20038 high-voltage eye diagram on the standard EV kit, with standard tuning components. Tuning inductors should be high-Q wire-wound inductors. Contact Maxim's application team for assistance with the tuning process for your specific application.

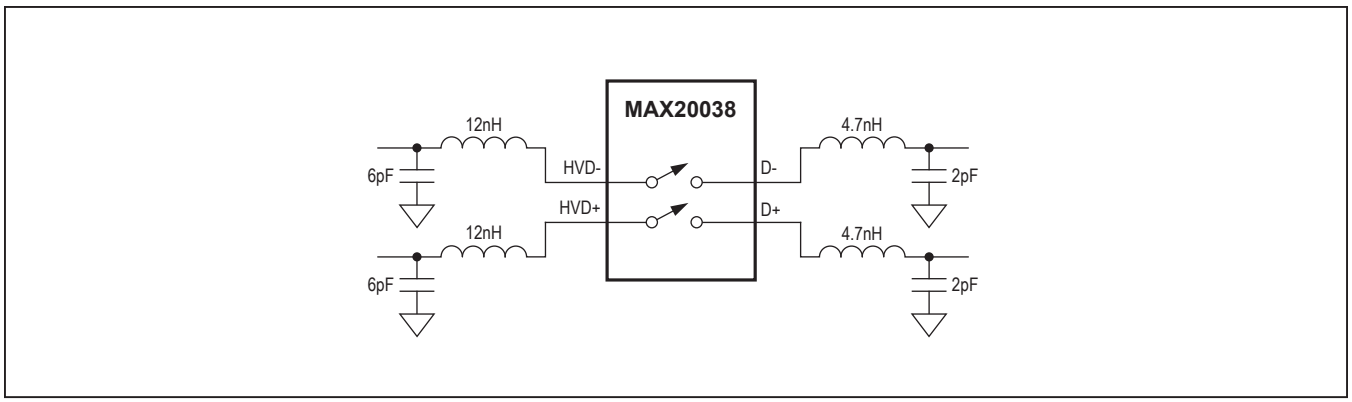

Figure 15. Tuning of Data Lines (MAX20038)

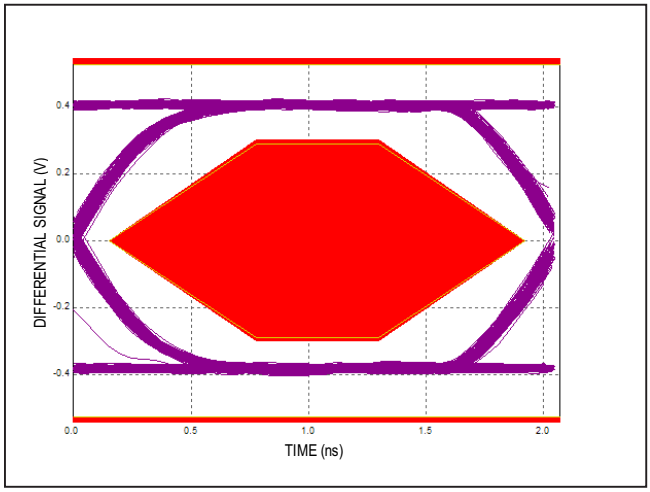

Figure 16. Near-Eye Diagram (with No Switch)

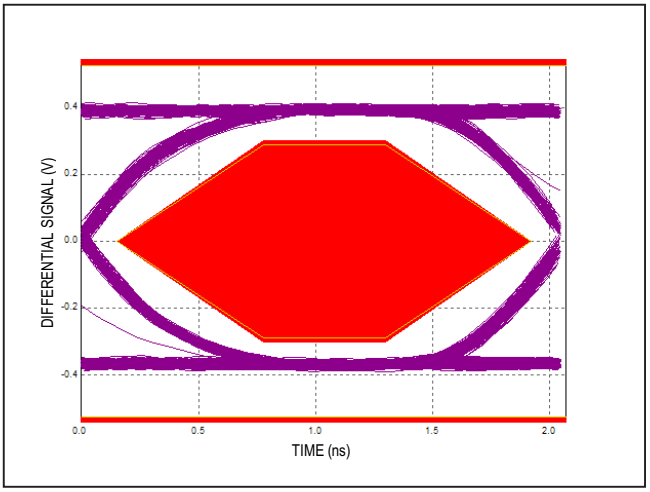

Figure 17. Untuned Near-Eye Diagram (with MAX20037)

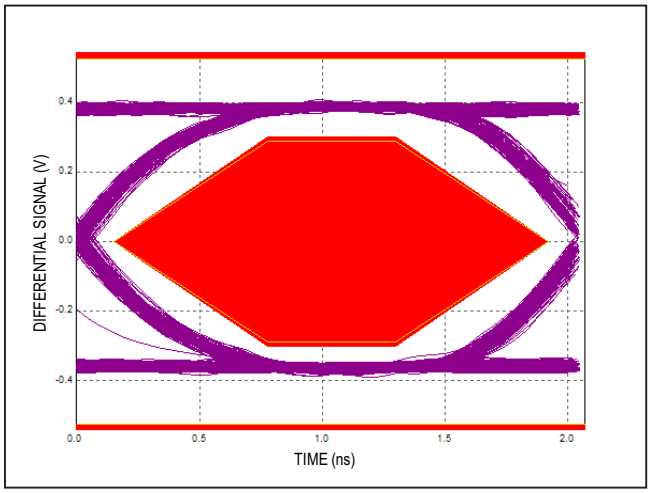

Figure 18. Untuned Near-Eye Diagram (with MAX20038)

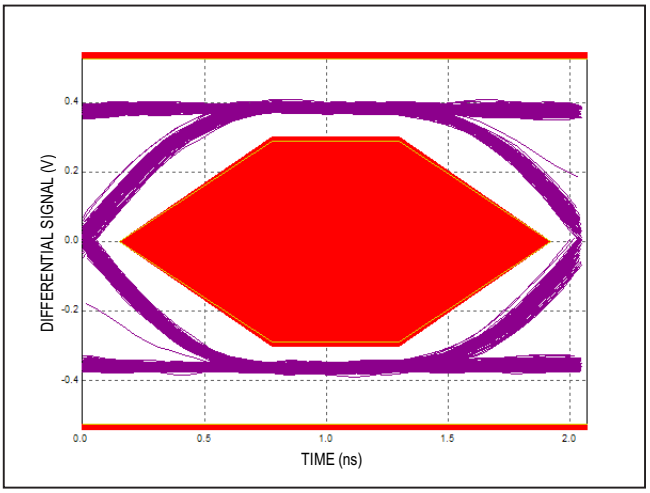

Figure 19. Tuned Near-Eye Diagram (with MAX20038)

USB Data Line Common-Mode Choke Placement

Most automotive applications use a USB-optimized common-mode choke to mitigate EMI signals from both leaving and entering the module. Optimal placement for this EMI choke is at the module's USB connector. This common-mode choke does not replace the need for the tuning inductors previously mentioned.

ESD Protection

The high-voltage MAX20038 variant requires no external ESD protection, but external ESD-protection diodes are required when using the low-voltage MAX20037 variant. All Maxim devices incorporate ESD- protection structures to protect against electrostatic discharges encountered during handling and assembly. After an ESD event, the ICs continue to work without latchup, while other competing solutions can latch up and require the power to be cycled. When used with the configuration shown in the *Typical Operating Circuit*, the ICs are characterized for protection to the following limits:

1) ±15kV ISO 10605 Air Gap (330pF, 2kΩ)
2) ±8kV ISO 10605 Contact (330pF, 2kΩ)
3) ±15kV IEC 61000-4-2 Air Gap (150pF, 330Ω)
4) ±8kV IEC 61000-4-2 Contact (150pF, 330Ω)
5) ±15kV ISO 10605 Air Gap (330pF, 330Ω)
6) ±8kV ISO 10605 Contact (330pF, 330Ω)

Note: All application-level ESD testing is performed on the standard evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body Model

Figure 20 shows the Human Body Model and Figure 22 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX20037/MAX20038 help users design equipment that meet Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 21), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 23 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

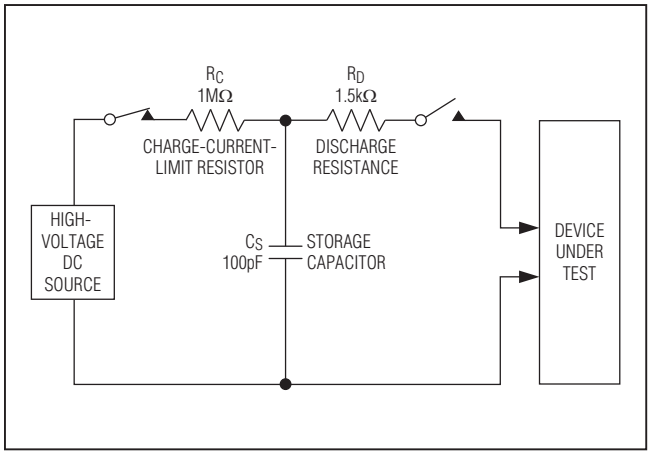

Figure 20. Human Body ESD Test Model

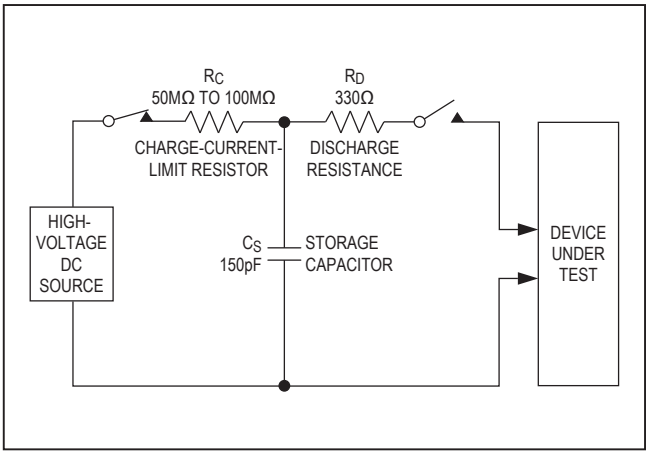

Figure 21. IEC 61000-4-2 ESD Test

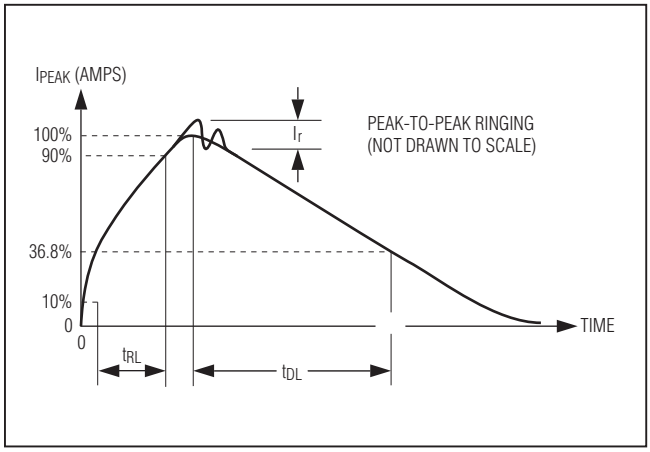

Figure 22. Human Body Current Waveform

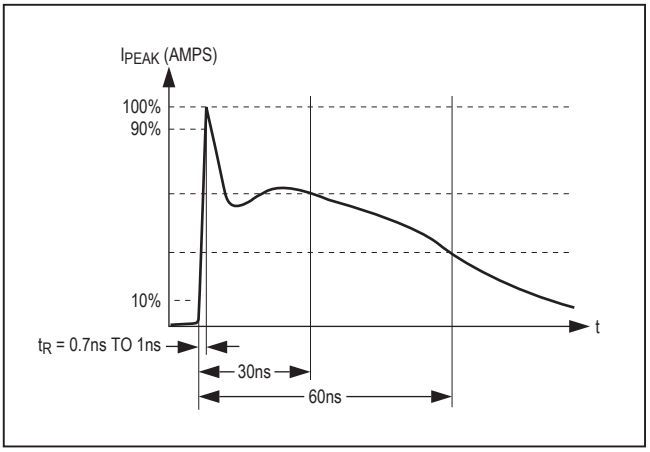

Figure 23. IEC 61000-4-2 ESD Generator Current Waveform

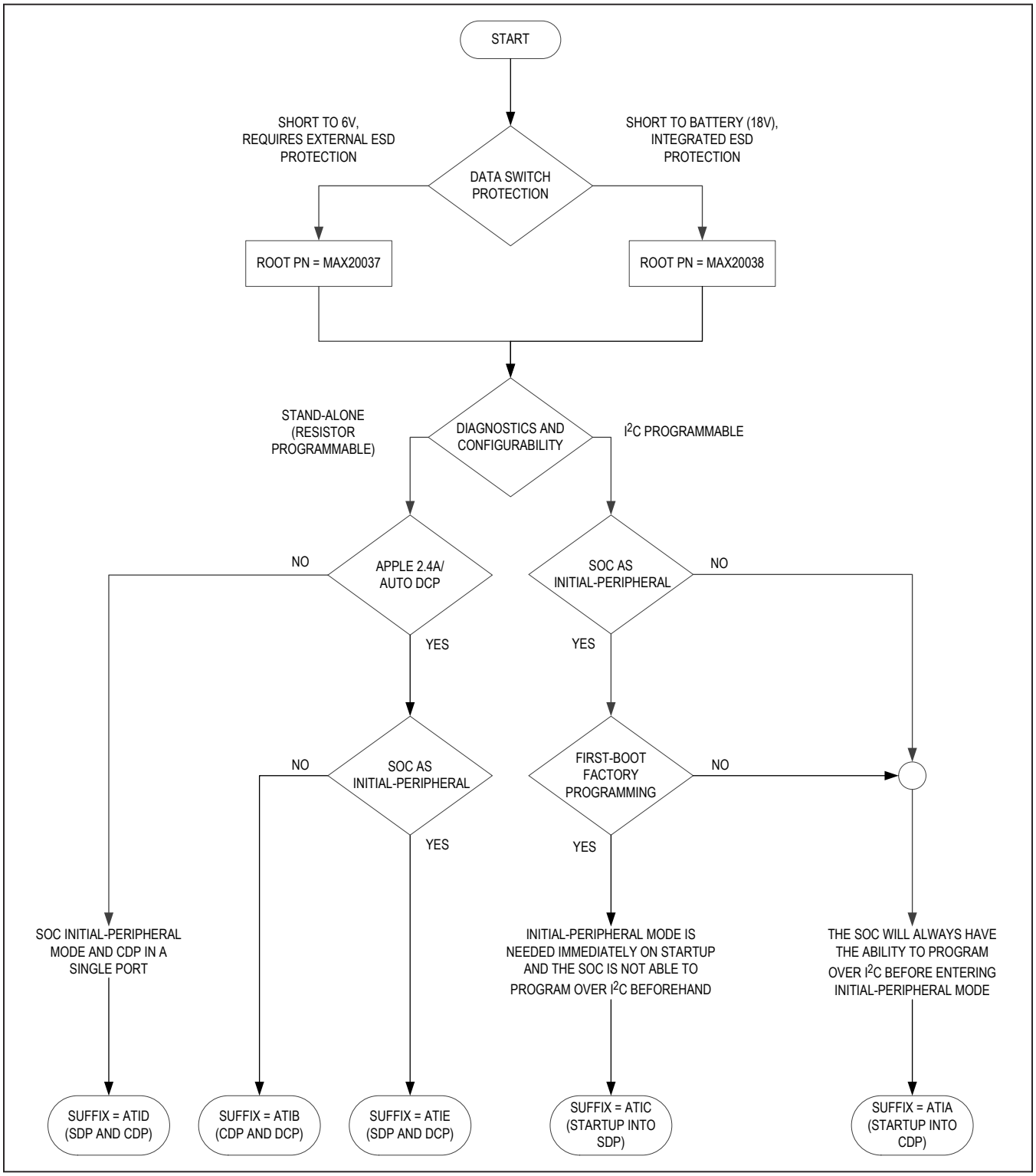

Figure 24. Selection Guide

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DATA-LINE VOLTAGE GRADE	STARTUP MODE (CDP/DCP pin = 0)	I²C
MAX20037ATIA/V+	-40°C to +125°C	28 TQFN-EP*	Low Voltage	Auto-CDP	Yes
MAX20037ATIB/V+	-40°C to +125°C	28 TQFN-EP*	Low Voltage	Auto-CDP	No
MAX20037ATIC/V+	-40°C to +125°C	28 TQFN-EP*	Low Voltage	HS Mode	Yes
MAX20037ATID/V+	-40°C to +125°C	28 TQFN-EP*	Low Voltage	HS Mode	No
MAX20037ATIE/V+	-40°C to +125°C	28 TQFN-EP*	Low Voltage	HS Mode	No
MAX20038ATIA/V+	-40°C to +125°C	28 TQFN-EP*	High Voltage	Auto-CDP	Yes
MAX20038ATIB/V+	-40°C to +125°C	28 TQFN-EP*	High Voltage	Auto-CDP	No
MAX20038ATIC/V+	-40°C to +125°C	28 TQFN-EP*	High Voltage	HS Mode	Yes
MAX20038ATIC/VY+	-40°C to +125°C	28 SWTQFN-EP*	High Voltage	HS Mode	Yes
MAX20038ATID/V+	-40°C to +125°C	28 TQFN-EP*	High Voltage	HS Mode	No
MAX20038ATIE/V+	-40°C to +125°C	28 TQFN-EP*	High Voltage	HS Mode	No

Note: *For variants with different options, contact factory.*

/V+ denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
Y = Side-wettable (SW) package.
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS