MAX20070/MAX20070B

Integrated TFT Power Supplies and LED Backlight Drivers

General Description

The MAX20070/MAX20070B are highly integrated power supplies and LED backlight drivers for automotive TFT-LCD applications. The devices integrate one buck-boost converter, one boost converter, two gate-driver supplies, and a boost/SEPIC converter that can power one to two strings of LEDs in the display backlight.

The source-driver power supplies consist of a boost converter and an inverting buck-boost converter that can generate voltages up to +15V and -15V. Both source-driver power supplies can deliver up to 100mA. The positive source-driver supply regulation voltage (V_{POS}) is set by connecting an external resistor-divider on FBP. Connecting the FBP pin to ground sets the regulation voltage (V_{POS}) to +6.5V. The negative source-driver supply voltage (V_{NEG}) is always tightly regulated to -V_{POS} within ±50mV. The source-driver supplies use an input voltage from 2.7V to 5.5V to generate the output voltages.

The gate-driver power supplies consist of regulated charge pumps that generate up to +22V and -22V and can deliver up to 3mA each. The regulation voltage (V_{GVDD}) on the positive charge pump is set by a resistor-divider on FBPG; the regulation voltage (V_{GVEE}) on the negative charge pump is set by a resistor-divider on FBNG.

The ICs feature a dual-string LED driver that operates off a separate input voltage (V_{BATT}) and can power up to two strings of LEDs with 160mA (max) of current per string.

The startup and shutdown sequences for all power domains are controlled using one of the seven preset modes that are selectable through a resistor on SEQ.

The MAX20070/MAX20070B are available in a 32-pin, 5mm x 5mm TQFN package with an exposed pad, and operate over the -40°C to +105°C ambient temperature range.

Applications

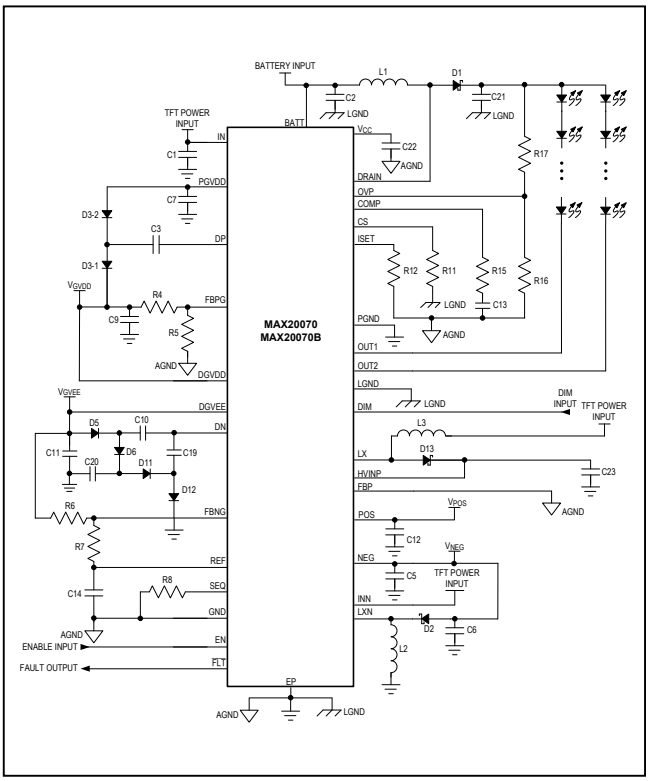
- Automotive Dashboards
- Automotive Central Information Displays
- Automotive Head-Up Displays
- Automotive Navigation Systems

Benefits and Features

- Integrates Both TFT Power Supplies and LED Backlight Driver in One IC, Reducing Component Count
- Alleviates EMI Due to Spread Spectrum on Both Source Driver Supplies and LED Driver
- 10000:1 Dimming Ratio at 200Hz Dimming Frequency
- Available in a 32-Pin (5mm x 5mm) TQFN with an Exposed Pad for Heat Dissipation and Operates Over the -40°C to +105°C Ambient Temperature Range

Ordering Information **appears at end of data sheet.**

Simplified Operating Circuit



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Absolute Maximum Ratings

BATT to GND .....-0.3V to +52V
OUT_, DRAIN, OVP to GND.....-0.3V to +52V
IN, INN, V_{CC}, $\overline{FLT}$, DIM, CS, EN to GND .....-0.3V to +6V
COMP, ISET to GND.....-0.3V to (V_{CC} + 0.3V)
DRAIN and CS Continuous Current.....2.4A
FBPG, FBNG, REF, FBP, SEQ to GND .....-0.3V to (V_{IN} + 0.3V)
LXP, HVINP to GND.....-0.3V to +22V
PGVDD, POS to GND..... -0.3V to V_{HVINP} + 0.3V
NEG to GND.....-24V to +0.3V
LXN to INN .....-24V to +0.3V
DP, DN to PGND .....-0.3V to (V_{HVINP} + 0.3V)
DGVDD to GND .....-0.3V to +24V
DGVEE to GND.....-24V to +0.3V
GND to PGND.....-0.3V to +0.3V
GND to LGND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C),
Multilayer Board.....2759mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
IN Voltage Range			2.7		5.5	V
IN UVLO Threshold		Rising	2.45	2.55	2.65	V
IN UVLO Hysteresis				100		mV
IN Quiescent Current		V_{EN} = V_{GND}, V_{IN} = 3.6V		4	10	µA
IN Quiescent Current		V_{EN} = V_{IN} = 3.6V, no switching		2.2		mA
REFERENCE						
Reference Output Voltage		No load	1.234	1.25	1.266	V
Reference UVLO Threshold		REF rising		1	1.2	V
Reference UVLO Hysteresis				100		mV
Reference Load Regulation		0 < I_{REF} < 100µA		10	20	mV
Reference Line Regulation		2.7V < V_{IN} < 5.5V		2	5	mV
BOOST REGULATOR						
Output Voltage Range	V_{HVINP}		VIN		15	V
	V_{POS}		5		15	
POS Output Regulation		V_{FBP} = V_{GND}, V_{IN} = 2.7V to 5.5V, 1mA < I_{POS} < 100mA	6.37	6.5	6.63	V
Operating Frequency		Dither disabled	850	1000	1150	kHz
Frequency Dither				+0/-12		%

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Maximum Duty Cycle			90	94	98	%
FBP Regulation Voltage			1.236	1.25	1.264	V
FBP Load Regulation		1mA < I_{POS} < 100mA		-1		%
FBP Line Regulation		V_{IN} = 2.7V to 5.5V	-0.4	0	+0.4	%
Maximum Load Current		V_{IN} = 2.7V, V_{POS} = 15V		50		mA
		V_{IN} = 3V, V_{POS} = 15V		70		
FBP Input Bias Current		V_{FBP} = 1.25V, T_A = +25°C	50	120	200	nA
FBP Internal-Divider Enable Threshold		FBP rising, hysteresis = 10mV		35	100	mV
LXP On-Resistance		I_{LXP} = 0.1A		0.5	1.0	Ω
LXP Leakage Current		EN = GND, V_{LXP} = 15V			20	µA
LXP Current Limit		Duty cycle = 80%	1.0	1.2	1.4	A
Soft-Start Period		I_{LIM} ramp		5		ms
INVERTING REGULATOR						
INN Voltage Range			2.7		5.5	V
INN Quiescent Current		EN = GND, V_{INN} = 3.6V			1	µA
INN Quiescent Current		V_{EN} = V_{INN} = 3.6V		1		mA
Operating Frequency		Dither disabled (test mode only)	850	1000	1150	kHz
Frequency Dither				+0/-12		%
Oscillator Maximum Duty Cycle			90	94	98	%
V_{POS} + V_{NEG} Regulation Voltage		V_{INN} = 2.7V to 5.5V, V_{POS} = 6.5V, 1mA < I_{NEG} < 100mA, I_{POS} = no load, T_A = 0°C to +105°C	-50		+50	mV
		V_{INN} = 2.7V to 5.5V, V_{POS} = 6.5V, 1mA < I_{NEG} < 100mA, I_{POS} = no load, T_A = -40°C to +105°C	-60		+60	
		V_{INN} = 2.7V to 5.5V, V_{POS} > 6.5V, 1mA < I_{NEG} < 100mA, I_{POS} = no load, T_A = 0°C to +105°C	-80		+80	
		V_{INN} = 2.7V to 5.5V, V_{POS} > 6.5V, 1mA < I_{NEG} < 100mA, I_{POS} = no load, T_A = -40°C to +105°C	-100		+100	
Maximum Load Current		V_{IN} = 2.7V, V_{NEG} = -15V		50		mA
		V_{IN} = 3V, V_{NEG} = -15V		70		
LXN On-Resistance		INN to LXN, V_{LXN} = 0.1A		0.6	1.2	Ω

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LXN Leakage Current		V_{IN} = 3.6V, V_{LXN} = V_{NEG} = -15V, T_A = +25°C			20	µA
LXN Current Limit		Duty cycle = 80%	1.2	1.5	1.8	A
Soft-Start Period		I_{LIM} ramp		5		ms
POSITIVE CHARGE-PUMP REGULATOR						
PGVDD Operating Voltage Range	V_{PGVDD}		6		V_{HVINP}	V
HVINP-DP Current Limit			15			mA
Oscillator Frequency			300	400	500	kHz
FBPG Regulation Voltage			1.236	1.25	1.264	V
FBPG Line Regulation		V_{HVINP} = 11 to 15V		0	0.2	%/V
FBPG Input Bias Current		V_{FBPG} = 1.25V, T_A = +25°C	-100		+100	nA
DP On-Resistance High		I_{DP} = 10mA		30	60	Ω
DP On-Resistance Low		I_{DP} = -10mA		15	30	Ω
NEGATIVE CHARGE-PUMP REGULATOR						
HVINP-DN Current Limit			15			mA
Oscillator Frequency			300	400	500	kHz
FBNG Regulation Voltage			-12	0	+12	mV
FBNG Line Regulation		V_{HVINP} = 11V to 15V		0	0.2	%/V
FBNG Input Bias Current		V_{FBNG} = 0V, T_A = +25°C	-100		+100	nA
DN On-Resistance High		I_{DN} = 10mA		30	60	Ω
DN On-Resistance Low		I_{DN} = -10mA		15	30	Ω
SEQUENCE SWITCHES						
POS Output Range	V_{POS}	Tracks HVINP	V_{IN}		15	V
POS On-Resistance		(HVINP-POS), I_{POS} = 100mA		0.8	1.5	Ω
		(HVINP-POS), I_{POS} = 100mA (MAX20070GTJA/V+ and MAX200700BGTJA/V+ only)		1.6	2.8	Ω
POS Charge Current Limit		Expires after soft-start period	120			mA
		(MAX20070GTJA/V+ and MAX200700BGTJA/V+ only)	130		260	mA
POS Discharge Resistance			2	3.4	6	kΩ
POS Soft-Start Charge Time		Current mode (0A to full current limit)		5		ms
NEG Output Range	V_{NEG}		-15			V
NEG Discharge Resistance			2	3.4	6	kΩ

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGVDD On-Resistance		(HVINP-PGVDD), I_{PGVDD} = 3mA		30	60	Ω
PGVDD Current Limit		Expires when PGVDD charging is completed	15	50		mA
DGVDD Input Voltage Range			6		22	V
DGVDD Discharge Resistance			7	12	17	kΩ
DGVEE Input Voltage Range			-22		-6	V
DGVEE Discharge Resistance			7	12	17	kΩ
SEQ Bias Current		V_{SEQ} = 1V	4.75	5	5.25	µA
TFT FAULT PROTECTION						
POS Undervoltage-Fault Threshold		FBP = GND, after POS soft-start, V_{POS} falling (MAX20070GTJA/V+ and MAX20070BGTJA/V+ only)	75	80	85	%
HVINP Undervoltage-Fault Threshold		Before end of POS soft-start, V_{HVINP} falling (MAX20070GTJA/V+ and MAX20070BGTJA/V+ only)	75	80	85	%
		V_{HVINP} falling	75	80	85	%
NEG Undervoltage-Fault Threshold		V_{NEG} rising (% of POS setting)	75	80	85	%
FBP Undervoltage-Fault Threshold		V_{FBP} falling	0.95	1.00	1.05	V
FBPG Undervoltage-Fault Threshold		V_{FBPG} falling	0.95	1.00	1.05	V
FBNG Undervoltage-Fault Threshold		V_{FBNG} rising	200	250	300	mV
Undervoltage-Fault Timer				50		ms
FBP Short-Circuit Fault Threshold		V_{FBP} falling	30	40	50	%
POS Short-Circuit Fault Threshold		POS falling (% of V_{HVINP}) (MAX20070GTJA/V+ and MAX20070BGTJA/V+ only)	70	73	76	%
NEG Short-Circuit Fault Threshold		V_{NEG} rising	30	40	50	%
Short-Circuit Fault Timer				10		µs

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATT INPUT						
Input Voltage Range	V_{BATT}	(Note 3)	4.75		40	V
		V_{BATT} = V_{CC}	4.5		5.5	
Quiescent Supply Current	I_Q	V_{DIM} = 5V, V_{OVP} = 1.3V; OUT1, OUT2 open		2.6	5.2	mA
Standby Supply Current	I_{SH}	EN = GND		15	30	µA
Undervoltage Lockout	$UVLO_{BATT}$	V_{BATT} rising	4.0	4.2	4.4	V
Undervoltage-Lockout Hysteresis				170		mV
V_{CC} REGULATOR						
Output Voltage		5.75V < V_{BATT} < 40V; I_{LOAD} = 0 to 30mA; C_{VCC} = 2.2µF	4.75	5	5.25	V
Dropout Voltage		V_{BATT} = 4.75V, I_{VCC} = 30mA		0.25	0.5	V
V_{CC} Undervoltage Lockout	UVLOVCC	V_{CC} rising	3.8	4	4.2	V
V_{CC} UVLO Hysteresis				150		mV
Short-Circuit Current Limit		V_{CC} shorted to GND		80		mA
BOOST/SEPIC CONTROLLER						
Switching Frequency (MAX20070)		Dither disabled	900	1000	1100	kHz
Maximum Duty Cycle (MAX20070)	D_{MAX}		88	92	96	%
Switching Frequency (MAX20070B)		Dither disabled	1800	2000	2200	kHz
Maximum Duty Cycle (MAX20070B)			90	94	98	%
Frequency Dither				+0/-12		%
SLOPE COMPENSATION						
Slope-Compensation Peak Voltage per Cycle		Voltage ramp added to CS		0.23		V
CS LIMIT COMPARATOR						
CS Threshold Voltage	V_{CS_MAX}		250	270	290	mV
CS Input Current		0 < V_{CS} < 0.35 (drain switch on)	-1.3		+0.5	µA
ERROR AMPLIFIER						
OUT_ Regulation Voltage		V_{DIM} = 5V		0.75		V
Transconductance	g_M		340	600	880	µS
COMP Sink Current		$V_{OUT\_}$ = 2.25V, V_{COMP} = 2V	160	400	900	µA
COMP Source Current		$V_{OUT\_}$ = 0V, V_{COMP} = 1V	160	400	900	µA

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER MOSFET						
Power Switch On-Resistance				0.15	0.35	Ω
Switch Leakage Current		V_{BATT} = V_{DRAIN} = 40V, V_{DIM} = 0V			10	µA
LED CURRENT SINK						
ISET Resistance Range			9.37		75	kΩ
Full-Scale OUT_ Output Current		R_{ISET} = 9.37kΩ	153	160	167	mA
		R_{ISET} = 15kΩ	95	100	105	mA
		R_{ISET} = 30kΩ	47.5	50	52.5	mA
		R_{ISET} = 75kΩ		20		mA
ISET Output Voltage			1.225	1.25	1.275	V
Current Regulation Between Strings		$I_{OUT\_}$ = 160mA	-1.5		+1.5	%
		$I_{OUT\_}$ = 100mA	-2		+2	%
		$I_{OUT\_}$ = 50mA	-2.5		+2.5	%
OUT_ Leakage Current		V_{BATT} = 12V , V_{OUT1} = V_{OUT2} = 40V, V_{DIM} = 0V, T_A = +25°C		2.5		µA
DIM to Led Turn-On Delay		DIM rising edge to 10% rise $I_{OUT\_}$		150		ns
DIM to Led Turn-Off Delay		DIM falling edge to 10% fall $I_{OUT\_}$		50		ns
$I_{OUT\_}$ Rise Time		10% to 90% $I_{OUT\_}$		200		ns
$I_{OUT\_}$ Fall Time		90% to 10% $I_{OUT\_}$		50		ns
LOGIC INPUTS AND OUTPUTS						
DIM Input High Level			2.1			V
DIM Input Low Level					0.8	V
DIM Hysteresis				350		mV
DIM On-Time to Enter LODIM Mode				25		µs
DIM Low Delay to Enter LODIM Mode		DIM = 0		40		ms
DIM Pullup Current				5		µA
EN Input Logic High			2.1			V
EN Input Logic Low					0.8	V
EN Hysteresis				125		mV
EN Input Current			-1		+1	µA
EN Blanking Time		V_{IN} = 3.6V		7		µs

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{BATT} = 12V, Typical operating circuit as Figure 5, = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FLT}$ Output Low Voltage		I_{SINK} = 5mA			0.4	V
$\overline{FLT}$ Output Leakage current		V_{FLT} = 5.5V	-1		+1	µA
$\overline{FLT}$ Frequency for Fault Detection			0.88	1	1.12	kHz
$\overline{FLT}$ Pin Duty Cycle on LED String Fault				25		%
$\overline{FLT}$ Pin Duty Cycle on TFT Rail Fault		Fault on at least one of POS, NEG, V_{GVDD}, or V_{GVEE}		50		%
$\overline{FLT}$ Pin Duty Cycle on LED String and TFT Rail Fault		Fault on at least one of POS, NEG, V_{GVDD}, or V_{GVEE}, and LED driver		75		%
$\overline{FLT}$ Switching Frequency on Thermal-Shutdown Event		$\overline{FLT}$ is forced low		0		Hz
OVERVOLTAGE PROTECTION (OVP)						
Overvoltage Trip Threshold		V_{OVP} rising	1.20	1.25	1.30	V
Overvoltage Hysteresis				70		mV
OVP Input Bias Current		0 < V_{OVP} < 1.3V	-500		+500	nA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				160		°C
Thermal-Shutdown Hysteresis				15		°C
LED FAULT DETECTION						
LED-Shorted Fault-Indicator Threshold		Other string in regulation	3.1		5.5	V
LED String Shorted-Shutoff Threshold		Other string in regulation	6		9.5	V
Shorted LED-Detection Delay				6		µs

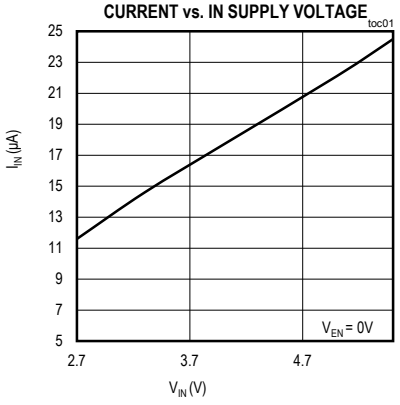
Note 2: 100% tested at T_A = +25°C. All limits over temperature are guaranteed by design, not production tested.

Note 3: The MAX20070/MAX20070B are designed for use in applications with continuous 14V operation, and meet the *Electrical Characteristics* table up to the maximum supply voltage.

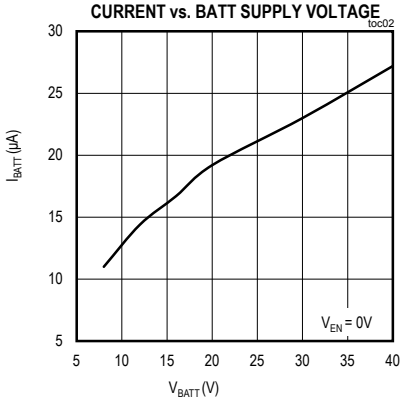
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

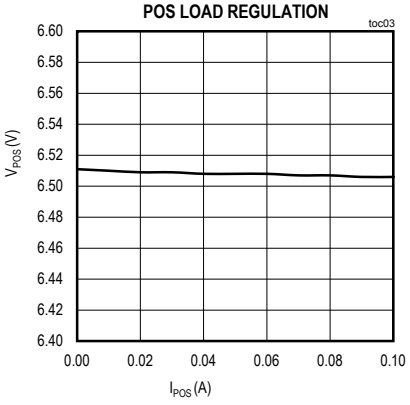
TOTAL IN SUPPLY STANDBY CURRENT vs. IN SUPPLY VOLTAGE



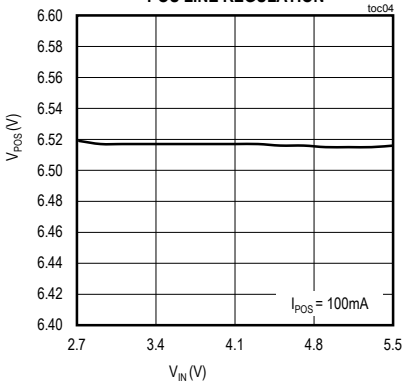
TOTAL BATT SUPPLY STANDBY CURRENT vs. BATT SUPPLY VOLTAGE



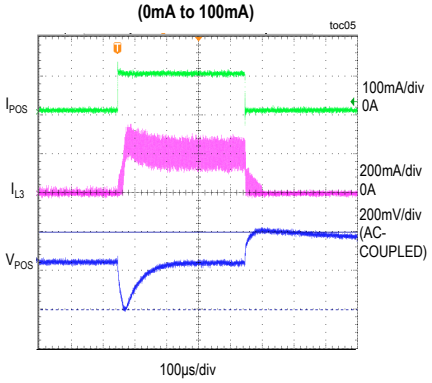
POS LOAD REGULATION



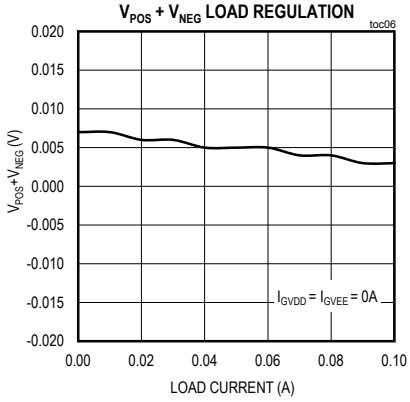
POS LINE REGULATION



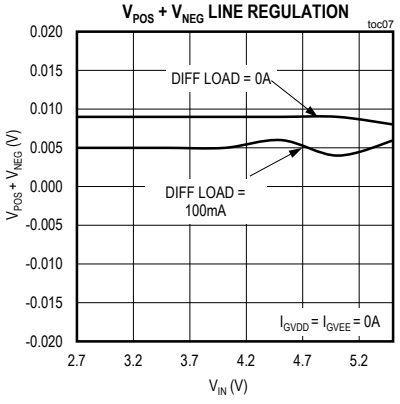
POS LOAD TRANSIENT RESPONSE (0mA to 100mA)



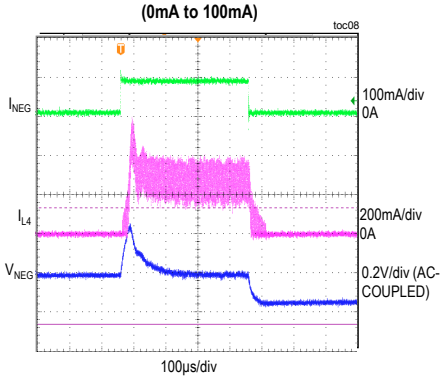
V_{POS} + V_{NEG} LOAD REGULATION



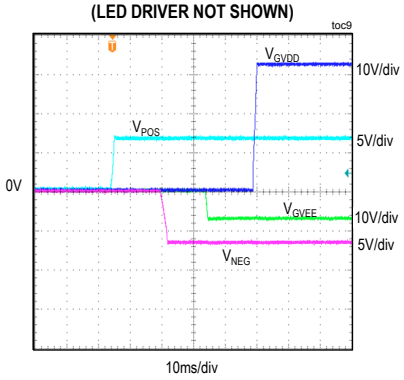
V_{POS} + V_{NEG} LINE REGULATION



NEG LOAD TRANSIENT RESPONSE (0mA to 100mA)



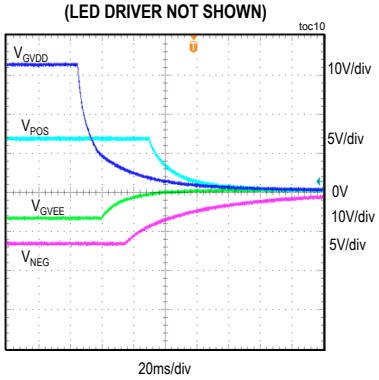
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



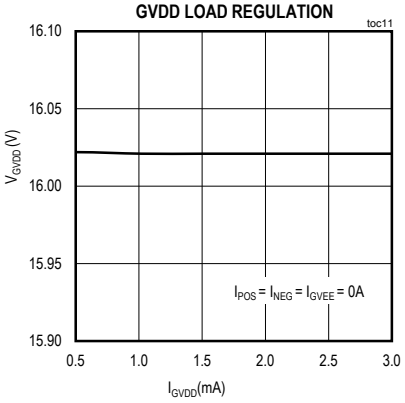
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

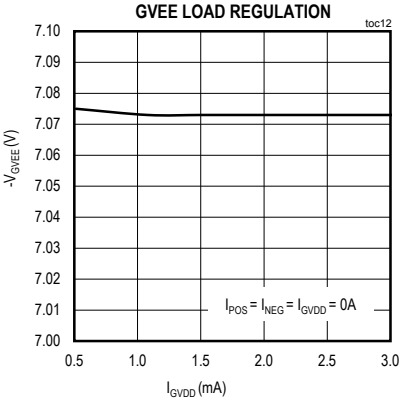
POWER SUPPLY SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



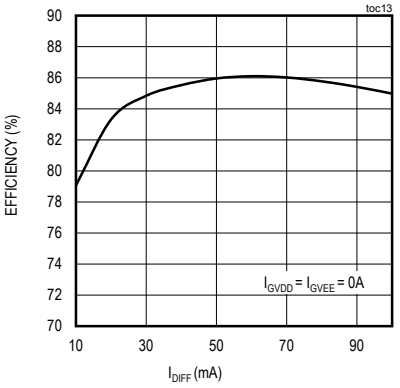
GVDD LOAD REGULATION



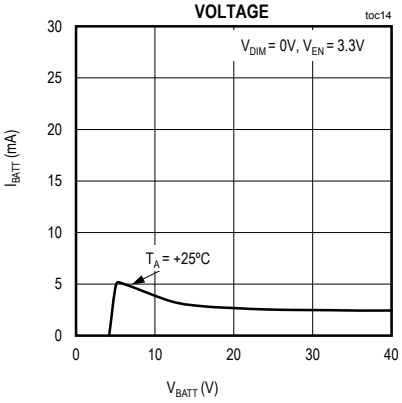
GVEE LOAD REGULATION



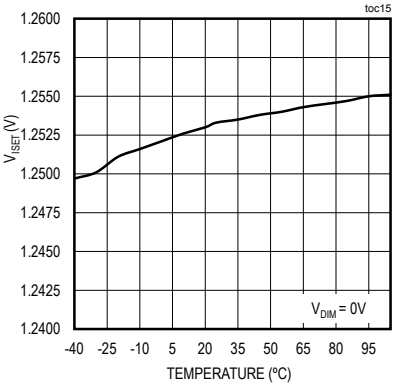
EFFICIENCY WITH DIFF LOAD FROM V_{POS} TO V_{NEG}



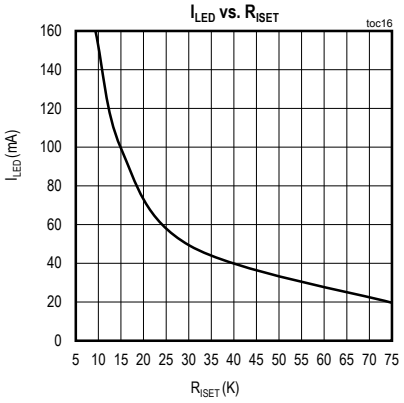
BATT SUPPLY CURRENT vs. BATT VOLTAGE



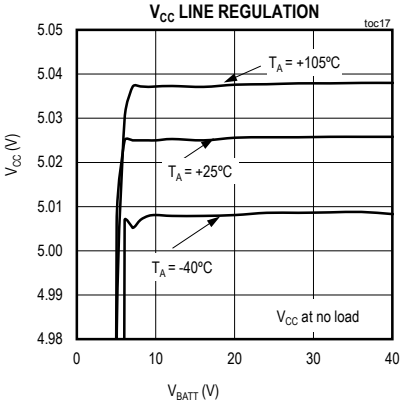
V_{ISET} vs. TEMPERATURE



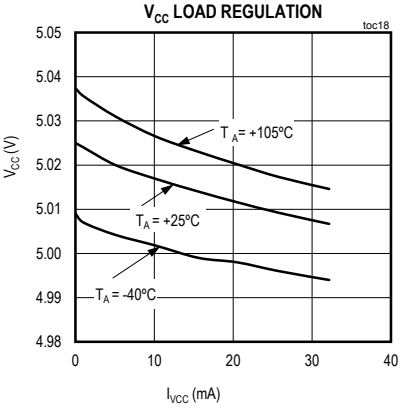
I_{LED} vs. R_{ISET}



V_{CC} LINE REGULATION



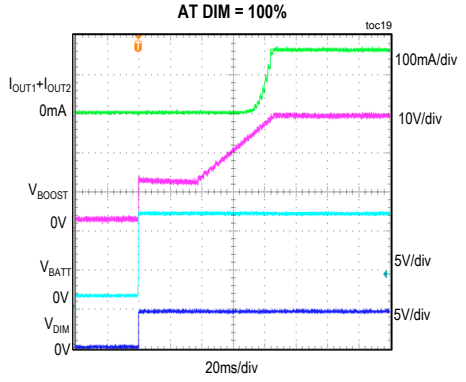
V_{CC} LOAD REGULATION



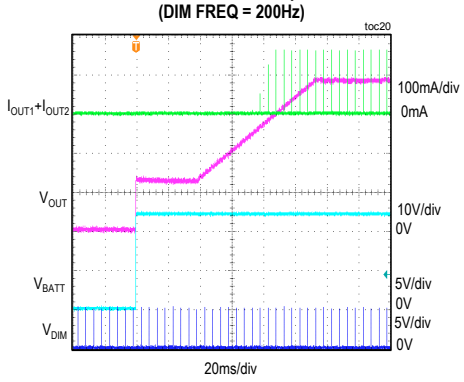
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

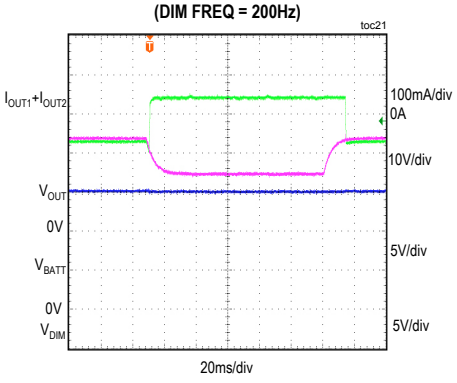
STARTUP BEHAVIOR OF LED DRIVER AT DIM = 100%



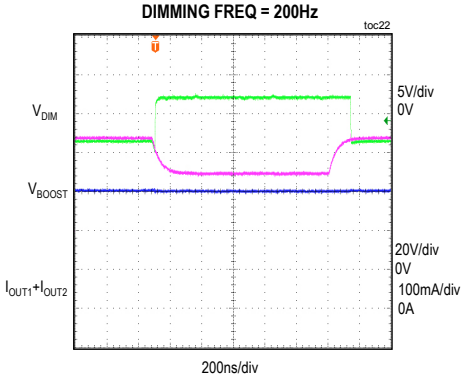
STARTUP WAVEFORM OF LED DRIVER WITH DIM PW = 25µs (DIM FREQ = 200Hz)



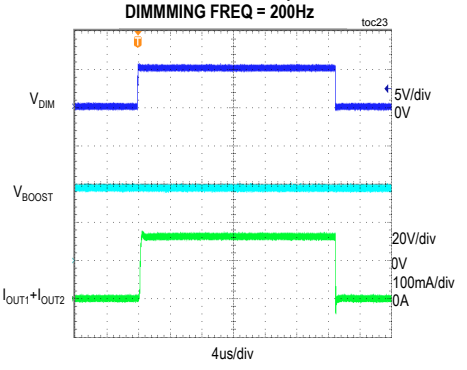
STARTUP WAVEFORM OF LED DRIVER WITH DIM DUTY = 25% (DIM FREQ = 200Hz)



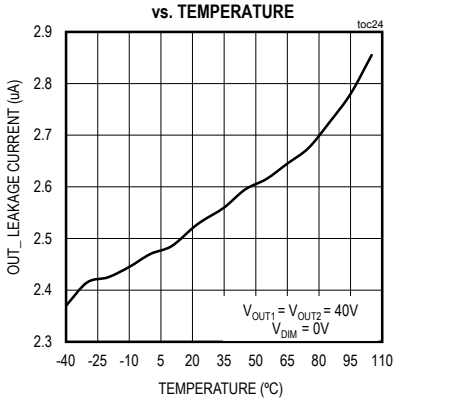
LED SWITCHING WITH DIMMING PULSE WIDTH OF 1µs DIMMING FREQ = 200Hz



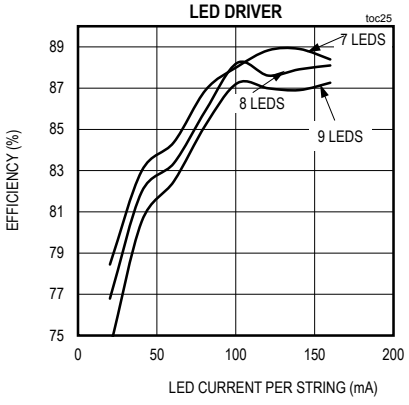
LED SWITCHING WITH DIMMING PULSE WIDTH OF 25µs DIMMMING FREQ = 200Hz



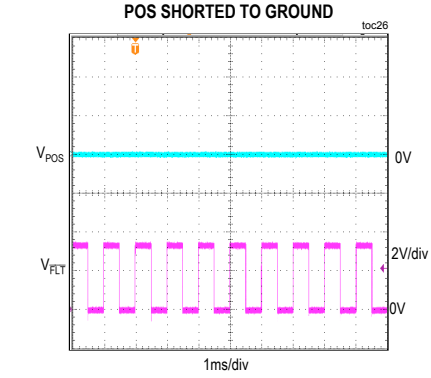
OUT_ LEAKAGE CURRENT vs. TEMPERATURE



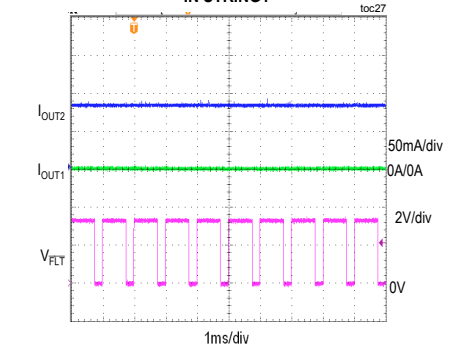
EFFICIENCY vs. LED CURRENT FOR LED DRIVER



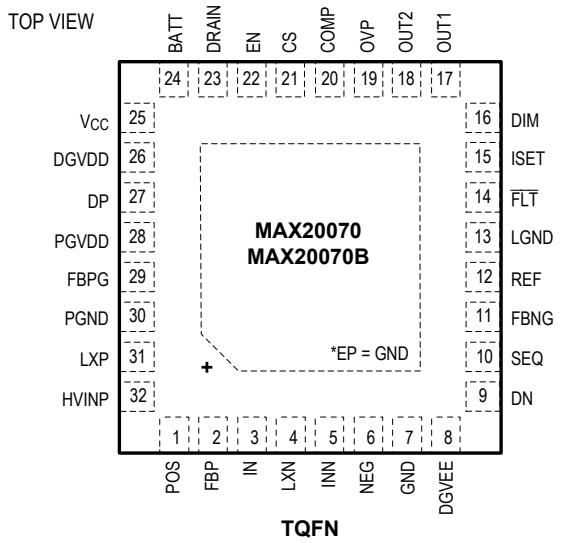
TFT FAULT POS SHORTED TO GROUND



LED FAULT CREATED BY SHORTING 3 LEDS IN STRING1



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	POS	Positive Source-Driver Output Voltage
2	FBP	Feedback Input for HVINP. Connect a resistor from this pin to ground to set the HVINP voltage.
3	IN	Supply Input. Connect a 1µF ceramic capacitor from this pin to ground for proper operation.
4	LXN	DC-DC Inverting Converter Inductor/Diode Connection
5	INN	Buck-Boost Converter Input. Connect a 1µF ceramic capacitor from this pin to ground for proper operation.
6	NEG	Negative Source-Driver Output Voltage
7	GND	Ground Connection
8	DGVEE	Connects directly to V_{GVEE} charge-pump output such that during V_{GVEE} discharge, V_{GVEE} is discharged through an internal switch connected between DGVEE and GND.
9	DN	Regulated Charge-Pump Driver for V_{GVEE}. Connect to flying capacitor.
10	SEQ	Sequencing Programming Pin. Connect appropriate resistor to ground to program desired sequencing.
11	FBNG	Feedback Input for V_{GVEE}
12	REF	1.25V Reference Output
13	LGND	Power-Ground Connection for LED Driver
14	$\overline{FLT}$	Active-Low Fault-Indicating Output
15	ISET	Full-Scale LED Current-Adjustment Pin. The resistance from ISET to GND controls the current in each LED string.
16	DIM	PWM Dimming Input
17	OUT1	LED String 1 Cathode Connection. Connect to ground if not used.

Pin Description (continued)

PIN	NAME	FUNCTION
18	OUT2	LED String 2 Cathode Connection. Connect to ground if not used.
19	OVP	LED Driver Output-Voltage-Sensing Input. This voltage is used for overvoltage protection.
20	COMP	LED Driver Switching-Converter Compensation Input. Connect an RC network from COMP to GND for compensation.
21	CS	LED Driver Switching-MOSFET Source Connection. Connect a sense resistor from CS to PGND to set the switching MOSFET current limit.
22	EN	Enable Input
23	DRAIN	Internal LED Driver Switching-MOSFET Drain
24	BATT	LED Driver Supply Input Connected to a 4.75V to 40V Supply. Bypass BATT to ground with a ceramic capacitor.
25	V_{CC}	5V Regulator Output. Place a 1µF ceramic capacitor as close as possible to V_{CC} and GND.
26	DGVDD	Connects directly to V_{GVDD} charge-pump output, such that during V_{GVDD} discharge, V_{GVDD} is discharged through an internal switch connected between DGVDD and GND.
27	DP	Regulated Charge-Pump Driver for V_{GVDD}. Connect to flying capacitor.
28	PGVDD	Slowly switches out the HVINP voltage to the positive charge pump to provide soft-start control of the V_{GVDD} output.
29	FBPG	Feedback Input for V_{GVDD}. Connect a resistor from this pin to ground to set the V_{GVDD} voltage.
30	PGND	Power-Ground Connection
31	LXP	Boost HVINP Converter Internal-Drain MOSFET Connection. Connect to external inductor and boost diode anode.
32	HVINP	Input Power for the POS Voltage Rail
—	EP	Exposed Pad. Connect to a large contiguous copper-ground plane for optimal heat dissipation. Do not use EP as the only electrical ground connection.

Typical Operating Circuits

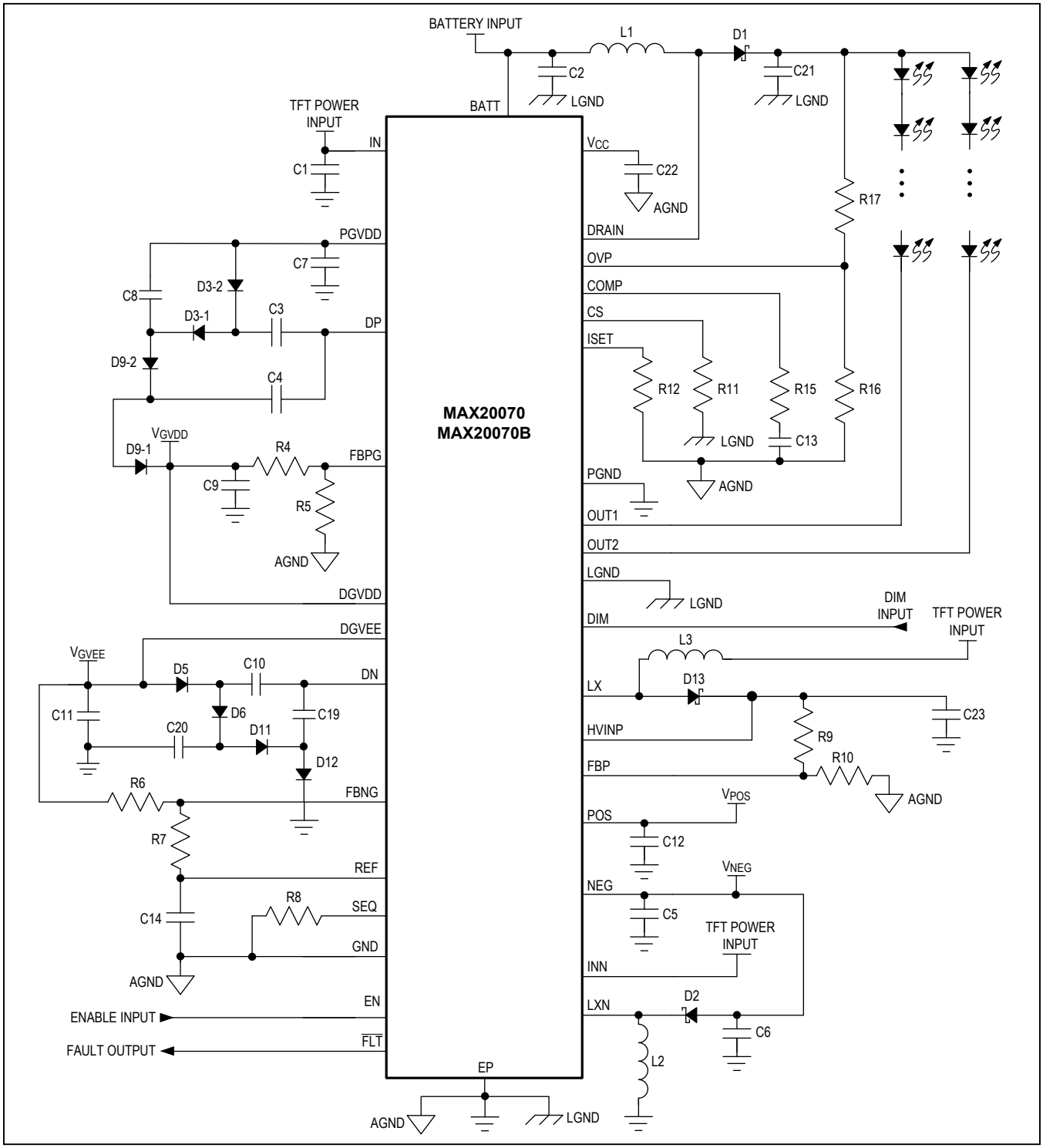


Figure 1. Simplified Operating Circuit for Boost LED Driver

Typical Operating Circuits (continued)

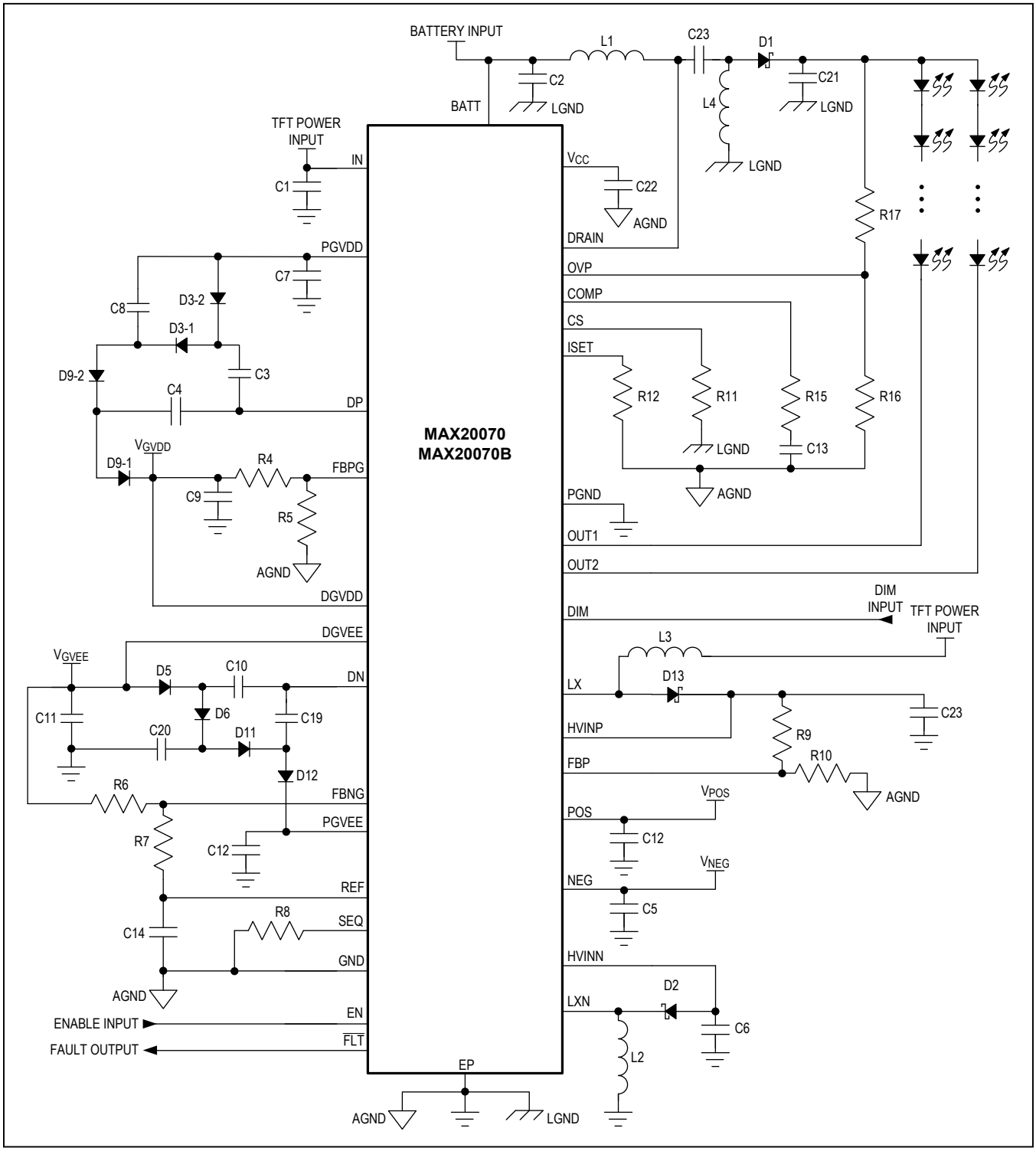


Figure 2. Simplified Operating Circuit for SEPIC LED Driver

Typical Operating Circuits (continued)

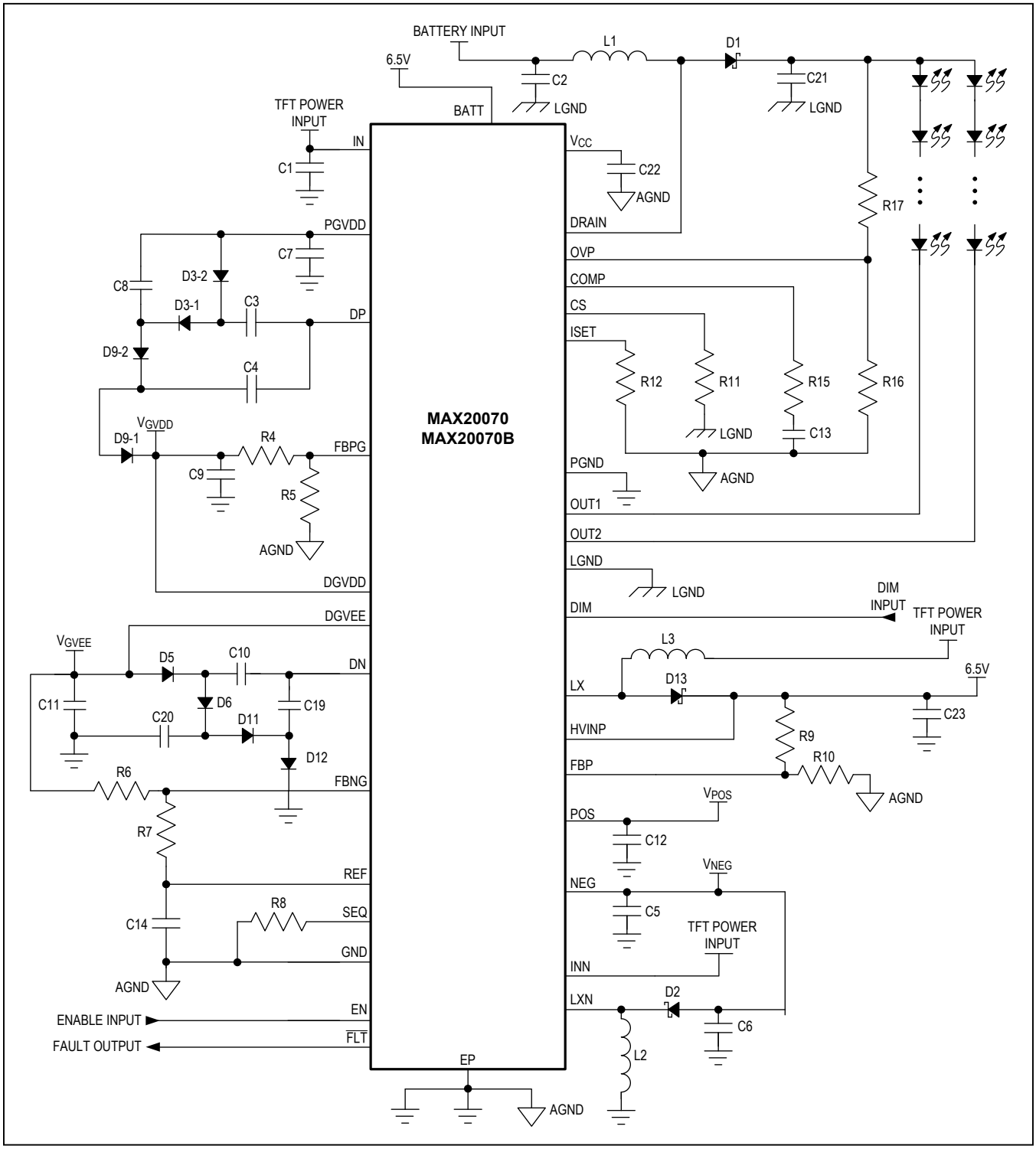


Figure 3. Simplified Operating Circuit for Coldcrank Below 4.5V

Typical Operating Circuits (continued)

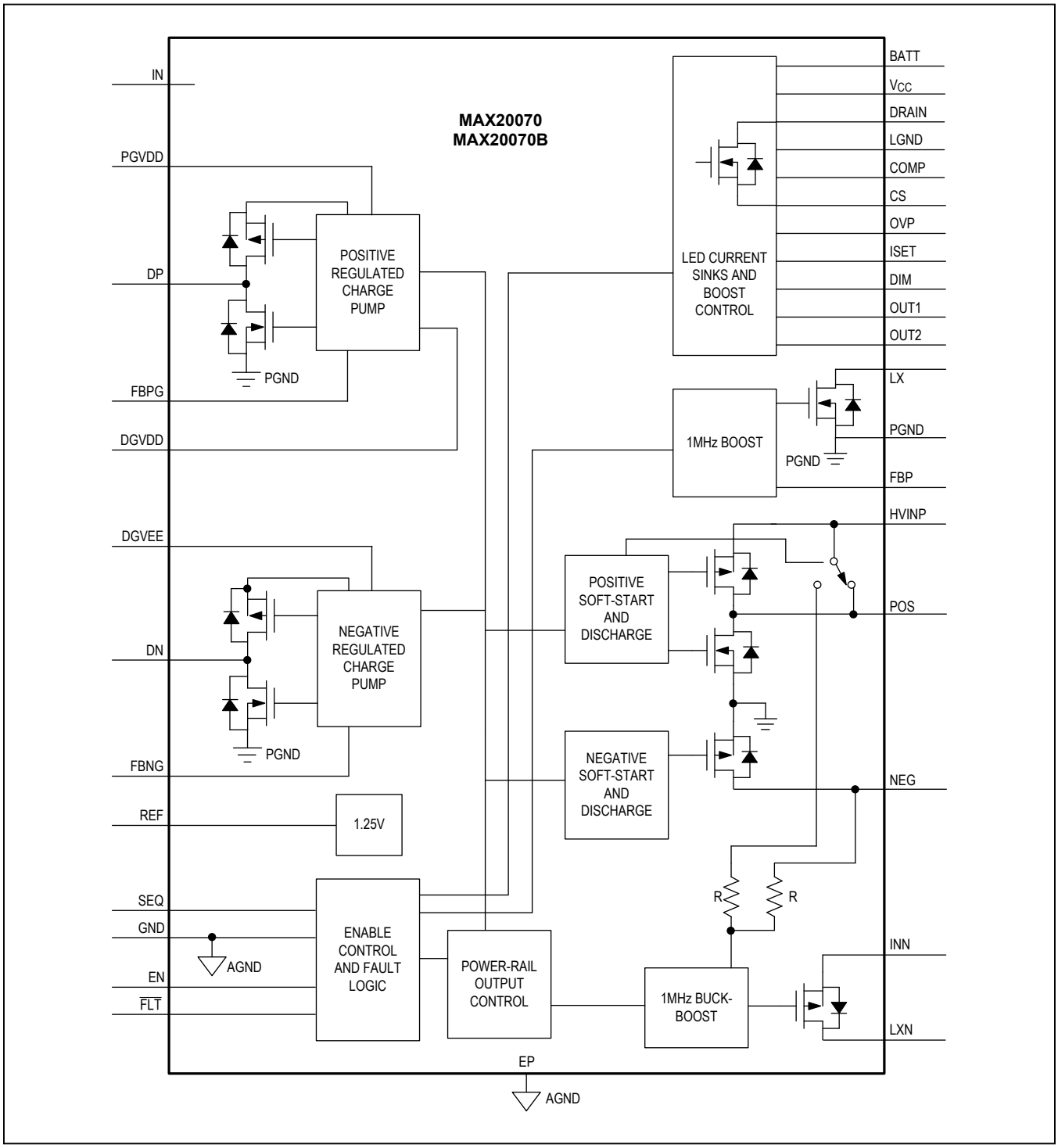


Figure 4. Functional Block Diagram

Typical Operating Circuit Schematic

The MAX20070/MAX20070B's typical operating circuit schematic shown in Figure 5 generates ±6.5V source-driver supplies at 100mA each and also generates +16V and -7V for gate-driver supplies. The current rating for the gate-driver supplies is 3mA (max) on each output. The input voltage for the TFT power section is 2.7V to 5.5V. The LED driver is a boost LED driver that operates from a 4.75V to 18V input and can withstand a 40V load dump. The LED current per string is set at 160mA and can power two strings with a 34V (max) output voltage. Table 1 lists recommended critical components and Table 2 lists contact information for the component suppliers.

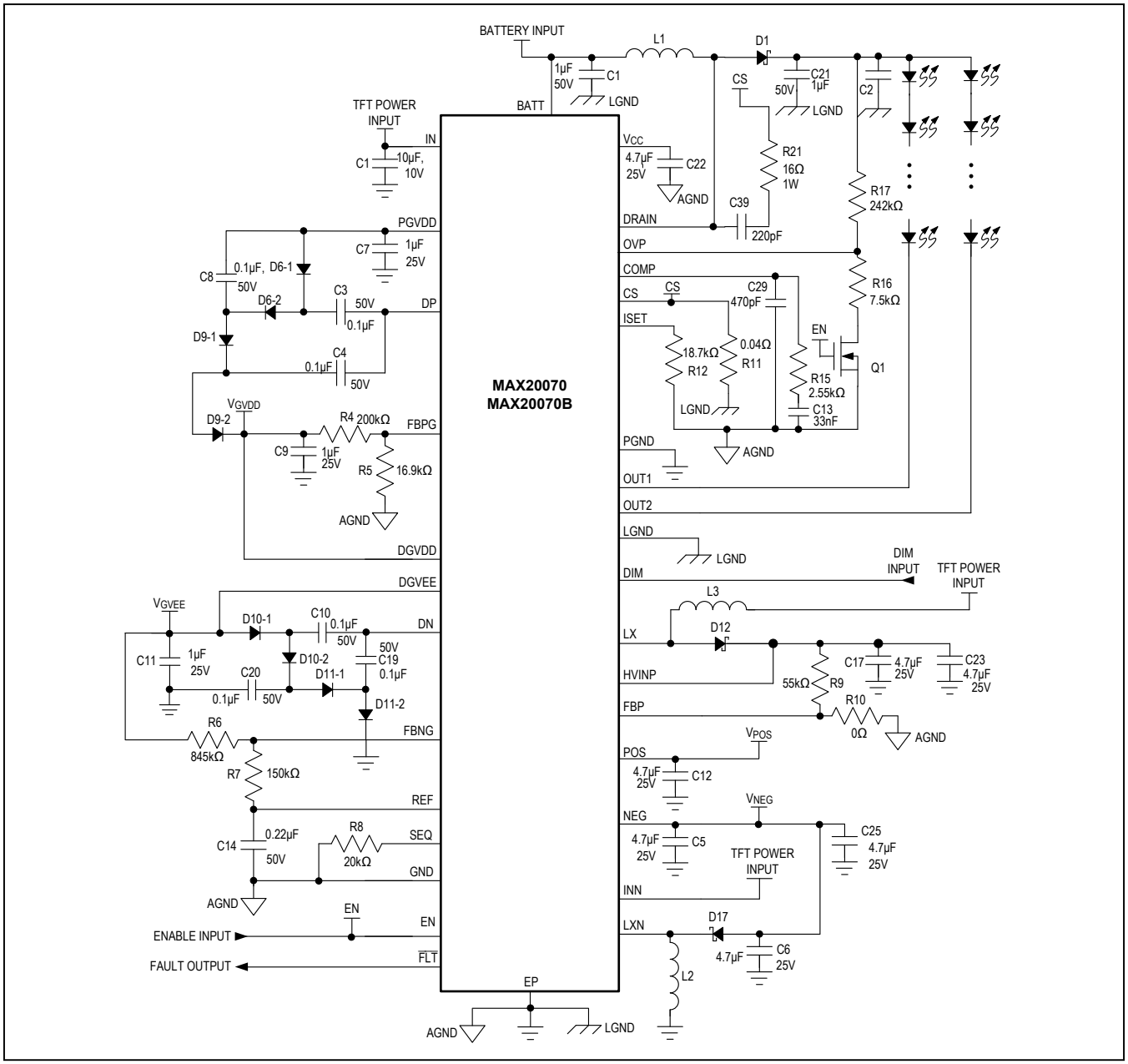


Figure 5. Typical Operating Circuit Schematic

Table 1. Component List

DESIGNATION	QTY	DESCRIPTION
C2	1	33µF, 50V hybrid conductive-polymer capacitor SUNCON 50HVH33M
D1	1	3A, 60V Schottky diode (SMB) Diodes Inc. B360B
D6, D9–D11	4	30V, 200mA dual in-series Schottky diodes (SOT323) Central Semi CBAT54SW
D12, D17	2	30V, 0.5A Schottky diodes (SOD323) Diodes Inc. B0530WS
L1	1	4.7µH inductor Coilcraft MSS1048-472
L2, L3	2	10µH inductors Coilcraft LPS4018-103
Q1	1	60V, 115mA n-channel MOSFET 2N7002

Note: *Other capacitors are surface-mount ceramic capacitors of X7R dielectric.*

Detailed Description

The MAX20070/MAX20070B are highly integrated power supplies and LED backlight drivers for automotive TFT-LCD applications. The devices integrate one buck-boost converter, one boost converter, two gate-driver supplies, and a boost/SEPIC converter that power a two-string LED driver.

The main power-supply section, consisting of the buck-boost converter, boost converter, and gate-driver supplies, operates from an available 2.7V to 5.5V supply. The boost/SEPIC converter that powers the LED drivers operates from a separate 4.75V and 40V supply voltage, making the devices ideal for automotive TFT-LCD applications. Both the buck-boost and boost converter and the LED driver have built-in spread spectrum for reducing EMI.

The boost converter provides an output voltage adjustable up to 15V (max), with a 100mA (max) output current. The buck-boost converter provides a negative output voltage that tracks the positive voltage from the boost converter.

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor	www.centralsemi.com
Coilcraft, Inc.	www.coilcraft.com
Diodes Inc.	www.diodes.com
Murata Americas	www.murataamericas.com
TDK Corp.	www.component.tdk.com
SUN Electronic Industries Corp.	www.sunelec.co.jp

There are two switching-frequency options (400kHz and 1MHz) for the boost and buck-boost converter. Both boost and buck-boost converters share a common clock. The buck-boost converter uses an internal p-channel MOSFET as the switching element, with a 100mA (max) output current. The boost converter uses an internal n-channel switching MOSFET as the switching element. With an appropriate resistor (140kΩ or 180kΩ) on the SEQ pin, the buck-boost converter can turn off completely.

The switching frequency for the LED boost/SEPIC converter is fixed at an internal clock frequency. There are three frequency options available: 400kHz, 1MHz, and 2MHz. The LED boost/SEPIC converter also has built-in spread spectrum for reduced EMI.

The LED-string channel current is adjustable from 20mA to 160mA using an external resistor. The external resistor sets all the channel currents to the same value. The devices facilitate connecting multiple strings in parallel to increase the current capability of the current sinks and also features pulsed dimming control with a minimum pulse width as low as 0.5µs through a logic-control input (DIM).

The devices provide gate-driver supplies using positive and negative charge-pump regulators, with a maximum current capability of 3mA each. Output voltage is adjustable with a maximum output of +22V on the positive charge pump and -22V on the negative charge pump.

The startup and shutdown sequences for all power domains, controlled by using one of the seven preset modes, is selectable through a resistor on the SEQ pin.

The MAX20070/MAX20070B are available in a 32-pin (5mm x 5mm) TQFN package with an exposed pad and operate over the -40°C to +105°C ambient temperature range.

Features

Additional features of the MAX20070/MAX20070B include:

- 2.7V to 5.5V input for TFT power
- 4.75V to 40V input for backlight LED driver
- Integrated 1MHz/400kHz boost and buck-boost converters for TFT power
- Integrated boost/SEPIC converter with two x 160mA LED drivers
- Adaptive voltage optimization on LED driver to reduce power dissipation in the LED current sinks
- Spread spectrum on LED driver and TFT for reduced EMI
- EN input to shut down all the converters and place part in low-quiescent-current standby mode
- Positive and negative 3mA gate-voltage regulators with adjustable output voltage
- Resistor-programmable flexible sequencing through SEQ pin

TFT Power Section

Source-Driver Power Supplies

The source-driver power supplies consist of a boost converter and an inverting buck-boost converter that generate +15V (max) and -15V (max), respectively, and can deliver up to +100mA on the positive regulator and -100mA on the negative regulator. The positive source-driver power supply's regulation voltage (V_{POS}) can be set by a resistor-divider on FBP, as shown in Figure 6, or provide 6.5V if the FBP pin is connected to ground at power-up. The positive source driver uses constant-frequency peak-current-mode control with internal fixed-slope compensation. Internal compensation stabilizes the control loop. When FBP is connected to ground, the POS regulation voltage is sensed in an internal resistor-divider from POS to ground inside the device. This determination occurs at power-up. If the resistance to ground is not zero at power-up, the device senses the FBP pin voltage and regulates this voltage to 1.25V. The negative source-driver supply voltage (V_{NEG}) is automatically tightly regulated to $-V_{POS}$ within ±50mV. V_{NEG} cannot be adjusted independently of V_{POS}. The negative source driver is a buck-boost DC-DC converter that uses peak current-mode control with internal fixed-slope compensation to regulate the output voltage. There is an internal resistor-divider from POS to NEG. The center point of this divider is regulated to 0V by the control loop for the negative source driver. The negative source driver can be turned off completely by setting the resistor between SEQ and ground to 140kΩ or 180kΩ.

A simplified block diagram of the TFT boost converter is shown in Figure 6. There is an internal error amplifier with a g_M = 23µS that has FBP and REF = 1.25V as inputs.

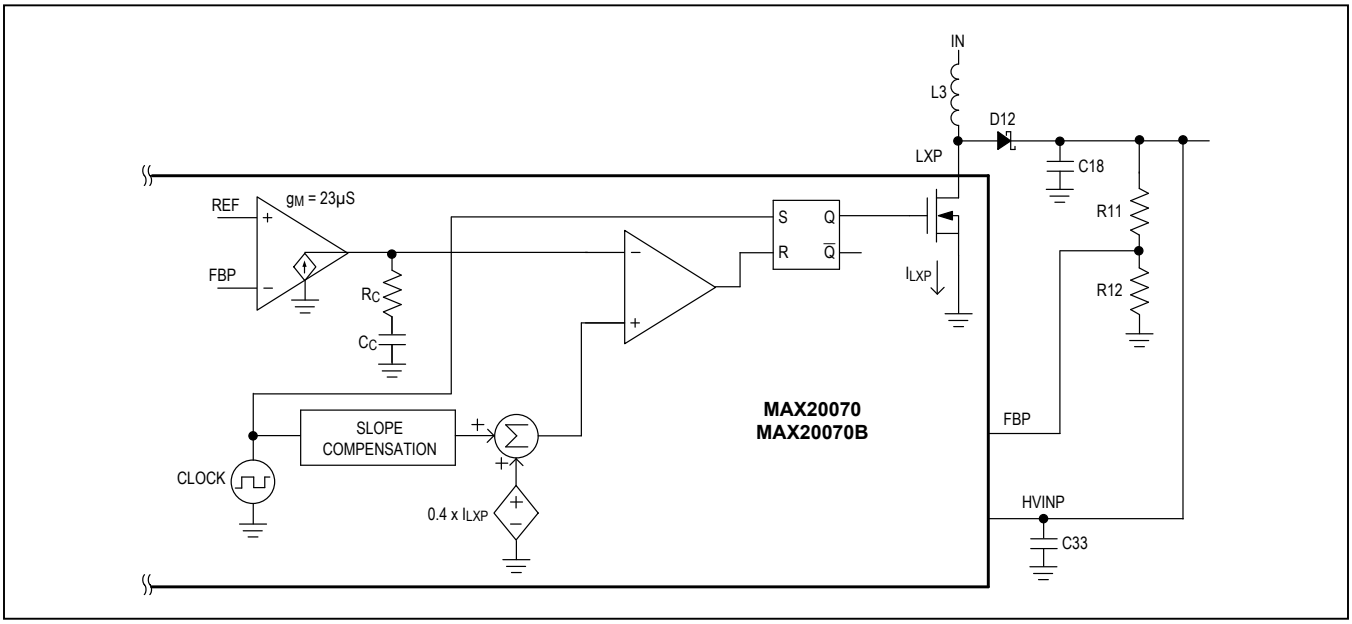


Figure 6. TFT Boost Converter Simplified Block Diagram

There is an internal compensation network at the output of the error amplifier. Different values of the compensation network switch in and out depending on the connection to the FBP pin. If FBP is grounded, the circuit regulates the output voltage to 6.5V and the POS voltage is sensed by an internal resistor-divider (not shown). When FBP is not shorted to ground and is connected to the junction of the resistor-divider (R9 and R10), external feedback is used to control the POS voltage.

C_C = 140pF, R_C = 490kΩ (when external feedback is used)

C_C = 180pF, R_C = 280kΩ (when internal feedback is used)

For the current loop, there is internal current sensing using a transresistance of R_T = 0.4V/A. The V_{CS} (I_inductor x R_T) sensing voltage is added to the slope compensation. The slope-compensation signal has a slope of 590mV per microsecond.

The resulting $V_{SUM} = V_{CS} + V_{SLOPE}$ is compared to the V_{COMP} (output of the error amplifier) at the input of the PWM comparator to regulate the LXP duty cycle.

Control-Loop Operation of the TFT Inverter Circuit

A simplified block diagram of the TFT inverter circuit is shown in Figure 7. There is an internal error amplifier with a g_M = 13µS that has V_{REF} = 0V and the midpoint of an internal resistor-divider (R-R), connected from POS to NEG, as inputs. At the output of the error amplifier, there is an internal compensation network:

$$C_C = 140pF, R_C = 360k\Omega$$

For the current loop, there is internal current sensing using a transresistance of R_T = 0.31V/A.

The V_{CS} (I_inductor x R_T) sensing voltage is added to the slope compensation. The slope-compensation signal has a slope of 590mV per microsecond. The resulting $V_{SUM} = V_{CS} + V_{SLOPE}$ is compared to the V_{COMP} (output of the error amplifier) at the input of the PWM comparator to regulate the LXN duty cycle.

Gate-Driver Power Supplies

The positive gate-driver power supply (V_{GVDD}) generates +22V (max) and the negative gate-driver power supply (V_{GVEE}) generates -22V (max). Both supplies can supply up to 3mA current. The V_{GVDD} and V_{GVEE} regulation voltages are both set using the external resistor networks shown in Figure 2. Both charge-pump regulators use a 400kHz switching frequency. The charge pumps regulate the output voltage by controlling the current that flows into the flying capacitors.

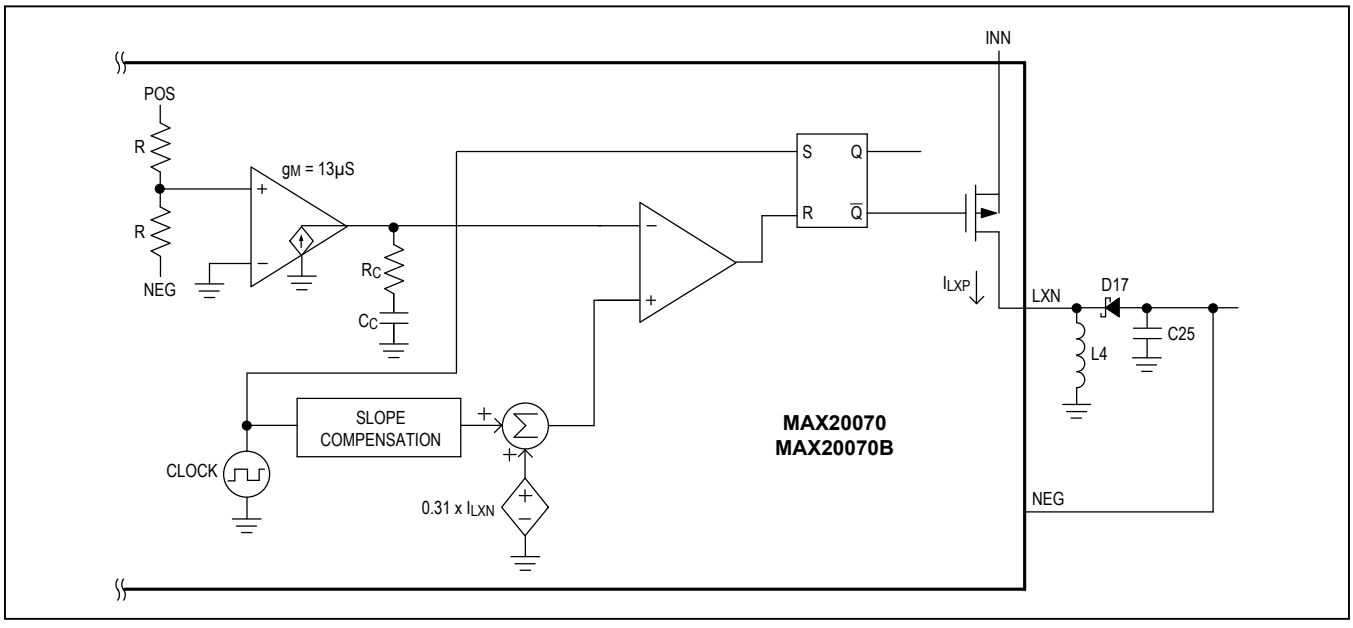


Figure 7. TFT Inverter Circuit Simplified Block Diagram

Operation of the Positive Charge Pump

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT-LCD gate-driver ICs.

The output voltage is set with an external resistive voltage-divider from its output to GND, with the midpoint connected to FBPG. The number of charge-pump stages and the setting of the feedback-divider determine the output voltage of the positive charge-pump regulator. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer (see Figure 8). The error amplifier compares the feedback signal (FBPG) with a 1.25V internal reference. If the feedback signal is below the reference, the charge-pump regulator turns on P1 and turns off N1 when the rising edge of the oscillator clock arrives, level shifting C3 and C4 by V_{PGVDD} volts. If the voltage across C9 plus a diode drop (V_{DGVDD} + V_{DIODE}) is smaller than the level-shifted flying-capacitor voltage (V_{C4} + V_{PGVDD}), charge flows from C4 to C9 until diode D9-1 turns off. Similarly, if the voltage at the D3-1 cathode plus a diode drop (V_{PGVDD} - V_{C8} + V_{DIODE}) is smaller than the level-shifted flying-capacitor voltage (V_{C3} + V_{PGVDD}), charge flows from C3 to C8 until diode D3-1 turns off. The falling edge of the oscillator clock turns off P1 and turns on N1, allowing V_{PGVDD} to charge up the flying capacitor C3 through D3-2 and C8 to charge C4 through diode D9-2. If the feedback signal is above the reference when the rising edge of the oscillator arrives, the regulator ignores this clock edge and keeps N1 on and P1 off. The charge-pump regulator also includes a discharge switch from DGVDD to ground, turned off to discharge the output capacitors during the sequential turn-off of the output voltage, as programmed by the resistor on the SEQ pin (R_{SEQ}). The node PGVDD is internally connected through a switch to the HVINP voltage. See Table 3 for the sequencing options.

Operation of the Negative Charge Pump

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT-LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF, with the midpoint connected to FBNG. The number of charge-pump stages and the setting of the feedback-divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer (see Figure 9).

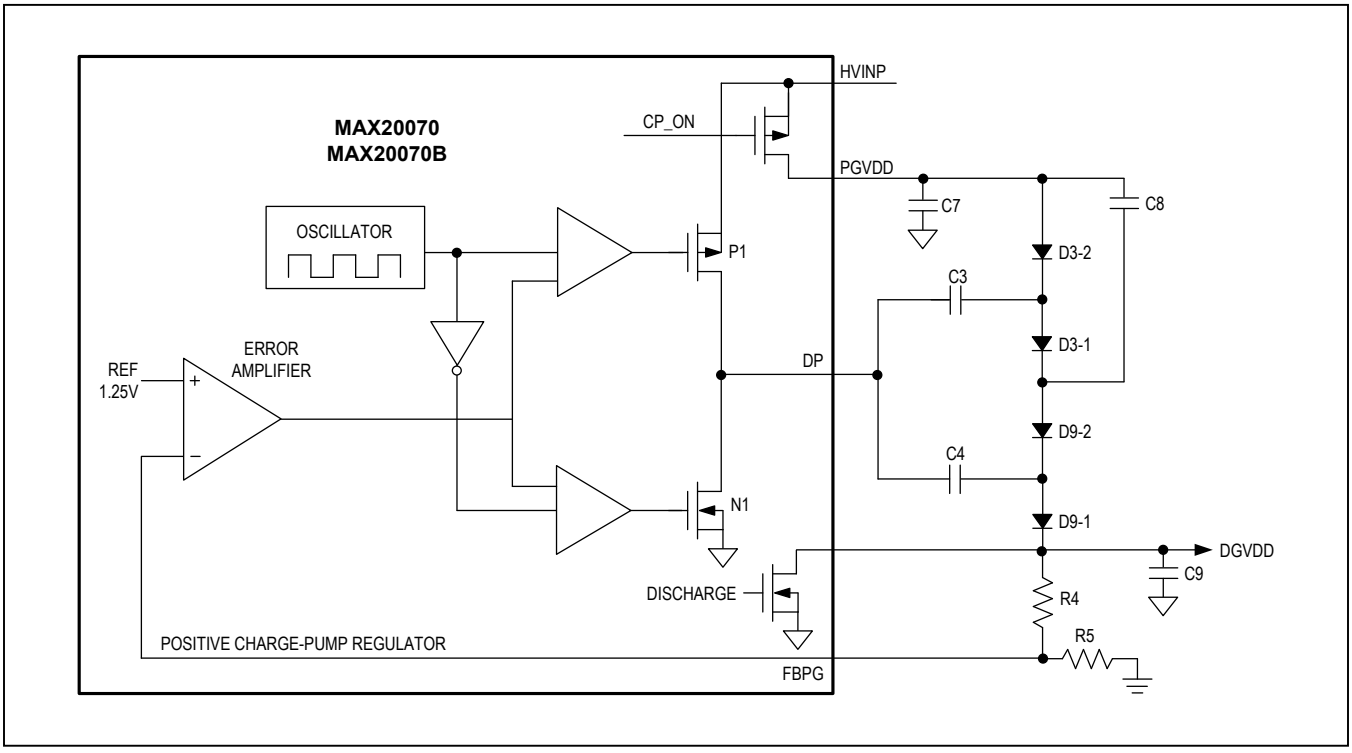


Figure 8. Positive Charge-Pump Block Diagram

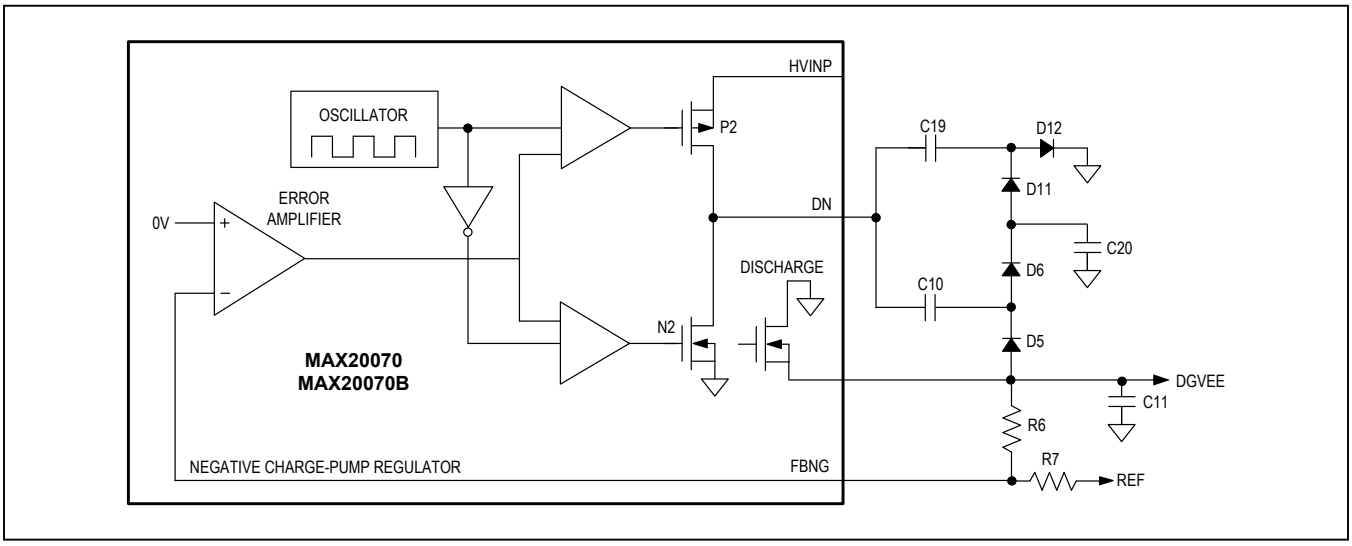


Figure 9. Negative Charge-Pump Block Diagram

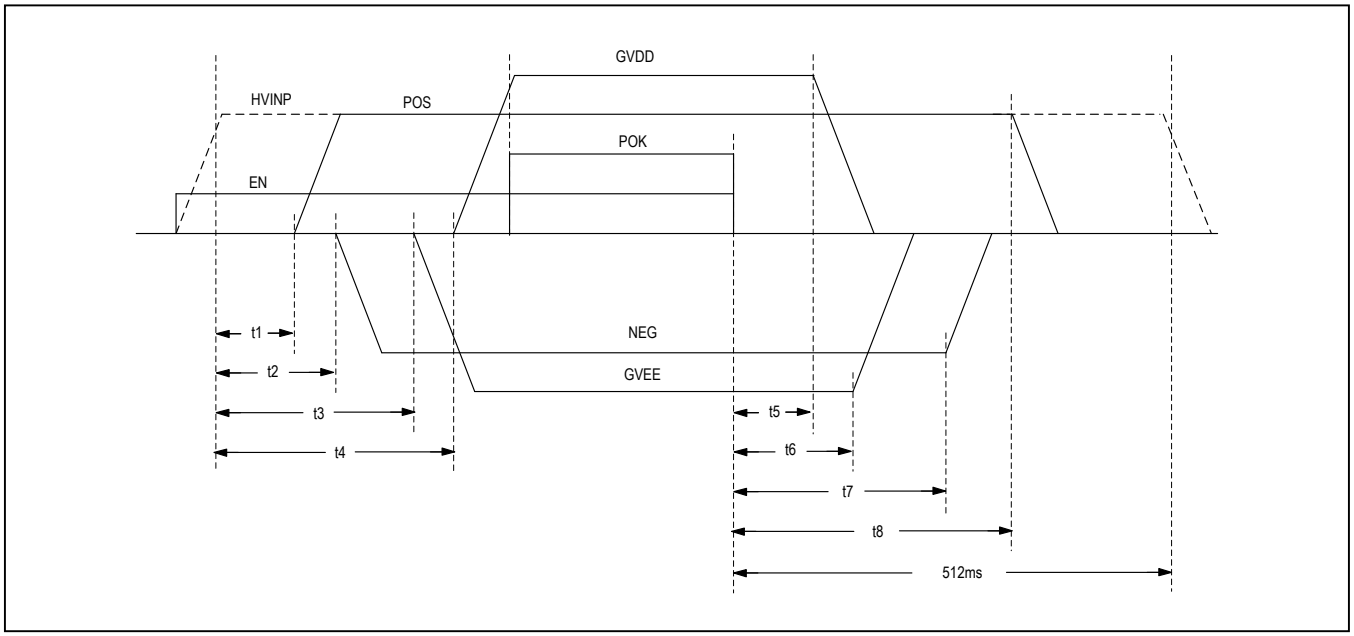


Figure 10. Sequencing Diagram

The error amplifier compares the feedback signal (FBNG) with a 0V internal reference. If the feedback signal is above the reference, the charge-pump regulator turns N2 on and P2 off when the rising edge of the oscillator clock arrives, level shifting C10 and C19. The falling edge of the oscillator clock turns N2 off and P2 on, allowing HVINP to charge up flying-capacitor C10 and C19. If the feedback signal is below the reference voltage of 0V when the rising edge of the oscillator arrives, the regulator ignores this clock edge and keeps P2 on and N2 off. In the Figure 9 diagram, the negative charge pump uses a doubler configuration; however, in cases where the absolute value of the negative charge-pump voltage is low enough, eliminate diodes D11 and D12. In that case, C19 and C20 are not needed and the cathode of D6 can be connnected to ground. For sequencing of the output voltages at turn-off, a discharge switch is connected from DGVEE to ground. The desired sequence is programmable by a resistor on the SEQ pin. See Table 3 for the sequencing options.

Fault Protection on the TFT Section

The devices have robust fault and overload protection. If any of the source-driver or gate-driver supplies fall below 80% (typ) of the programmed regulation voltage for more than 50ms (typ), all the outputs latch off and a fault condition is set. If a short condition occurs on any of the source-driver supplies for more than 10µs, all the outputs latch off and a fault condition is set. A short condition is detected when the output voltage falls below 40% of the intended regulation voltage. With MAX20070GTJA/V+ and MAX20070BGTJA/V+, a short condition is also detected when POS voltage falls below 73% of HVINP voltage. The output with the fault turns off immediately, while the other outputs follow the turn-off sequence programmed by the resistor on the SEQ pin. The LED driver section is not turned off during a TFT fault event. The fault condition is cleared when the EN pin or IN supply is cycled. In the case of a thermal fault, both the TFT power section and the LED drivers turn off immediately and remain latched off. EN pin cycling or input power cycling is required to unlatch the fault and restart switching.

True Shutdown

The devices completely disconnect the loads from the input (IN) when in shutdown mode. In most boost converters, the external rectifying diode and inductor form a DC current path from the battery to the output. If a load is connected to the boost-converter output, it can drain the battery even in shutdown. The devices have an internal switch at POS. When this switch turns off during shutdown, there is no DC path from the input to POS.

Output Control

The devices' source-driver and gate-driver outputs (V_{GVEE}, NEG, POS, and V_{GVDD}) can be controlled by the resistor value connected from SEQ to ground. All outputs are brought up with soft-start control to limit the inrush current. Table 3 lists the sequencing options that are programmable with a resistor on the SEQ pin.

Table 3. Power Sequencing

SEQ PIN RESISTOR (R_{SEQ}) (kΩ)	POWER-ON SUPPLY SEQUENCING (t1–t4 IS THE TIME FROM THE EXPIRATION OF HVINP SOFT-START PERIOD)				POWER-OFF SUPPLY SEQUENCING (REVERSE ORDER OF POWER-UP) (t5–t8 IS THE TIME FROM WHEN EN IS DRIVEN LOW)			
	1st AFTER t1ms	2nd AFTER t2ms	3rd AFTER t3ms	4th AFTER t4ms	1st AFTER t5ms	2nd AFTER t6ms	3rd AFTER t7ms	4th AFTER t8ms
20 ±1%	POS	NEG	V_{GVEE}	V_{GVDD}	V_{GVDD}	V_{GVEE}	NEG	POS
60 ±1%	POS	NEG	V_{GVDD}	V_{GVEE}	V_{GVEE}	V_{GVDD}	NEG	POS
100 ±1%	NEG	POS	V_{GVEE}	V_{GVDD}	V_{GVDD}	V_{GVEE}	POS	NEG
140 ±1%	POS	V_{GVEE}	V_{GVDD}	No NEG output	V_{GVDD}	V_{GVEE}	POS	No NEG output
180 ±1%	POS	V_{GVDD}	V_{GVEE}	No NEG output	V_{GVEE}	V_{GVDD}	POS	No NEG output
220 ±1%	POS NEG	—	—	V_{GVDD}, V_{GVEE}	V_{GVDD}, V_{GVEE}	—	—	POS, NEG
260 ±1%	V_{GVEE}	V_{GVDD}	NEG	POS	POS	NEG	V_{GVDD}	V_{GVEE}

Note: *t1 = t5 = 15ms*
t2 = t6 = 30ms
t3 = t7 = 45ms
t4 = t8 = 60ms

Power-Up/Power-Down Sequencing and Timing

The devices allow for flexible power-up/power-down sequencing and timing of the source-driver and gate-driver power supplies (V_{GVEE}, NEG, POS, and V_{GVDD}). Toggling the EN pin from low to high initiates an adjustable preset power-up sequence. Toggling the EN pin from high to low initiates an adjustable preset power-down sequence. The EN pin has an internal deglitching filter of 7µs (typ). Figure 11 shows a waveform of the internal EN signal, along with the EN input. **Note:** A glitch in the EN signal with a period less than 7µs is ignored by the internal enable circuitry.

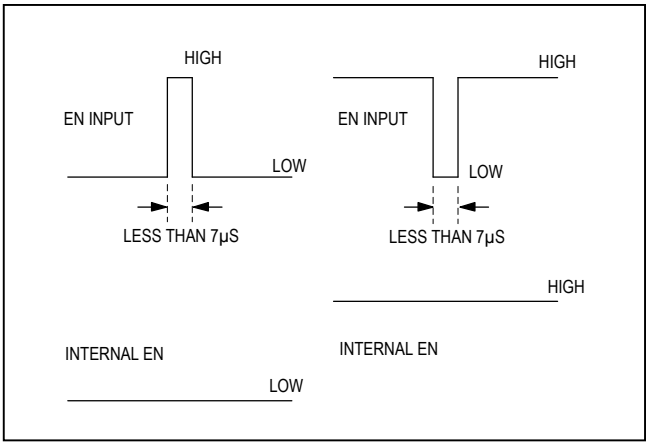


Figure 11. Power-Up/Power-Down Sequencing and Timing Waveform

LED Driver Section

The MAX20070/MAX20070B also include a high-efficiency HB LED driver, which integrates all the features necessary to implement a high-performance backlight driver to power LEDs in small-to-medium-sized displays for automotive as well as general applications. The devices provide load-dump voltage protection up to 40V in automotive applications and incorporates a DC-DC controller with peak-current-mode control to implement a boost or SEPIC-type switched-mode power supply and a 2-channel LED driver with 20mA to 160mA constant-current-sink capability per channel.

The boost/SEPIC controller features constant-frequency peak-current-mode control with internal slope compensation to control the duty cycle of the PWM controller. The DC-DC converter generates the required supply voltage for the LED strings from a wide battery input supply range. Connect LED strings from the DC-DC converter output to the 2-channel constant-current sinks that control the current through the LED strings. A single resistor connected from ISET to ground sets the forward current through both LED strings.

The devices feature adaptive LED voltage control that adjusts the converter output voltage depending on the forward voltage of the LED strings. This feature minimizes the voltage drops across the constant-current sinks and reduces power dissipation in the device. The devices provide a very wide PWM dimming range where a dimming pulse as narrow as 0.5µs is possible at a 200Hz dimming frequency.

The devices include output overvoltage protection that limits the converter output voltage to the programmed overvoltage threshold in the event of an open-LED condition, and also features an overtemperature protection that shuts down the controller if the die temperature exceeds +165°C. In addition, the devices have a shorted-LED string detection and an open-drain $\overline{FLT}$ signal to indicate open-LED, shorted-LED, and overtemperature conditions.

Current-Mode DC-DC Controller

The MAX20070/MAX20070B use current-mode control to provide the required supply voltage for the LED strings. The internal MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (see R11 in Figure 1), connected from the source of the internal MOSFET to PGND. A PWM comparator compares the current-sense voltage plus the internal slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the internal MOSFET when the voltage at CS exceeds the error amplifier's output voltage. This process repeats every switching cycle to achieve peak current-mode control.

Error Amplifier

The internal error amplifier compares an internal feedback (FB) signal with an internal reference voltage (V_{REF}) and regulates its output to adjust the inductor current. An internal minimum string detector measures the minimum LED string cathode voltage with respect to GND. During normal operation, this minimum $V_{OUT\_}$ voltage is regulated to 0.75V through feedback. The resulting DC-DC converter output voltage is 0.75V above the maximum required total LED voltage.

The converter stops switching when LED strings turn off during PWM dimming. The error amplifier disconnects from the COMP output to retain the compensation capacitor charge. This allows the converter to settle to a steady-state level immediately when the LED strings turn on again. This unique feature provides fast dimming response without having to use large output capacitors. If the PWM dimming on-pulse is less than 25µs, the feedback controls the voltage on OVP, such that the converter output voltage regulates at 95% of the OVP threshold. This mode ensures that narrow PWM dimming pulses are not affected by the response time of the converter. During this mode, the error amplifier remains connected to the COMP output.

Adaptive-LED Voltage Control

The devices reduce power dissipation using an adaptive-LED voltage-control scheme. The adaptive-LED voltage control regulates the DC-DC converter output based on the operating voltage of the LED strings. The voltage at each of the current-sink outputs (OUT1, OUT2) is the difference between the DC-DC regulator output voltage (V_{LED}) and the total forward voltage of the LED string connected to the output (OUT_). The DC-DC converter then adjusts V_{LED} until the output channel with the lowest voltage at OUT_ is 0.75V relative to GND. As a result, the device minimizes power dissipation in the current sinks and still maintains LED current regulation. For efficient adaptive-control functionality, use an equal number of HB LEDs of the same forward-voltage rating in each string.

LED Current Control (ISET)

The devices feature two identical constant-current sinks used to drive multiple HB LED strings. The current through each of the channels is adjustable between 20mA and 160mA using an external resistor (R_{ISET}) connected between ISET and GND. For single-channel operation, connect channel 1 (OUT1) and channel 2 (OUT2) together. When the OUT_ pins are connected, the current in the LEDs will be twice the current programmed by the ISET pin. If only single-string operation is needed, the OUT_ pin for the unused channel should be connected to ground. This disables the string at power-up.

Current Limit

The devices include a fast current-limit comparator to terminate the on-cycle during an overload or a fault condition. The current-sense resistor (R_{CS}) connected between the source of the internal MOSFET and ground sets the current limit. The CS input has a 0.27V (typ) voltage trip level (V_{CS}). Use the following equation to calculate R_{CS}:

$$R_{CS} = (V_{CS})/I_{PEAK}$$

where I_{PEAK} is the peak current that flows through the MOSFET. The bond-wire resistance to the CS pin is 13mΩ (typ) and the actual value of R_{CS} should take into account the bond-wire resistance.

Undervoltage Lockout

The devices feature two undervoltage lockouts (UVLOBATT and UVLOVC). The undervoltage-lockout threshold for V_{BATT} is 4.2V (typ) and the undervoltage-lockout threshold for V_{CC} is 4V (typ). When V_{CC} is below its UVLO, the LED driver completely turns off, including the dimming and switching of the DC-DC converter. If there is a V_{CC} short and the voltage is below the UVLO, the LED driver turns off, but the TFT power section keeps working unless a thermal shutdown is triggered.

LED Driver Soft-Start

The devices' boost/SEPIC converter features a soft-start that is activated during power-up. The soft-start ramps up the output of the converter in 64 steps in a period of 100ms (typ), unless both strings reach current regulation point, in which case the soft-start would terminate to resume normal operation immediately. Once the soft-start ends, the internal soft-start circuitry is disabled and normal operation begins. The 100ms soft-start period begins when the LED driver section is enabled.

LED Dimming Control

The devices feature LED brightness control using an external PWM signal applied to DIM. A logic-high signal on the DIM input enables all two LED current sources and a logic-low signal disables them. The duty cycle of the PWM signal applied to DIM also controls the DC-DC converter's output voltage. If the pulse-width duration of the PWM signal is less than 25µs (DIM pulse width increasing), the boost converter regulates its output based on feedback from the OVP input. While in this mode, the converter output voltage regulates to 95% of the overvoltage threshold at the OVP pin. If the pulse-width duration of the PWM signal is greater than or equal to 25µs (DIM pulse width increasing), the converter regulates its output so that the minimum voltage at OUT_ is 0.75V. At power-up, if the device has completed the soft-start period of 100ms (typ) and the PWM signal at the DIM pin is still low, the device regulates the output voltage based on the feedback signal coming from the OVP pin. Once a PWM pulse width greater than 25µs is applied, the converter regulates its output so that the minimum voltage at the OUT_ pin is 0.75V. When dimming pulse width is less than 25µs, the converter regulates the voltage on the OVP pin to 95% of the OVP voltage. This is referred to as LODIM mode. If at any time after power-up the DIM input goes low for more than 40ms, the converter will regulate the output at the OVP pin to 95% of OVP voltage. To bring the converter out of this mode, the dimming-signal pulse width needs to be greater than 25µs.

Open-LED Management and Overvoltage Protection

On power-up, the devices detect and disconnect any unused current-sink channels before entering the DC-DC converter soft-start. Disable the unused current-sink channels by connecting the corresponding OUT_ to LED ground (referred to as LEDGND). This avoids asserting the $\overline{FLT}$ output for the unused channels. After soft-start, the device detects open LED and disconnects any strings with an open LED from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency. During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, OVP input, and GND. The overvoltage-protection threshold at the DC-DC converter output (V_{OVP}) is determined using the following formula:

$$V_{OVP} = 1.25 \times (1 + R17/R16)$$

where 1.25V (typ) is the OVP threshold. Select R16 and R17 such that the voltage at OUT_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the PWM controller switches off. Any current-sink output with $V_{OUT\_}$ < 300mV (typ) is disconnected from the minimum voltage detector.

Connect the OUT_ of all channels without LED connections to GND before power-up to avoid OVP triggering at startup. When an open-LED overvoltage condition occurs, $\overline{FLT}$ is asserted. Open-LED detection is disabled when the PWM dimming pulse width is less than 25µs. If an open-LED fault is detected when the dimming pulse width is greater than 25µs and the dimming pulse is below 25µs, the fault flag remains asserted. To remove the fault assertion, EN or BATT must be cycled.

Short-LED Detection

The devices feature two-level short-LED detection circuitry. A level 1 short is detected if the difference between the total forward LED voltages of the two strings exceeds 4.2V (typ). If a level 1 short is detected on either of the strings, $\overline{FLT}$ is asserted. The strings continue to operate normally when a level 1 fault is detected. A level 2 short is detected if the difference between the total forward LED voltages of the two strings exceeds +7.8V (typ). If a level 2 short is detected on either of the strings, the particular LED string with the short is turned off after 6µs and $\overline{FLT}$ is asserted. The strings are reevaluated on each DIM rising edge and $\overline{FLT}$ is deasserted if the short is removed. The short-LED detection is disabled when the dimming pulse width is less than 25µs. However, if a short-LED fault asserts when the dimming pulse width is above 25µs and then reduced to below 25µs, the fault flag stays asserted even if the fault is removed. To deassert the fault, the dimming pulse width has to be higher than 25µs and the short fault removed. During load-dump conditions, the minimum string voltage goes above 0.75V and the converter stops switching. Under these conditions, if an LED-short fault occurs and the minimum string voltage is above 1.5V, the fault signal does not assert. Once the input voltage is lowered and the minimum string voltage goes below 1.5V, the fault asserts. Once a fault asserts and the input voltage increases such that the minimum string voltage goes above 1.5V, the fault remains asserted. The fault deasserts only if the minimum string voltage goes below 1.5V and the LED-short fault is removed.

Applications Information

TFT Power Section

Setting the POS Voltage

The positive output voltage is set by connecting FBP to a resistive voltage-divider between the output and GND (see Figure 2). Select feedback resistor R10 in the 30kΩ to 100kΩ range. R9 is then given by:

$$R9 = R10\left(\frac{V_{POS}}{V_{FBP}} - 1\right)$$

where V_{FBP} = 1.25V.

Setting the Gate-Driver Voltages

The positive gate-driver voltage is set by connecting FBPG to a resistive voltage-divider between the output and GND (Figure 1). Select foldback resistor R5 in the 10kΩ to 20kΩ range. R4 is then given by:

$$R4 = R5\left(\frac{V_{GVDD}}{V_{FBPG}} - 1\right)$$

where V_{FBPG} = 1.25V.

The negative gate-driver voltage is set by connecting FBNG to a resistive voltage-divider between the output and REF (Figure 1). Select foldback resistor R7 in the 100kΩ to 200kΩ range. R6 is then given by:

$$R6 = R7\left(\frac{-V_{GVEE}}{V_{REF}}\right)$$

where V_{FBNG} = 1.25V. The voltage at FBNG is regulated to 0V by the MAX20070/MAX20070B ICs.

Inductor Selection

The high switching frequencies in the devices allows the use of small inductors. For most applications, 4.7µH and 10µH inductors are recommended. Larger inductances reduce the peak inductor current, but result in skipping pulses at light loads. Smaller inductances require less board space, but can cause greater peak current due to current-sense comparator propagation delay. Use inductors with ferrite core or equivalent. Powder iron cores are not recommended for use with high switching frequencies. The inductor's saturation rating must exceed the peak current-limit setting of 1.2A. For highest efficiency, use inductors with a low DC resistance (under 200mΩ); however, for smallest circuit size, higher resistance is acceptable.

Diode Selection

High switching frequency demands a high-speed rectifier. Schottky diodes, such as CMHSH5-2L, MBR0520L, or MBR0530L are recommended. For the boost converter, make sure that the diode's peak current rating exceeds the current limit and its breakdown voltage exceeds the output voltage; for the buck-boost converter, make sure that the diode's peak current rating exceeds the current limit and its breakdown voltage rating exceeds the sum of the absolute maximum output voltage and maximum input voltage. Ultra-high-speed silicon rectifiers are also acceptable, but Schottky diodes provide better efficiencies.

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determine the amplitude of the high-frequency ripple seen on the output voltage. For stability, the positive output filter capacitor (C23 + C12) should satisfy the following:

$$(C23 + C12) > 10\mu F \times V_{POS}/15V \times I_{LOAD}/100mA$$

Most of the capacitance (2/3 of total) should be on the HVINP node and 1/3 at POS.

For stability, the inverter output capacitor (C5 + C6) should also satisfy the following:

$$(C5 + C6) > 10\mu F \times |V_{NEG}|/15V \times I_{LOAD}/100mA$$

Input Bypass Capacitor Selection

Although the output current of most MAX20070/MAX20070B applications may be relatively small, the input must be designed to withstand current transients equal to the inductor current limit. The input bypass capacitors reduce the peak currents drawn from the voltage source and reduce noise caused by the switching action. The input source impedance determines the size of the capacitor required at the input. As with the output filter capacitor, a low-ESR capacitor is recommended. A 4.7µF low-ESR capacitor is adequate for most applications, although a smaller bypass capacitor may also be acceptable with low-impedance sources, or if the source supply is already well filtered.

DC-DC Converter for the LED Driver

Three different converter topologies are possible with the DC-DC controller in the MAX20070/MAX20070B ICs, which have the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always more than the input-supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply voltage range, use the buck-boost-converter topology. Implement a buck-boost topology using either a conventional SEPIC configuration or a coupled-inductor buck-boost configuration. The latter is a flyback converter with 1:1 turns ratio. 1:1-coupled inductors are available with tight coupling suitable for this application. The boost-converter topology provides the highest efficiency among the above-mentioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor over the SEPIC configuration. Also, the feedback-loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough.

LED Current Setting

Select the resistor on the ISET pin based on the required LED current per string:

$$R_{ISET} = 1500/I_{STRING}$$

where R_{ISET} is in kΩ and I_{STRING} is the current per string in mA.

OVP Resistor Settings

Determine the maximum output voltage based on the forward-voltage drop of the LEDs. The maximum output voltage is given by V_{LED}:

$$V_{LED} = V_{FMAX} \times N_{STRING} + 0.75V$$

where V_{FMAX} is the maximum forward voltage on each LED at the required LED current (I_{STRING}) and N_{STRING} is the number of LEDs in each string.

When the dimming pulse width goes below 25µs, the boost voltage should regulate to:

$$V_{BOOST} = (V_{LED} + 2) \text{ volts}$$

Under this condition, the device regulates the boost voltage to 95% of OVP setting. Therefore the overvoltage setting is given by:

$$V_{BOOST} = (V_{LED} + 2)/0.95$$

In most automotive applications, the highest value of a single resistor cannot exceed 100kΩ. Based on this, the R17 resistor in Figure 1 is 100kΩ. The R16 resistor is given by:

$$R16 = 1.25 \times 100/(V_{BOOST} - 1.25)\ k\Omega$$

Select a value of R16 that is lower than the calculated value.

Power-Circuit Design

First, select a converter topology based on the input voltage range and the desired output voltage. Determine the required input-supply voltage range, the maximum voltage needed to drive the LED strings, including the 0.75V (min) across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}) as follows:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the LED current per string in amperes and N_{STRING} is the number of strings used.

Calculate the maximum duty cycle (D_{MAX}) using the following equations.

For boost configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN\_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.27V)}$$

For SEPIC configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1})}{(V_{IN\_MIN} - V_{DS} - 0.27V + V_{LED} + V_{D1})}$$

where:

V_{D1} is the forward drop of the rectifier diode in volts (approximately +0.6V).

V_{IN_MIN} is the minimum input supply voltage in volts.

V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on.

and:

0.27V is the peak current-sense voltage.

Initially, use an approximate value of +0.2V for V_{DS} to calculate D_{MAX}.

Boost Configuration

The average inductor current varies with the line voltage, and the maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended peak-to-peak ripple is 60% of the average inductor current.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔIL to be ±30% of the average inductor current:

$$\Delta IL = IL_{AVG} \times 0.3 \times 2$$

and:

$$IL_P = IL_{AVG} + \frac{\Delta IL}{2}$$

Calculate the minimum inductance value (L_{MIN}) in henries with the inductor current ripple set to the maximum value:

$$L_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.3V\right) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where 0.3V is the peak current-sense voltage. Choose an inductor with a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. It is necessary to verify that the chosen inductor allows operation at the minimum required dimming pulse width and at the minimum input voltage. When the dimming pulse width needed is below 25µs, it is necessary to verify proper operation at a pulse width of 25µs. The maximum possible duty cycle is 90%. The minimum required inductance for proper operation during a dimming pulse width of 25µs is given by the following equation:

$$L_{DIM} = \frac{\left(V_{IN\_MIN} \times 0.9 - (V_{LED} - V_{IN\_MIN}) \times 0.1\right) \times 25}{I_{LED} \times 20}$$

in µH for the boost configuration

$$L_{DIM} = \frac{\left(V_{IN\_MIN} \times 0.9 - (V_{LED} \times 0.1\right) \times 25}{I_{LED} \times 20}$$

in µH for the SEPIC configuration

The selected inductor value should be the lower of L_{MIN} and L_{DIM}.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input-supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see Figure 3 for the SEPIC configuration).

One of the inductors (L4) takes LED current as the average current and the other (L1) takes input current as the average current. Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL4_{AVG}$) and peak inductor currents ($IL1_P$, $IL4_P$) in amperes:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

$$IL4_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔIL is ±30% of the average inductor current:

$$\Delta IL1 = IL1_{AVG} \times 0.3 \times 2$$

and:

$$IL1_P = IL1_{AVG} + \frac{\Delta IL1}{2}$$

$$\Delta IL4 = IL4_{AVG} \times 0.3 \times 2$$

and:

$$IL4_P = IL4_{AVG} + \frac{\Delta IL2}{2}$$

Calculate the minimum inductance values ($L1_{MIN}$ and $L4_{MIN}$) in henries with the inductor current ripples set to the maximum value as follows:

$$L1_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3V) \times D_{MAX}}{f_{SW} \times \Delta IL1}$$

$$L4_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3V) \times D_{MAX}}{f_{SW} \times \Delta IL4}$$

where 0.3V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L4_{MIN}$ and current rating greater than $IL1_P$ and $IL4_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

For simplifying further calculations, consider L1 and L4 as a single inductor with L1 and L4 connected in parallel. The combined inductance value and current is calculated as follows:

$$L_{MIN} = \frac{L1_{MIN} \times L4_{MIN}}{L1_{MIN} + L4_{MIN}}$$

and:

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors connected together for SEPIC configuration. Use these values in the calculations for SEPIC configuration in the following sections.

Select coupling-capacitor C23 so the peak-to-peak ripple on it is less than 2% of the minimum input-supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1, C23, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of C23:

$$C23 \geq \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where C23 is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, and the factor 0.02 accounts for 2% ripple.

Current-Sense Resistor and Slope Compensation

The current-sense resistor (R_{CS}) should be selected such that at the lowest input-line voltage, the peak voltage on the internal MOSFET current-sense resistor is 0.9 x 0.25V. The bond-wire resistance of the CS pin should also be taken into account in the calculations. The typical bond-wire resistance is 13mΩ. The actual value of R_{CS} used should have a resistance 15mΩ lower than the calculated value. Once the current-sense resistor is selected, verify that the built-in internal slope compensation is adequate. If the actual desired slope-compensation ramp is greater than the internal slope, adjust the value of the current-sense resistor and the inductor such that the desired ramp is lower than the built-in internal ramp. The chosen value of R_{CS} should satisfy the following criteria:

$$0.23 > \frac{\left((V_{LED} - 2 \times V_{IN\_MIN}) \times R_{CS} \times 2\right)}{L_{MIN} \times 3 \times f_{SW}}$$

for the boost configuration

$$0.23 > \frac{\left((V_{LED} - V_{IN\_MIN}) \times R_{CS} \times 2\right)}{L_{MIN} \times 3 \times f_{SW}}$$

for the SEPIC configuration

Under certain conditions, the peak current limit may limit the LED current from reaching regulation when the dimming pulse width is close to 25µs. Lower the current-sense resistor (R_{CS}) such that the LED current is in regulation.

It may be necessary to change the size of the inductor to prevent inductor saturation after deciding the actual value of the current-sense resistor. The value of the inductance should stay as calculated earlier.

Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across constant-current sink outputs because the LED string voltages are stable due to the constant current. For the MAX20070/MAX20070B, limit the peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output is usually minimized. In this case, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance. Assuming an output-ripple voltage of 100mV when operating at a dimming duty cycle of 100%, the desired output capacitance is given by the following:

$$C_{OUTRIPPLE} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times 0.1}$$

The minimum output capacitance for proper operation during dimming down to very narrow duty cycles is given by the following:

$$C_{OUTMIN} = \frac{1.25}{R16 \times f_{PWM} \times 0.25}$$

where R16 is the bottom resistor in the OVP divider of Figure 1 and f_{PWM} is the dimming frequency. The actual capacitance used should be higher than both C_{OUTMIN} and $C_{OUTRIPPLE}$.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least amount of burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that calculated in the following equation:

$$I_D = I_{LED} \times 1.2$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to 0.75V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the steady-state condition in the form of capacitor voltages, mainly the output filter-capacitor voltage and compensation-capacitor voltage. When the PWM dimming pulses are less than 25µs switching clock cycles, the feedback loop regulates the converter output voltage to 95% of the OVP threshold.

The worst-case condition for the feedback loop is when the LED driver is in normal mode, regulating the minimum OUT_ voltage to 0.75V. The switching converter small-signal transfer function has a right-half plane (RHP) zero for boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The worst-case RHP zero frequency (f_{ZRHP}) is calculated in the following equations.

For boost configuration:

$$f_{ZRHP} = \frac{V_{LED}(1-D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

For SEPIC configuration:

$$f_{ZRHP} = \frac{V_{LED}(1-D_{MAX})^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes. A simple way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}) that is calculated in the following equations.

For boost configuration:

$$f_{P1} = \frac{I_{LED}}{2 \times \pi \times V_{LED} \times C_{OUT}}$$

For SEPIC configuration:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{2 \times \pi \times V_{LED} \times C_{OUT}}$$

where f_{P1} is in hertz, V_{LED} is in volts, I_{LED} is in amperes, and C_{OUT} is in farads. Compensation components (R_{COMP} and C_{COMP}) perform two functions: C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at the output pole frequency (f_{P1}), so it provides a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1} so the total loop gain crosses 0dB with -20dB/ decade slope at 1/5 the RHP zero frequency, is calculated in the following equations.

For boost configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1-D_{MAX})}$$

For the SEPIC configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1-D_{MAX})}$$

where R_{COMP} is the compensation resistor in ohms, f_{ZRHP} and f_{P1} are in hertz, R_{CS} is the switch current-sense resistor in ohms, and GM_{COMP} is the transconductance of the error amplifier (600µS).

The value of C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{Z1}}$$

where f_{Z1} is the compensation zero placed at 1/5 of the crossover frequency, which is, in turn, set at 1/5 of the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency may fall within the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This is usually implemented by connecting a capacitor in parallel with C_{COMP} and R_{COMP}.

PCB Layout and Guidelines

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the inner-loop area created by the boost converter high switching-current connections. Place D13 and C23 close to the device so the traces connecting the LX pin to the anode of D13, the cathode of D13 to C23, and C23 to the PGND pin are all kept as short as possible to minimize the loop area contained within these connections. Make these connections with short, wide traces.
- Minimize the inner-loop area created by the buck-boost converter high switching-current connections. Place C6, C1, and D2 close to the device so the traces connecting C1 to the INN pin, the LXN pin to the cathode of D2, the anode of D2 to C6, and C1 ground connection to C6 are all kept as short as possible to minimize the loop area contained within these connections. Make these connections with short, wide traces.
- Minimize the inner-loop area created by the boost-converter LED driver (Figure 2) high switching-current connections. Place D1 and C21 close to the device so the traces connecting the DRAIN pin to the anode of D1, the cathode of D1 to C21, and C21 to the PGND pin are all kept as short as possible to minimize the loop area contained within these connections. Make these connections with short, wide traces.
- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power-ground island (PGND) consisting of the PGND pin, the input and output-capacitor ground connections, the charge-pump capacitor ground connections, and the buck-boost inductor ground connection. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power-ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (GND) consisting of the GND pin, all the feedback-divider ground connections, the IN, V_{CC}, and REF bypass capacitor ground connections, and the device's exposed backside pad.
- Connect the GND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place the feedback voltage-divider resistors as close as possible to their respective feedback pins. Keep the traces connecting the feedback resistors as short as possible to their respective feedback pins. Placing the resistors farther away causes the feedback trace to become an antenna that may pick up switching noise. Do not run any feedback trace near the LXP, LXN, DRAIN, DP, or DN switching nodes.
- Place the IN, V_{CC}, BATT, and REF bypass capacitors as close as possible to the device. The ground connections of the IN, V_{CC}, BATT, and REF bypass capacitors should be connected directly to the analog ground plane or directly to the GND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Keep sensitive signals away from the LXP, LXN, DRAIN, DP, and DN switching nodes. If necessary, use DC traces as a shield.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20070GTJ/V+	-40°C to +105°C	32 TQFN-EP*
MAX20070GTJA/V+	-40°C to +105°C	32 TQFN-EP*
MAX20070BGTJ/V+	-40°C to +105°C	32 TQFN-EP*
MAX20070BGTJA/V+	-40°C to +105°C	32 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+4	21-0140	90-0012

Chip Information

PROCESS: CMOS